RCA Solid State

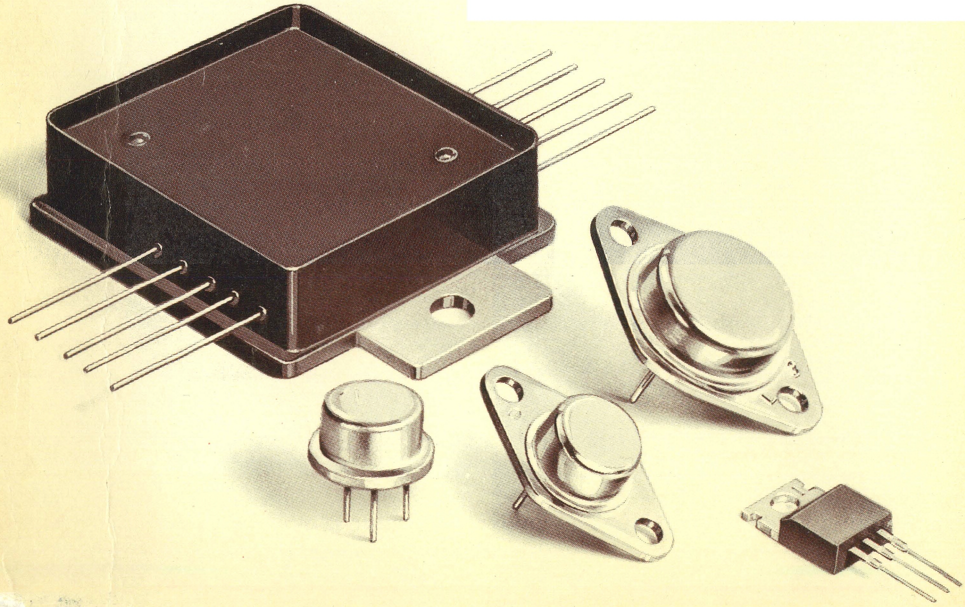
'74 DATABOOK Series

SSD-204B

Power Transistors

and Power Hybrid Circuits

Selection Guide
Data
Application Notes



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RCA Solid State
'74 DATABOOK Series

Power Transistors
and Power Hybrid Circuits

This DATABOOK contains complete data and related application notes on power transistors and power hybrid circuits presently available from RCA Solid State Division as standard products. For ease of type selection, product matrix charts for major power-transistor categories are given on pages 10—22. Data sheets are then grouped in the following categories: (a) hometaxial-base types; (b) epitaxial-base types; (c) high-voltage types; (d) high-speed switching types; (e) monolithic Darlington types; (f) special audio power types; (g) small-signal low-noise types; (h) power-transistor chips; (i) power hybrid circuits. Application notes are included in numerical order following the data sheets.

A feature of this DATABOOK is the complete Guide to RCA Solid State Devices at the back of the book. This section includes a developmental-to-commercial-number cross-reference index, a comprehensive subject index, and a complete index to all standard devices in the solid-state product line: linear integrated circuits, MOS field-effect (MOS/FET) devices, COS/MOS integrated circuits, power transistors, power hybrid circuits, rf power devices, thyristors, rectifiers, and diacs. All listings include references to volume number and page number in the 1974 7-volume DATABOOK series described on the facing page.

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Function: (Check One)

- A ☐ Executive/Administration
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- C ☐ Research/Development
- D ☐ Design Engineer
- E ☐ Application/Components Engineer
- F ☐ Production/Manufacturing
- G ☐ Documentation/Library
- H ☐ Reliability/QA
- I ☐ Education/Training
- J ☐ Program/Project Management
- K ☐ Marketing

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- A ☐ Broadcast
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- F ☐ Automotive
- G ☐ Industrial
- H ☐ Medical
- I ☐ Research
- J ☐ Transportation
- K ☐ Consumer, Electronic
- L ☐ Consumer, Appliance
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- N ☐ Ordnance
- O ☐ Avionics
- P ☐ Electronic Warfare

Product Interest:
(Indicate order of interest if more than one is marked)

- A ☐ Linear IC's
- B ☐ Digital IC's, COS/MOS
- C ☐ Digital IC's, Bipolar
- D ☐ Thyristors/Rectifiers
- E ☐ Liquid Crystals
- F ☐ Semiconductor Diodes
- G ☐ RF Power Semiconductors
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2N699	22	495	120	2	40-120
2N918	83	692	30	0.3	20 min.
2N1613	106	498	75	3	20 min.
2N1711	26	503	75	3	35 min.
2N1893	34	507	120	3	40-120
2N2102	106	498	120	5	20 min.
2N2270	24	513	60	5	50-200
2N2405	34	507	120	5	60-200
2N2857	61	714	30	0.3	30-150
2N2895	143	517	120	1.8	40-120
2N2896	143	517	140	1.8	60-200
2N2897	143	517	60	1.8	50-200
2N3053	432	404	60	5	50-250
2N3054	527	45	90	25	25-100
2N3055	524	102	100	115	20-70
2N3263	54	475	150	20	25-75
2N3264	54	475	120	30	20-80
2N3265	54	475	150	24	25-75
2N3266	54	475	120	28	20-80
2N3439	64	286	450	10	40-160
2N3440	64	286	300	10	40-160
2N3441	529	69	160	25	25-100
2N3442	528	133	160	117	20-70
2N3478	77	696	30	0.2	25-150
2N3583	138	304	250	2.5	40 min.
2N3584	138	304	375	2.5	25-100
2N3585	138	304	500	2.5	25-100
2N3600	83	692	30	0.3	20-150
2N3771	525	141	50	150	15-60
2N3772	525	141	100	150	15-60
2N3773	526	149	160	150	15-60
2N3839	229	718	30	0.3	30-150
2N3878	299	443	120	35	50-200
2N3879	299	443	120	35	20-80
2N4036	216	410	-90	7	20-200
2N4037	216	410	-60	7	50-250
2N4063	64	286	450	—	40-160
2N4064	64	286	300	10	40-160
2N4240	138	304	500	2.5	30-150
2N4314	216	410	-90	7	50-250
2N4347	528	133	140	100	15-60
2N4348	526	149	140	120	15-60
2N5038	698	461	150	140	50-200
2N5039	698	461	120	140	30-150
2N5109	281	722	40	3.5	40-120
2N5179	288	700	20	0.3	25-250
2N5189	296	418	60	5	30 min.
2N5202	299	443	120	35	10-100
2N5239	321	373	300	100	20-80
2N5240	321	373	375	100	20-80
2N5262	313	423	75	5	35 min.
2N5293	322	61	80	36	30-120
2N5294	322	61	80	36	30-120
2N5295	322	61	60	36	30-120
2N5296	322	61	60	36	30-120
2N5297	322	61	80	36	20-80
2N5298	322	61	80	36	20-80
2N5320	325	429	100	10	30-130
2N5321	325	429	75	10	40-250
2N5322	325	429	-100	10	30-130
2N5323	325	429	-75	10	40-250
2N5415	336	292	-200	10	30-150
2N5416	336	292	-350	10	30-120
2N5490	353	90	60	50	20-100
2N5491	353	90	60	50	20-100
2N5492	353	90	75	50	20-100
2N5493	353	90	75	50	20-100
2N5494	353	90	60	50	20-100
2N5495	353	90	60	50	20-100
2N5496	353	90	90	50	20-100
2N5497	353	90	90	50	20-100
2N5575	359	162	70	300	10-40
2N5578	359	162	90	300	10-40
2N5671	383	481	120	140	20-100
2N5672	383	481	150	140	20-100
2N5781	413	34	-80	10	20-100
2N5782	413	34	-65	10	20-100
2N5783	413	34	-45	10	20-100
2N5784	413	34	80	10	20-100
2N5785	413	34	65	10	20-100
2N5786	413	34	45	10	20-100
2N5804	407	379	300	110	10-100
2N5805	407	379	375	110	10-100
2N5838	410	356	275	100	8-40
2N5839	410	356	300	100	10-50
2N5840	410	356	375	100	10-50
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2N5955	675	170	-70	40	20-100
2N5956	675	170	-50	40	20-100
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2N6033	462	487	150	140	10-50
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2N6056	563	527	60	100	100-18000
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2N6078	492	318	275	45	12-70
2N6079	492	318	375	45	12-50
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2N6099	485	121	70	75	20-80
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2N6103	485	121	45	75	15-60
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2N6107	676	177	-80	40	30-150
2N6108	676	177	-60	40	30-150
2N6109	676	177	-60	40	30-150
2N6110	676	177	-40	40	30-150
2N6111	676	177	-40	40	30-150
2N6175	508	278	300	20	30-190
2N6176	508	278	350	20	30-150
2N6177	508	278	450	20	30-150
2N6178	562	435	100	25	30-130
2N6179	562	435	75	25	40-250
2N6180	562	435	-100	25	30-130
2N6181	562	435	-75	25	40-250
2N6211	507	312	-275	35	30-175
2N6212	507	312	-350	35	30-175
2N6213	507	312	-400	35	30-150
2N6214	507	312	-450	20	10-100
2N6246	677	217	-70	125	20-100
2N6247	677	217	-90	125	20-100
2N6248	677	217	-110	125	20-100
2N6249	523	385	300	175	20-100
2N6250	523	385	375	175	20-100
2N6251	523	385	450	175	20-100
2N6253	524	102	55	115	20-70
2N6254	524	102	100	150	20-70
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2N6260	527	45	50	29	20-100
2N6261	527	45	90	50	25-100
2N6262	528	133	170	150	20-70
2N6263	529	69	140	20	20-100
2N6264	529	69	170	50	20-60
2N6288	676	177	40	40	30-150
2N6289	676	177	40	40	30-150
2N6290	676	177	60	40	30-150
2N6291	676	177	60	40	30-150
2N6292	676	177	80	40	30-150
2N6293	676	177	80	40	30-150
2N6354	582	469	150	140	20-150
2N6371	607	97	50	117	15-60
2N6372	675	170	50	40	20-100
2N6373	675	170	70	40	20-100
2N6374	675	170	90	40	20-100
2N6383	609	532	40	100	1000-20000
2N6384	609	532	60	100	1000-20000
2N6385	609	532	80	100	1000-20000
2N6386	610	538	40	40	1000-20000
2N6387	610	538	60	40	1000-20000
2N6388	610	538	80	40	1000-20000
2N6389	617	732	20	0.2	25-250
2N6467	675	170	-110	40	15-150
2N6468	675	170	-130	40	15-150
2N6469	677	217	-50	125	20-150
2N6470	677	217	50	125	20-150
2N6471	677	217	70	125	20-150
2N6472	677	217	90	125	20-150
2N6473	676	177	110	40	15-150
2N6474	676	177	130	40	15-150
2N6475	676	177	-110	40	15-150
2N6476	676	177	-130	40	15-150
2N6477	680	83	140	20	25-100
2N6478	680	83	160	25	25-100
2N6479	702	454	100	50	20-300
2N6480	702	454	100	50	20-300
2N6481	702	454	100	67	20-300
2N6482	702	454	100	67	20-300
2N6486	678	226	50	75	20-150
2N6487	678	226	70	75	20-150
2N6488	678	226	90	75	20-150
2N6489	678	226	-50	75	20-150
2N6490	678	226	-70	75	20-150
2N6491	678	226	-90	75	20-150
2N6496	698	461	150	140	12-100
40309	78	655	18*	5	70-350
40310	78	655	35*	29	20-120
40311	78	655	30*	5	70-350
40312	78	655	60#	29	20-120
40313	78	655	300#	35	40-250
40314	78	655	40*	5	70-350
40315	78	655	35*	5	70-350
40316	78	655	40#	29	20-120
40317	78	655	40*	5	40-200
40318	78	655	300#	35	50 min.
40319	78	655	-40*	5	35-200
40320	78	655	40*	5	40-200
40321	78	655	300#	5	25-200
40322	78	655	300#	35	75 min.
40323	78	655	10*	5	70-350
40324	78	655	35*	29	20-120
40325	78	655	35*	117	12-60
40326	78	655	40*	5	40-200

Type No.	Data Sheet File No.	Page No.	Collector-to-Base Voltage (Max.) — V	Power Dissipation (Max.) — W	DC Current Transfer Ratio
40327	78	655	300#	5	40-250
40328	78	655	300#	35	40 min.
40346	211	393	175#	10	25 min.
40346V1	211	393	175#	10	25 min.
40346V2	211	393	175#	4	25 min.
40347	88	26	60	8.75	25-100
40347V1	88	26	60	4.4	25-100
4034V2	88	26	60	11.7	25-100
40348	88	26	90	8.75	30-125
40348V1	88	26	90	4.4	30-125
40348V2	88	26	90	11.7	30-125
40349	88	26	160	8.75	30-125
40349V1	88	26	160	4.4	30-125
40349V2	88	26	160	11.7	30-125
40360	78	655	70*	5	40-200
40361	78	655	70#	5	70-350
40362	78	655	-70#	5	35-200
40363	78	655	70#	115	20-70
40364	78	655	60#	35	35-175
40366	215	397	120	5	40-120
40367	215	397	100	5	35-100
40368	215	397	100	25	35-100
40369	215	397	100	75	25-75
40372	527	45	90	25	25-100
40373	529	69	160	25	25-100
40374	138	304	250	5.8	40 min.
40375	299	443	120	5.8	50-200
40385	215	397	450	5	40-160
40389	432	404	60	3.5	50-250
40390	64	286	300	3.5	40-160
40391	216	410	-60	3.5	50-250
40392	432	404	60	7	50-250
40394	216	410	-60	7	50-250
40406	219	660	-50*	1	30-200
40407	219	660	50*	1	40-200
40408	219	660	90*	1	40-200
40409	219	660	90#	3	50-250
40410	219	660	-90#	3	50-250
40411	219	660	90#	150	35-100
40412	211	393	250#	10	40 min.
40412V1	211	393	250#	4	40 min.
40412V2	211	393	250#	10	40 min.
40537	302	667	-55#	5	50-300
40538	302	667	-55#	5	15-90
40539	303	670	55#	5	15-90
40542	304	674	50#	83	20-70
40543	304	674	60#	83	20-70
40544	303	670	50#	7	35-200
40594	358	680	95#	10	70-350
40595	358	680	-95#	10	70-350
40608	356	728	40	3.5	35-120
40611	358	680	25*	5	70-500
40613	358	680	25*	36	30-120
40616	358	680	32*	5	70-500
40618	358	680	30*	36	30-120
40621	358	680	32*	36	25-100
40622	358	680	40*	36	25-100
40624	358	680	45*	50	20-100
40625	358	680	45*	3.5	100-300
40627	358	680	55*	50	20-100
40628	358	680	55*	3.5	100-300
40629	358	680	35#	36	20-70
40630	358	680	40#	36	20-70
40631	358	680	45#	36	20-70
40632	358	680	60#	50	20-70

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40635	358	680	75#	5	50-250
40636	358	680	95#	115	20-70
40829	675	170	-90	40	20-100
40830	675	170	-70	40	20-100
40831	675	170	-50	40	20-100
40850	498	368	450	35	25 min.
40851	498	368	450	45	12 min.
40852	498	368	450	100	12 min.
40853	498	368	450	100	10 min.
40854	498	368	450	110	10 min.
40871	699	684	100*	40	50-250
40872	699	684	-100*	40	50-250
40873	699	684	70*	40	30-150
40874	699	684	-70*	40	30-150
40875	699	684	50*	40	20-120
40876	699	684	-50*	40	20-120
40885	508	278	300	20	30-190
40886	508	278	350	20	30-150
40887	508	278	450	20	30-150
40894	548	706	20	0.3	50-250
40895	548	706	20	0.3	40-250
40896	548	706	20	0.3	27-250
40897	548	706	20	0.3	70-250
40910	527	45	50	29	20-100
40911	527	45	90	50	25-100
40912	529	69	140	20	20-100
40913	529	69	170	50	20-60
40915	574	710	35	0.2	20 min.
41508	622	157	160	150	15-60
45190	559	273	40	40	25-100
45191	559	273	60	40	25-100
45192	559	273	80	40	20-80
45193	559	273	-40	40	25-100
45194	559	273	-60	40	25-100
45195	559	273	-80	40	20-80
BD142	701	110	50	117	125-160
BD181	700	115	55	117	20-70
BD182	700	115	70	117	20-70
BD183	700	115	85	117	20-70
BD239	669	193	55	30	40 min.
BD239A	669	193	70	30	40 min.
BD239B	669	193	90	30	40 min.
BD239C	669	193	115	30	40 min.
BD240	670	197	-55	30	40 min.
BD240A	670	197	-70	30	40 min.
BD240B	670	197	-90	30	40 min.
BD240C	670	197	-115	30	40 min.
BD241	671	201	55	40	25 min.
BD241A	671	201	70	40	25 min.
BD241B	671	201	90	40	25 min.
BD241C	671	201	115	40	25 min.
BD242	672	205	-55	40	25 min.
BD242A	672	205	-70	40	25 min.
BD242B	672	205	-90	40	25 min.
BD242C	672	205	-115	40	25 min.
BD243	673	209	55	65	30 min.
BD243A	673	209	70	65	30 min.
BD243B	673	209	90	65	30 min.
BD243C	673	209	115	65	30 min.
BD244	674	213	-55	65	30 min.
BD244A	674	213	-70	65	30 min.
BD244B	674	213	-90	65	30 min.
BD244C	674	213	-115	65	30 min.
BD277	667	189	-45	70	30-150

Type No.	Data Sheet File No.	Page No.	Collector-to-Base Voltage (Max.) — V	Power Dissipation (Max.) — W	DC Current Transfer Ratio
BD278	668	129	55	75	15-75
BDX33	693	545	45	70	750 min.
BDX33A	693	545	60	70	750 min.
BDX33B	693	545	80	70	750 min.
BDX33C	693	545	100	70	750 min.
BDX34	694	551	-45	70	750 min.
BDX34A	694	551	-60	70	750 min.
BDX34B	694	551	-80	70	750 min.
BDX34C	694	551	-100	70	750 min.
BFT19	683	298	-200	5	20 min.
BFT19A	683	298	-300	5	20 min.
BFT19B	683	298	-400	5	20 min.
BU106	716	363	325	75	8 min.
CH2102	632	737	60*	–	50 min.
CH2270	632	737	45*	–	50 min.
CH2405	632	737	90*	–	50 min.
CH3053	632	737	30*	–	50 min.
CH3439	632	737	325*	–	30 min.
CH3440	632	737	250*	–	30 min.
CH4036	632	737	-65*	–	35 min.
CH4037	632	737	-40*	–	35 min.
CH5320	632	737	80*	–	30 min.
CH5321	632	737	55*	–	30 min.
CH5322	632	737	-80*	–	30 min.
CH5323	632	737	-55*	–	30 min.
CH5262	632	737	35*	–	30 min.
CH6479	632	737	60*	–	40 min.
RCA1A01	651	636	70*	5	40-200
RCA1A02	651	636	-50*	7	30-200
RCA1A03	651	636	95	10	70-300
RCA1A04	651	636	-95	10	70-300
RCA1A05	651	636	-75	5	50-250
RCA1A06	651	636	75	5	50-250
RCA1A07	651	636	50	5	50-250
RCA1A08	651	636	-50	7	70-250
RCA1A09	651	636	175*	10	20-100
RCA1A10	651	636	-175*	10	40-250
RCA1A11	651	636	175*	10	40-250
RCA1A15	651	636	100*	10	20-100
RCA1A16	651	636	-100*	10	40-250
RCA1A17	651	636	90*	5	40-200
RCA1A18	651	636	10*	7	40-250
RCA1A19	651	636	-10*	7	40-250
RCA1B01	647	600	95	115	20-70
RCA1B04	649	618	225	150	15-75
RCA1B05	650	627	275	150	15-75
RCA1B06	648	609	120	150	10-50
RCA1C03	652	647	120	40	50-250
RCA1C04	652	647	-120	40	50-250
RCA1C05	644	575	60	40	20-120
RCA1C06	644	575	-60	40	20-120
RCA1C07	646	592	75	75	20-120
RCA1C08	646	592	-75	75	20-120
RCA1C09	645	583	75	75	20-120
RCA1C10	642	558	40	40	50-250
RCA1C11	642	558	-40	40	50-250
RCA1C12	652	647	140	40	40-250
RCA1C13	652	647	-140	40	40-250
RCA1C14	643	566	60	50	20-70
RCA1E02	653	651	200	35	30-150
RCA1E03	653	651	-200	35	30-150
RCA29	583	232	40	30	15-75
RCA29A	583	232	60	30	15-75
RCA29B	583	232	80	30	15-75
RCA29C	583	232	100	30	15-75

Index to Power Transistors and Power Hybrid Circuits (Cont'd)

Type No.	Data Sheet File No.	Page No.	Collector-to-Base Voltage (Max.) – V	Power Dissipation (Max.) – W	DC Current Transfer Ratio
RCA30	584	237	-40	30	15-75
RCA30A	584	237	-60	30	15-75
RCA30B	584	237	-80	30	15-75
RCA30C	584	237	-100	30	15-75
RCA31	585	242	40	40	10-50
RCA31A	585	242	60	40	10-50
RCA31B	585	242	80	40	10-50
RCA31C	585	242	100	40	10-50
RCA32	586	247	-40	40	10-50
RCA32A	586	247	-60	40	10-50
RCA32B	586	247	-80	40	10-50
RCA32C	586	247	-100	40	10-50
RCA41	587	252	40	65	15-75
RCA41A	587	252	60	65	15-75
RCA41B	587	252	80	65	15-75
RCA41C	587	252	100	65	15-75
RCA42	588	257	-40	65	15-75
RCA42A	588	257	-60	65	15-75
RCA42B	588	257	-80	65	15-75
RCA42C	588	257	-100	65	15-75
RCA101	557	262	-40	75	25-150
RCA102	557	262	-60	75	25-150
RCA103	557	262	-60	75	30-150
RCA104	557	262	-80	75	30-150
RCA105	556	266	-50	65	25-100
RCA201	557	262	40	75	25-150
RCA202	557	262	60	75	25-150
RCA203	557	262	60	75	30-150
RCA204	557	262	80	75	30-150
RCA205	556	266	50	65	25-100
RCA370	558	270	-30	40	25 min.
RCA371	558	270	-40	40	40 min.
RCA410	509	326	200	125	30-90
RCA411	510	332	300	125	30-90
RCA413	511	338	400	125	20-80
RCA423	512	344	400	125	30-90
RCA431	513	350	400	125	15-35
RCA520	558	270	30	40	25 min.
RCA521	558	270	40	40	40 min.
RCA1000	594	524	60	90	750 min.
RCA1001	594	524	80	90	750 min.
RCA3054	618	53	90	36	25-100
RCA3055	618	53	100	75	20-70
RCA3441	666	77	140	36	20-150
RCA6263	666	77	160	36	20-150

Index to Power Hybrid Circuits

Type No.	File No.	Page No.	Supply Voltage V	Power Dissipation W	Output Current A
HC2000H	566	744	75	35	7
HC2500	681	749	75	⩽100	7

* = V_{CEO} # = V_{CER}

Application Notes for Transistors and Power Hybrid Circuits

HOMETAXIAL-BASE N-P-N POWER TYPES

I_C to 80 A . . . P_T to 300 W . . . V_{CE} to 170 V

I_c = 1.5 A max. P_T = 8.75 W max. (TO-5)*	I_c = 1.5 A max. P_T = 8.75 W max. (TO-5)*	I_c = 3.5 A max. P_T = 10 W max. (TO-5)*	I_c = 4 A max. P_T = 50 W max. (TO-66)**	I_c = 4 A max. P_T = 36 W max. VERSAWATT (TO-220)
90 x 90▲	90 x 90	90 x 90	130 x 130	130 x 130
		Family Designation		
2N1482	40349	2N5786	2N3054	2N5298
40347 V_{CEV}(sus) = 60 V h_{FE} = 25-100 @ 450 mA f_T = 1.5 MHz typ. File No. 88 Page 26	**40349** V_{CEV}(sus) = 160 V h_{FE} = 30-125 @ 150 mA f_T = 1.5 MHz typ. File No. 88 Page 26	**2N5786** V_{CER}(sus) = 45 V h_{FE} = 20-100 @ 1.6 A f_T = 1 MHz min. File No. 413 Page 34	**2N6260** V_{CEV}(sus) = 50 V h_{FE} = 20-100 @ 1.5 A f_T = 0.8 MHz min. P_T = 29 W File No. 527 Page 45	**2N5295** **2N5296** V_{CER}(sus) = 50 V h_{FE} = 30-120 @ 1 A f_T = 0.8 MHz min. File No. 322 Page 61
40348 V_{CEV}(sus) = 90 V h_{FE} = 30-125 @ 300 mA f_T = 1.5 MHz typ. File No. 88 Page 26		**2N5785** V_{CER}(sus) = 65 V h_{FE} = 20-100 @ 1.2 A f_T = 1 MHz min. File No. 413 Page 34	**2N3054** V_{CER}(sus) = 60 V h_{FE} = 25-100 @ 0.5 A f_T = 0.8 MHz min. P_T = 25 W File No. 527 Page 45	**2N5297** **2N5298** V_{CER}(sus) = 70 V h_{FE} = 20-80 @ 1.5 A f_T = 0.8 MHz min. File No. 322 Page 61
		2N5784 V_{CER}(sus) = 80 V h_{FE} = 20-100 @ 1 A f_T = 1 MHz min. File No. 413 Page 34	**2N6261** V_{CER}(sus) = 85 V h_{FE} = 25-100 @ 1.5 A f_T = 0.8 MHz min. P_T = 50 W File No. 527 Page 45	**2N5293** **2N5294** V_{CER}(sus) = 75 V h_{FE} = 30-120 @ 0.5 A f_T = 0.8 MHz min. File No. 322 Page 61

▲Pellet size—values shown are edge dimensions in thousands-of-an-inch (mils)

*Available with:
a. flange for easy heat sinking $R\theta_{JC}$ = 15° C/W
b. free-air radiator $R\theta_{JA}$ = 40-50° C/W

**Available with free-air radiator $R\theta_{JA}$ = 30° C/W

HOMETAXIAL-BASE N-P-N POWER TYPES

I_C to 80 A . . . P_T to 300 W . . . V_{CE} to 170 V

I_c = 3 A max. P_T = 50 W max. (TO-66)**	I_c = 3A max. P_T = 36 W max. VERSAWATT (TO-220)	I_c = 7 A max. P_T = 50 W max. VERSAWATT (TO-220)	I_c = 15 A max. P_T = 150 W max. (TO-3)	I_c = 15 A max. P_T = 150 W max. (TO-3)
130 x 130▲	130 x 130	150 x 150	180 x 180	180 x 180
		Family Designation		
2N3441	TA8343	2N5496	2N3055	2N3055
2N6263 $V_{CER}(sus)$ = 130 V h_{FE} = 20-100 @ 0.5 A f_T = 1.2 MHz typ. P_T = 20 W File No. 529 Page 69	**2N6477** $V_{CER}(sus)$ = 130 V h_{FE} = 25-100 @ 1 A f_T = 0.8 MHz min. File No. 680 Page 83	**2N5491** **2N5490** $V_{CER}(sus)$ = 50 V h_{FE} = 20-100 @ 2 A f_T = 0.8 MHz min. File No. 353 Page 90	**2N6371** $V_{CEV}(sus)$ = 50 V h_{FE} = 15-60 @ 8 A f_T = 1 MHz typ. P_T = 117 W File No. 607 Page 97	**BD181** $V_{CER}(sus)$ = 55 V h_{FE} = 20-70 @ 3 A f_T = 800 kHz min. P_T = 117 W File No. 700 Page 115
2N3441 $V_{CER}(sus)$ = 150 V h_{FE} = 25-100 @ 0.5 A f_T = 1.2 MHz typ. P_T = 25 W File No. 529 Page 69	**2N6478** $V_{CER}(sus)$ = 150 V h_{FE} = 25-100 @ 1 A f_T = 0.8 MHz min. File No. 680 Page 83	**2N5495** **2N5494** $V_{CER}(sus)$ = 50 V h_{FE} = 20-100 @ 3 A f_T = 0.8 MHz min. File No. 353 Page 90	**2N6253** $V_{CER}(sus)$ = 55 V h_{FE} = 20-70 @ 3 A f_T = 0.8 MHz min. P_T = 115 W File No. 524 Page 102	**BD182** $V_{CER}(sus)$ = 70 V h_{FE} = 20-70 @ 4 A f_T = 800 kHz min. P_T = 117 W File No. 700 Page 115
2N6264 $V_{CER}(sus)$ = 170 V h_{FE} = 20-60 @ 1 A f_T = 1.2 MHz typ. P_T = 50 W File No. 529 Page 69		**2N5493** **2N5492** $V_{CER}(sus)$ = 65 V h_{FE} = 20-100 @ 2.5 A f_T = 0.8 MHz min. File No. 353 Page 90	**2N3055** $V_{CER}(sus)$ = 70 V h_{FE} = 20-70 @ 4 A f_T = 0.8 MHz min. P_T = 115 W File No. 524 Page 102	**BD183** $V_{CER}(sus)$ = 85 V h_{FE} = 20-70 @ 3 A f_T = 800 kHz min. P_T = 117 W File No. 700 Page 115
		2N5497 **2N5496** $V_{CER}(sus)$ = 80 V h_{FE} = 20-100 @ 3.5 A f_T = 0.8 MHz min. File No. 353 Page 90	**2N6254** $V_{CER}(sus)$ = 85 V h_{FE} = 20-70 @ 5 A f_T = 0.8 MHz min. P_T = 150 W File No. 524 Page 102	**BD142** $V_{CEV}(sus)$ = 50 V h_{FE} = 12.5 - 160 @ 4 A f_T = 800 kHz min. P_T = 117 W File No. 701 Page 110

▲ Pellet size—values shown are edge dimensions in thousands-of-an-inch (mils)

** Available with free-air radiator $R\theta_{JA}$ = 30° C/W

HOMETAXIAL-BASE N-P-N POWER TYPES

I_C to 80 A . . . P_T to 300 W . . . V_{CE} to 170 V

I_c = 16 A max. P_T = 75 W max. VERSAWATT (TO-220)	I_c = 10 A max. P_T = 150 W max. (TO-3)	I_c = 30 A max. P_T = 250 W max. (TO-3)	I_c = 16 A max. P_T = 250 W max. (TO-3)	I_c = 80 A max. P_T = 300 W max. (Modified TO-3)
180 x 180▲	180 x 180	250 x 250	250 x 250	380 x 380
Family Designation				
2N6103	2N3442	2N3771	2N3773	2N5578
2N6102 2N6103 V_{CER}(sus) = 45 V h_{FE} = 15-60 @ 8 A f_T = 0.8 MHz min. I_c = 16 A max. File No. 485 Page 121	**2N4347** V_{CEV}(sus) = 140 V h_{FE} = 15-60 @ 2 A f_T = 0.8 MHz typ. P_T = 100 W File No. 528 Page 133	**2N6257** V_{CER}(sus) = 45 V h_{FE} = 15-75 @ 8 A f_T = 0.6 MHz min. P_T = 150 W I_c = 20 A File No. 525 Page 141	**2N4348** V_{CEV}(sus) = 140 V h_{FE} = 15-60 @ 5 A f_T = 0.7 MHz typ. P_T = 120 W I_c = 10A File No. 526 Page 149	**2N5575** V_{CEO}(sus) = 50 V h_{FE} = 10-40 @ 60 A f_T = 0.4 MHz min. File No. 359 Page 162
2N6098 2N6099 V_{CER}(sus) = 65 V h_{FE} = 20-80 @ 4 A f_T = 0.8 MHz min. I_c = 10 A max. File No. 485 Page 121	**2N3442** V_{CEV}(sus) = 160 V h_{FE} = 20-70 @ 3 A f_T = 0.8 MHz typ. P_T = 117 W File No. 528 Page 133	**2N3771** V_{CER}(sus) = 45 V h_{FE} = 15-60 @ 15 A f_T = 0.8 MHz min. P_T = 150 W I_c = 30 A File No. 525 Page 141	**2N3773** V_{CEV}(sus) = 160 V h_{FE} = 15-60 @ 8 A f_T = 0.7 MHz typ. P_T = 150 W I_c = 16 A File No. 526 Page 149	**2N5578** V_{CEO}(sus) = 70 V h_{FE} = 10-40 @ 40 A f_T = 0.4 MHz min. File No. 359 Page 162
2N6100 2N6101 V_{CER}(sus) = 75 V h_{FE} = 20-80 @ 5 A f_T = 0.8 MHz min. I_c = 10 A max. File No. 485 Page 121	**2N6262** V_{CEV}(sus) = 170 V h_{FE} = 20-70 @ 3 A f_T = 0.8 MHz min. P_T = 150 W File No. 528 Page 133	**2N3772** V_{CER}(sus) = 70 V h_{FE} = 15-60 @ 10 A f_T = 0.8 MHz min. P_T = 150 W File No. 525 Page 141	**2N6259** V_{CER}(sus) = 160 V h_{FE} = 15-60 @ 8 A f_T = 0.6 MHz min. P_T = 250 W I_c = 16 A File No. 526 Page 149	
BD278 V_{CER}(sus) = 55 V h_{FE} = 15-75 @ 4 A f_T = 0.8 MHz min. I_c = 10 A max. File No. 668 Page 129		**2N6258** V_{CER}(sus) = 85 V h_{FE} = 20-60 @ 15 A f_T = 0.6 MHz min. P_T = 250 W I_c = 30 A File No. 525 Page 141		

▲Pellet size—values shown are edge dimensions in thousands-of-an-inch (mils)

EPITAXIAL-BASE N-P-N and P-N-P POWER TYPES

I_C to 15 A . . . P_T to 200 W . . . V_{CE} to 125 V

I_c = −3.5 max P_T = 10 W max. (TO-5)	I_c = 6 A max. P_T = 40 W max. (TO-66)**	I_c = −6 A max. P_T = 40 W max. (TO-66)**	I_c = 7 A max. P_T = 40 W max. VERSAWATT (TO-220)	I_c = 7 A max. P_T = 40 W max. VERSAWATT (TO-220)
90 x 90▲	90 x 90	90 x 90	90 x 90	90 x 90
Family Designation				
2N5783 [P-N-P]	2N6372 [N-P-N]	2N5954 [P-N-P]	2N6292 [N-P-N]	2N6292 [N-P-N]
2N5783 V_{CER}(sus) = −45 V h_{FE} = 20-100 @ −1.6 A f_T = 8 MHz min. File No. 413 Page 34	**2N6374** V_{CER}(sus) = 45 V h_{FE} = 20-100 @ 3 A f_T = 4 MHz min. File No. 675 Page 170	**2N5956** V_{CER}(sus) = −45 V h_{FE} = 20-100 @ −3 A f_T = 5 MHz min. File No. 675 Page 170	**2N6288** **2N6289** V_{CER}(sus) = 40 V h_{FE} = 30-150 @ 3 A f_T = 4 MHz min. File No. 676 Page 177	**BD239** V_{CER} = 55 V h_{FE} = 40 min. @ 0.2 A f_T = 3 MHz min. File No. 669 Page 193
2N5782 V_{CER}(sus) = −65 V h_{FE} = 20-100 @ −1.2 A f_T = 8 MHz min. File No. 413 Page 34	**2N6373** V_{CER}(sus) = 65 V h_{FE} = 20-100 @ 2.5 A f_T = 4 MHz min. File No. 675 Page 170	**2N5955** V_{CER}(sus) = −65 V h_{FE} = 20-100 @ −2.5 A f_T = 5 MHz min. File No. 675 Page 170	**2N6290** **2N6291** V_{CER}(sus) = 60 V h_{FE} = 30-150 @ 2.5 A f_T = 4 MHz min. File No. 676 Page 177	**BD239A** V_{CER} = 70 V h_{FE} = 40 min. @ 0.2 A f_T = 3 MHz min. File No. 669 Page 193
2N5781 V_{CER}(sus) = −80 V h_{FE} = 20-100 @ −1 A f_T = 8 MHz min. File No. 413 Page 34	**2N6372** V_{CER}(sus) = 85 V h_{FE} = 20-100 @ 2 A f_T = 4 MHz min. File No. 675 Page 170	**2N5954** V_{CER}(sus) = −85 V h_{FE} = 20-100 @ −2 A f_T = 5 MHz min. File No. 675 Page 170	**2N6292** **2N6293** V_{CER}(sus) = 80 V h_{FE} = 30-150 @ 2 A f_T = 4 MHz min. File No. 676 Page 177	**BD239B** V_{CER} = 90 V h_{FE} = 40 min. @ 0.2 A f_T = 3 MHz min. File No. 669 Page 193
		2N6467 V_{CER}(sus) = −105 V h_{FE} = 20-100 @ −1 A f_T = 5 MHz min. File No. 675 Page 170	**2N6473** V_{CER}(sus) = 110 V h_{FE} = 30-150 @ 1.5 A f_T = 5 MHz typ. File No. 676 Page 177	**BD239C** V_{CER} = 115 V h_{FE} = 40 min. @ 0.2 A f_T = 3 MHz min. File No. 669 Page 193
		2N6468 V_{CER}(sus) = −125 V h_{FE} = 20-100 @ −1 A f_T = 5 MHz min. File No. 675 Page 170	**2N6474** V_{CER}(sus) = 130 V h_{FE} = 30-150 @ 1 A f_T = 5 MHz typ. File No. 676 Page 177	

▲Pellet size—values shown are edge dimensions in thousands-of-an-inch (mils).

**Available with free-air radiator $R\theta_{JA}$ = 30° C/W

EPITAXIAL-BASE N-P-N and P-N-P TYPES

I_C to 15 A . . . P_T to 200 W . . . V_{CE} to 125 V

I_c = −7A max. P_T = 40 W max. VERSAWATT (TO-220)	I_c = 7 A max. P_T = 40 W max. VERSAWATT (TO-220)	I_c = −7 A max. P_T = 40 W max. VERSAWATT (TO-220)	I_c = −7 A max. P_T = 40 W max. VERSAWATT (TO-220)	I_c = 15 A max. P_T = 125 W max. (TO-3)
90 x 90▲	90 x 90	90 x 90	90 x 90	150 x 150
Family Designation				
2N6107 [P-N-P]	2N6292 [N-P-N]	2N6107 [P-N-P]	2N6107 [P-N-P]	TA8441 [N-P-N]
BD240 V_{CER} = −55 V h_{FE} = 40 min. @ −0.2 A f_T = 3 MHz min. File No. 670 Page 197	**BD241** V_{CER} = 55 V h_{FE} = 25 min. @ 1 A f_T = 3 MHz min. File No. 671 Page 201	**BD242** V_{CER} = −55 V h_{FE} = 25 min. @ −1 A f_T = 3 MHz min. File No. 672 Page 205	**2N6110** **2N6111** V_{CER}(sus) = −40 V h_{FE} = 30-150 @ −3 A f_T = 10 MHz min. File No. 676 Page 177	**2N6470** V_{CER}(sus) = 45 V h_{FE} = 20-100 @ 5 A f_T = 5 MHz typ. File No. 677 Page 217
BD240A V_{CER} = −70 V h_{FE} = 40 min. @ −0.2 A f_T = 3 MHz min. File No. 670 Page 197	**BD241A** V_{CER} = 70 V h_{FE} = 25 min. @ 1 A f_T = 3 MHz min. File No. 671 Page 201	**BD242A** V_{CER} = −70 V h_{FE} = 25 min. @ −1 A f_T = 3 MHz min. File No. 672 Page 205	**2N6108** **2N6109** V_{CER}(sus) = −60 V h_{FE} = 30-150 @ −2.5 A f_T = 10 MHz min. File No. 676 Page 177	**2N6471** V_{CER}(sus) = 65 V h_{FE} = 20-100 @ 7 A f_T = 5 MHz typ. File No. 677 Page 217
BD240B V_{CER} = −90 V h_{FE} = 40 min. @ −0.2 A f_T = 3 MHz min. File No. 670 Page 197	**BD241B** V_{CER} = 90 V h_{FE} = 25 min. @ 1 A f_T = 3 MHz min. File No. 671 Page 201	**BD242B** V_{CER} = −90 V h_{FE} = 25 min. @ −1 A f_T = 3 MHz min. File No. 672 Page 205	**2N6106** **2N6107** V_{CER}(sus) = −80 V h_{FE} = 30-150 @ −2 A f_T = 10 MHz min. File No. 676 Page 177	**2N6472** V_{CER}(sus) = 85 V h_{FE} = 20-100 @ 6 A f_T = 5 MHz typ. File No. 677 Page 217
BD240C V_{CER} = −115 V h_{FE} = 40 min. @ −0.2 A f_T = 3 MHz min. File No. 670 Page 197	**BD241C** V_{CER} = 115 V h_{FE} = 25 min. @ 1 A f_T = 3 MHz min. File No. 671 Page 201	**BD242C** V_{CER} = −115 V h_{FE} = 25 min. @ −1 A f_T = 3 MHz min. File No. 672 Page 205	**2N6475** V_{CER}(sus) = −110 V h_{FE} = 30-150 @ −1.5 A f_T = 5 MHz typ. File No. 676 Page 177	
		BD277 V_{CEO} = −45 V h_{FE} = 30-150 @ −1.75 A f_T = 10 MHz min. File No. 667 Page 205	**2N6476** V_{CER}(sus) = −130 V h_{FE} = 30-150 @ −1 A f_T = 5 MHz typ. File No. 676 Page 177	

▲Pellet size—values shown are edge dimensions in thousands-of-an-inch (mils).

EPITAXIAL-BASE N-P-N and P-N-P POWER TYPES

I_C to 15 A . . . P_T to 200 W . . . V_{CE} to 125 V

I_c = −15 A max. P_T = 125 W max. (TO-3)	I_c = 15 A max. P_T = 75 W max. VERSAWATT (TO-220)	I_c = 15 A max. P_T = 75 W max. VERSAWATT (TO-220)	I_c = −15 A max. P_T = 75 W max. VERSAWATT (TO-220)	I_c = −15 A max. P_T = 75 W max. VERSAWATT (TO-220)
150 x 150▲	150 x 150	150 x 150	150 x 150	150 x 150
Family Designation				
2N6248 [P-N-P]	TA8323 [N-P-N]	TA8323 [N-P-N]	TA8326 [P-N-P]	TA8326 [P-N-P]
2N6469 $V_{CER}(sus)$ = −45 V h_{FE} = 20-100 @ −5 A f_T = 6 MHz min. File No. 677 Page 217	**2N6486** $V_{CER}(sus)$ = 50 V h_{FE} = 30-150 @ 6 A f_T = 5 MHz typ. File No. 678 Page 226	**BD243** V_{CER} = 55 V h_{FE} = 30 min. @ 0.3 A f_T = 3 MHz min. File No. 673 Page 209	**2N6489** $V_{CER}(sus)$ = −50 V h_{FE} = 30-150 @ −6 A f_T = 5 MHz typ. File No. 678 Page 226	**BD244** V_{CER} = −55 V h_{FE} = 30 min. @ −0.3 A f_T = 3 MHz min. File No. 674 Page 213
2N6246 $V_{CER}(sus)$ = −65 V h_{FE} = 20-100 @ −7 A f_T = 6 MHz min. File No. 677 Page 217	**2N6487** $V_{CER}(sus)$ = 70 V h_{FE} = 30-150 @ 5 A f_T = 5 MHz typ. File No. 678 Page 226	**BD243A** V_{CER} = 70 V h_{FE} = 30 min. @ 0.3 A f_T = 3 MHz min. File No. 673 Page 209	**2N6490** $V_{CER}(sus)$ = −70 V h_{FE} = 30-150 @ −5 A f_T = 5 MHz typ. File No. 678 Page 226	**BD244A** V_{CER} = −70 V h_{FE} = 30 min. @ −0.3 A f_T = 3 MHz min. File No. 674 Page 213
2N6247 $V_{CER}(sus)$ = −85 V h_{FE} = 20-100 @ −6 A f_T = 6 MHz min. File No. 677 Page 217	**2N6488** $V_{CER}(sus)$ = 90 V h_{FE} = 30-150 @ 4 A f_T = 5 MHz typ. File No. 678 Page 226	**BD243B** V_{CER} = 90 V h_{FE} = 30 min. @ 0.3 A f_T = 3 MHz min. File No. 673 Page 209	**2N6491** $V_{CER}(sus)$ = −90 V h_{FE} = 30-150 @ −4 A f_T = 5 MHz typ. File No. 678 Page 226	**BD244B** V_{CER} = −90 V h_{FE} = 30 min. @ −0.3 A f_T = 3 MHz min. File No. 674 Page 213
2N6248 $V_{CER}(sus)$ = −105 V h_{FE} = 20-100 @ −5 A f_T = 6 MHz min. File No. 677 Page 217		**BD243C** V_{CER} = 115 V h_{FE} = 30 min. @ 0.3 A f_T = 3 MHz min. File No. 673 Page 209		**BD244C** V_{CER} = −115 V h_{FE} = 30 min. @ −0.3 A f_T = 3 MHz min. File No. 674 Page 213

▲Pellet size—values shown are edge dimensions in thousands-of-an-inch (mils).

HIGH-VOLTAGE N-P-N and P-N-P POWER TYPES
I_C to 30 A . . . f_T to 20 MHz . . . P_T to 175 W

I_c = 1 A max. P_T = 20 W max. (Plastic TO-5)	I_c = 1 A max. P_T = 10 W max. (TO-39)*	I_c = −1 A max. P_T = 10 W max. (TO-5)*	I_c = −1 A max. P_T = 10 W max. (TO-39)	I_c = 5 A max. P_T = 35 W max. (TO-66)**	I_c = −5 A max. P_T = 35 W max. (TO-66)**
32 x 32▲	42 x 42	42 x 42	42 x 42	103 x 103	125 x 125
Family Designation					
2N6177 [N-P-N]	2N3439● [N-P-N]	2N5415 [P-N-P]	2N5415 [P-N-P]	2N3585 [N-P-N]	2N6214 [P-N-P]
2N6175 **40885■** "Plastic 2N3440" V_{CER}(sus) = 300 V h_{FE} = 30-190 @ 20 mA f_T = 20 MHz min. File No. 508 Page 278	**2N3440** V_{CER}(sus) = 300 V h_{FE} = 40-160 @ 20 mA f_T = 15 MHz min. File No. 64 Page 286	**2N5415** V_{CEO}(sus) = −200 V h_{FE} = 30-150 @ −50 mA f_T = 15 MHz min. File No. 336 Page 292	**BFT19** V_{CER}(sus) = −200 V h_{FE} = 20 min. @ −10 mA f_T = 25 MHz min. File No. 683 Page 298	**2N3583** V_{CER}(sus) = 250 V h_{FE} = 40 min. @ 100 mA h_{FE} = 10 min. @ 1 A f_T = 15 MHz min. File No. 138 Page 304	**2N6211** V_{CER}(sus) = −250 V h_{FE} = 10-100 @ −1 A f_T = 20 MHz min. File No. 507 Page 312
2N6176 **40886■** V_{CER}(sus) = 350 V h_{FE} = 30-150 @ 20 mA f_T = 20 MHz min. File No. 508 Page 278	**2N3439** V_{CER}(sus) = 400 V h_{FE} = 40-160 @ 20 mA f_T = 15 MHz min. File No. 64 Page 286	**2N5416** V_{CER}(sus) = −350 V h_{FE} = 30-120 @ −50 mA f_T = 15 MHz min. File No. 336 Page 292	**BFT19A** V_{CER}(sus) = −300 V h_{FE} = 20 min. @ −10 mA f_T = 25 MHz min. File No. 683 Page 298	**2N3584** V_{CER}(sus) = 300 V h_{FE} = 40 min. @ 100 mA h_{FE} = 25-100 @ 1 A f_T = 15 MHz min. File No. 138 Page 304	**2N6212** V_{CER}(sus) = −325 V h_{FE} = 10-100 @ −1 A f_T = 20 MHz min. File No. 507 Page 312
2N6177 **40887■** "Plastic 2N3439" V_{CER}(sus) = 400 V h_{FE} = 30-150 @ 50 mA f_T = 20 MHz min. File No. 508 Page 278			**BFT19B** V_{CER}(sus) = −400 V h_{FE} = 20 min. @ −10 mA f_T = 25 MHz min. File No. 683 Page 298	**2N3585** V_{CER}(sus) = 400 V h_{FE} = 40 min. @ 100 mA h_{FE} = 25-100 @ 1 A f_T = 15 MHz min. File No. 138 Page 304	**2N6213** V_{CER}(sus) = −375 V h_{FE} = 10-100 @ −1 A f_T = 20 MHz min. File No. 507 Page 312
				2N4240 V_{CER}(sus) = 400 V h_{FE} = 40 min. @ 100 mA h_{FE} = 30-150 @ 750 mA f_T = 15 MHz min. File No. 138 Page 304	**2N6214** V_{CER}(sus) = −425 V h_{FE} = 10-100 @ −1 A f_T = 20 MHz min. File No. 507 Page 312
				40850 V_{CER}(sus) = 400 V h_{FE} = 25 min. @ 750 mA f_T = 15 MHz min. File No. 498 Page 368	

▲ Pellet size—values shown are edge dimensions in thousands-of-an-inch (mils)

* Available with:
a. flange for easy heat sinking $R\theta_{JC}$ = 15° C/W
b. free-air radiator $R\theta_{JA}$ = 45° C/W

** Available with free-air radiator $R\theta_{JA}$ = 30° C/W

■ Type with a factory-attached heat clip

● These transistors are also available in TO-5 packages in U.S.A., Canada, Latin America, and Far East.

HIGH-VOLTAGE N-P-N and P-N-P POWER TYPES

I_C to 30 A . . . f_T to 20 MHz . . . P_T to 175 W

I_c = 10 A peak P_T = 45 W max. (TO-66)**	I_c = 10 A peak P_T = 125 W max. (TO-3)	I_c = 10 A peak P_T = 100 W max. (TO-3) Switching	Linear	I_c = 15 A peak P_T = 110 W max. (TO-3)	I_c = 30 A peak P_T = 175 W max. (TO-3) Switching
130 x 130▲	130 x 130	130 x 130	130 x 130	210 x 210	260 x 260
Family Designation 2N6079 [N-P-N]	2N5840 [N-P-N]	2N5840 [N-P-N]	2N5240 [N-P-N]	2N5804 [N-P-N]	2N6251 [N-P-N]
2N6078 V_{CER}(sus) = 275 V h_{FE} = 12-70 @ 1.2A t_r = 0.3 µs typ. t_f = 0.3 µs typ. File No. 492 Page 318	**RCA 410#** V_{CEO}(sus) = 200 V h_{FE} = 30-90 @ 1 A t_r = 0.35 µs typ. t_f = 0.15 µs typ. File No. 509 Page 326	**2N5838** V_{CER}(sus) = 275 V h_{FE} = 20 min. @ 0.5 A h_{FE} = 8-40 @ 3 A t_r = 0.8 µs typ. t_f = 0.4 µs typ. File No. 410 Page 356	**2N5239** V_{CER}(sus) = 250 V h_{FE} = 20 min. @ 2 A h_{FE} = 20-80 @ 0.4 A f_T = 5 MHz min. File No. 321 Page 373	**2N5804** V_{CER}(sus) = 300 V h_{FE} = 25-250 @ 0.5 A h_{FE} = 10-100 @ 5 A t_r = 0.4 µs typ. t_f = 1.2 µs typ. File No. 407 Page 379	**2N6249** V_{CER}(sus) = 225 V h_{FE} = 10-50 @ 10 A t_r = 0.8 µs typ. t_f = 0.5 µs typ. File No. 523 Page 385
2N6077 V_{CER}(sus) = 300 V h_{FE} = 12-70 @ 1.2 A t_r = 0.3 µs typ. t_f = 0.3 µs typ. File No. 492 Page 318	**RCA 411#** V_{CEO}(sus) = 300 V h_{FE} = 30-90 @ 1 A t_r = 0.35 µs typ. t_f = 0.15 µs typ. File No. 510 Page 332	**2N5839** V_{CER}(sus) = 300 V h_{FE} = 20 min. @ 0.5 A h_{FE} = 10-50 @ 2 A t_r = 0.6 µs typ. t_f = 0.35 µs typ. File No. 410 Page 356	**2N5240** V_{CER}(sus) = 350 V h_{FE} = 20 min. @ 2 A h_{FE} = 20-80 @ 0.4 A f_T = 5 MHz min. File No. 321 Page 373	**2N5805** V_{CER}(sus) = 375 V h_{FE} = 25-250 @ 0.5 A h_{FE} = 10-100 @ 5 A t_r = 0.4 µs typ. t_f = 1.2 µs typ. File No. 407 Page 379	**2N6250** V_{CER}(sus) = 300 V h_{FE} = 8-50 @ 10 A t_r = 0.8 µs typ. t_f = 0.5 µs typ. File No. 523 Page 385
2N6079 V_{CER}(sus) = 375 V h_{FE} = 12-50 @ 1.2 A t_r = 0.3 µs typ. t_f = 0.3 µs typ. File No. 492 Page 318	**RCA 413#** V_{CEO}(sus) = 325 V h_{FE} = 20-80 @ 0.5 A t_r = 0.35 µs typ. t_f = 0.15 µs typ. File No. 511 Page 338	**BU106** V_{CEV}(sus) = 325 V h_{FE} = 8 min. @ 4 A t_s = 3 µs max. t_f = 1.5 µs max. File No. 716 Page 363		**40853** V_{CER}(sus) = 375 V h_{FE} = 10 min. @ 5 A t_r = 0.4 µs typ. t_f = 1.2 µs typ. File No. 498 Page 368	**2N6251** V_{CER}(sus) = 375 V h_{FE} = 6-50 @ 10 A t_r = 0.8 µs typ. t_f = 0.5 µs typ. File No. 523 Page 385
40851 V_{CER}(sus) = 375 V h_{FE} = 12 min. @ 1.2 A t_r = 0.3 µs typ. t_f = 0.3 µs typ. File No. 498 Page 368	**RCA 423#** V_{CEO}(sus) = 325 V h_{FE} = 30-90 @ 1 A t_r = 0.35 µs typ. t_f = 0.15 µs typ. File No. 512 Page 344	**2N5840** V_{CER}(sus) = 375 V h_{FE} = 20 min. @ 0.5 A h_{FE} = 10-50 @ 2 A t_r = 0.6 µs typ. t_f = 0.35 µs typ. File No. 410 Page 356			**40854** V_{CER}(sus) = 325 V h_{FE} = 8 min. @ 10 A t_r = 0.8 µs typ. t_f = 0.5 µs typ. File No. 498 Page 368
	RCA 431# V_{CEO}(sus) = 325 V h_{FE} = 15-35 @ 2.5 A t_r = 0.35 µs typ. t_f = 0.15 µs typ. File No. 513 Page 350	**40852** V_{CER}(sus) = 375 V h_{FE} = 12 min. @ 1.2 A t_r = 0.5 µs typ. t_f = 0.35 µs typ. File No. 498 Page 368			

▲Pellet size—values shown are edge dimensions in thousands-of-an-inch (mils)

#For new equipment design only—not recommended for retrofit.

HIGH-SPEED SWITCHING N-P-N and P-N-P POWER TYPES

f_T to 250 MHz . . . I_C to 60 A . . . P_T to 140 W

I_c = 1 A max. P_T = 5 W max. (TO-39)*	I_c = −1 A max. P_T = 7 W max. (TO-39)*	I_c = 2 A max. P_T = 5 W max. (Lo Profile TO-39)	I_c = 2 A max. P_T = 10 W max. (TO-39)*	I_c = −2 A max. P_T = 10 W max. (TO-39)*	I_c = 2 A max. P_T = 25 W max. (Plastic TO-5)
30 x 30▲	30 x 30	32 x 32	42 x 42	42 x 42	42 x 42
Family Designation					
2N2102● [N-P-N]	2N4036● [P-N-P]	2N5262 [N-P-N]	2N5320● [N-P-N]	2N5322● [P-N-P]	2N6179 [N-P-N]
2N3053 $V_{CER}(sus)$ = 50 V h_{FE} = 50-250 @ 150 mA f_T = 100 MHz min. File No. 432 Page 404	**2N4037** $V_{CER}(sus)$ = −60 V h_{FE} = 50-250 @ −150 mA f_T = 60 MHz min. File No. 216 Page 410	**2N5189** $V_{CEO}(sus)$ = 35 V h_{FE} = 15 min. @ 1 A f_T = 250 MHz min. t_{on} = 40 ns max. t_{off} = 70 ns max. File No. 296 Page 418	**2N5321** $V_{CER}(sus)$ = 65 V h_{FE} = 40-250 @ 500 mA f_T = 50 MHz min. t_{on} = 80 ns max. t_{off} = 800 ns max. File No. 325 Page 429	**2N5323** $V_{CER}(sus)$ = −65 V h_{FE} = 40-250 @ −500 mA f_T = 50 MHz min. File No. 325 Page 429	**2N6179** "Plastic 2N5321" $V_{CER}(sus)$ = 65 V h_{FE} = 40-250 @ 500 mA f_T = 50 MHz min. t_{on} = 80 ns max. t_{off} = 800 ns max. File No. 562 Page 435
2N2102 $V_{CER}(sus)$ = 80 V h_{FE} = 40-120 @ 150 mA f_T = 120 MHz min. File No. 106 Page 498	**2N4036** $V_{CER}(sus)$ = −85 V h_{FE} = 40-140 @ −150 mA f_T = 60 MHz min. File No. 216 Page 410	**2N5262** $V_{CEO}(sus)$ = 50 V h_{FE} = 25 min. @ 1 A f_T = 250 MHz min. t_{on} = 30 ns max. t_{off} = 60 ns max. File No. 313 Page 423	**2N5320** $V_{CER}(sus)$ = 90 V h_{FE} = 30-130 @ 500 mA f_T = 50 MHz min. t_{on} = 80 ns max. t_{off} = 800 ns max. File No. 325 Page 429	**2N5322** $V_{CER}(sus)$ = −90 V h_{FE} = 30-130 @ −500 mA h_{FE} = 10 min. @ −1A f_T = 50 MHz min. File No. 325 Page 429	**2N6178** "Plastic 2N5320" $V_{CER}(sus)$ = 90 V h_{FE} 30-130 @ 500 mA f_T = 50 MHz min. t_{on} = 80 ns max. t_{off} = 800 ns max. File No. 562 Page 435
	2N4314 $V_{CER}(sus)$ = −85 V h_{FE} = 50-250 @ −150 mA f_T = 60 MHz min. File No. 216 Page 410				

▲Pellet size—values shown are edge dimensions in thousands-of-an-inch (mils).

*Available with:
a. flange for easy heat sinking $R\theta_{JC}$ = 15° C/W
b. free-air radiator $R\theta_{JA}$ = 50° C/W

●These transistors are also available in TO-5 packages in U.S.A., Canada, Latin America, and Far East.

HIGH-SPEED SWITCHING N-P-N and P-N-P POWER TYPES

f_T to 250 MHz . . . I_C to 60 A . . . P_T to 140 W

I_c = −2A max. P_T = 25 W max. (Plastic TO-5)	I_c = 7 A max. P_T = 35 W max. (TO-66)**	I_c = 15 A max. P_T = 85 W max. (Radial)	I_c = 20 A max. P_T = 140 W max. (TO-3)	I_c = 25 A max. P_T = 125 W max. (TO-63)	I_c = 30 A max. P_T = 140 W max. (TO-3)	I_c = 60 A max. P_T = 140 W max. (Modified TO-3)
42 x 42▲	103 x 103	155 x 155	146 x 183	215 x 222	220 x 220	220 x 220 [2 CHIPS]
			Family Designation			
2N6181 [P-N-P]	2N3879 [N-P-N]	TA8007 [N-P-N]	2N5038 [N-P-N]	2N3263 [N-P-N]	2N5671 [N-P-N]	2N6033 [N-P-N]
2N6181 "Plastic 2N5323" $V_{CER}(sus)$ = −65 V h_{FE} = 40-250 @ −500 mA f_T = 50 MHz min. File No. 562 Page 435	**2N3878‡** $V_{CER}(sus)$ = 60 V h_{FE} = 20 min. @ 4 A h_{FE} = 50-200 @ 0.5 A f_T = 60 MHz min. t_r = 400 ns max. t_f = 400 ns max. File No. 299 Page 443	**2N6479** (Isolated Collector) **2N6481** (Non Isolated Coll.) $V_{CER}(sus)$ = 80 V h_{FE} = 20 min. @ 12 A f_T = 100 MHz typ. Radiation Hard File No. 702 Page 454	**2N5039** $V_{CER}(sus)$ = 95 V h_{FE} = 20 min. @ 10 A h_{FE} = 30-150 @ 2 A f_T = 60 MHz min. t_{on} = 0.5 µs max. t_{off} = 2 µs max. File No. 698 Page 461	**2N3266** **2N3264■** $V_{CER}(sus)$ = 80 V h_{FE} = 20-80 @ 15 A f_T = 20 MHz min. t_{on} = 0.5 µs max. t_{off} = 2 µs max. File No. 54 Page 475	**2N5671** $V_{CER}(sus)$ = 110 V h_{FE} = 20 min. @ 20 A h_{FE} = 20-100 @ 15 A f_T = 50 MHz min. t_{on} = 0.5 µs max. t_{off} = 2 µs max. File No. 383 Page 481	**2N6032** $V_{CER}(sus)$ = 110 V h_{FE} = 10-50 @ 50 A f_T = 50 MHz min. t_r = 1 µs max. t_f = 0.5 µs max. File No. 462 Page 487
2N6180 "Plastic 2N5322" $V_{CER}(sus)$ = −90 V h_{FE} = 30-130 @ −500 mA h_{FE} = 10 min. @ −1 A f_T = 50 MHz min. File No. 562 Page 435	**2N3879** $V_{CER}(sus)$ = 90 V h_{FE} = 40 min. @ 0.4 A h_{FE} = 20-80 @ 4 A f_T = 60 MHz min. t_r = 400 ns max. t_f = 400 ns max. File No. 299 Page 443	**2N6480** (Isolated Collector) **2N6482** (Non Isolated Coll.) $V_{CER}(sus)$ = 80 V h_{FE} = 20 min. @ 12 A f_T = 100 MHz typ. Radiation Hard File No. 702 Page 454	**2N5038** $V_{CER}(sus)$ = 110 V h_{FE} = 20 min. @ 12 A h_{FE} = 50-200 @ 2 A f_T = 60 MHz min. t_{on} = 0.5 µs max. t_{off} = 2 µs max. File No. 698 Page 461	**2N3265** **2N3263■** $V_{CER}(sus)$ = 110 V h_{FE} = 25-75 @ 15 A f_T = 20 MHz min. t_{on} = 0.5 µs max. t_{off} = 2 µs max. File No. 54 Page 475	**2N5672** $V_{CER}(sus)$ = 140 V h_{FE} = 20 min. @ 20 A h_{FE} = 20-100 @ 15 A f_T = 50 MHz min. t_{on} = 0.5 µs max. t_{off} = 2 µs max. File No. 383 Page 481	**2N6033** $V_{CER}(sus)$ = 140 V h_{FE} = 10-50 @ 40 A f_T = 50 MHz min. t_r = 1 µs max. t_f = 0.5 µs max. File No. 462 Page 487
	2N5202 $V_{CER}(sus)$ = 75 V h_{FE} = 10-100 @ 4 A f_T = 60 MHz min. t_r = 400 ns max. t_f = 400 ns max. File No. 299 Page 443		**2N6496** $V_{CER}(sus)$ = 130 V h_{FE} = 12-100 @ 8 A f_T = 60 MHz min. t_r = 0.5 µs max. t_s = 1.5 µs max. t_f = 0.5 µs max. File No. 698 Page 461			
			2N6354 $V_{CER}(sus)$ = 130 V h_{FE} = 20-150 @ 5 A h_{FE} = 10-100 @ 10 A f_T = 80 MHz min. t_r = 0.3 µs max. t_f = 0.2 µs max. I_c = 12 A peak File No. 582 Page 469			

▲Pellet size—values shown are edge dimensions in thousands-of-an-inch (mils).

**Available with free-air radiator $R\theta_{JA}$ = 30° C/W

‡Also available with heat radiator (40375).

■Flat radial lead version.

TYPES FOR AUDIO-FREQUENCY LINEAR AMPLIFIERS

Power Output (8 Ω Imped.)	Bull. File No.	Circuit No.	Output Transistors N-P-N	Output Transistors P-N-P	Class B Driver Transistors N-P-N	Class B Driver Transistors P-N-P	V_{BE} Mult. (Bias)
12 W	642	A012B (True Comp.)	RCA1C10 (2N6292)	RCA1C11 (2N6107)	–	–	–
	642	A012D (IC Driving True Comp.)	RCA1C10 (2N6292)	RCA1C11 (2N6107)	–	–	–
25 W	643	A025C (Quasi-Comp.)	RCA1C14 [2] (2N5496)	–	RCA1A06 (2N2102)	RCA1A05 (2N4036)	–
	644	A025B (Full-Comp.)	RCA1C05 (2N6292)	RCA1C06 (2N6107)	RCA1A06 (2N2102)	RCA1A05 (2N4036)	–
40 W	645	A040C (Quasi-Comp.)	RCA1C09 [2] (2N6103)	–	RCA1A06 (2N2102)	RCA1A05 (2N4036)	
	646	A040B (Full-Comp.)	RCA1C07 (TA8323)	RCA1C08 (TA8326)	RCA1A06 (2N2102)	RCA1A05 (2N4036)	–
70 W	647	A070A (Quasi-Comp.) Hom. Output)	RCA1B01 [2] (2N3055)	–	RCA1A03 (2N5320)	RCA1A04 (2N5322)	–
	648	A070C (Quasi-Comp.)	RCA1B06 [2] (2N5840)	–	RCA1C03 (2N6474)	RCA1A04 (2N6476)	RCA1A18 (2N2102)
120 W	649	A120C (Quasi-Comp. Parallel Output)	RCA1B04 [4] (2N5240)	–	RCA1C12 (2N6474)	RCA1C13 (2N6476)	RCA1A18 (2N2102)
200 W	650	A200C (Quasi-Comp. Parallel Output)	RCA1B05 [6] (2N5240)	–	RCA1B05 [2] (2N5240)	–	RCA1A18 (2N2102)

Numbers in brackets indicate number of devices used in the stage.
Type numbers in parentheses indicate the transistor-family designation.

Typical Power Output for 4 Ω and 16 Ω Load for AF Linear Amplifiers

Amplifier Circuit No.	A012B		A012D		A025A		A025B		A040A		A040B		A070A		A070C		A120C		A200C	
Impedance – Ω (Load)	4	16	4	16	4	16	4	16	4	16	4	16	4	16	4	16	4	16	4	16
Typical Power Output – W	12*	6.5	9*	6.5	45	16	45	16	55	25	75	25	100	40	100	50	180	80	300	130

*Power output limited by driver-circuit capability.

TYPES FOR AUDIO-FREQUENCY LINEAR AMPLIFIERS

Class B Pre-Driver Transistors N-P-N	Class B Pre-Driver Transistors P-N-P	Protection Circuit N-P-N	Protection Circuit P-N-P	Class A Pre-Driver Transistors N-P-N	Class A Pre-Driver Transistors P-N-P	Input Devices
–	–	–	–	–	RCA1A08 (2N4036)	RCA1A07 [2] (2N2102)
–	–	–	–	–		CA3094AT
–	–	RCA1A18 (2N2102)	RCA1A19 (2N4036)	RCA1A01 (2N2102)		RCA1A02 [2] (2N4036)
–	–	RCA1A18 (2N2102)	RCA1A19 (2N4036)	RCA1A01 (2N2102)		RCA1A02 [2] (2N4036)
–	–	RCA1A18 (2N2102)	RCA1A19 (2N4036)	RCA1A01 (2N2102)		RCA1A02 [2] (2N4036)
–	–	RCA1A18 (2N2102)	RCA1A19 (2N4036)	RCA1A01 (2N2102)		RCA1A02 [2] (2N4036)
–	–	RCA1A18 (2N2102)	RCA1A19 (2N4036)	RCA1A17 (2N2102)		RCA1A02 [2] (2N4036)
–	–	RCA1A18 (2N2102)	RCA1A19 (2N4036)	RCA1A15■ [2] (2N3439)	RCA1A16 [2] (2N5415)	RCA1A17 [2] (2N2102)
–	–	RCA1A18 (2N2102)	RCA1A19 (2N4036)	RCA1A09■ [2] (2N3439)	RCA1A10 [2] (2N5415)	RCA1A11 [2] (2N3439)
RCA1E02 (1N3585)	RCA1E03 (2N6211)	RCA1A18 (2N2102)	RCA1A19 (2N4036)	RCA1A09■ [2] (2N3439)	RCA1A10 [2] (2N5415)	RCA1A11 [2] (2N3439)

■Current Source

Other applications for the types above. . .
Audio Power Amplifiers–Linear Modulators–Servo Amplifiers–Operational Amplifiers

MONOLITHIC DARLINGTON TYPES

I_C to 10 A . . . P_T to 100 W . . . h_{FE} to 1000 min.

I_c = 8 A max. P_T = 90 W max. (TO-3)	I_c = 8 A max. PT = 100 W max. (TO-3)	I_c = 10 A max. PT = 100 W max. (TO-3)	I_c = 10 A max. P_T = 40 W max. VERSAWATT (TO-220)	I_c = 10 A max. P_T = 40 W max. VERSAWATT (TO-220)	I_c = −15 A max. P_T = 40 W max. VERSAWATT (TO-220)
90 x 90▲	136 x 136	136 x 136	136 x 136	136 x 136	136 x 136
Family Designation					
2N6385 [N-P-N]	2N6385 [N-P-N]	2N6385 [N-P-N]	2N6388 [N-P-N]	2N6388 [N-P-N]	TA8203 [P-N-P]
RCA1000 $V_{CEO}(sus)$ = 60 V h_{FE} = 1000 min. @ 3 A t_{on} = 1 μs typ. t_f = 3 μs typ. t_s = 1 μs typ. File No. 594 Page 524	**2N6055** $V_{CEO}(sus)$ = 60 V h_{FE} = 750 min. @ 4 A t_{on} = 1 μs typ. t_f = 3 μs typ. t_s = 1 μs typ. File No. 563 Page 527	**2N6383** $V_{CEO}(sus)$ = 40 V h_{FE} = 1000 min. @ 5 A t_{on} = 1 μs typ. t_f = 3 μtyp. t_s = 1 μs typ. File No. 609 Page 532	**2N6386** $V_{CEO}(sus)$ = 40 V h_{FE} = 1000 min. @ 3 A t_{on} = 1 μs typ. t_f = 3 μs typ. t_s = 1 μs typ. File No. 610 Page 538	**BDX33** $V_{CEO}(sus)$ = 45 V h_{FE} = 750 min. @ 4 A FileNo. 693 Page 545	**BDX34** $V_{CEO}(sus)$ = −45 V h_{FE} = 750 min. @ −4 A File No. 694 Page 551
RCA1001 $V_{CEO}(sus)$ = 80 V h_{FE} = 1000 min. @ 3 A t_{on} = 1 μs typ. t_f = 3 μs typ. t_s = 1 μs typ. File No. 594 Page 524	**2N6056** $V_{CEO}(sus)$ = 80 V h_{FE} = 750 min. @ 4 A t_{on} = 1 μs typ. t_f = 3 μs typ. t_s = 1 μs typ. File No. 563 Page 527	**2N6384** $V_{CEO}(sus)$ = 60 V h_{FE} = 1000 min. @ 5 A t_{on} = 1 μs typ. t_f = 3 μs typ. t_s = 1 μs typ. File No. 609 Page 532	**2N6387** $V_{CEO}(sus)$ = 60 V h_{FE} = 1000 min. @ 5 A t_{on} = 1 μs typ. t_f = 3 μs typ. t_s = 1 μs typ. File No. 610 Page 538	**BDX33A** $V_{CEO}(sus)$ = 60 V h_{FE} = 750 min @ 4 A File No. 693 Page 545	**BDX34A** $V_{CEO}(sus)$ = −60 V h_{FE} = 750 min @ −4A File No. 694 Page 551
		2N6385 $V_{CEO}(sus)$ = 80 V h_{FE} = 1000 min. @ 5 A t_{on} = 1 μs typ. t_f = 3 μs typ. t_s = 1 μs typ. File No. 609 Page 532	**2N6388** $V_{CEO}(sus)$ = 80 V h_{FE} = 1000 min. @ 5 A t_{on} = 1 μs typ. t_f = 3 μs typ. t_s = 1 μs typ. File No. 610 Page 538	**BDX33B** $V_{CEO}(sus)$ = 80 V h_{FE} = 750 min. @ 3 A File No. 693 Page 545	**BDX34B** $V_{CEO}(sus)$ = −80 V h_{FE} = 750 min. @ −3 A File No. 694 Page 551
				BDX33C $V_{CEO}(sus)$ = 100 V h_{FE} = 750 min. @ 3 A File No. 693 Page 545	**BDX34C** $V_{CEO}(sus)$ = −100 V h_{FE} = 750 min. @ −3 A File No. 694 Page 551

▲Pellet size—values shown are edge dimensions in thousands-of-an-inch (mils).

CROSS-REFERENCE GUIDE

This guide provides a quick reference to more than 500 industry power transistors and their nearest RCA replacements. The nearest RCA device is determined on the basis of electrical similarity as well as package similarity. Further information on RCA power transistors is available in Power Transistor Directory PTD-187D, and in the data sheets for RCA commercial power transistors.

INDUSTRY No.	RCA No.	INDUSTRY No.	RCA No.
DTS410	RCA410	D44H1	2N6288
DTS411	RCA411	D44H2	2N6288
DTS413	RCA413	D44H4	2N6290
DTS423	RCA423	D44H5	2N6290
DTS431	RCA431	D44H7	2N6292
D40D1	2N6288	D44H8	2N6292
D40D2	2N6288	D44H10	2N6292
D40D4	2N6290	D44H11	2N6292
D40D5	2N6290	D45C1	2N6111
D40D7	2N6292	D45C2	2N6111
D40D8	2N6292	D45C3	2N6111
D40D10	2N6292	D45C4	2N6109
D40D11	2N6292	D45C5	2N6109
D40N1	2N6175	D45C6	2N6109
D40N2	2N6175	D45C7	2N6107
D40N3	2N6176	D45C8	2N6107
D40N4	2N6176	D45C9	2N6107
D40P1	2N6175	D45C10	2N6107
D40P3	2N6175	D45C11	2N6107
D40P5	2N6175	D45H1	2N6111
D41D1	2N6111	D45H2	2N6111
D41D2	2N6111	D45H4	2N6109
D41D4	2N6109	D45H5	2N6109
D41D5	2N6109	D45H7	2N6107
D41D7	2N6107	D45H8	2N6107
D41D8	2N6107	D45H10	2N6107
D41D10	2N6107	D45H11	2N6107
D41D11	2N6107	MJE101	RCA101
D42C1	2N6288	MJE102	RCA102
D42C2	2N6288	MJE103	RCA103
D42C3	2N6288	MJE104	RCA104
D42C4	2N6290	MJE105	RCA105
D42C5	2N6290	MJE201	RCA201
D42C6	2N6290	MJE202	RCA202
D42C7	2N6292	MJE203	RCA203
D42C8	2N6292	MJE204	RCA204
D42C9	2N6292	MJE205	RCA205
D42C10	2N6292	MJE370	RCA370
D42C11	2N6292	MJE371	RCA371
D43C1	2N6111	MJE520	RCA520
D43C2	2N6111	MJE521	RCA521
D43C3	2N6111	MJE1290	2N6109
D43C4	2N6109	MJE1291	2N6107
D43C5	2N6109	MJE1660	2N6103
D43C6	2N6109	MJE1661	2N6101
D43C7	2N6107	MJE2370	2N6109
D43C8	2N6107	MJE2371	2N6107
D43C9	2N6107	MJE2480	2N6290
D43C10	2N6107	MJE2481	2N6292
D43C11	2N6107	MJE2482	2N6290
D44C1	2N6288	MJE2483	2N6292
D44C2	2N6288	MJE2490	2N6109
D44C3	2N6288	MJE2491	2N6107
D44C4	2N6290	MJE2520	2N6290
D44C5	2N6290	MJE2521	2N6292
D44C6	2N6290	MJE2522	2N6290
D44C7	2N6292	MJE2523	2N6292
D44C8	2N6292	MJE2801	2N6099
D44C9	2N6292	MJE2901	2N6107
D44C10	2N6292	MJE2955	2N6107
D44C11	2N6292	MJE3054	2N5298

INDUSTRY No.	RCA No.	INDUSTRY No.	RCA No.
MJE3055	2N6099	SDT3552	2N5783
MJE3740	2N6107	SDT3553	2N5781
MJE3741	2N6107	SDT3575	2N5956
MJ400	2N3585	SDT3576	2N5955
MJ410	RCA410	SDT3577	2N5954
MJ411	RCA411	SDT3701	2N5956
MJ413	RCA413	SDT3702	2N5955
MJ423	RCA423	SDT3703	2N5956
MJ431	RCA431	SDT3704	2N5955
MJ450	2N6246	SDT3705	2N5954
MJ490	2N6246	SDT3706	2N5956
MJ491	2N6246	SDT3707	2N5955
MJ802	2N6258	SDT3708	2N5955
MJ1800	2N5838	SDT3709	2N5956
MJ2249	2N3879	SDT3710	2N5955
MJ2250	2N3879	SDT3711	2N5955
MJ2251	2N3584	SDT3712	2N5956
MJ2252	2N3585	SDT3713	2N5955
MJ2253	2N5955	SDT3714	2N5954
MJ2254	2N5954	SDT3715	2N5956
MJ2267	2N6246	SDT3716	2N5956
MJ2268	2N6246	SDT3717	2N5955
MJ2801	40251	SDT3718	2N5954
MJ2840	2N3055	SDT3720	2N5956
MJ2841	2N6254	SDT3721	2N5956
MJ2901	2N6246	SDT3722	2N5955
MJ2940	2N6246	SDT3723	2N5954
MJ2941	2N6247	SDT3725	2N5956
MJ3026	2N5839	SDT3726	2N5956
MJ3027	2N5840	SDT3727	2N5955
MJ3202	2N3585	SDT3728	2N5954
MJ3430	2N5840	SDT3729	2N5956
MJ3701	2N5956	SDT3730	2N5955
MJ3771	2N3771	SDT3731	2N5954
MJ3772	2N3772	SDT3733	2N5956
MJ4502	2N6248	SDT3750	2N6246
MJ5600	2N3772	SDT3751	2N6246
MJ5601	2N6258	SDT3752	2N6246
MJ5602	2N3773	SDT3753	2N6246
MJ5603	2N3773	SDT3754	2N6247
MJ6000	2N3772	SDT3755	2N6248
MJ6001	2N6258	SDT3756	2N6246
MJ6002	2N3773	SDT3757	2N6246
MJ6003	2N6258	SDT3758	2N6246
MJ6004	2N6258	SDT3759	2N6247
MJ7000	2N3265	SDT3760	2N6248
MJ9000	2N5805	SDT3761	2N6246
SDI345	2N6290	SDT3762	2N6246
SDI445	2N6109	SDT3763	2N6246
SDJ345	2N6290	SDT3764	2N6247
SDJ445	2N6109	SDT3765	2N6248
SDK345	2N6290	SDT3766	2N6246
SDK445	2N6109	SDT3825	2N6246
SDL345	2N6292	SDT3826	2N6247
SDL445	2N6107	SDT3827	2N6246
SDT410	RCA410	SDT4901	2N6078
SDT411	RCA411	SDT4902	2N6078
SDT413	RCA413	SDT4903	2N6078
SDT423	RCA423	SDT4904	2N6077
SDT431	RCA431	SDT4905	2N6079
SDT3550	2N5781	SDT6901	2N6078

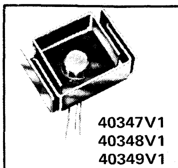
INDUSTRY No.	RCA No.	INDUSTRY No.	RCA No.
SDT6902	2N6078	TIP32	RCA32
SDT6903	2N6078	TIP32A	RCA32A
SDT6904	2N6078	TIP32B	RCA32B
SDT6905	2N6078	TIP32C	RCA32C
SDT6906	2N6078	TIP41	RCA41
SDT6907	2N6078	TIP41A	RCA41A
SDT6908	2N6078	TIP41B	RCA41B
SDT7601	2N5039	TIP41C	RCA41C
SDT7602	2N5039	TIP42	RCA42
SDT7603	2N5038	TIP42A	RCA42A
SDT7604	2N6249	TIP42B	RCA42B
SDT7605	2N6249	TIP42C	RCA42C
SDT7607	2N5039	TIP3055	2N6099
SDT7608	2N5039	2N3036	2N5320
SDT7609	2N5038	2N3122	2N5321
SDT7610	2N6249	2N3171	2N6246
SDT7611	2N6249	2N3172	2N6246
SDT7612	2N6249	2N3173	2N6247
SDT7731	2N6254	2N3174	2N6248
SDT7732	2N6254	2N3183	2N6246
SDT7733	2N6254	2N3184	2N6246
SDT7734	2N3773	2N3185	2N6247
SDT7735	2N3773	2N3186	2N6248
SDT7736	2N6259	2N3195	2N6246
SDT8002	2N3266	2N3196	2N6246
SDT8003	2N3265	2N3197	2N6247
SDT8012	2N3266	2N3198	2N6248
SDT8013	2N3265	2N3202	2N5783
SDT8015	2N3266	2N3203	2N5781
SDT8016	2N3265	2N3208	2N5783
SDT8105	2N3264	2N3224	2N5415
SDT8106	2N3263	2N3225	2N5415
SDT8112	2N3264	2N3226	2N6253
SDT8113	2N3263	2N3232	2N3055
SDT8301	2N3266	2N3233	2N3442
SDT8302	2N3265	2N3234	2N6262
SDT8303	2N3266	2N3235	2N3055
SDT8304	2N3265	2N3236	2N6254
SDT9201	2N3055	2N3237	2N6258
SDT9202	2N6254	2N3238	2N6258
SDT9203	2N4348	2N3239	2N6258
SDT9204	2N4348	2N3240	2N6259
SDT9205	2N3055	2N3464	2N3053
SDT9206	2N3055	2N3597	2N3266
SDT9207	2N6254	2N3598	2N3266
SDT9208	2N4348	2N3599	2N3265
SDT9209	2N4348	2N3712	2N3440
SDT9210	2N6253	2N3713	2N3055
SDT9701	2N6258	2N3714	2N6254
SDT9702	2N3773	2N3715	2N3055
SDT9703	2N3773	2N3716	2N6254
SDT9704	2N6254	2N3738	2N3584
SDT9705	2N3773	2N3739	2N3585
SDT9706	2N3773	2N3740	2N5955
SDT9707	2N3055	2N3741	2N5954
SDT9801	2N6254	2N3742	2N3439
SDT9802	2N6254	2N3743	2N5416
SDT9803	2N6254	2N3766	2N3879
SDT9804	2N3773	2N3767	2N3879
SPC410	RCA410	2N3774	2N5783
SPC411	RCA411	2N3775	2N5781
SPC413	RCA413	2N3778	2N5783
SPC423	RCA423	2N3779	2N5781
SPC431	RCA431	2N3782	2N5783
STS410	RCA410	2N3788	2N5840
STS411	RCA411	2N3789	2N6246
STS413	RCA413	2N3790	2N6247
STS423	RCA423	2N3791	2N6246
STS431	RCA431	2N3792	2N6247
TIP29	RCA29	2N3795	2N5415
TIP29A	RCA29A	2N3863	2N3055
TIP29B	RCA29B	2N3864	2N3442
TIP29C	RCA29C	2N3865	2N6262
TIP30	RCA30	2N3902	2N5840
TIP30A	RCA30A	2N3945	2N2102
TIP30B	RCA30B	2N4000	2N5320
TIP30C	RCA30C	2N4002	2N3265
TIP31	RCA31	2N4004	2N3263
TIP31A	RCA31A	2N4054	2N6176
TIP31B	RCA31B	2N4055	2N6175
TIP31C	RCA31C	2N4056	2N6175

INDUSTRY No.	RCA No.	INDUSTRY No.	RCA No.
2N4057	2N6175	2N5618	2N5038
2N4070	2N5038	2N5619	2N6248
2N4071	2N6249	2N5620	2N5038
2N4210	2N3266	2N5624	2N5038
2N4211	2N3265	2N5628	2N5038
2N4231	2N6260	2N5629	2N6259
2N4232	2N3054	2N5630	2N6259
2N4233	2N6261	2N5631	2N6259
2N4234	2N5783	2N5632	2N3773
2N4235	2N5781	2N5633	2N3773
2N4237	2N5786	2N5634	2N3773
2N4238	2N5784	2N5655	2N6175
2N4387	2N5956	2N5656	2N6176
2N4388	2N5955	2N5657	2N6177
2N4438	2N3439	2N5660	2N6078
2N4898	2N5956	2N5661	2N6079
2N4899	2N5955	2N5664	2N6078
2N4900	2N5954	2N5665	2N6079
2N4901	2N6246	2N5685	2N6032
2N4902	2N6246	2N5686	2N6032
2N4903	2N6247	2N5732	2N5671
2N4904	2N6246	2N5733	2N3265
2N4905	2N6246	2N5734	2N5671
2N4906	2N6247	2N5737	2N6246
2N4907	2N6246	2N5738	2N6248
2N4908	2N6246	2N5758	2N6262
2N4909	2N6247	2N5759	2N6262
2N4910	2N6260	2N5760	2N6262
2N4911	2N3054	2N5867	2N6246
2N4912	2N6261	2N5868	2N6247
2N4913	2N6253	2N5869	2N3055
2N4914	2N3055	2N5870	2N6254
2N4915	2N6254	2N5871	2N6246
2N4926	2N3440	2N5872	2N6247
2N4927	2N3440	2N5873	2N3055
2N4930	2N5415	2N5874	2N6254
2N4931	2N5416	2N5875	2N6246
2N5050	2N3584	2N5876	2N6247
2N5051	2N3584	2N5877	2N6254
2N5052	2N3584	2N5878	2N6254
2N5058	2N3439	2N5879	2N6246
2N5059	2N3440	2N5880	2N6247
2N5067	2N6253	2N5881	2N6254
2N5068	2N3055	2N5882	2N6254
2N5069	2N6254	2N5885	2N6258
2N5091	2N5416	2N5886	2N6258
2N5092	2N3439	2N5929	2N5671
2N5110	2N5783	2N5930	2N5672
2N5157	2N5840	2N5932	2N5671
2N5190	45190	2N5933	2N5672
2N5191	45191	2N5935	2N6032
2N5192	45192	2N5936	2N6033
2N5193	45193	2N5968	2N3265
2N5194	45194	2N5970	2N6254
2N5195	45195	2N5971	2N6254
2N5241	2N5805	2N5972	2N6254
2N5264	2N5804	2N5973	2N6254
2N5279	2N3439	2N6046	2N3266
2N5280	2N4063	2N6047	2N3265
2N5281	2N5415	2N6048	2N3265
2N5282	2N5416	2N6049	2N5955
2N5301	2N6258	2N6062	2N3265
2N5302	2N6258	2N6063	2N3265
2N5303	2N6258	2N6121	2N6290
2N5331	2N3265	2N6122	2N6290
2N5344	2N6211	2N6123	2N6292
2N5345	2N6212	2N6124	2N6109
2N5539	2N3265	2N6125	2N6109
2N5560	2N3265	2N6126	2N6107
2N5597	2N5955	2N6129	2N6290
2N5598	2N5202	2N6130	2N6290
2N5599	2N5954	2N6131	2N6292
2N5600	2N3879	2N6132	2N6109
2N5601	2N5954	2N6133	2N6109
2N5602	2N3879	2N6134	2N6107
2N5608	2N3879	2N6226	2N6248
2N5613	2N6246	2N6229	2N6248
2N5614	2N5039	2N6233	2N6078
2N5615	2N6247	2N6234	2N6077
2N5616	2N5038	2N6235	2N6079
2N5617	2N6247	2N6270	2N5671
		2N6271	2N5672

Hometaxial-Base Power Transistors

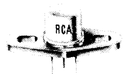
RCA
Solid State
Division

Power Transistors
40347
40348
40349



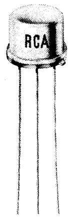
40347V1
40348V1
40349V1

H-1468



40347V2
40348V2
40349V2

H-1375



40347
40348
40349

JEDEC TO-5

H-1380

"Hometaxial"-Base Silicon N-P-N Medium- and High-Voltage Types

General-Purpose Transistors for Industrial and Commercial Equipment

Features

- **High second-breakdown resistance**
- **V_{CE}(sat) typically less than 1 volt at 1 ampere for types 40347 & 40348**
- **V_{CEV}(sus) for type 40349 is 160 volts min.**
- **Hermetically-sealed packages**

RCA-40347, 40348, and 40349 are Hometaxial-base*, silicon n-p-n transistors intended for a wide variety of low- and medium-power applications requiring medium- and high-voltage power transistors.

All three of these devices employ the popular TO-5 package; they differ primarily in their breakdown-voltage ratings.

Types 40347V1, 40348V1, and 40349V1 are 40347, 40348, and 40349, respectively, with factory-attached heat radiators; they are intended for printed circuit-board applications.

Types 40347V2, 40348V2, and 40349V2, are 40347, 40348, and 40349, respectively, with factory-attached diamond-shaped mounting flanges.

Typical applications for these transistors include switching regulators, converters, inverters, relay controls, oscillators, pulse amplifiers, and audio amplifiers (in low-power driver and output stages). These transistors are especially suitable for use in low-cost AC/DC af amplifier circuits.

* "Hometaxial" was coined by RCA for "homogeneous" and "axial" to describe a single-diffused transistor with a base region of homogeneous resistivity silicon in the axial direction.

MAXIMUM RATINGS, *Absolute-Maximum Values*		40347 40347V1 40347V2	40348 40348V1 40348V2	40349 40349V1 40349V2	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	60	90	160	V
COLLECTOR-TO-EMITTER VOLTAGE:					
With – 1.5 V (V_{BE}) of reverse bias	V_{CEV}	60	90	160	V
With base open	V_{CEO}	40	65	140	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	7	7	7	V
CONTINUOUS COLLECTOR CURRENT	I_C	1.5	1.5	1.5	A
PEAK COLLECTOR CURRENT		3.0	3.0	3.0	A
CONTINUOUS BASE CURRENT	I_B	0.5	0.5	0.5	A
TRANSISTOR DISSIPATION	P_T				
At case temperature up to 25°C		11.7 (40347V2) 8.75 (40347)	11.7 (40348V2) 8.75 (40348)	11.7 (40349V2) 8.75 (40349)	W W
At case temperature above 25°C		← See Figs. 2 & 3 →			
At free-air temperature up to 25°C		1.0 (40347) 4.4 (40347V1)	1.0 (40348) 4.4 (40348V1)	1.0 (40349) 4.4 (40349V1)	W W
At free-air temperature above 25°C		← See Fig. 1 →			
TEMPERATURE RANGE:					
Storage & Operating (Junction)		← –65 to 200 →			°C
LEAD TEMPERATURE (During soldering):					
At distances ≥ 1/32 in. from seating plane for 10 s max.		← 230 →			°C

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ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C unless otherwise specified*

Characteristic	Symbol	TEST CONDITIONS: DC Collector Voltage-V V_{CE}	DC Emitter or Base Voltage-V V_{EB}	V_{BE}	DC Current A I_C	I_B	LIMITS: Type 40347 Min.	Type 40347 Max.	Type 40348 Min.	Type 40348 Max.	Type 40349 Min.	Type 40349 Max.	Units
Collector-Cutoff Current R_{BE} = 1,000 Ω	I_{CER}	30					–	1.0	–	–	–	–	µA
		60					–	–	–	1.0	–	–	
		90					–	–	–	–	–	2.0	
R_{BE} = 1,000 Ω, T_C = 150°C	I_{CER}	30					–	1.0	–	–	–	–	mA
		60					–	–	–	1.0	–	–	
		90					–	–	–	–	–	1.0	
Emitter-Cutoff Current	I_{EBO}		7				–	10	–	10	–	10	µA
DC Forward-Current Transfer Ratio	h_{FE}	4			0.15		–	–	–	–	30	125	
		4			0.30		–	–	30	125	–	–	
		4			0.45		25	100	–	–	10	–	
		4			1.00		–	–	10	–	–	–	
Collector-to-Emitter Sustaining Voltage: *(See Figs. 4, 5 & 6)* With base-emitter junction reverse biased	V_{CEV}(sus)			−1.5	.050		60	–	90	–	160[a]	–	V
With base open	V_{CEO}(sus)				.050		40	–	65	–	140[a]	–	V
Base-to-Emitter Voltage	V_{BE}	4			0.15		–	–	–	–	–	1.1	V
		4			0.30		–	–	–	1.3	–	–	
		4			0.45		–	1.5	–	–	–	–	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)				0.15	15 mA	–	–	–	–	–	0.5	V
					0.30	30 mA	–	–	–	0.75	–	–	
					0.45	45 mA	–	1.0	–	–	–	–	
Thermal Resistance: Junction-to-Case	θ_{J-C}						20(max.) 40347 15(max.) 40347V2		20(max.) 40348 15(max.) 40348V2		20(max.) 40349 15(max.) 40349V2		°C/W
Thermal Resistance: Junction-to-Ambient	θ_{J-A}						40(max.) 40347V1		40(max.) 40348V1		40(max.) 40349V1		°C/W

a Pulsed; pulse duration = 300 µs, duty factor = 1.8%.

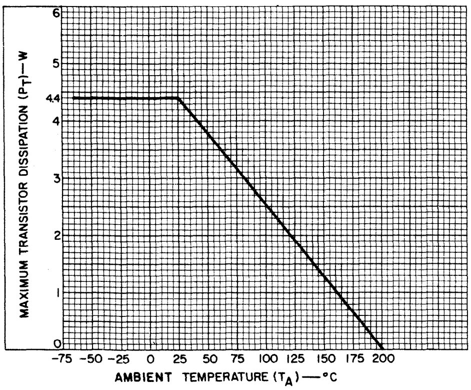


Fig. 1 - Dissipation derating curve for types 40347V1, 40348V1, and 40349V1.

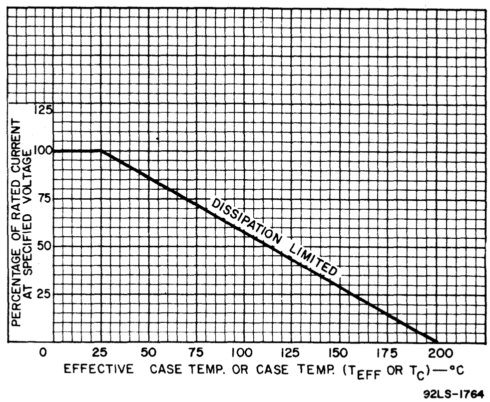
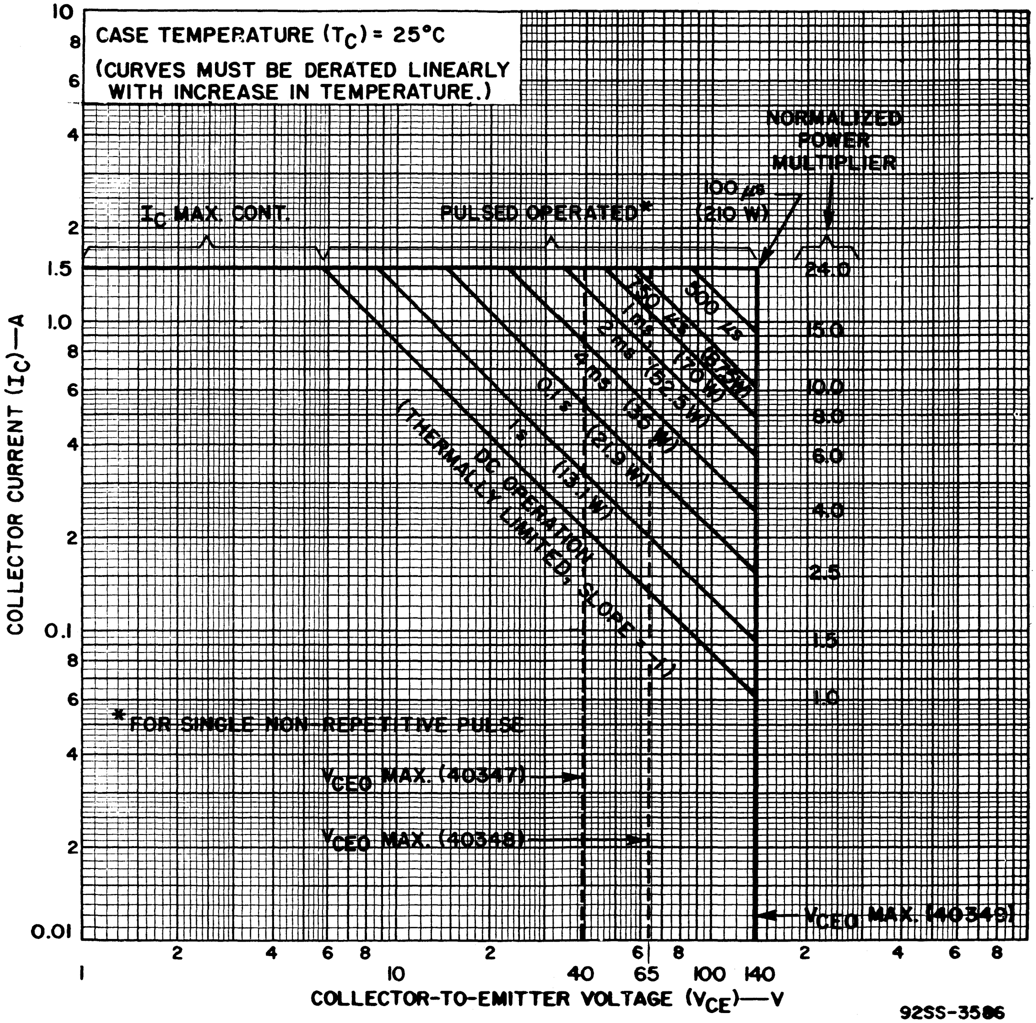


Fig. 2 - Dissipation derating curve for types 40347, 40348, and 40349.


CASE TEMPERATURE (TC) = 25°C
(CURVES MUST BE DERATED LINEARLY WITH INCREASE IN TEMPERATURE.)
NORMALIZED POWER MULTIPLIER
IC MAX. CONT.
PULSED OPERATED*
100 µs (210 W)
500 µs (87.5 W)
250 µs (70 W)
1 ms (52.5 W)
2 ms (35 W)
4 ms (21.9 W)
0.1 s (13.1 W)
1 s
DC OPERATION (THERMALLY LIMITED, SLOPE = -1)
24.0
15.0
10.0
8.0
6.0
4.0
2.5
1.5
1.0
* FOR SINGLE NON-REPETITIVE PULSE
VCEO MAX. (40347)
VCEO MAX. (40348)
VCEO MAX. (40349)
COLLECTOR CURRENT (IC)—A
COLLECTOR-TO-EMITTER VOLTAGE (VCE)—V
92SS-3586

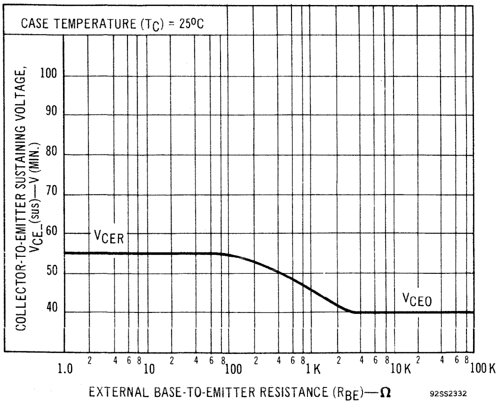


Fig. 4 - Sustaining voltage vs. base-to-emitter resistance for types 40347, 40347V1 and 40347V2.

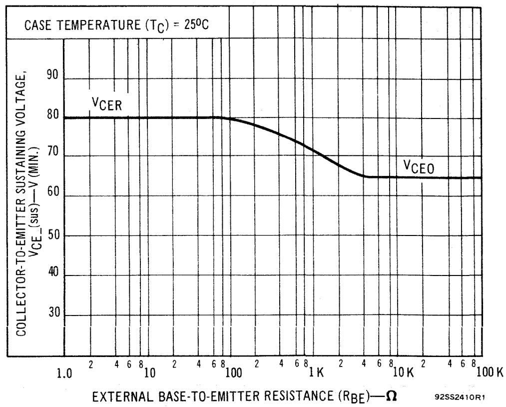


Fig. 5 - Sustaining voltage vs. base-to-emitter resistance for types 40348, 40348V1 and 40348V2.

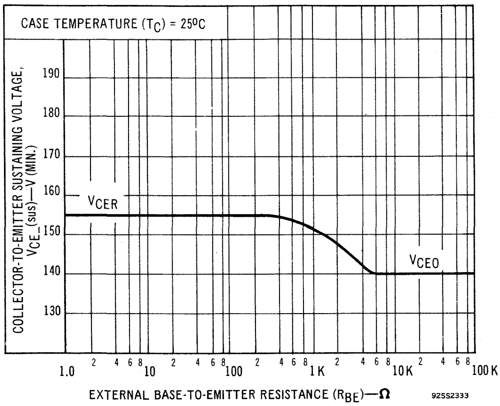


Fig. 6 - Sustaining voltage vs. base-to-emitter resistance for types 40349, 40349V1 and 40349V2.

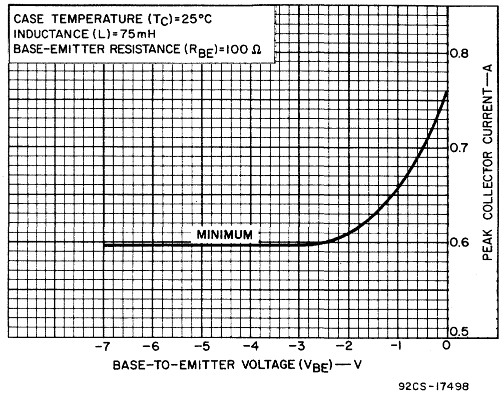


Fig. 7 - Reverse-bias second-breakdown characteristics for types 40347, 40348 and 40349.

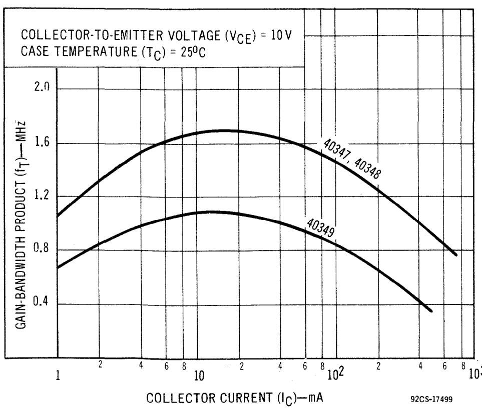


Fig. 8 - Typical gain-bandwidth product vs. collector current for types 40347, 40348 and 40349.

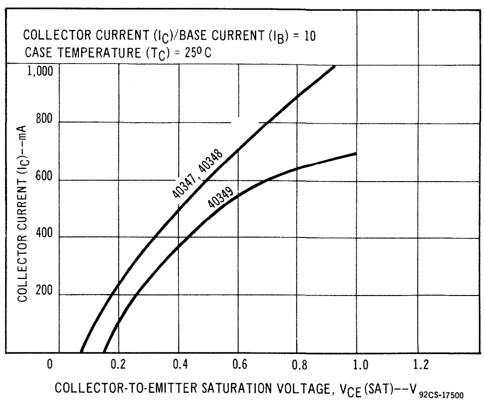


Fig. 9 - Typical saturation characteristic for types 40347, 40348 and 40349.

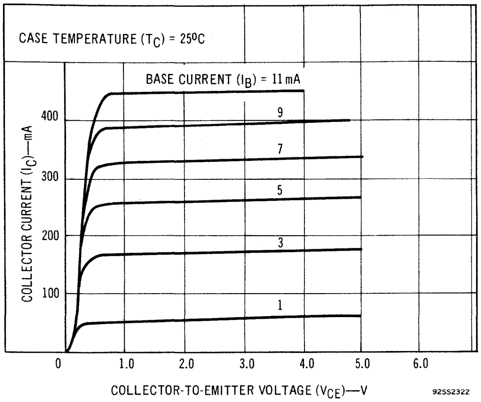


Fig. 10 - Typical output characteristics for type 40347.

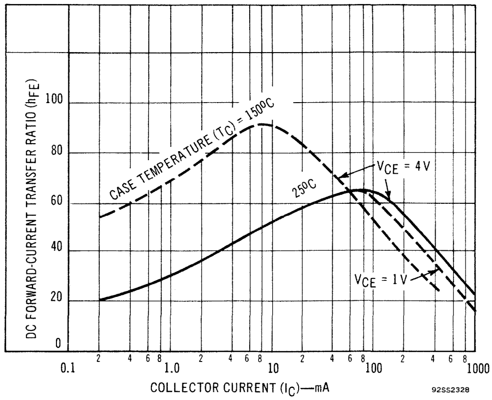


Fig. 11 - Typical dc beta characteristics for type 40347.

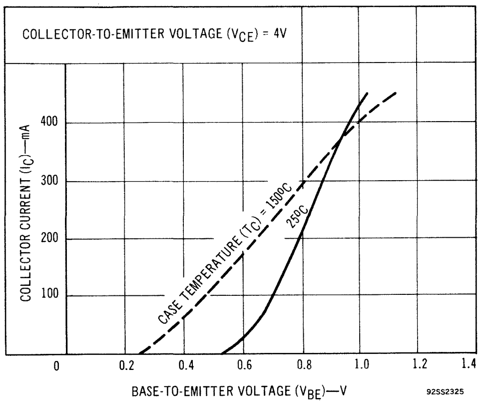


Fig. 12 - Typical transfer characteristics for type 40347.

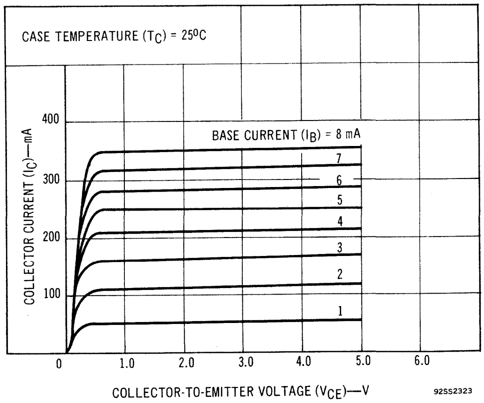


Fig. 13 - Typical output characteristics for type 40348.

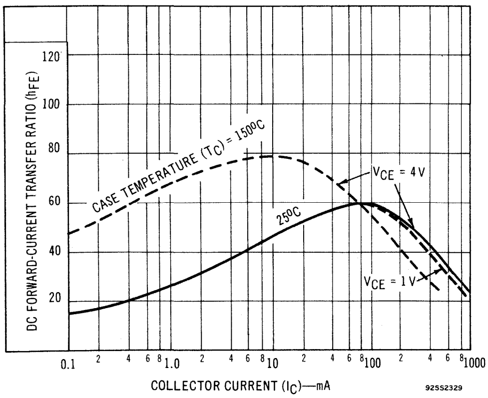


Fig. 14 - Typical dc beta characteristics for type 40348.

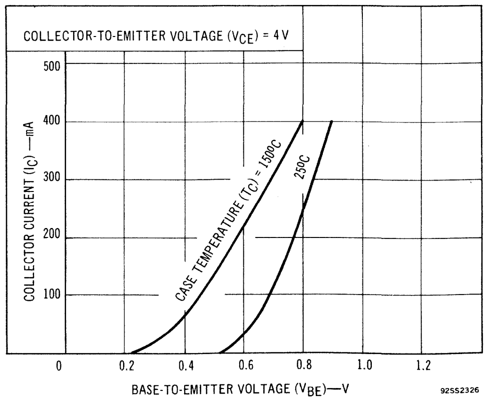


Fig. 15 - Typical transfer characteristics for type 40348.

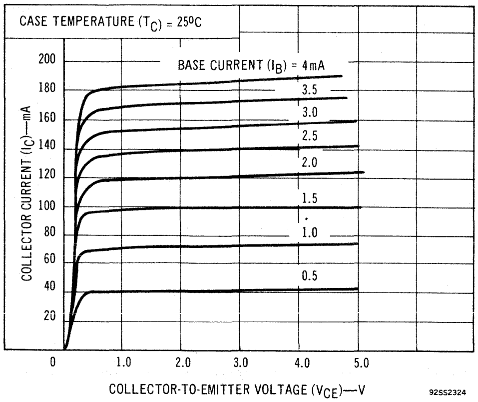


Fig. 16 - Typical output characteristics for type 40349.

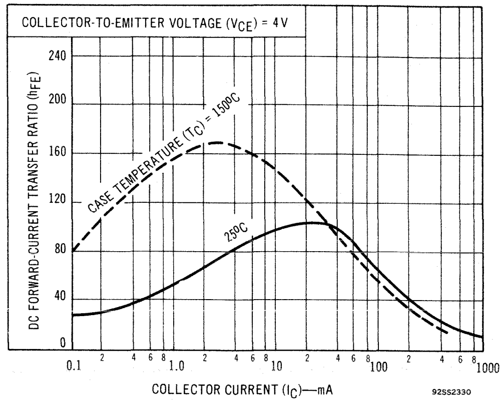


Fig. 17 - Typical dc beta characteristics for type 40349.

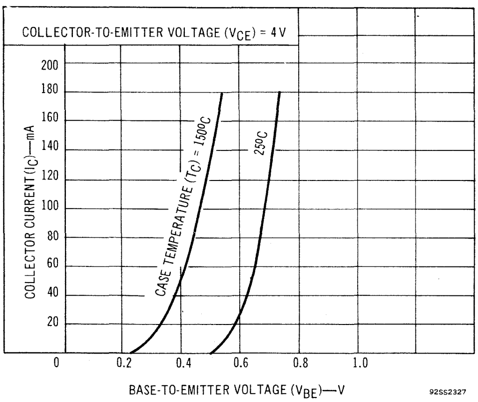


Fig. 18 - Typical transfer characteristics for type 40349.

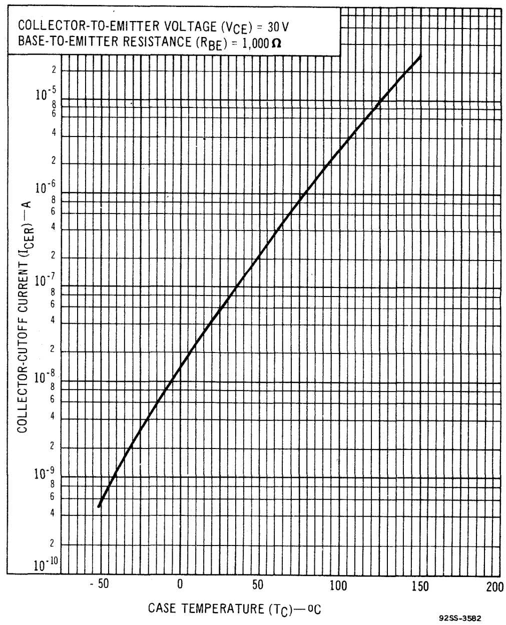


Fig. 19 - Collector-cutoff-current characteristic for type 40347.

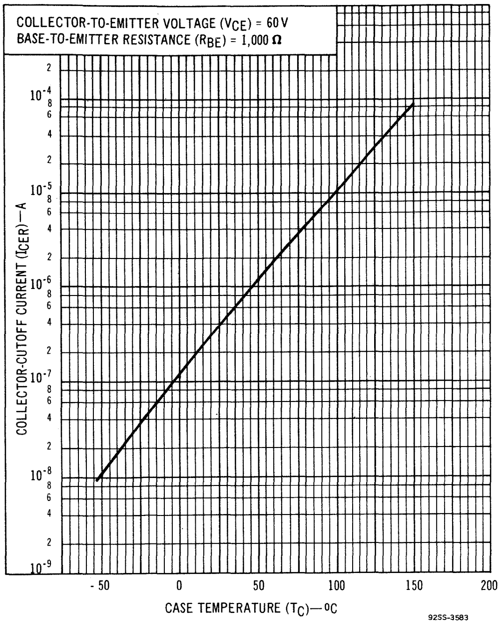


Fig. 20 - Collector-cutoff-current characteristic for type 40348.

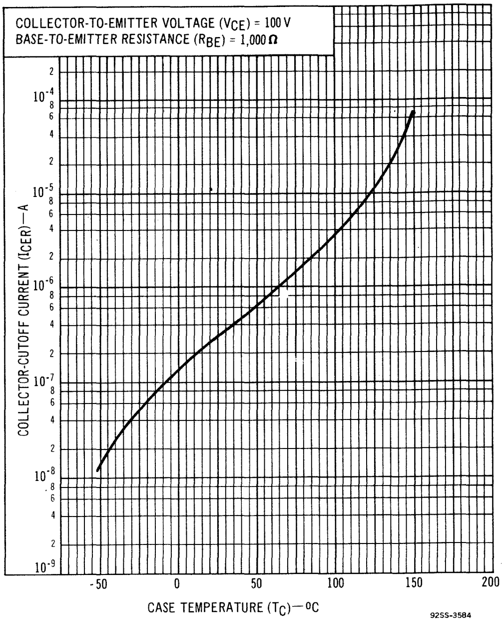
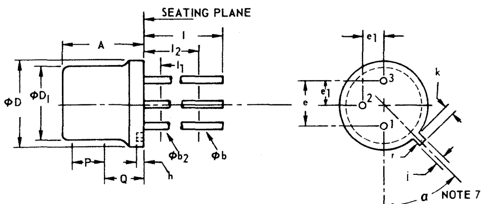


Fig. 21 - Collector-cutoff-current characteristic for type 40349.

DIMENSIONAL OUTLINE FOR TYPES 40347, 40348, 40349 JEDEC TO-5



NOTES:

1. This zone is controlled for automatic handling. The variation in actual diameter within the zone shall not exceed 0.010 in. (0.254 mm).
2. (Three leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and 1.5 in. (38.10 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond 1.5 in. (38.10 mm) from seating plane.
3. Measured from maximum diameter of the actual device.
4. Leads having maximum diameter 0.019 in. (0.483 mm) measured in gaging plane 0.054 in. (1.37 mm) + 0.001 in. (0.25 mm) – 0.000 in. (0.000 mm) below the seating plane of the device shall be within 0.007 in. (0.178 mm) of their true positions relative to the maximum-width tab.
5. The device may be measured by direct methods or by the gage and gaging procedure described on gage drawing GS-1.
6. Details of outline in this zone optional.
7. Tab centerline.

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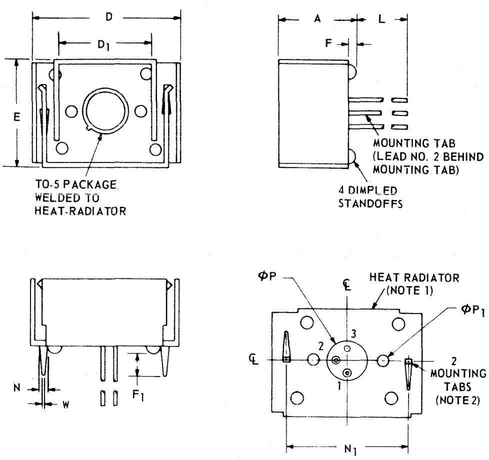
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.240	0.260	6.10	6.60	
ϕb	0.016	0.021	0.406	0.533	2
ϕb_2	0.016	0.019	0.406	0.483	2
ϕD	0.335	0.370	8.51	9.40	
ϕD_1	0.305	0.335	7.75	8.51	
e	0.200 T.P.		5.08 T.P.		4, 5
e_1	0.100 T.P.		2.54 T.P.		5
h	0.009	0.125	0.229	3.18	
i	0.028	0.034	0.711	0.864	5
k	0.029	0.045	0.737	1.14	3, 5
l	1.500	–	38.10	–	2
l_1	–	0.050	–	1.27	2
l_2	0.250	–	6.35	–	2
P	0.100	–	2.54	–	1
Q	–	–	–	–	6
r	–	0.007	–	0.179	
α	45° T. P.		–		5, 7

TERMINAL CONNECTIONS FOR TYPES 40347, 40348, & 40349

Lead 1 - Emitter
Lead 2 - Base
Case, Lead 3 - Collector

DIMENSIONAL OUTLINE FOR TYPE 40347V1, 40348V1, 40349V1 JEDEC TO-5 WITH HEAT RADIATOR



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	0.630	–	16.00	
D	1.205	1.235	30.61	31.37	
D_1	0.775	0.785	19.69	19.93	
E	0.875	0.905	22.22	22.99	
F	0.040	0.055	1.02	1.40	
F_1	0.160	0.195	4.06	4.95	
L	1.410	–	35.81	–	
ϕP	0.295	0.305	7.493	7.747	
ϕP_1	0.093	0.095	2.362	2.413	
N	0.048	0.062	1.21	1.57	
N_1	0.998	1.002	25.349	25.450	3
W	0.048	0.052	1.219	1.320	

NOTES:

1. 0.035 C.R.S., finish—electroless nickel plate.
2. Recommended hole size for printed-circuit board is 0.070 dia.
3. Measured at bottom of heat-radiator

92SS-2546R2

TERMINAL CONNECTIONS FOR TYPES 40347V1, 40348V1, & 4049V1

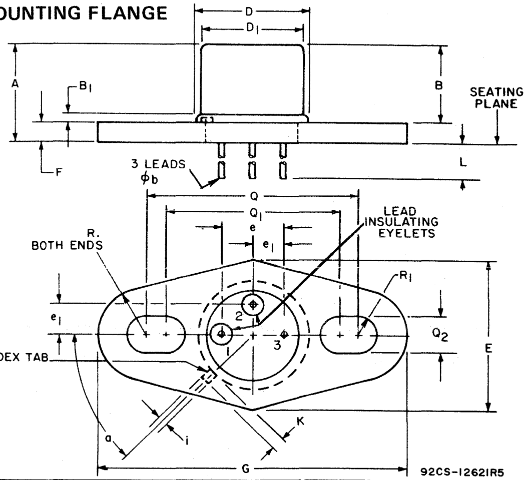
Lead 1 - Emitter
Lead 2 - Base
Heat Radiator, Lead 3 - Collector

TERMINAL CONNECTIONS FOR TYPES 40347V2, 40348V2, & 40349V2

Lead 1 - Emitter
Lead 2 - Base
Case, Lead 3 - Collector

In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

DIMENSIONAL OUTLINE FOR TYPE 40347V2, 40348V2, JEDEC TO-5 WITH MOUNTING FLANGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	0.328	–	8.33	
B	0.240	0.260	6.10	6.60	
B_1	0.009	0.125	0.229	3.18	
ϕb	0.016	0.019	0.406	0.483	
D	0.335	0.370	8.51	9.40	
D_1	0.305	0.335	7.75	8.51	
E	0.495	0.505	12.57	12.83	
e	0.200 T.P.		5.08 T.P.		1
e_1	0.100 T.P.		2.54 T.P.		1
F	0.062	0.068	1.57	1.74	
G	0.995	1.005	25.27	25.53	
i	0.028	0.034	0.711	0.864	
k	0.029	0.045	0.737	1.14	
L	1.43	–	36.32	–	
Q	0.685	0.691	17.40	17.55	
Q_1	0.559	0.565	14.20	14.35	
Q_2	0.128	0.132	3.25	3.35	
R	0.156 T.P.		3.96 T.P.		1
R_1	0.064	0.066	1.63	1.67	
α	45° T.P.				1, 2

NOTES:
1. True Position
2. Tab centerline

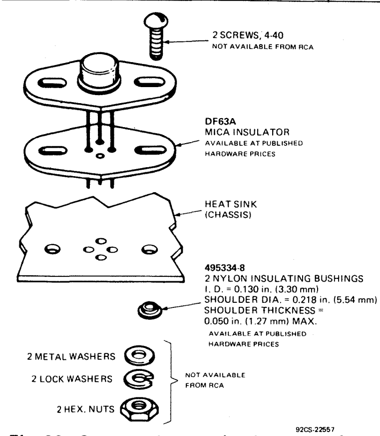


Fig. 22 - Suggested mounting hardware for types 40347V2, 40348V2 and 40349V2 (JEDEC TO-5 with mounting flange).

RCA
Solid State
Division

Power Transistors
2N5781 2N5784
2N5782 2N5785
2N5783 2N5786

RCA-2N5781, 2N5782, and 2N5783 are diffused, epitaxial-base mesa silicon p-n-p transistors -- complements of the hometaxial-base silicon n-p-n types 2N5784, 2N5785, and 2N5786, ** respectively.

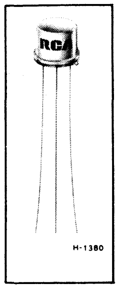
All six of these devices employ the JEDEC TO-5 package; the three types in each family differ primarily in voltage ratings and saturation characteristics.

These transistors are intended for medium-power switching and complementary-symmetry audio amplifier applications

**Formerly RCA Dev. Types TA7270, TA7271, TA7272, TA7289, TA7290, and TA7291 respectively.

SILICON N-P-N AND P-N-P TYPES

General-Purpose Complementary-Symmetry Types



JEDEC TO-5

For Switching and Amplifier Applications in Military, Industrial, and Commercial Equipment

FEATURES

- Low Saturation Voltages
- Maximum Safe-Area-of-Operation Curves
- Hermetically Sealed JEDEC TO-5 Package
- High Min. h_{FE} at High Current
- High Breakdown Voltages

MAXIMUM RATINGS, ***Absolute-Maximum Values:***

		P-N-P Types 2N5781 2N5782 2N5783			N-P-N Types 2N5784 2N5785 2N5786			
		2N5781	2N5782	2N5783	2N5784	2N5785	2N5786	
* COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	-80	-65	-45	80	65	45	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:								
*With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$	-80	-65	-45	80	65	45	V
With base open	$V_{CEO}(sus)$	-65	-50	-40	65	50	40	V
* EMITTER-TO-BASE VOLTAGE	V_{EBO}	-5	-5	-3.5	5	5	3.5	V
* CONTINUOUS COLLECTOR CURRENT	I_C	-3.5	-3.5	-3.5	3.5	3.5	3.5	A
* CONTINUOUS BASE CURRENT	I_B	-1	-1	-1	1	1	1	A
TRANSISTOR DISSIPATION:	P_T							
*At case temperatures up to 25 °C		10	10	10	10	10	10	W
At ambient temperatures up to 25 °C		1	1	1	1	1	1	W
*At case temperatures above 25 °C		Derate linearly at 0.057 W/°C, or see Fig. 3.						
At ambient temperatures above 25 °C		Derate linearly at 0.0057 W/°C.						
* TEMPERATURE RANGE:								
Storage & Operating (Junction)		← -65 to +200 →						°C
* LEAD TEMPERATURE (During Soldering):								
At distances > 1/32 in. (0.8 mm) from seating plane for 10 s max		← +230 →						°C

* In accordance with JEDEC registration data format (JS-6 RDF-2)

ELECTRICAL CHARACTERISTICS, *Case Temperature (T_C) = 25 °C, unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: DC Collector Volts V_{CE}▲	DC Emitter Volts V_{EB}▲	DC Current (Amperes) I_C▲	I_B▲	LIMITS P-N-P TYPES 2N5781 Min.	2N5781 Max.	2N5782 Min.	2N5782 Max.	2N5783 Min.	2N5783 Max.	N-P-N TYPES 2N5784 Min.	2N5784 Max.	2N5785 Min.	2N5785 Max.	2N5786 Min.	2N5786 Max.	UNITS
* Collector-Cutoff Current With base open	I_{CEO}	-50, 50				–	100	–	–	–	–	–	100	–	–	–	–	µA
		-35, 35				–	–	–	-100	–	–	–	–	–	100	–	–	
		-25, 25				–	–	–	–	–	-100	–	–	–	–	–	100	
With external base-to-emitter resistance (R_{BE}) = 100 Ω	I_{CER}	-65, 65				–	-10	–	–	–	–	–	10	–	–	–	–	µA
		-50, 50				–	–	–	-10	–	–	–	–	–	10	–	–	
		-40, 40				–	–	–	–	–	-10	–	–	–	–	–	10	
	I_{CER} (T_C = 150 °C)	-65, 65				–	-1	–	–	–	–	–	1	–	–	–	–	mA
		-50, 50				–	–	–	-1	–	–	–	–	–	1	–	–	
		-40, 40				–	–	–	–	–	-1	–	–	–	–	–	1	
* With base-emitter junction reverse-biased and external base-to-emitter resistance (R_{BE}) = 100 Ω	I_{CEX}	-75, 75	1.5, -1.5 (V_{BE})[g]			–	-10	–	–	–	–	–	10	–	–	–	–	µA
		-60, 60				–	–	–	-10	–	–	–	–	–	10	–	–	
		-45, 45				–	–	–	–	–	-10	–	–	–	–	–	10	
*	I_{CEX} (T_C = 150 °C)	-75, 75	1.5, -1.5 (V_{BE})[g]			–	-1	–	–	–	–	–	1	–	–	–	–	mA
		-60, 60				–	–	–	-1	–	–	–	–	–	1	–	–	
		-45, 45				–	–	–	–	–	-1	–	–	–	–	–	1	
* Emitter-Cutoff Current	I_{EBO}		-3.5, 3.5			–	–	–	–	–	-10	–	–	–	–	–	10	µA
			-5, 5			–	-10	–	-10	–	–	–	10	–	10	–	–	
* DC Forward-Current Transfer Ratio	h_{FE}	-2, 2		-1[c], 1[c]		20	100	–	–	–	–	20	100	–	–	–	–	
		-2, 2		-1.2[c], 1.2[c]		–	–	20	100	–	–	–	–	20	100	–	–	
		-2, 2		-1.6[c], 1.6[c]		–	–	–	–	20	100	–	–	–	–	20	100	
		-2, 2		-3.2[c], 3.2[c]		4	–	4	–	4	–	4	–	4	–	4	–	
* Common-Emitter, Small-Signal, Short-Circuit, Forward-Current Transfer Ratio (f = 1 kHz)	h_{fe}	-2, 2		-0.1, 0.1		25	–	25	–	25	–	25	–	25	–	25	–	
* Collector-to-Emitter Sustaining Voltage: With base open	$V_{CEO}(sus)$			-0.1, 0.1		-65	–	-50	–	-40	–	65	–	50	–	40	–	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω *(See Figs. 4 & 5)*	$V_{CER}(sus)$			-0.1, 0.1		-80	–	-65	–	-45	–	80	–	65	–	45	–	V
* Base-to-Emitter Voltage	V_{BE}	-2, 2		-1, 1		–	-1.5	–	–	–	–	–	1.5	–	–	–	–	V
		-2, 2		-1.2, 1.2		–	–	–	-1.5	–	–	–	–	–	1.5	–	–	
		-2, 2		-1.6, 1.6		–	–	–	–	–	-1.5	–	–	–	–	–	1.5	
Collector-to-Emitter Saturation Voltage [Measured ¼ in. (6.35 mm) from case][f]	$V_{CE}(sat)$			-1, 1	-0.1, 0.1	–	-0.5	–	–	–	–	–	0.5	–	–	–	–	V
				-1.2, 1.2	-0.12, 0.12	–	–	–	-0.75	–	–	–	–	–	0.75	–	–	
				-1.6, 1.6	-0.16, 0.16	–	–	–	–	–	-1.0	–	–	–	–	–	1.0	
*				-3.2, 3.2	-0.8, 0.8	–	-2	–	-2	–	-2	–	2	–	2	–	2	
* Magnitude of Common Emitter, Small-Signal, Short-Circuit, Forward-Current Transfer Ratio	$\|h_{fe}\|$[e]	-2		-0.1	f = 4 MHz	2	15	2	15	2	15	–	–	–	–	–	–	
		2		0.1	f = 200 kHz	–	–	–	–	–	–	5	20	5	20	5	20	
Saturated Switching Time: Turn-on	t_{on}	-30[d], 30[d]		-1, 1	-0.1[a], 0.1[a]	–	.5	–	.5	–	.5	–	5	–	5	–	5	µs
Turn-off	t_{off}	-30[d], 30[d]		-1, 1	-0.1[b], 0.1[b]	–	2.5	–	2.5	–	2.5	–	15	–	15	–	15	
Thermal Resistance: Junction-to-Case	θ_{J-C}					–	17.5	–	17.5	–	17.5	–	17.5	–	17.5	–	17.5	°C/W
Junction-to-Ambient	θ_{J-A}					–	175	–	175	–	175	–	175	–	175	–	175	°C/W

[a] I_{B_1} Value (turn-on base current)

[b] I_{B_2} Value (turn-off base current)

[c] Pulsed, pulse duration = 300 µs, duty factor = 0.018

[d] V_{CC} Value

[e] Measured at a frequency where $|h_{fe}|$ is decreasing at approximately 6 dB per octave

▲ Use negative values for P-N-P types.

* In accordance with JEDEC registration data format (JS-6 RDF-2)

[f] Lead resistance is critical in this test.

[g] Reverse bias; use negative value for N-P-N

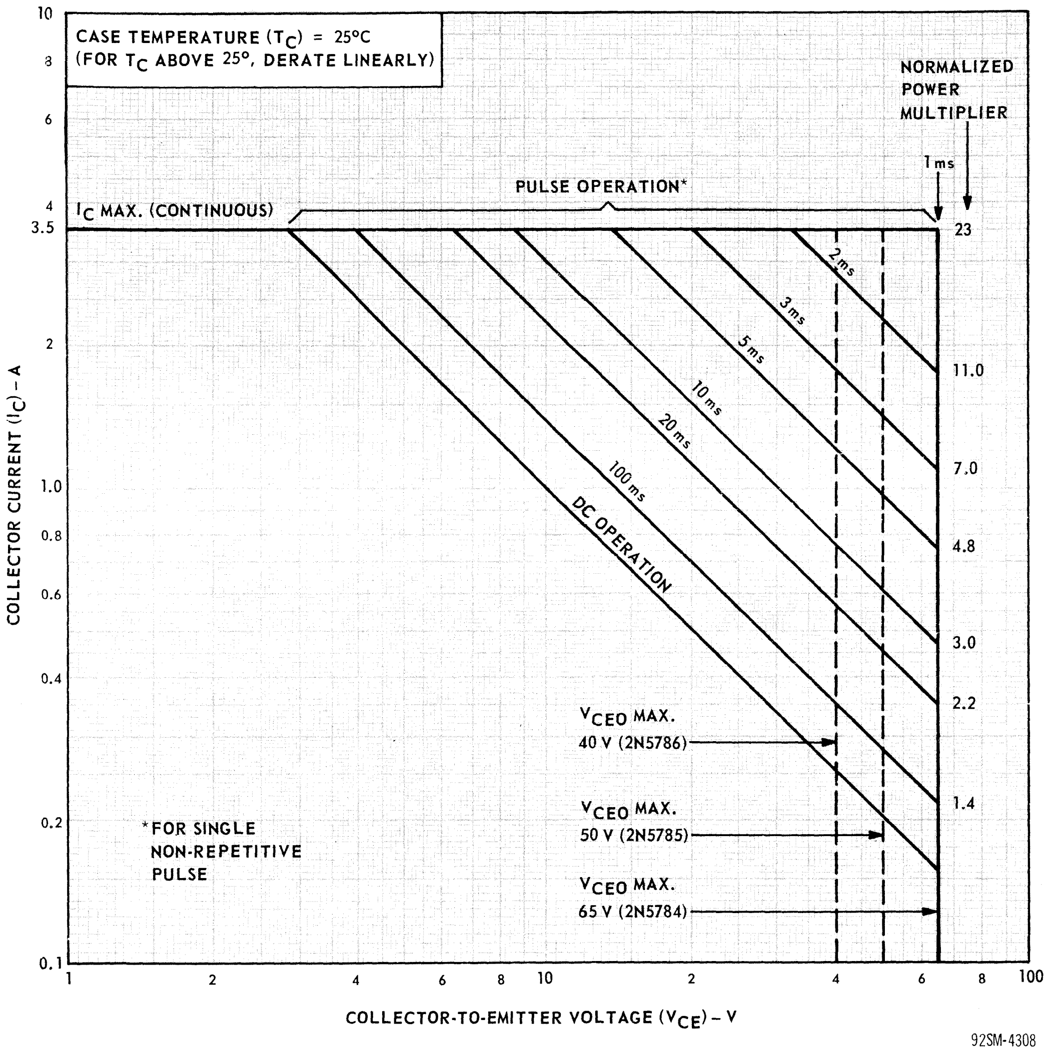


Fig. 1 - Maximum operating areas for types 2N5784, 2N5785, and 2N5786.

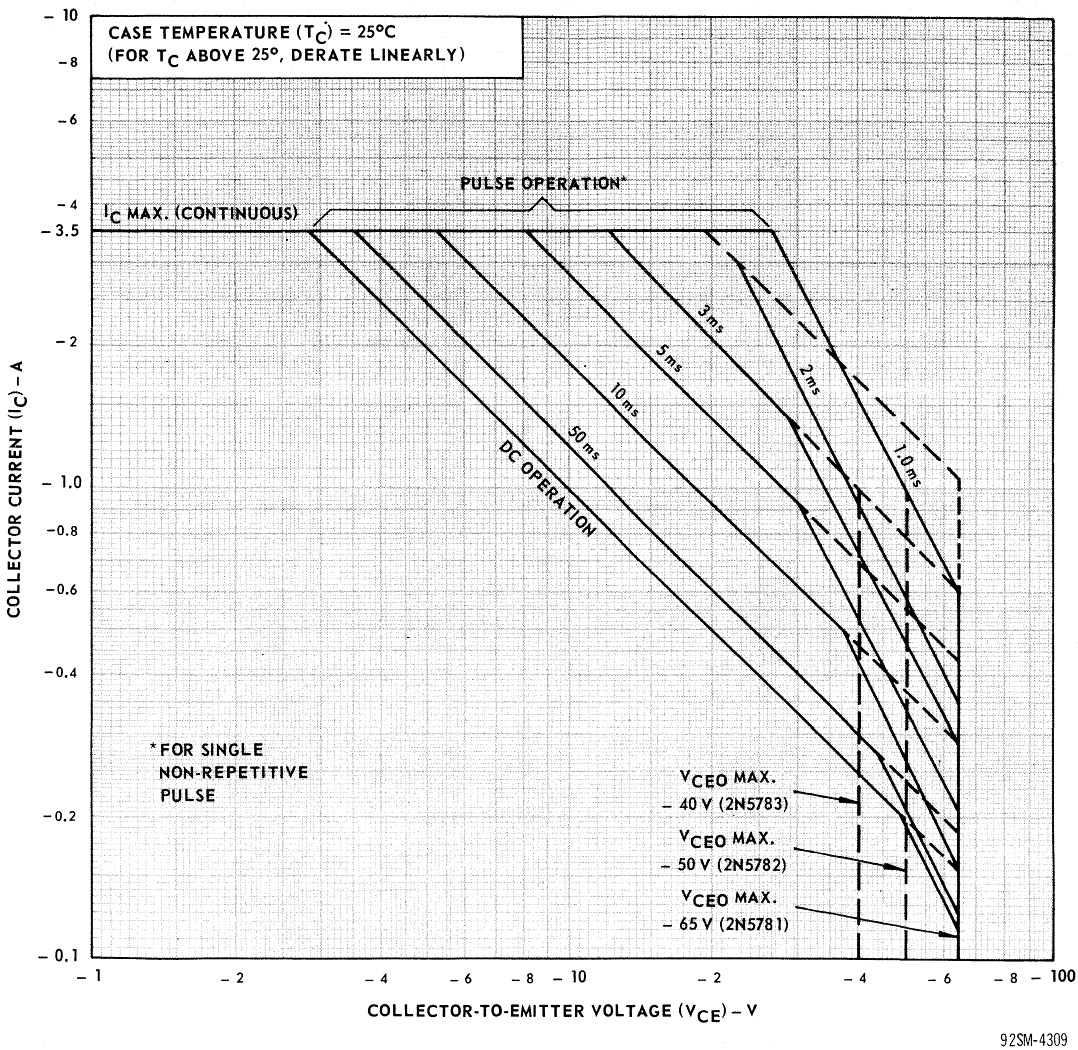


Fig. 2 - Maximum operating areas for types 2N5781, 2N5782, and 2N5783.

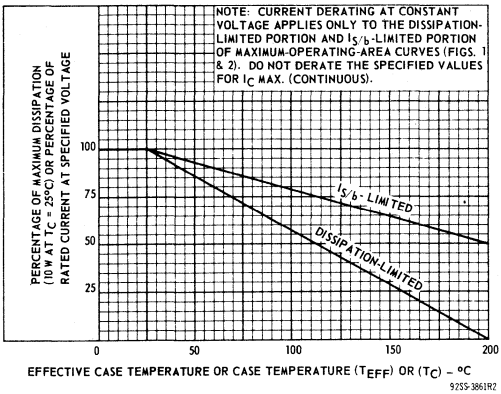


Fig. 3 - Dissipation derating curve for all types.

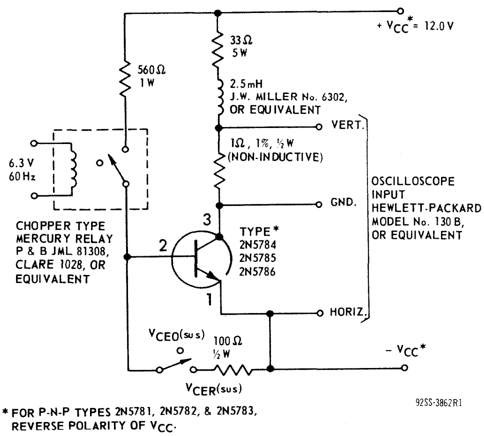
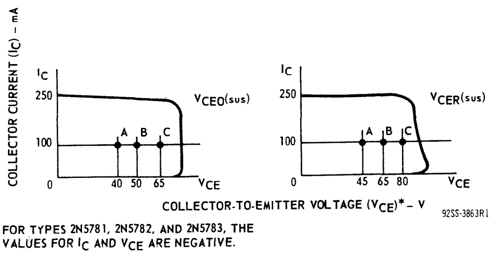


Fig. 4 - Circuit used to measure sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$.



The sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$ are acceptable when the trace falls to the right and above point "A" (2N5783 & 2N5786), "B" (2N5782 & 2N5785), or "C" (2N5781 & 2N5784).

Fig. 5 - Oscilloscope display for measurement of sustaining voltages. (Test circuit shown in Fig. 4.)

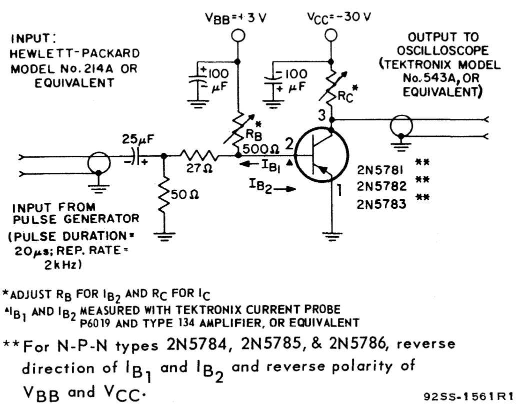


Fig. 6 - Circuit used to measure saturated switching times.

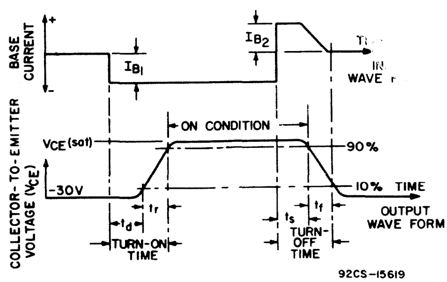


Fig. 7 - Oscilloscope display for measurement of switching times. (Test circuit shown in Fig. 6.)

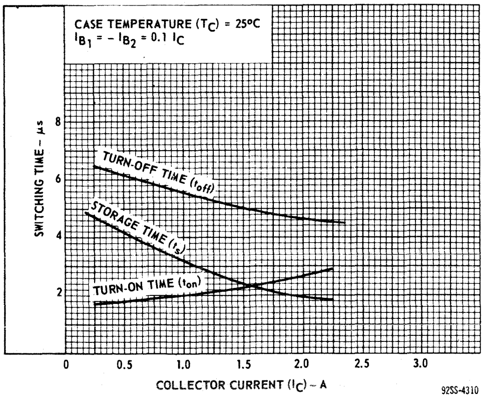


Fig. 8 - Typical saturated switching characteristics for types 2N5784, 2N5785, & 2N5786.

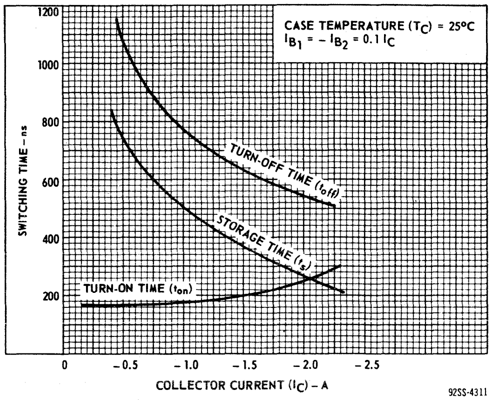


Fig. 9 - Typical saturated switching characteristics for types 2N5781, 2N5782, & 2N5783.

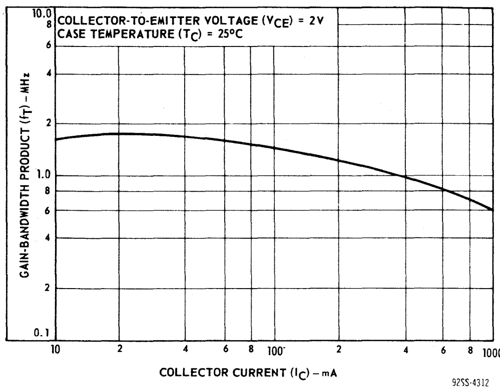


Fig. 10 - Typical gain-bandwidth product for types 2N5784, 2N5785, & 2N5786.

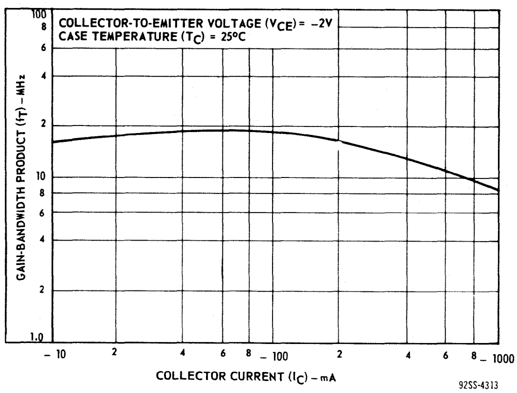


Fig. 11 - Typical gain-bandwidth product for types 2N5781, 2N5782, & 2N5783.

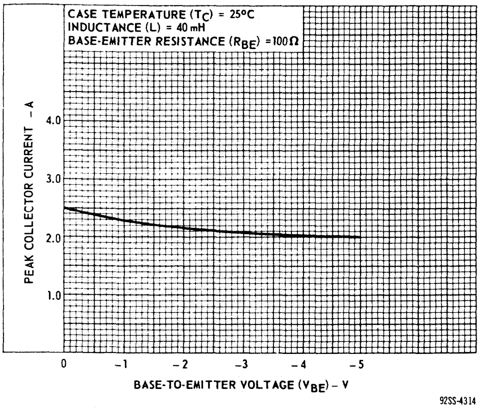


Fig. 12 - Reverse-bias second-breakdown characteristics for types 2N5784, 2N5785, & 2N5786.

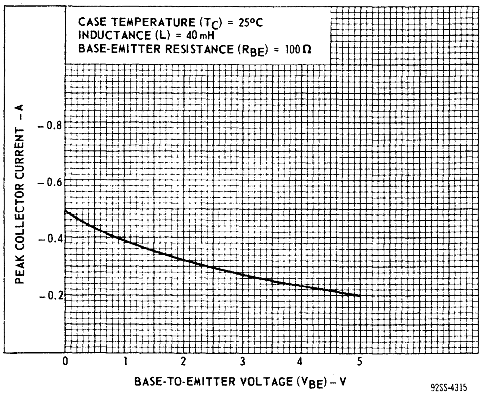


Fig. 13 - Reverse-bias second-breakdown characteristics for types 2N5781, 2N5782, & 2N5783.

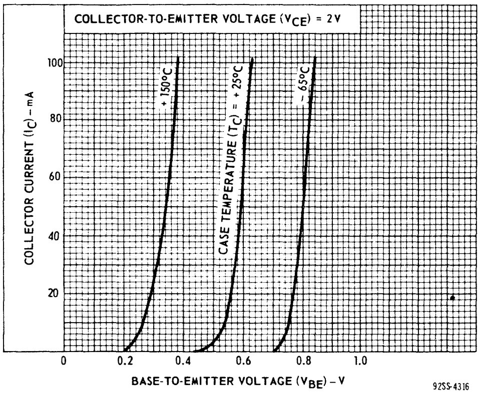


Fig. 14 - Typical transfer characteristics for types 2N5784, 2N5785, & 2N5786.

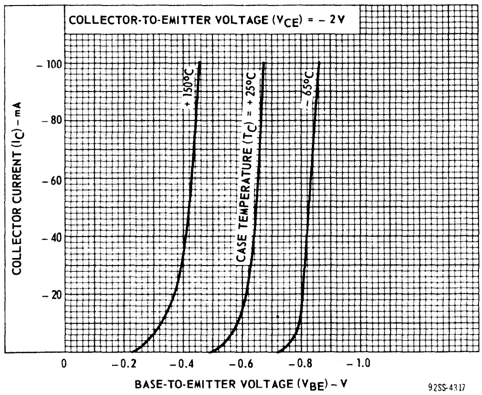


Fig. 15 - Typical transfer characteristics for types 2N5781, 2N5782, & 2N5783.

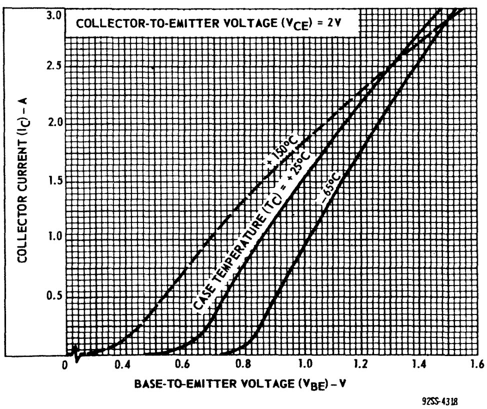


Fig. 16 - Typical transfer characteristics for types 2N5784, 2N5785, & 2N5786.

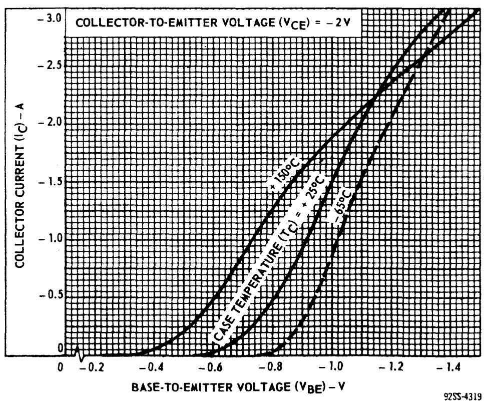


Fig. 17 - Typical transfer characteristics for types 2N5781, 2N5782, 2N5783.

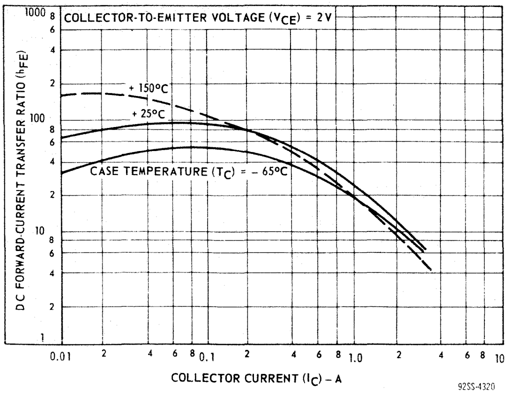


Fig. 18 - Typical DC-beta characteristics for type 2N5784.

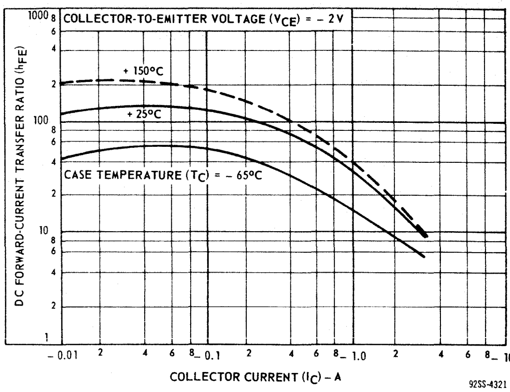


Fig. 19 - Typical DC-beta characteristics for type 2N5781.

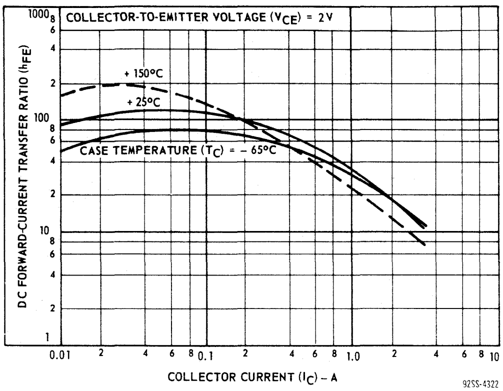


Fig. 20 - Typical DC-beta characteristics for type 2N5785.

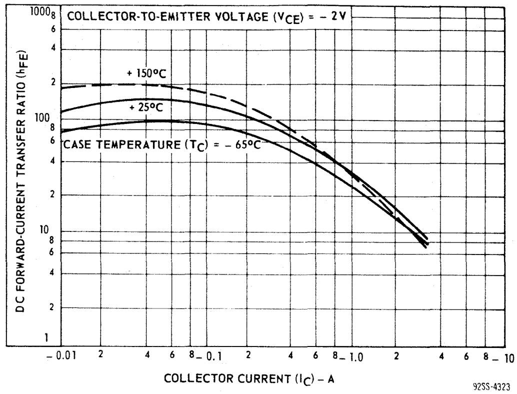


Fig. 21 - Typical DC-beta characteristics for type 2N5782.

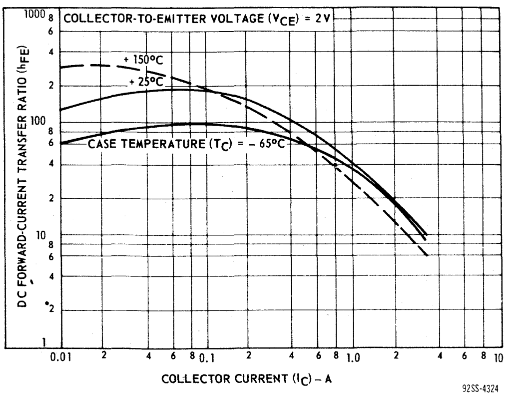


Fig. 22 - Typical DC-beta characteristics for type 2N5786.

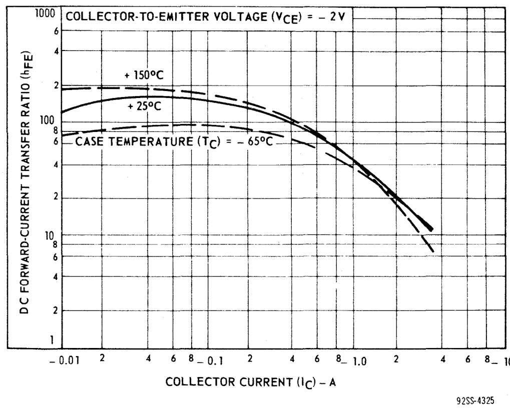


Fig. 23 - Typical DC-beta characteristics for type 2N5783.

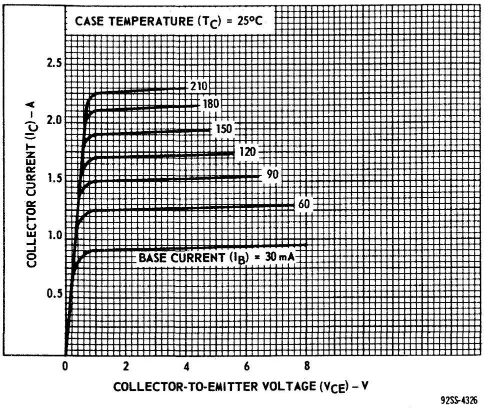


Fig. 24 - Typical output characteristics for type 2N5784.

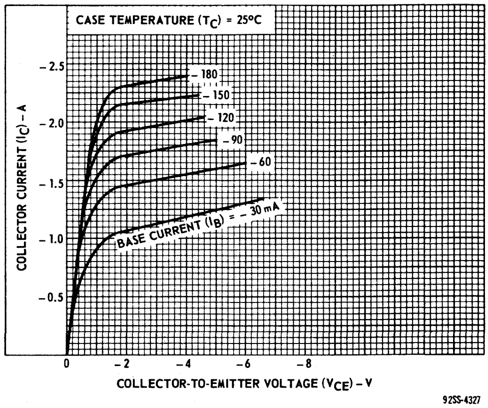


Fig. 25 - Typical output characteristics for type 2N5781.

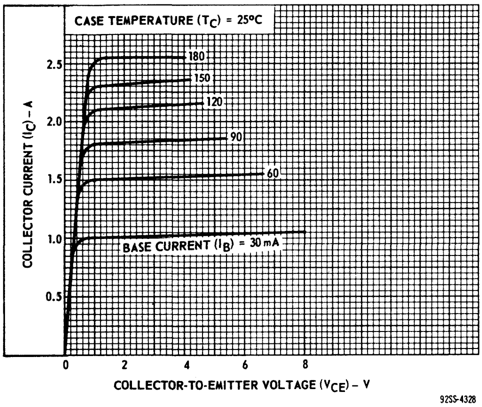


Fig. 26 - Typical output characteristics for type 2N5785.

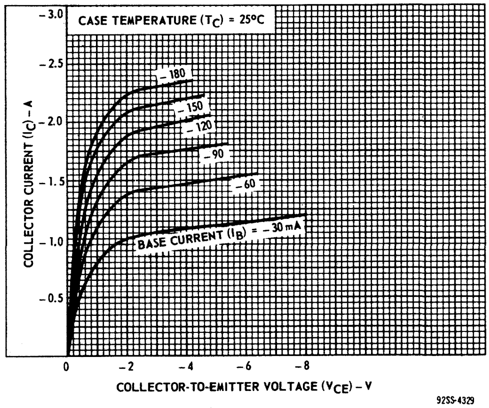


Fig. 27 - Typical output characteristics for type 2N5782.

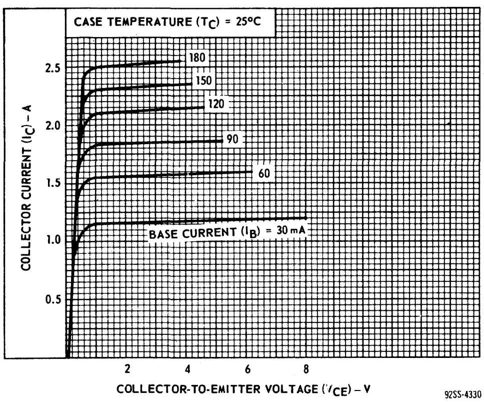


Fig. 28 - Typical output characteristics for type 2N5786.

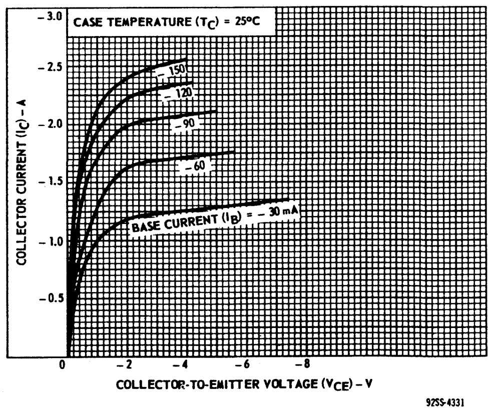


Fig. 29 - Typical output characteristics for type 2N5783.

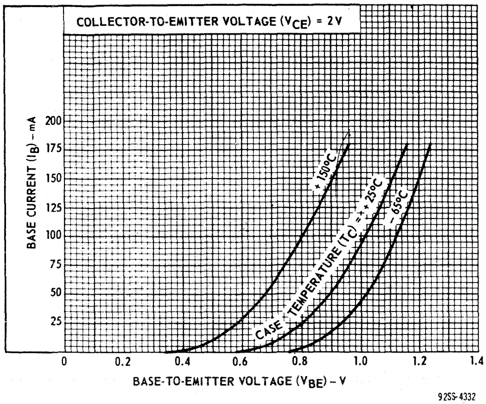


Fig. 30 - Typical input characteristics for type 2N5784.

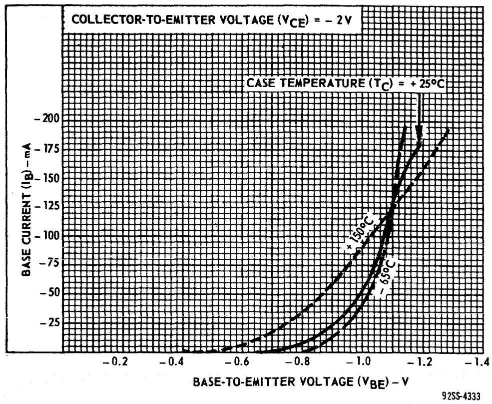


Fig. 31 - Typical input characteristics for type 2N5781.

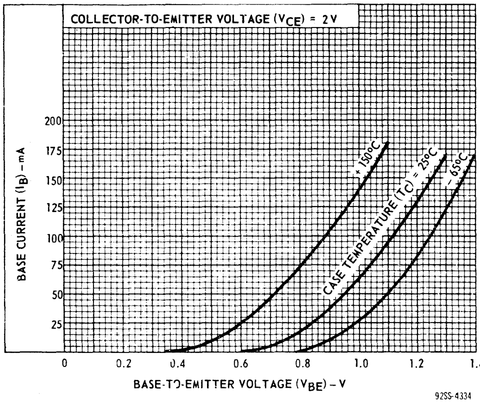


Fig. 32 - Typical input characteristics for type 2N5785.

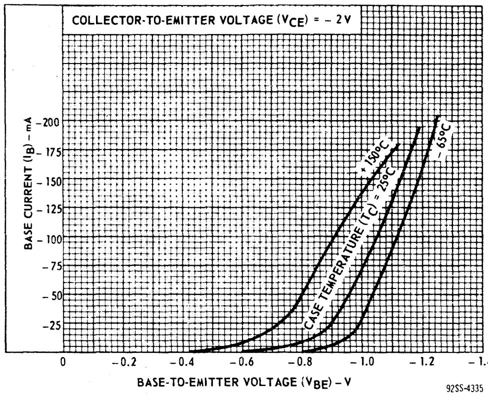


Fig. 33 - Typical input characteristics for type 2N5782.

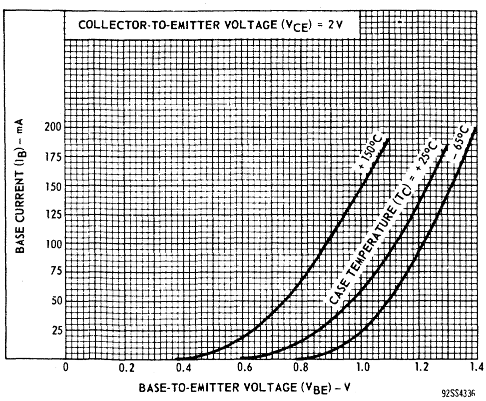


Fig. 34 - Typical input characteristics for type 2N5786.

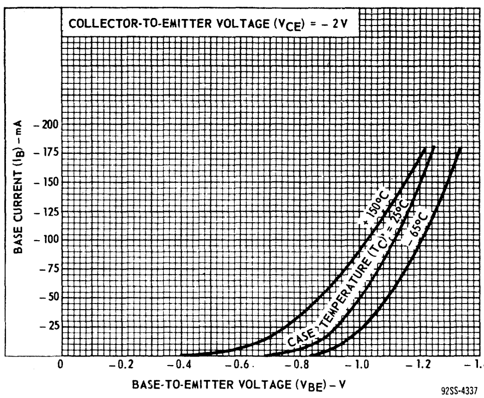
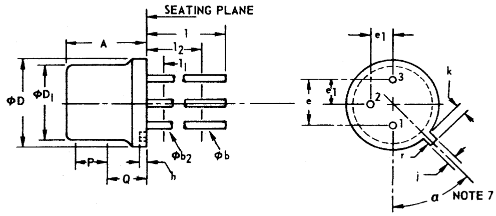


Fig. 35 - Typical input characteristics for type 2N5783.

DIMENSIONAL OUTLINE
(TO-5)



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	.240	.260	6.10	6.60	
Φb	.016	.021	.406	.533	2
Φb_2	.016	.019	.406	.483	2
ΦD	.335	.370	8.51	9.40	
ΦD_1	.305	.335	7.75	8.51	
e	.200 T.P.		5.08 T.P.		4,5
e_1	.100 T.P.		2.54 T.P.		5
h	.009	.125	.229	3.18	
i	.028	.034	.711	.864	5
k	.029	.045	.737	1.14	3,5
l	1.500		38.10		2
l_1		.050		1.27	2
l_2	.250		6.35		2
P	.100		2.54		1
Q					6
r		.007		.179	
α	45° T.P.				5,7

NOTES:

1. This zone is controlled for automatic handling. The variation in actual diameter within the zone shall not exceed 0.010 in. (0.254 mm).
2. (Three leads) Φb_2 applies between l_1 and l_2. Φb applies between l_2 and 1.5 in. (38.10 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond 1.5 in. (38.10 mm) from seating plane.
3. Measured from maximum diameter of the actual device.
4. Leads having maximum diameter 0.019 in. (0.483 mm) measured in gaging plane 0.054 in. (1.37 mm) + 0.001 in. (0.25 mm) – 0.000 in. (0.000 mm) below the seating plane of the device shall be within 0.007 in. (0.178 mm) of their true positions relative to the maximum-width tab.
5. The device may be measured by direct methods or by the gage and gaging procedure described on gage drawing GS-1.
6. Details of outline in this zone optional.
7. Tab centerline.

92SS-3821

TERMINAL CONNECTIONS

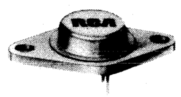
Lead 1 – Emitter
Lead 2 – Base
Lead 3 – Collector
Case – Collector

RCA

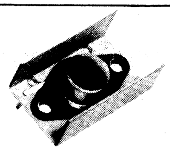
Solid State Division

Power Transistors

2N3054 2N6260 2N6261 40372 40910 40911



JEDEC TO-66 H-1340



JEDEC TO-66
With Integral Heat Radiator H-1470A

Hometaxial II• Medium-Power Silicon N-P-N Transistors

Rugged Devices for Intermediate-Power Applications in Industrial and Commercial Equipment

Features:

- **Maximum safe-area-of-operation curves for dc and pulse operation**
- **V_{CEV}(sus) = 90 V min (2N3054, 2N6261)**
- **Low saturation voltage: V_{CE}(sat) = 1.0 V at I_C = 0.5 A (2N3054)**

RCA 2N3054, 2N6260, and 2N6061 are hometaxial-base• silicon n-p-n transistors intended for a wide variety of medium- to high-power applications.

Types 40372, 40910, and 40911 are the 2N3054, 2N6260, and 2N6061 with factory-attached heat radiators intended for printed-circuit-board applications.

• "Hometaxial" was coined by RCA from "homogeneous" and "axial" to describe a single-diffused transistor with a base region of homogeneous-resistivity in the axial direction (emitter-to-collector).

Applications:

- **Power switching circuits**
- **Series- and shunt-regulator driver and output stages**
- **High-fidelity amplifiers**
- **Solenoid drivers**

"Hometaxial II" is a term used to describe RCA's expanded line of transistors produced by the hometaxial process.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N6260 40910	2N3054 40372	2N6261 40911	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	90	90	V
COLLECTOR-TO-EMITTER VOLTAGE:					
* With base open	V_{CEO}	40	55	80	V
* With external base-to-emitter resistance (R_{BE}) = 100Ω	V_{CER}(sus)	45	60	85	V
With base reverse-biased (V_{BE} = -1.5 V)	V_{CEV}(sus)	50	90	90	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	7	7	V
*CONTINUOUS COLLECTOR CURRENT	I_C	3	4	4	A
*CONTINUOUS BASE CURRENT	I_B	2	2	2	A
TRANSISTOR DISSIPATION:	P_T				
* At case temperature up to 25°C		29 (2N6260)	25 (2N3054)	50 (2N6261)	W
At ambient temperatures up to 25°C		5.8 (40910)	5.8 (40372)	5.8 (40911)	W
* At temperatures above 25°C		*See Figs. 4 & 11*	*See Figs. 4 & 9*	*See Figs. 1 & 7*	
*TEMPERATURE RANGE:					
Storage & Operating (Junction)		←	-65 to 200	→	°C
*PIN TEMPERATURE (During Soldering): At distance ≥1/32 in. (0.8 mm) from seating plane for 10 s max.		←	235	→	°C

*In accordance with JEDEC registration data format JS-9 RDF-10 (2N3054), JS-6 RDF-2 (2N6260, 2N6261)

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	DC Collector Voltage V V_{CE}	DC Emitter or Base Voltage V V_{EB}	V_{BE}	DC Current A I_C	I_B	LIMITS 2N6260 40910 Min.	Max.	2N3054 40372 Min.	Max.	2N6261 40911 Min.	Max.	UNITS
*Collector-Cutoff Current: With base open	I_{CEO}	30				0	–	1	–	0.5	–	–	mA
		60				0	–	–	–	–	–	0.5	
With base-emitter junction reverse-biased	I_{CEX}	40		−1.5			–	5	–	–	–	–	mA
		80		−1.5			–	–	–	–	–	0.5	
		90		−1.5			–	–	–	1.0	–	–	
At T_C = 150°C	I_{CEX}	40		−1.5			–	25	–	–	–	–	mA
		80		−1.5			–	–	–	–	–	1.0	
		90		−1.5			–	–	–	6.0	–	–	
*Emitter-Cutoff Current	I_{EBO}		5			0	–	5	–	–	–	–	mA
			7			0	–	–	–	1.0	–	0.2	
Collector-to-Emitter Sustaining Voltage: *With base open	V_{CEO}(sus)				0.1[a]	0	40	–	55	–	80	–	V
With external base-to-emitter resistance (R_{BE}) = 100Ω	V_{CER}(sus)				0.1[a]		45	–	60	–	85	–	V
*DC Forward-Current Transfer Ratio	h_{FE}	2			4[a]		3	–	–	–	5	–	
		2			1.5[a]		–	–	–	–	25	100	
		4			3[a]		–	–	5	–	–	–	
		4			0.5[a]		–	–	25	100	–	–	
		4			1.5[a]		20	100	–	–	–	–	
*Collector-to-Emitter Saturation Voltage	V_{CE}(sat)				0.5[a]	0.05[a]	–	–	–	1.0	–	–	V
					1.5[a]	0.15[a]	–	1.5	–	–	–	0.5	
					3[a]	1[a]	–	–	–	6.0	–	–	
*Base-to-Emitter Voltage	V_{BE}	2			1.5		–	–	–	–	–	1.5	V
		4			1.5		–	2.2	–	–	–	–	
		4			0.5		–	–	–	1.7	–	–	
*Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio Cutoff Frequency	f_{hfe}	4			0.1		0.03	–	0.03	–	0.03	–	MHz
*Magnitude of Common-Emitter, Small-Signal, Short-Circuit Forward Current Transfer Ratio (f = 0.4 MHz)	$\|h_{fe}\|$	4			0.1		2	–	–	–	2	–	
Gain-Bandwidth Product	f_T				0.2		–	–	800	–	–	–	kHz
*Common-Emitter, Small-Signal, Short-Circuit Forward Current Transfer Ratio (f = 1 kHz)	h_{fe}	4			0.1		25	–	25	–	25	–	
Forward-Bias Second Breakdown Collector Circuit	$I_{S/b}$	40			0.725		1	–	–	–	–	–	s
		80			0.625		–	–	–	–	1	–	
		55			0.455		–	–	1	–	–	–	
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$						6 (max.) 2N6260		7 (max.) 2N3054		3.5 (max.) 2N6261		°C/W
Junction-to-Ambient	$R_{\theta JA}$						30 (max.) 40910		30 (max.) 40372		30 (max.) 40911		

[a]Pulsed: Pulse duration = 300 μs, duty factor = 1.8%.

*In accordance with JEDEC registration data format JS- 9 RDF-10 (2N3054) JS-6 RDF-2 (2N6260-61)

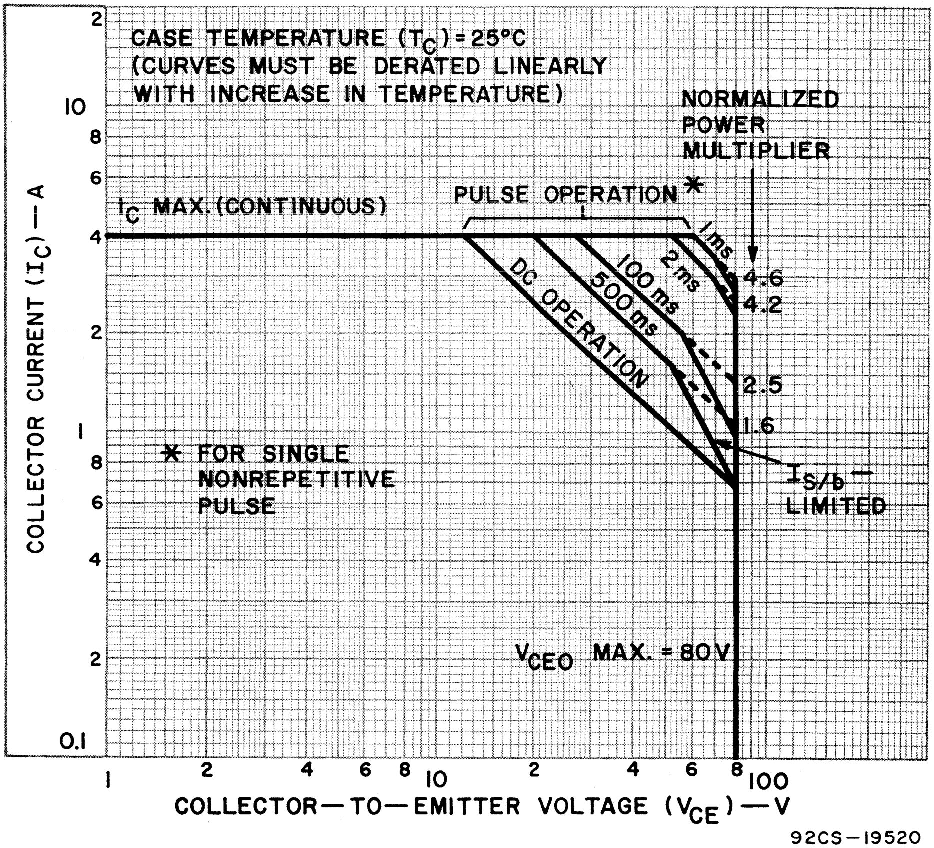


Fig. 1—Maximum operating areas for type 2N6261.

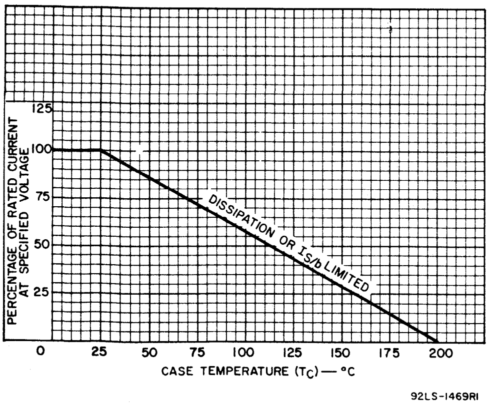


Fig. 2—Current derating curve for all types.

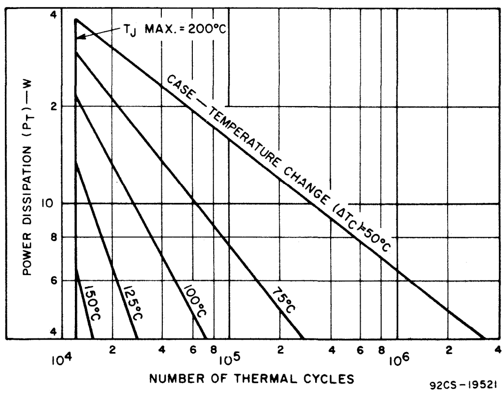


Fig. 3—Thermal-cycle rating chart for type 2N6261.

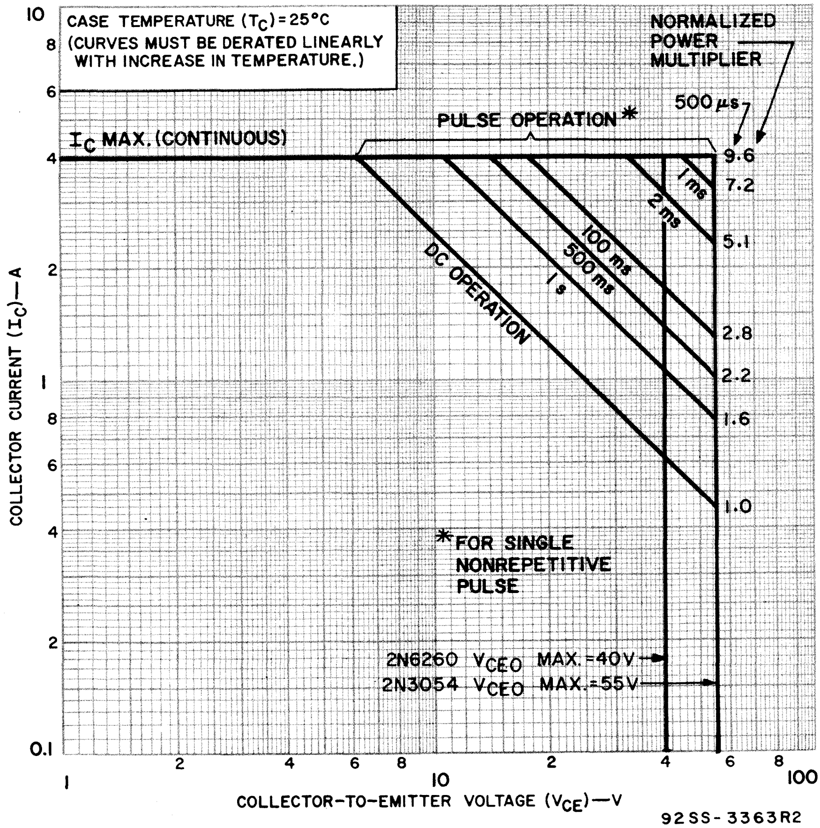


Fig.4—Maximum operating areas for types 2N3054 and 2N6260.

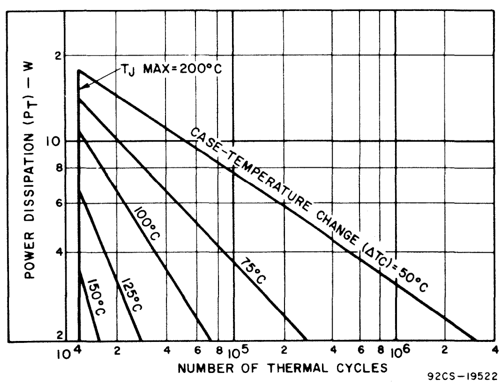


Fig.5— Thermal-cycle rating chart for type 2N3054.

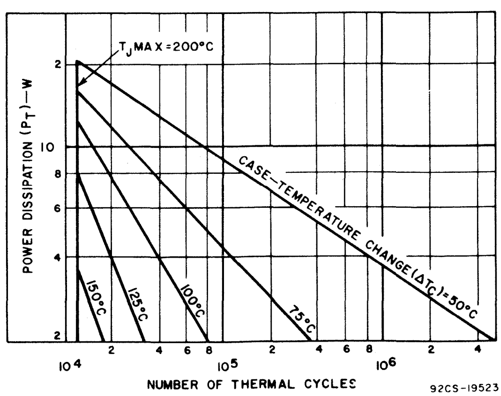


Fig.6—Thermal-cycle rating chart for type 2N6260.

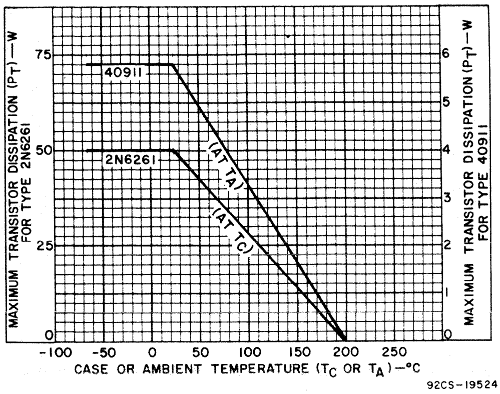


Fig.7—Dissipation derating curve for types 2N6261 and 40911.

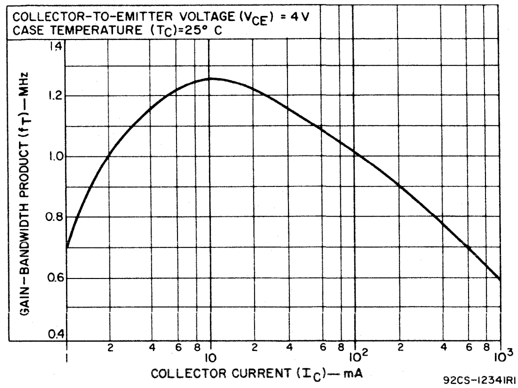


Fig.8—Typical gain-bandwidth product for all types.

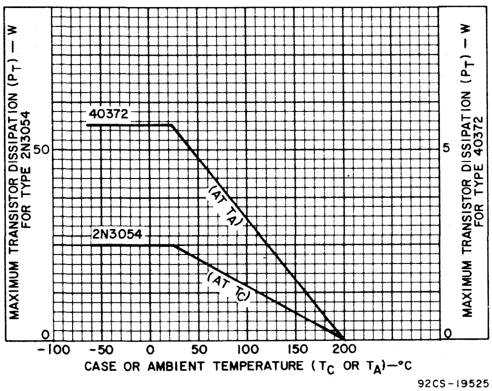


Fig.9—Dissipation derating curve for types 2N3054 and 40372.

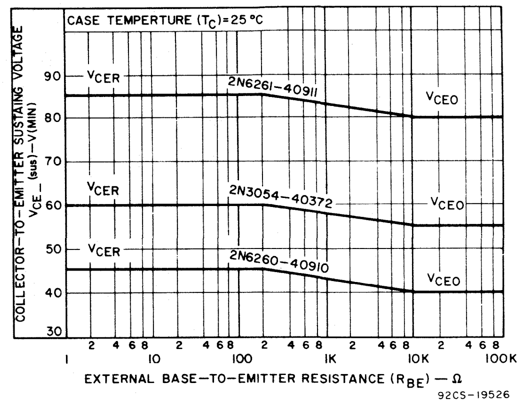


Fig.10—Sustaining voltage vs. base-to-emitter resistance for all types.

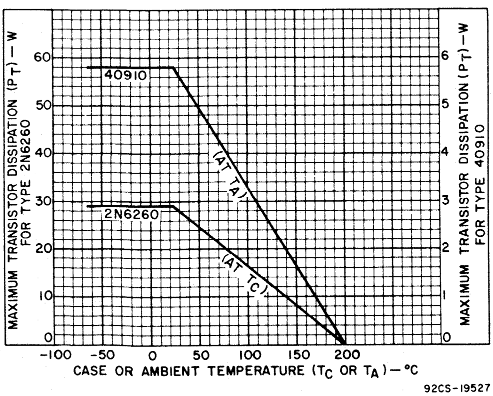


Fig.11—Dissipation derating curve for types 2N6260 and 40910.

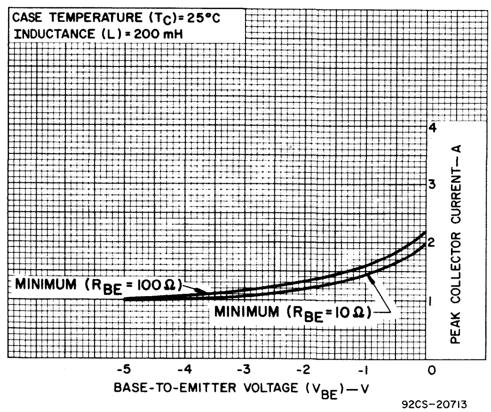


Fig.12—Reverse-bias second-breakdown characteristics for all types.

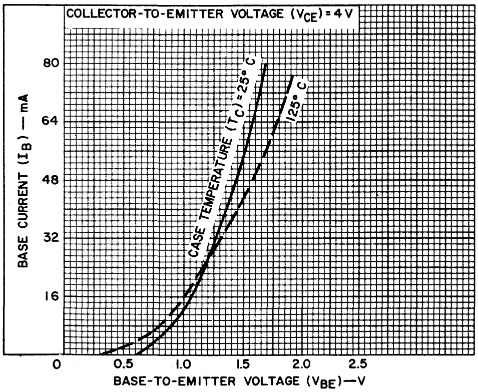


Fig. 13—Typical input characteristics for types 2N6261 and 40911.

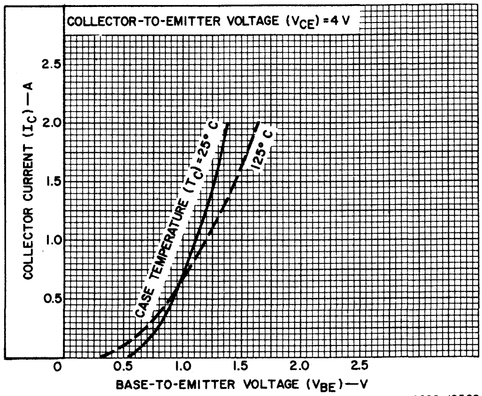


Fig. 14—Typical transfer characteristics for types 2N6261 and 40911.

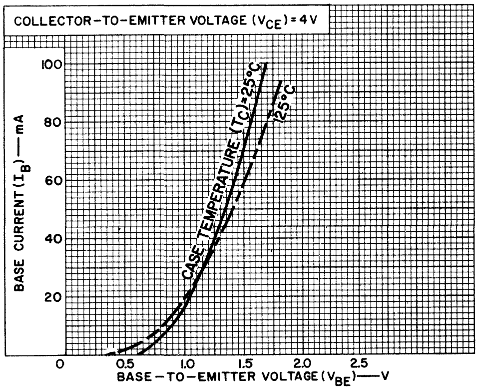


Fig. 15—Typical input characteristics for types 2N3054 and 40372.

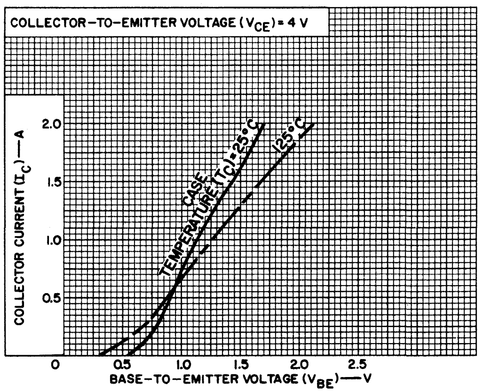


Fig. 16—Typical transfer characteristics for types 2N3054 and 40372.

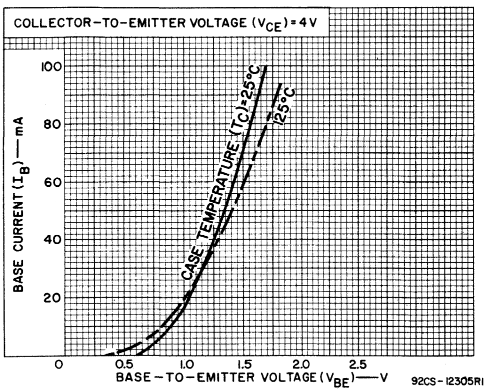


Fig. 17—Typical input characteristics for types 2N6260 and 40910.

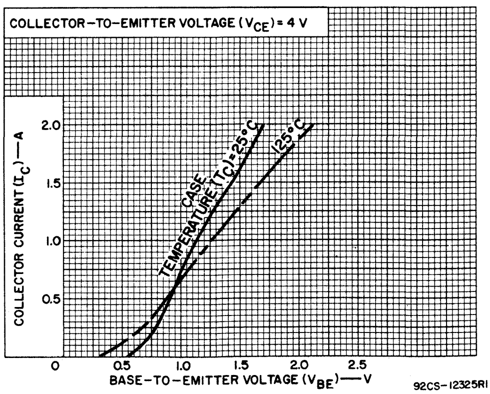


Fig. 18—Typical transfer characteristics for types 2N6260 and 40910.

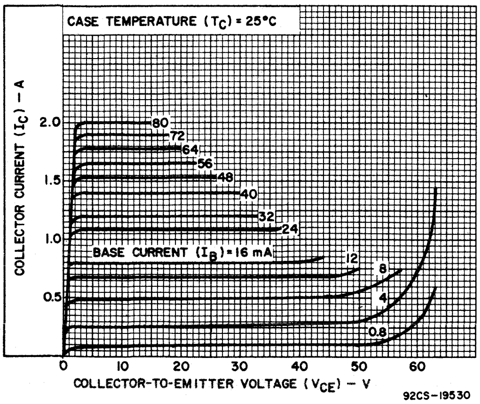


Fig.19—Typical output characteristics for types 2N6261 and 40911.

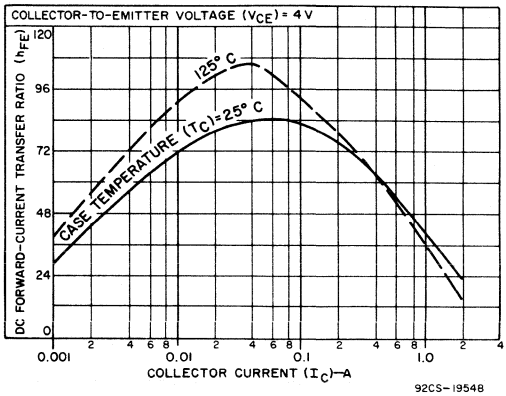


Fig.20—Typical dc beta characteristics for types 2N6261 and 40911.

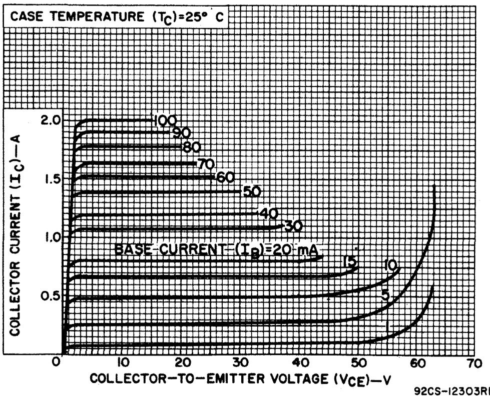


Fig.21—Typical output characteristics for types 2N3054 and 40372.

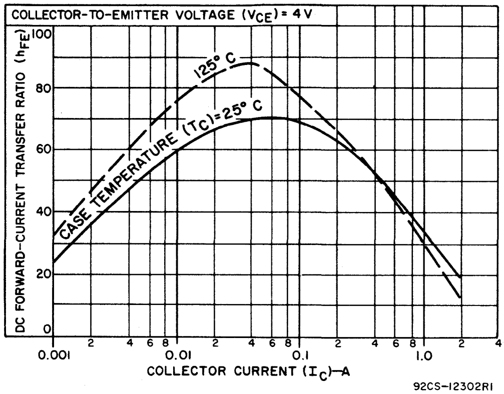


Fig.22—Typical dc beta characteristics for types 2N3054 and 40372.

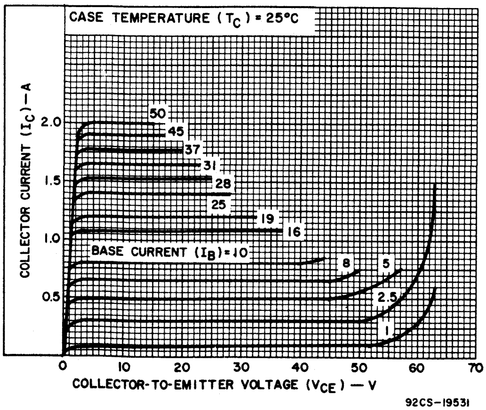


Fig.23—Typical output characteristics for types 2N6260 and 40910.

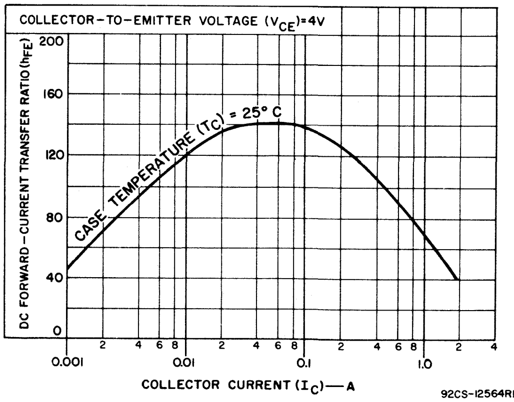
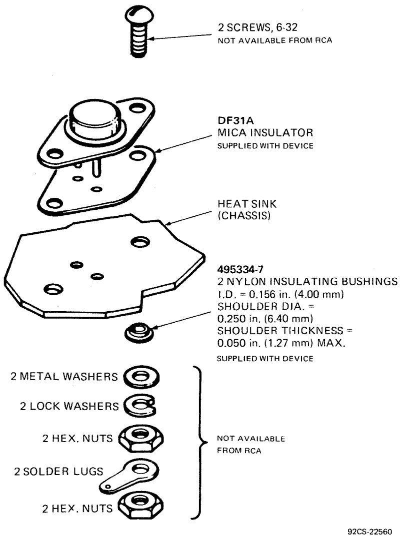


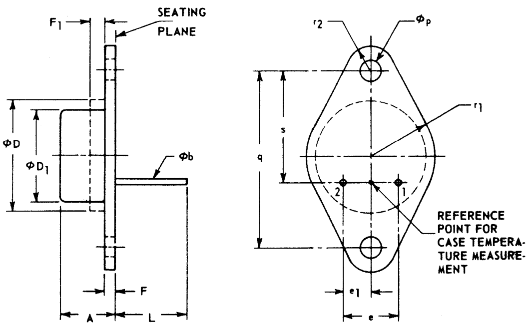
Fig.24—Typical dc beta characteristics for types 2N6260 and 40910.



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.25—Suggested mounting hardware for 2N3054, 2N6260, and 2N6261.

DIMENSIONAL OUTLINE FOR 2N3054, 2N6260, and 2N6261 JEDEC TO-66



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	0.250	0.340	6.35	8.64	
φb	0.028	0.034	0.711	0.863	
φD	—	0.620	—	15.75	
φD1	0.470	0.500	11.94	12.70	
e	0.190	0.210	4.83	5.33	
e1	0.093	0.107	2.36	2.72	
F	0.050	0.075	1.27	1.91	2
F1	—	0.050	—	1.27	1
L	0.360	—	9.14	—	
φp	0.142	0.152	3.61	3.86	
q	0.958	0.962	24.33	24.43	
r1	—	0.350	—	8.89	
r2	—	0.145	—	3.68	
s	0.570	0.590	14.48	14.99	

NOTES:
1. The outline contour is optional within zone defined by φD and F1.
2. Dimensions does not include seating flanges.

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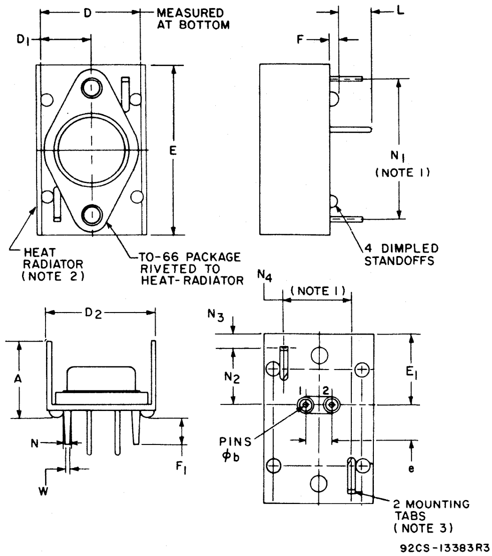
DIMENSIONAL OUTLINE FOR JEDEC TO-66 WITH HEAT RADIATOR



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A		0.595		15.11	
φb	0.028	0.034	0.711	0.864	
D	0.750	0.760	19.05	19.30	
D1	0.375	0.380	9.52	9.65	
D2	0.820	0.920	20.83	23.37	
E	1.297	1.327	32.94	33.70	
E1	0.551	0.561	13.99	14.25	
e	0.190	0.210	4.83	5.33	
F	0.040	0.055	1.02	1.40	
F1	0.175	0.210	4.44	5.33	
L	0.270		0.686		
N	0.052	0.065	1.32	1.65	
N1	1.098	1.102	27.89	27.99	1
N2	0.448	0.452	11.38	11.47	
N3	0.099	0.113	0.25	0.29	
N4	0.498	0.502	12.65	12.75	
W	0.048	0.060	1.22	1.52	

NOTES:
1. Measured at bottom of heat radiator.
2. 0.035 in. (0.889) C.R.S., tin plated.
3. Recommended hole size for printed-circuit board is 0.070 in. (1.778) dia.

TERMINAL CONNECTIONS FOR 40372, 40910 & 40911

Pin 1 - Base
Pin 2 - Emitter
Heat Radiator-Collector

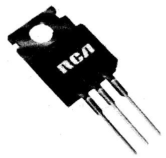
TERMINAL CONNECTIONS FOR 2N3054, 2N6260, & 2N6261

Pin 1 - Base
Pin 2 - Emitter
Case, Mounting Flange - Collector

RCA
Solid State Division

Power Transistors

RCA3054 RCA3055



RCA3054
RCA3055

JEDEC TO-220AB H-1535R1

Hometaxial-Base Silicon N-P-N VERSAWATT Transistors

Designed for Medium-Power Linear and Switching Service in Consumer, Automotive, and Industrial Applications

Features:
- **Maximum safe-area-of-operation curves**
- **Low saturation voltages**
- **High dissipation ratings**
- **Thermal-cycle rating curves**

Applications:
- **Series and shunt regulators**
- **High-fidelity amplifiers**
- **Power-switching circuits**
- **Solenoid drivers**

RCA3054 and RCA3055 are silicon n-p-n transistors intended for a wide variety of high-current applications. The hometaxial-base construction of these devices renders them highly resistant to second breakdown over a wide range of operating conditions.

The VERSAWATT case has a proven thermal-cycle capability. This capability is assured by real-time quality controls in our manufacturing locations. The RCA3054 and RCA3055 are supplied in the JEDEC TO-220AB straight-lead version of the package. They are also available on special order in a variety of lead-form configurations. Two popular variations have leads formed to fit TO-66 sockets (specify formed lead No. 6201) or printed-circuit boards (specify formed lead No. 6207). Detailed information on these and other VERSAWATT outlines is contained in "RCA's Lineup of Power Transistors" (PSP-704).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		RCA3054	RCA3055	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	90	100	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:				
With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$	60	70	V
With base open	$V_{CEO}(sus)$	55	60	V
With base reverse-biased V_{BE} = −1.5 V	$V_{CEV}(sus)$	90	90	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	7	7	V
CONTINUOUS COLLECTOR CURRENT	I_C	4	15	A
CONTINUOUS BASE CURRENT	I_B	2	4	A
TRANSISTOR DISSIPATION:	P_T			
At case temperatures up to 25°C		36	75	W
At case temperatures above 25°C		See Fig.3		
TEMPERATURE RANGE:				
Storage and Operating (Junction)		−65 to +150		°C
PIN TEMPERATURE (During Soldering):				
At distances ≥ 1/32 in. (0.8 mm) from seating plane for 10 s max.		235		°C

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ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS				UNITS
		VOLTAGE V dc			CURRENT A dc		RCA3054		RCA3055		
		V_{CE}	V_{EB}	V_{BE}	I_C	I_B	MIN.	MAX.	MIN.	MAX.	
Collector-Cutoff Current: With base open	I_{CEO}	30				0	–	0.5	–	0.7	
With base-emitter junction reverse-biased	I_{CEX}	90 100		−1.5 −1.5			– –	1 –	– –	– 5	mA
At T_C = 150°C	I_{CEX}	90 100		−1.5 −1.5			– –	6 –	– –	– 30	
Emitter-Cutoff Current	I_{EBO}		7		0		–	1.0	–	5	mA
Collector-to-Emitter Sustaining Voltage: With base open	$V_{CEO}(sus)$				0.1[a] 0.2[a]	0 0	55 –	– –	– 60	– –	
With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$				0.1[a] 0.2[a]		60 –	– –	– 70	– –	V
With base-emitter junction reverse-biased	$V_{CEV}(sus)$			−1.5	0.1[a]		90	–	90	–	
DC Forward-Current Transfer Ratio	h_{FE}	4 4 4 4			3[a] 10[a] 0.5[a] 4[a]		5 – 25 –	– – 100 –	– 5 – 20	– – – 70	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				0.5[a] 4[a]	0.05[a] 0.4[a]	– –	1.0 –	– –	– 1.1	V
Base-to-Emitter Voltage	V_{BE}	4 4			0.5[a] 4[a]		– –	1.7 –	– –	– 1.8	V
Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio Cutoff Frequency	f_{hfe}	4 4			0.1 1		30 –	– –	– 10	– –	kHz
Magnitude of Common-Emitter, Small-Signal Short-Circuit Forward Current Transfer Ratio (f = 0.4 MHz)	$\|h_{fe}\|$	4 4			0.1 1		2 –	– –	– 2	– –	
Common-Emitter, Small-Signal, Short-Circuit Forward Current Transfer Ratio (f = 1 kHz)	h_{fe}	4 4			0.1 1		25 –	– –	– 15	– 120	
Forward-Bias Second Breakdown Collector Current[b] (t ≥ 1 s)	$I_{S/b}$	55 60					0.65 –	– –	– 1.2	– –	A
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$						–	3.5	–	1.67	°C/W
Junction-to-Ambient	$R_{\theta JA}$						–	70	–	70	

[a] Pulsed: Pulse duration = 300 μs, duty factor = 1.8%.
[b] Pulsed: 1-second non-repetitive pulse.

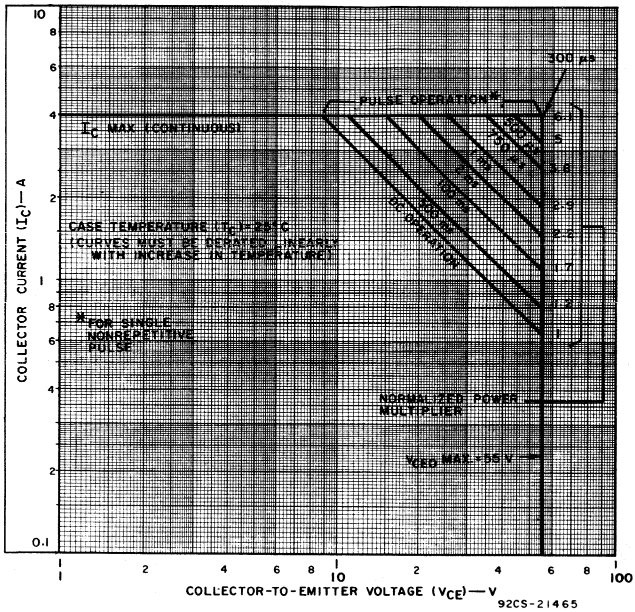


Fig. 1—Maximum operating areas for RCA3054.

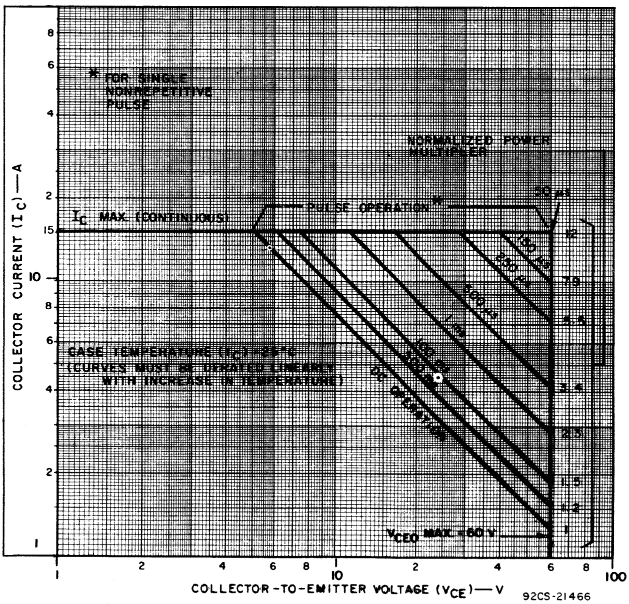


Fig. 2—Maximum operating areas for RCA3055.

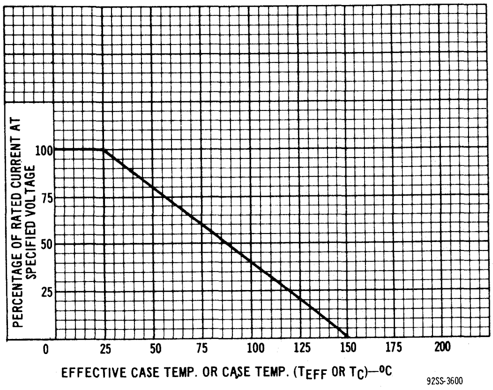


Fig.3 — Derating curve for both types.

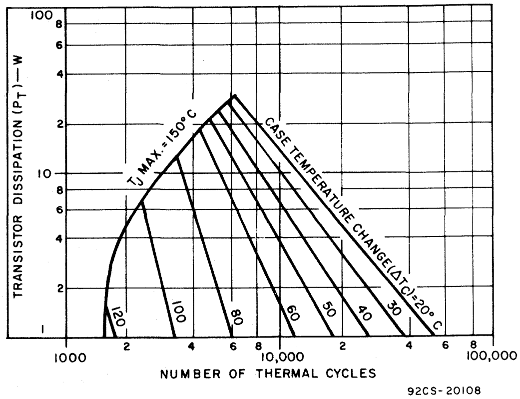


Fig.4 — Thermal-cycling rating chart for RCA3054.

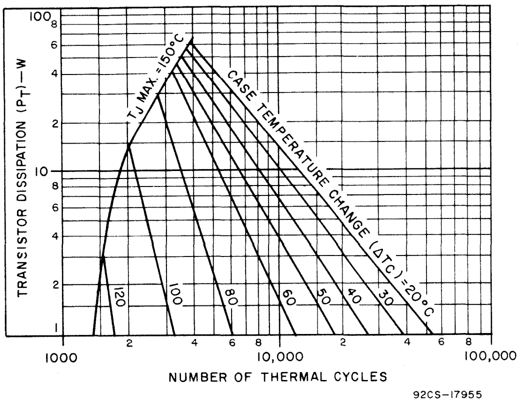


Fig.5 — Thermal-cycling rating chart for RCA3055.

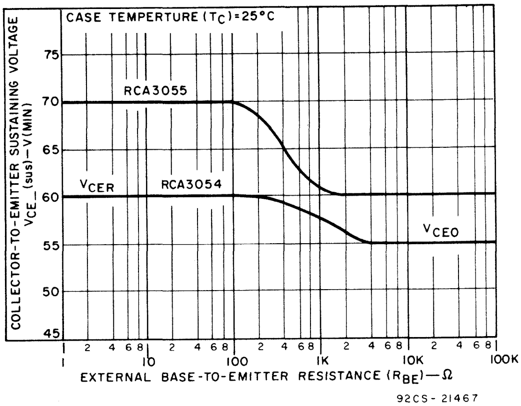


Fig.6 — Sustaining voltage vs. base-to-emitter resistance for both types.

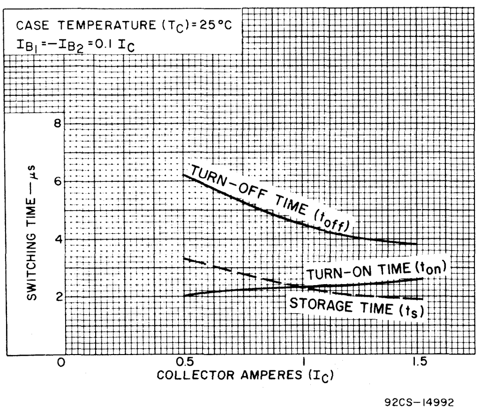


Fig.7 — Typical saturated switching characteristics for RCA3054.

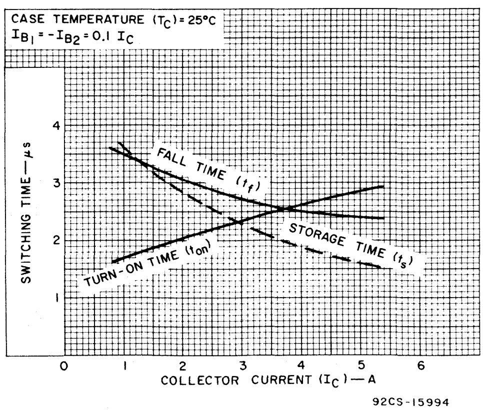


Fig.8 — Typical saturated switching characteristics for RCA3055.

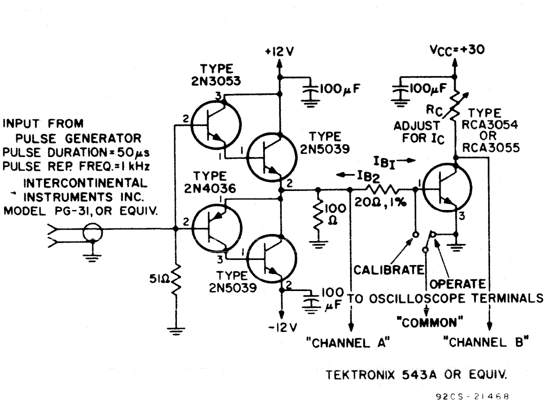


Fig.9 – Circuit used to measure switching times.

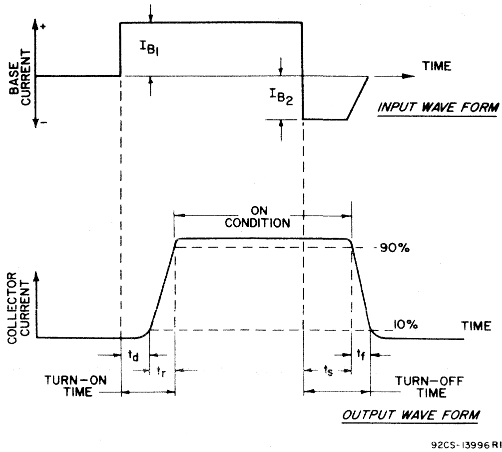


Fig.10 – Phase relationship between input current and output current showing reference points for specification of switching times. (Test circuit shown in Fig.9).

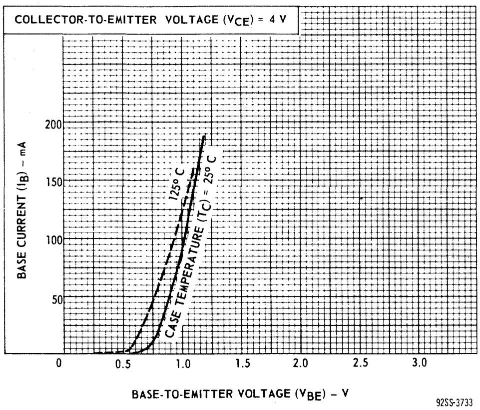


Fig.11 – Typical input characteristics for RCA3054.

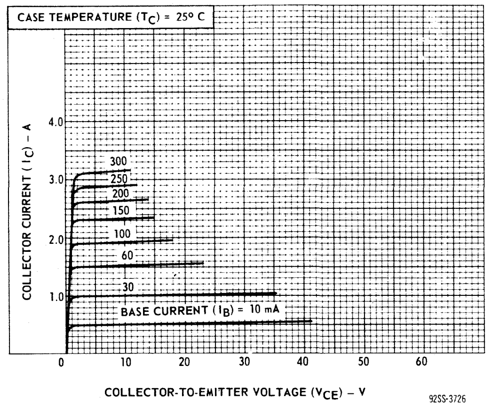


Fig.12 – Typical output characteristics for RCA3054.

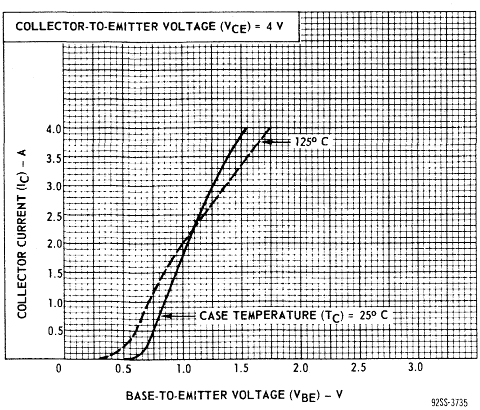


Fig.13 – Typical transfer characteristics for RCA3054.

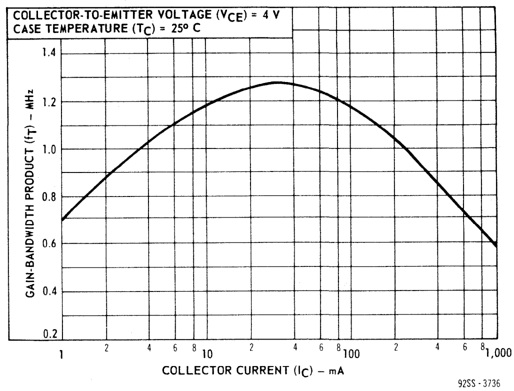


Fig.14 – Typical gain-bandwidth product for RCA3054.

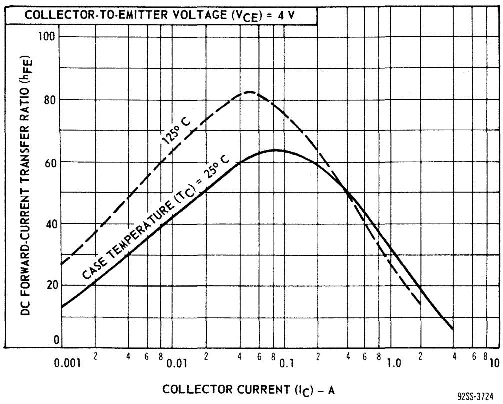


Fig.15 – Typical dc beta characteristics for RCA3054.

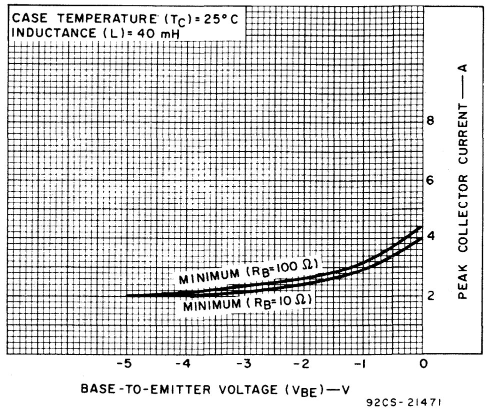


Fig.16 – Reverse-bias second breakdown characteristics for RCA3054.

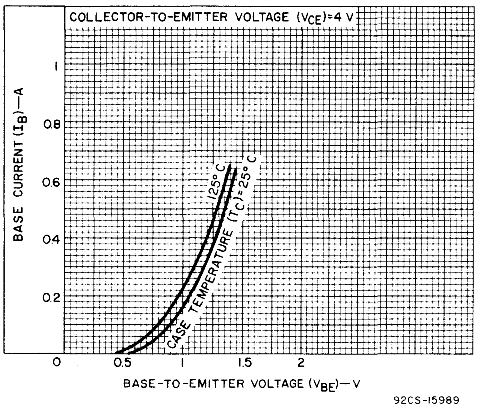


Fig.17 – Typical input characteristics for RCA3055.

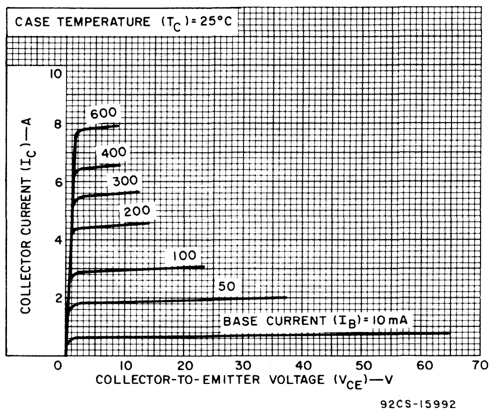


Fig.18 – Typical output characteristics for RCA3055.

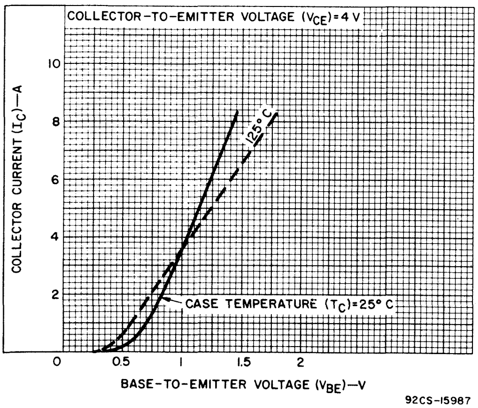


Fig.19 – Typical transfer characteristics for RCA3055.

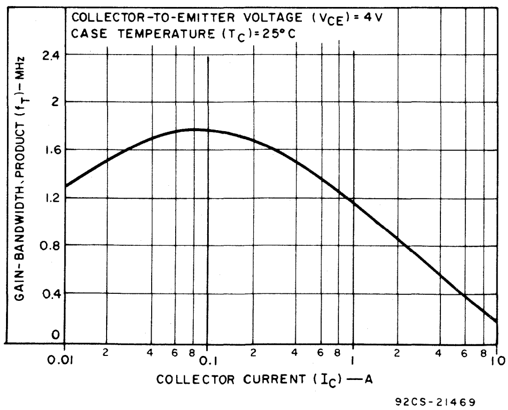


Fig.20 – Typical gain-bandwidth product for RCA3055.

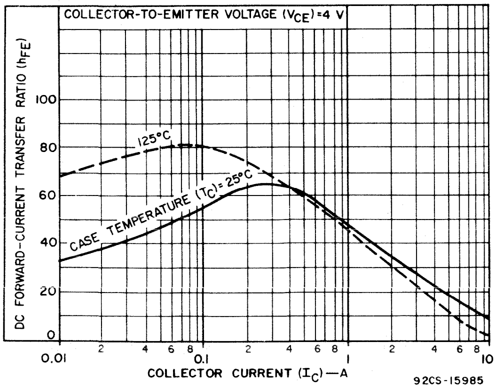


Fig.21 — Typical dc beta characteristics for RCA3055.

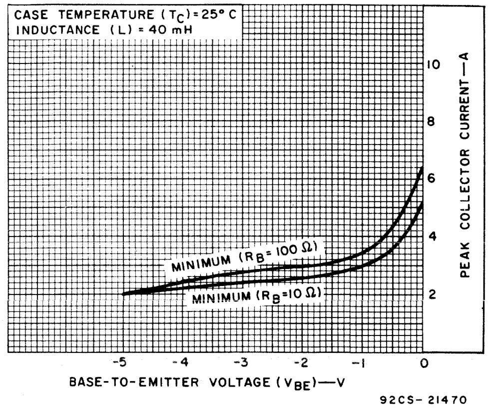
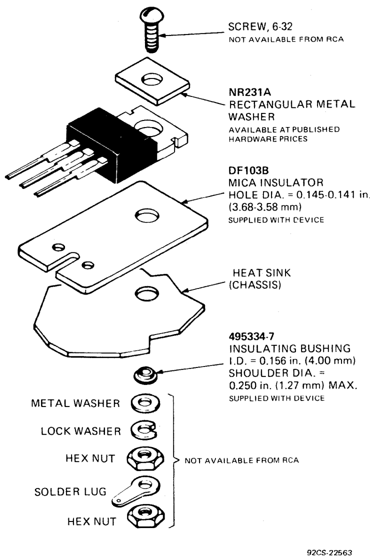


Fig.22 — Reverse-bias second-breakdown characteristics for RCA3055.



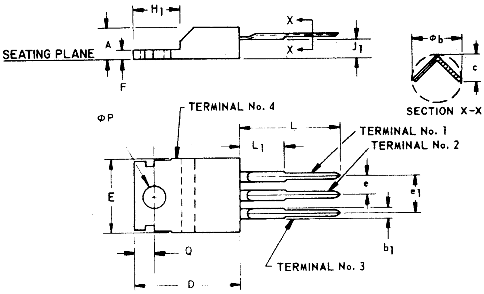
In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.23—Suggested mounting hardware for JEDEC TO-220AB

VERSAWATT PACKAGE MOUNTING . . . . .

For complete discussion on handling and mounting of RCA molded-plastic power devices, refer to RCA application note AN-4124.

DIMENSIONAL OUTLINE
JEDEC TO-220AB



BOTTOM VIEW

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS
JEDEC TO-220AB

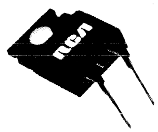
Terminal No.1 – Base
Terminal No.2 – Collector
Terminal No.3 – Emitter
Terminal No.4 – Collector

For basic transistor theory, circuits, and application information, refer to "RCA Solid-State Power Circuits Designer's Handbook", SP-52, or "RCA Transistor, Thyristor, & Diode Manual", SC-15.

Solid State Division

Power Transistors

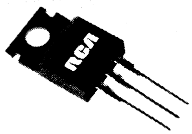
2N5293 2N5294 2N5295 2N5296 2N5297 2N5298



2N5293
2N5295
2N5297

For TO-66 Sockets

H 1534R1



2N5294
2N5296
2N5298

H 1535R1

Hometaxial-Base, Silicon N-P-N VERSAWATT Transistors

General-Purpose Types for Medium-Power Switching and Amplifier Applications in Military, Industrial, and Commercial Equipment

FEATURES

- **Low saturation voltage–**
  $V_{CE}(sat)$ = 1 V max. at I_C = 0.5 A (2N5293, 2N5294)
  = 1 V max. at I_C = 1 A (2N5295, 2N5296)
  = 1 V max. at I_C = 1.5 A (2N5297, 2N5298)
- **VERSAWATT package (molded-silicone plastic)**
- **Maximum safe-area-of-operation curves specified for DC and pulse service**

RCA-2N5293, 2N5294, 2N5295, 2N5296, 2N5297 and 2N5298* are hometaxial-base silicon n-p-n transistors. They are intended for a wide variety of medium-power switching and amplifier applications such as series and shunt regulators, and in driver and output stages of high-fidelity amplifiers. Types 2N5293, 2N5295, and 2N5297 have formed emitter and base leads for easy insertion into TO-66 sockets. Types 2N5294, 2N5296, and 2N5298 are electrically identical to the 2N5293, 2N5295, and 2N5297, respectively, but have straight leads.

These new plastic power transistors differ in voltage ratings and in the currents at which the parameters are controlled.

* Formerly RCA Dev. Type Nos.TA7155, TA2911, TA7156, TA7137, TA7362, and TA7363, respectively.

OPTIONAL LEAD CONFIGURATION

An additional lead forming for printed-circuit-board mounting is also available. (See page 6).

Please submit requirements to your RCA Technical Sales Representative, or write to RCA Low-Frequency Power Marketing, Somerville, N. J. 08876.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N5293 2N5294	2N5295 2N5296	2N5297 2N5298	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	80	60	80	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:					
With −1.5 volts (V_{BE}) of reverse bias	$V_{CEV}(sus)$	80	60	80	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$	75	50	70	V
With base open	$V_{CEO}(sus)$	70	40	60	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	7	5	5	V
COLLECTOR CURRENT	I_C	4	4	4	A
BASE CURRENT	I_B	2	2	2	A
TRANSISTOR DISSIPATION:	P_T				
At case temperatures up to 25°C		36	36	36	W
At case temperatures above 25°C		Derate linearly at 0.288 W/°C or see Fig. 1 & 2.			
At ambient temperatures up to 25°C		1.8	1.8	1.8	W
At ambient temperatures above 25°C		Derate linearly at 0.0144 W/°C			
TEMPERATURE RANGE:					
Storage & Operating (Junction)		−65 to +150			°C
LEAD TEMPERATURE (During Soldering):					
At distance ≥ 1/8 in. (3.17 mm) from case for 10 s max.		235			°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C, Unless Otherwise Specified.*

Characteristic	Symbol	TEST CONDITIONS: DC Collector Voltage (V) V_{CE}	DC Emitter or Base Voltage (V) V_{EB}	DC Emitter or Base Voltage (V) V_{BE}	DC Current (A) I_C	DC Current (A) I_B	LIMITS 2N5293 2N5294 Min.	2N5293 2N5294 Max.	2N5295 2N5296 Min.	2N5295 2N5296 Max.	2N5297 2N5298 Min.	2N5297 2N5298 Max.	Units
Collector-Cutoff Current With base-emitter junction reverse biased	I_{CEV}	65		-1.5			–	0.5	–	–	–	0.5	mA
		35		-1.5			–	–	–	2	–	–	
	I_{CEV} (T_C = 150°C)	65		-1.5			–	3	–	–	–	3	mA
		35		-1.5			–	–	–	5	–	–	
Collector-Cutoff Current With external base-to-emitter resistance (R_{BE}) = 100 Ω	I_{CER}	50					–	0.5	–	–	–	0.5	mA
	I_{CER} (T_C = 150°C)	50					–	2	–	–	–	2	mA
Emitter-Cutoff Current	I_{EBO}		7				–	1	–	–	–	–	mA
			5				–	–	–	1	–	1	
DC Forward-Current Transfer Ratio	h_{FE}[c]	4			0.5		30	120	–	–	–	–	
		4			1		–	–	30	120	–	–	
		4			1.5		–	–	–	–	20	80	
Collector-to-Emitter Sustaining Voltage With base open	$V_{CEO}(sus)$[c]				0.1	0	70	–	–	–	–	–	V
					0.1	0	–	–	40	–	–	–	
					0.1	0	–	–	–	–	60	–	
With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$[c]				0.1		75	–	–	–	–	–	V
					0.1		–	–	50	–	–	–	
					0.1		–	–	–	–	70	–	
With base-emitter junction reverse biased	$V_{CEV}(sus)$[c]			-1.5	0.1		80	–	–	–	–	–	V
				-1.5	0.1		–	–	60	–	–	–	
				-1.5	0.1		–	–	–	–	80	–	
Base-to-Emitter Voltage	V_{BE}[c]	4			0.5		–	1.1	–	–	–	–	V
		4			1		–	–	–	1.3	–	–	
		4			1.5		–	–	–	–	–	1.5	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$[c]				0.5	0.05	–	1	–	–	–	–	V
					1	0.1	–	–	–	1	–	–	
					1.5	0.15	–	–	–	–	–	1	
Gain-Bandwidth Product	f_T	4			0.2		0.8	–	0.8	–	0.8	–	MHz
Sat. Switching Time Turn-On (See Figs. 22 - 24)	t_{on}	V_{CC} = 30			0.5	0.05[a]	–	5	–	–	–	–	μs
					1	0.1[a]	–	–	–	5	–	–	
					1.5	0.15[a]	–	–	–	–	–	5	
Turn-Off (See Figs. 22 - 24)	t_{off}	V_{CC} = 30			0.5	-0.05[a]	–	15	–	–	–	–	μs
					1	-0.1[b]	–	–	–	15	–	–	
					1.5	-0.15[b]	–	–	–	–	–	15	
Thermal Resistance (Junction-to-Case)	θ_{J-C}						–	3.5	–	3.5	–	3.5	°C/W
(Junction-to-Ambient)	θ_{J-A}						–	70	–	70	–	70	°C/W

[a] I_{B_1} value (turn-on base current).

[b] I_{B_2} value (turn-off base current).

[c] Pulsed, pulse duration = 300 μs, duty factor = .018.

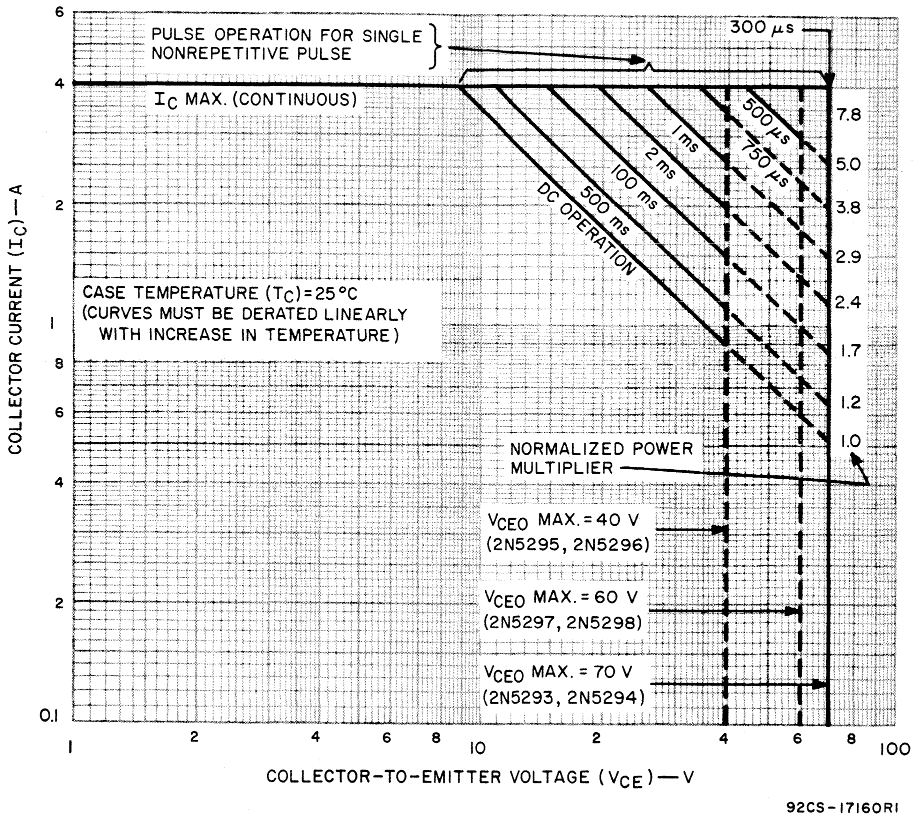


Fig.1—Maximum operating areas for all types.

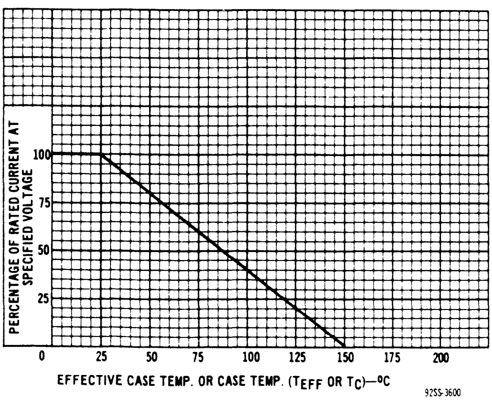


Fig.2—Derating curve for all types.

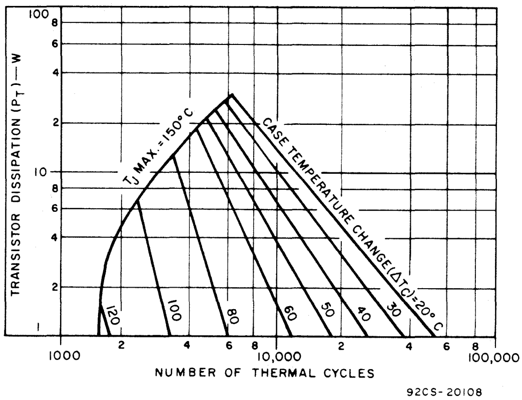


Fig.3—Thermal-cycling rating chart for all types.

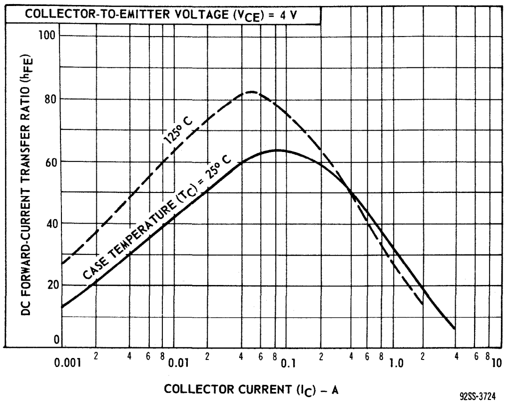


Fig.4 — Typical DC beta for types 2N5293 & 2N5294.

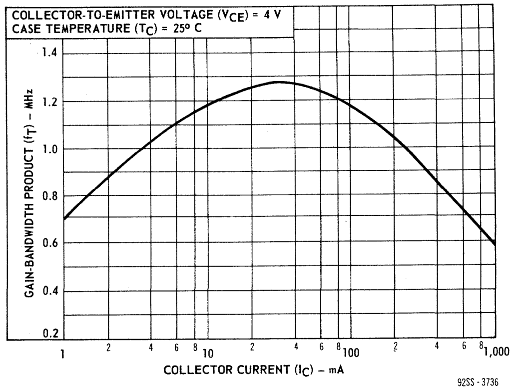


Fig.5—Typical gain-bandwidth product for types 2N5293 & 2N5294.

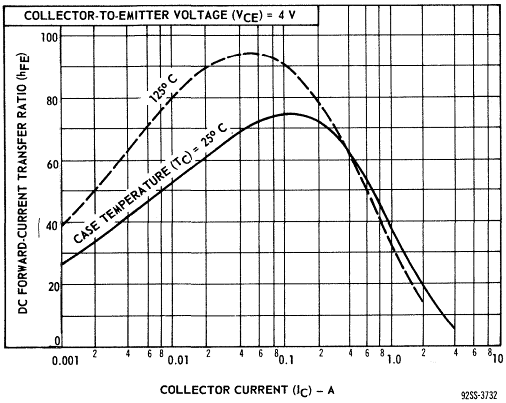


Fig.6—Typical DC beta for types 2N5295 & 2N5296.

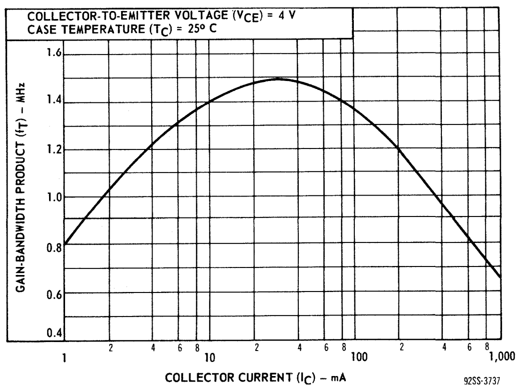


Fig.7—Typical gain-bandwidth product for types 2N5295 & 2N5296.

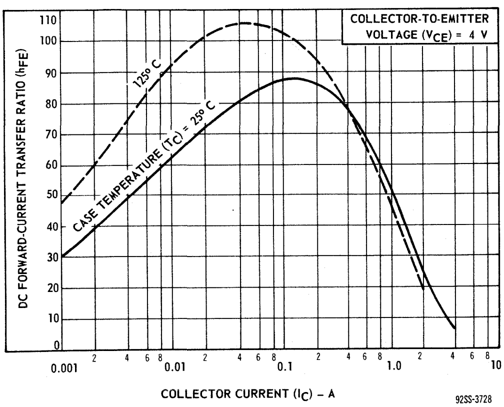


Fig.8—Typical DC beta for types 2N5297 & 2N5298.

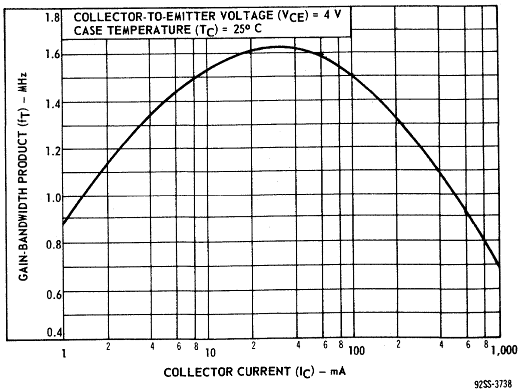


Fig.9—Typical gain-bandwidth product for types 2N5297 & 2N5298.

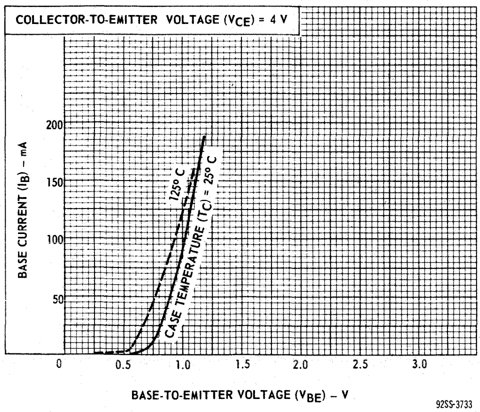


Fig. 10—Typical input characteristics for types 2N5293 & 2N5294.

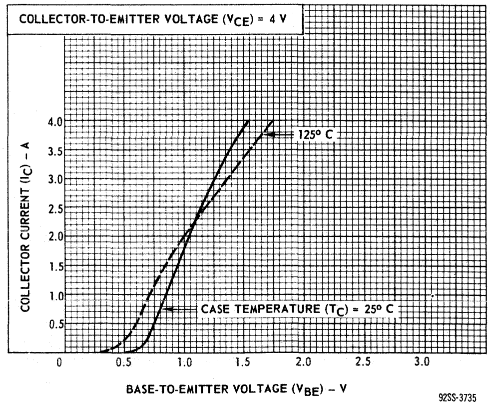


Fig. 11—Typical transfer characteristics for types 2N5293 & 2N5294.

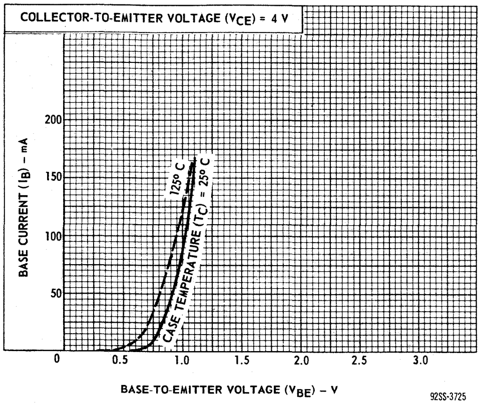


Fig. 12—Typical input characteristics for types 2N5295 & 2N5296.

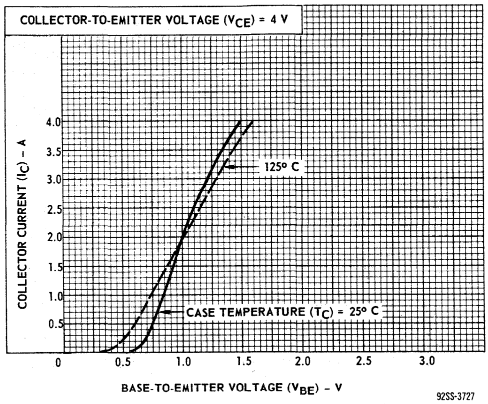


Fig. 13—Typical transfer characteristics for types 2N5295 & 2N5296.

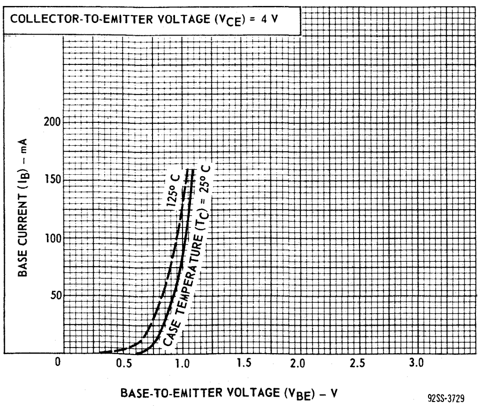


Fig. 14—Typical input characteristics for types 2N5297 & 2N5298.

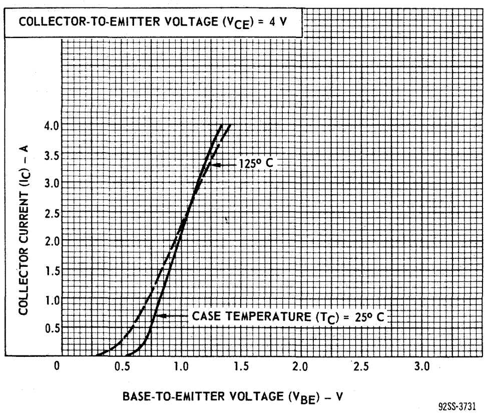


Fig. 15—Typical transfer characteristics for types 2N5297 & 2N5298.

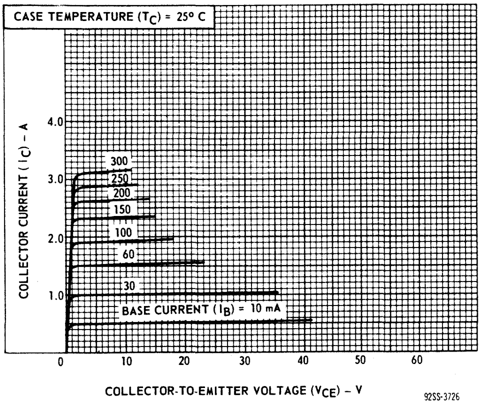


Fig.16—Typical output characteristics for types 2N5293 & 2N5294.

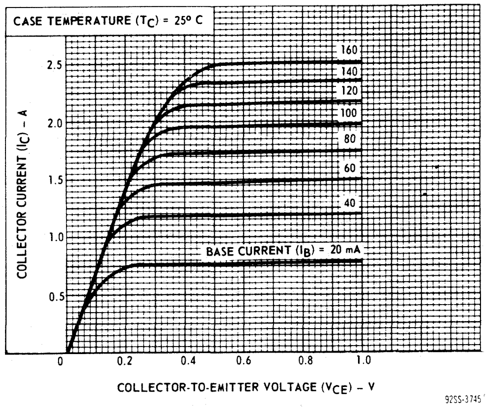


Fig.17—Typical output characteristics for types 2N5295 & 2N5296.

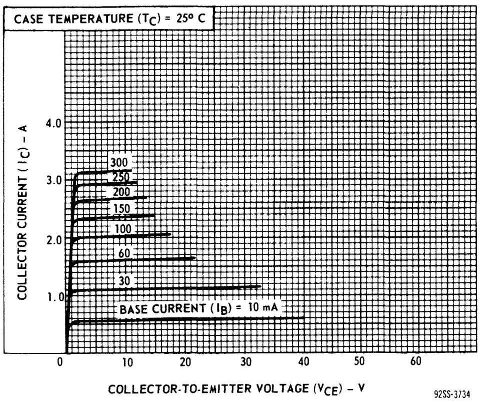


Fig.18—Typical output characteristics for types 2N5295 & 2N5296.

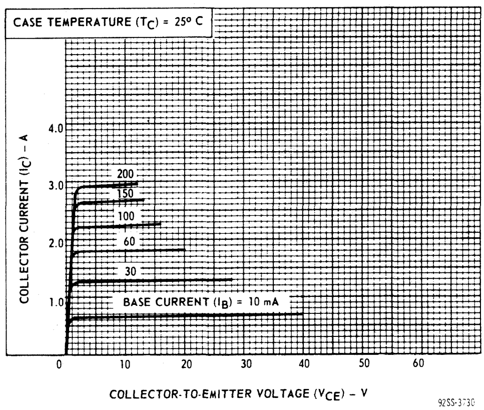


Fig.19—Typical output characteristics for types 2N5297 & 2N5298

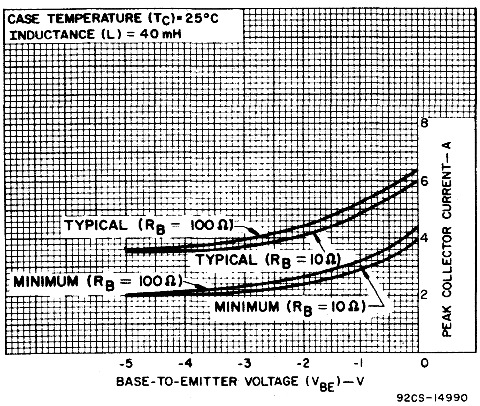


Fig.20—Reverse-bias, second-breakdown characteristics for all types.

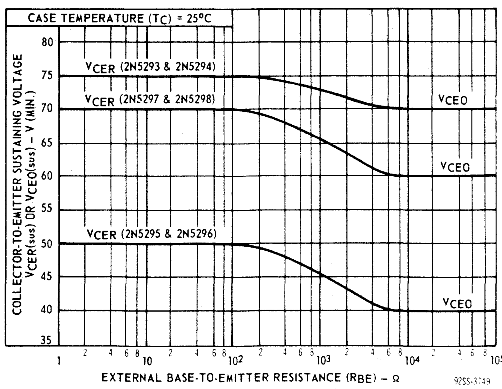
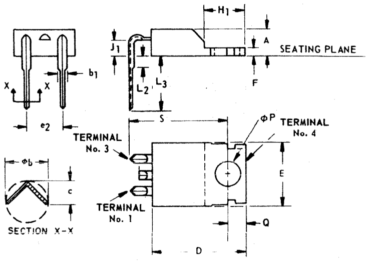


Fig.21—Sustaining voltage vs. base-to-emitter resistance for all types.

DIMENSIONAL OUTLINE FOR TYPES 2N5293, 2N5295, AND 2N5297



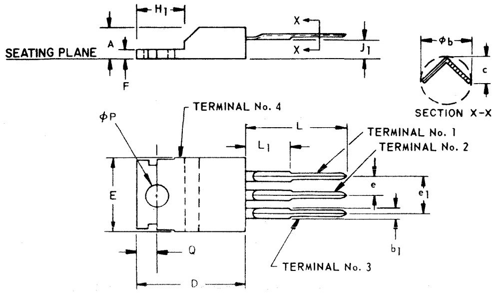
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
ϕb	0.02	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e_2	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L_2	–	0.050	–	1.27	–
L_3	0.360	0.422	9.15	10.71	–
ϕP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–
S	0.580	0.610	14.74	15.49	–

92CS-17990R1

NOTES:

1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.050 – 0.055 (1.27 – 1.40 mm) below seating plane.

DIMENSIONAL OUTLINE FOR TYPES 2N5294, 2N5296, AND 2N5298



BOTTOM VIEW

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
ϕb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
ϕP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

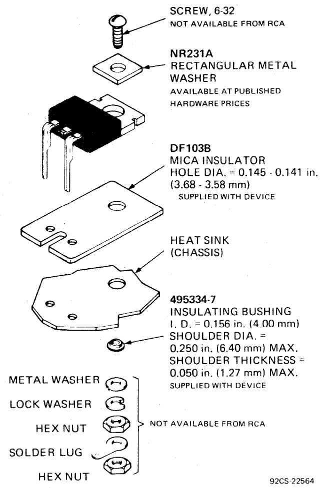
1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS FOR TYPES 2N5293, 2N5295, AND 2N5297

Lead No.1 - Base
Lead No.3 - Emitter
Mounting Flange - Collector
● - Do not use stub as tie point.

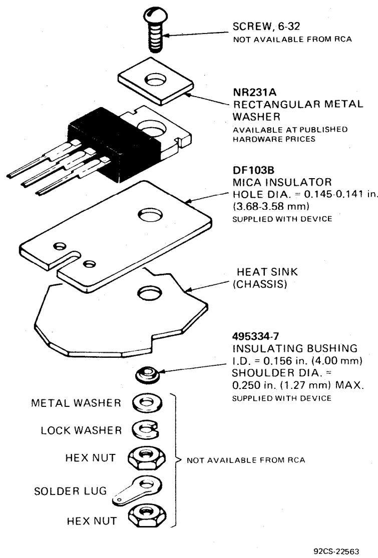
TERMINAL CONNECTIONS FOR TYPES 2N5294, 2N5296, AND 2N5298

Lead No.1 - Base
Lead No.2 - Collector
Lead No.3 - Emitter
Mounting Flange - Collector



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.27—Suggested mounting hardware for types 2N5293, 2N5295 & 2N5297.



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.28—Suggested mounting hardware for types 2N5294, 2N5296 & 2N5298.

VERSAWATT PACKAGE MOUNTING . . . .

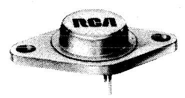
For complete discussion on handling and mounting of RCA molded-plastic power devices, refer to RCA application note, AN-4124.

RCA

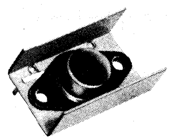
Solid State
Division

Power Transistors

2N3441 2N6263 2N6264
40373 40912 40913



JEDEC TO-66 H-1340



JEDEC TO-66
With Integral Heat Radiator H-1470A

Hometaxial II• Medium-Power Silicon N-P-N Transistors

Rugged Devices for Intermediate Power Applications in Industrial and Commercial Equipment

Features:

- 2N6264: premium type from 2N3441 family
- Maximum safe-area-of-operation curves for dc and pulse operation
- High voltage ratings
- Low saturation voltages
- Thermal-cycling rating curves

Applications:

- Series and shunt regulators
- High-fidelity amplifiers
- Power switching circuits
- Solenoid drivers

RCA 2N3441, 2N6263, and 2N6264 are hometaxial-base• silicon n-p-n transistors intended for a wide variety of medium- to-high power, high-voltage applications.

Types 40373, 40912, and 40913 are the 2N3441, 2N6263, and 2N6264 with factory-attached heat-radiators intended for printed-circuit-board applications.

• "Hometaxial" was coined by RCA from "homogenous" and "axial" to describe a single-diffused transistor with a base region of homogeneous-resistivity in the axial direction (emitter-to-collector).

"Hometaxial II" is a term used to describe RCA's expanded line of transistors produced by the hometaxial process.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N6263 40912	2N3441 40373	2N6264 40913	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	140	160	170	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:					
* With base open	$V_{CEO}(sus)$	120	140	150	V
With external base-to-emitter resistance (R_{BE}) = 100Ω	$V_{CER}(sus)$	130	150	160	V
With base reverse-biased (V_{BE} = -1.5 V)	$V_{CEV}(sus)$	140	160	170	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	7	7	7	V
*CONTINUOUS COLLECTOR CURRENT	I_C	3	3	3	A
PEAK COLLECTOR CURRENT		4	4	4	A
*CONTINUOUS BASE CURRENT	I_B	2	2	2	A
TRANSISTOR DISSIPATION:	P_T				
* At case temperature up to 25°C		20 (2N6263)	25 (2N3441)	50 (2N6264)	W
At ambient temperatures up to 25°C		5.8 (40912)	5.8 (40373)	5.8 (40913)	W
* At temperatures above 25°C		*See Figs. 4 & 7*	*See Figs. 4 & 8*	*See Figs. 1 & 7*	
*TEMPERATURE RANGE:					
Storage & Operating (Junction)			-65 to 200		°C
*PIN TEMPERATURE (During Soldering):					
At distances ≥ 1/32 in. (0.8 mm) from seating plane for 10 s max.			235		°C

*In accordance with JEDEC registration data format JS-6 RDF-2

11-73

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C, Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	DC Collector Voltage (V)	DC Emitter or Base Voltage (V)		DC Current (A)		LIMITS 2N6263 40912		2N3441 40373		2N6264 40913		UNITS
		V_{CE}	V_{EB}	V_{BE}	I_C	I_B	Min.	Max.	Min.	Max.	Min.	Max.	
Collector-Cutoff Current:													
		100				0	–	5	–	–	–	–	
* With base open	I_{CEO}	130				0	–	–	–	–	–	1	mA
		140				0	–	–	–	100	–	–	
Collector-Cutoff Current:													
		120		–1.5			–	2*	–	–	–	–	
	I_{CEX}	140		–1.5			–	–	–	5*	–	–	
		140		–1.5			–	–	–	1	–	–	
With base-emitter junction reversed biased		150		–1.5			–	–	–	–	–	0.05*	mA
		120		–1.5			–	10*	–	–	–	–	
	I_{CEX} (T_C = 150°C)	140		–1.5			–	–	–	6*	–	–	
		140		–1.5			–	–	–	5	–	–	
		150		–1.5			–	–	–	–	–	1*	
* Emitter-Cutoff Current	I_{EBO}		5				–	2	–	–	–	–	mA
			7				–	–	–	1	–	0.2	
Collector-to-Emitter Sustaining Voltage:[a]	V_{CEO}(sus)												
* With base open					0.1	0	120	–	140	–	150	–	
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}(sus)				0.1		130	–	150	–	160	–	V
With base-emitter junction reversed biased	V_{CEV}(sus)			–1.5	0.1		140	–	160	–	170	–	
		2			1		–	–	–	–	20	60	
* DC Forward-Current Transfer Ratio	h_{FE}	2			3		3	–	–	–	5	–	
		4			0.5		20	100	25	100	–	–	
		4			2.7		–	–	5	–	–	–	
					0.5	0.05	–	1.2*	–	1	–	–	
Collector-to-Emitter Saturating Voltage	V_{CE}(sat)				1	0.1	–	–	–	–	–	0.5*	V
					2.7	0.9	–	–	–	6*	–	–	
		2			1		–	–	–	–	–	1.5*	
Base-to-Emitter Voltage	V_{BE}	4			0.5		–	2*	–	1.7	–	–	V
		4			2.7		–	–	–	6*	–	–	
* Magnitude of Common-Emitter, Small-Signal, Short-Circuit Forward Current Transfer Ratio (f = 0.4 MHz)	$\|h_{fe}\|$	4			0.2		8	–	–	–	2	–	
		4			0.5		–	–	5	–	–	–	
Gain-Bandwidth Product	f_T	4			0.2		800	–	800	–	800	–	kHz
* Common-Emitter, Small-Signal, Short-Circuit Forward Current Transfer Ratio (f = 1 kHz)	h_{fe}	4			0.1		25	–	–	–	25	–	
		4			0.5		–	–	15	75	–	–	
Forward-Bias Second Breakdown Collector Current, Pulse Duration (non-repetitive) = 1 s	$I_{S/b}$	120					0.167	–	–	–	–	–	
		120					–	–	–	–	0.417	–	A
		120					–	–	0.21	–	–	–	
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$						8.75 (max.) 2N6263		7 (max.) 2N3441		3.5 (max.) 2N6264		°C/W
Junction-to-Free Air	$R_{\theta JA}$						30 (max.) 40912		30 (max.) 40373		30 (max.) 40913		

*In accordance with JEDEC registration data format (JS-6 RDF-2).

[a]**CAUTION:** The sustaining voltage V_{CEO}(sus), V_{CER}(sus), and V_{CEV}(sus) MUST NOT be measured on a curve tracer. These sustaining voltages should be measured by means of the test circuit shown in Fig. 11.

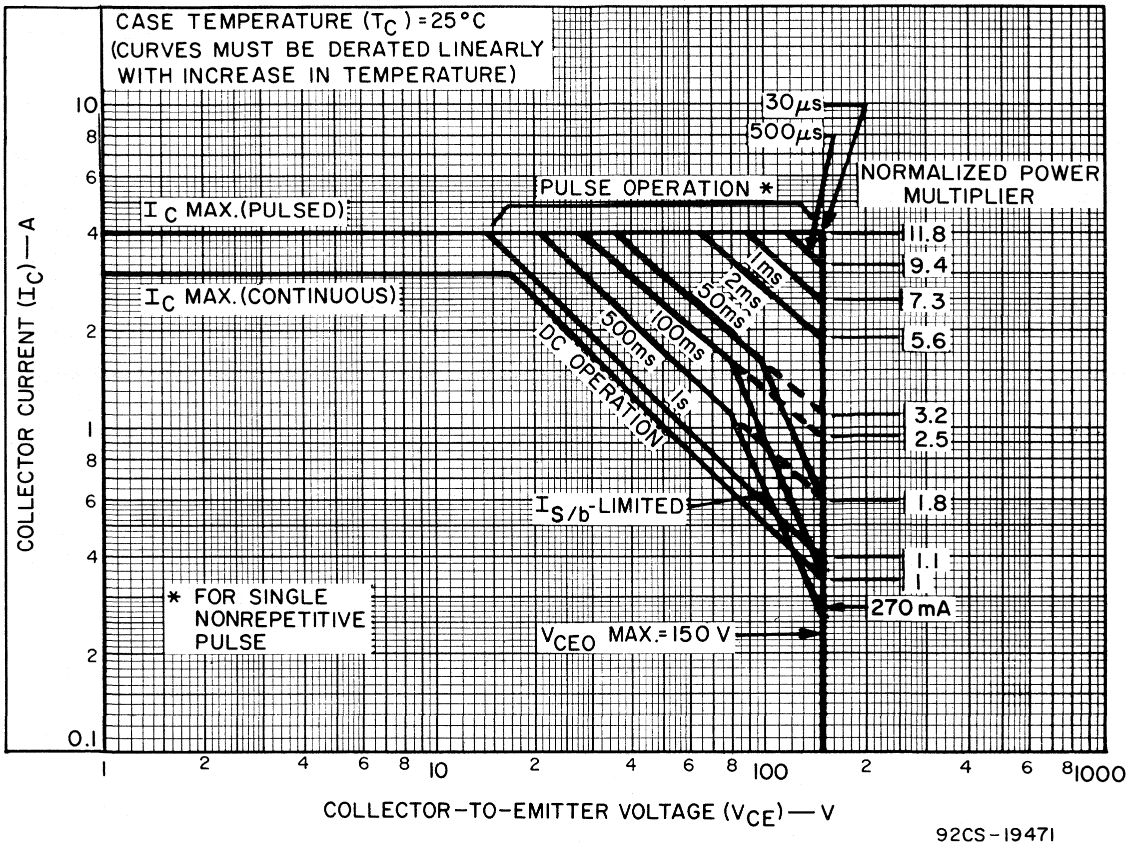


Fig.1 — Maximum operating areas for type 2N6264.

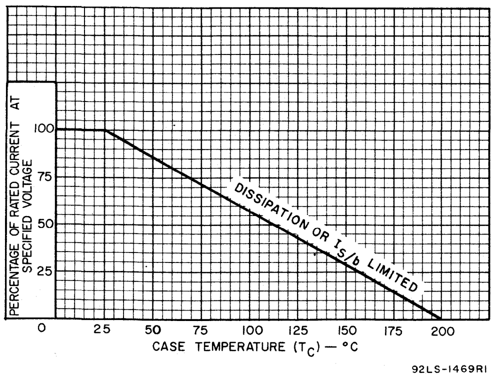


Fig.2 — Current derating curve for all types.

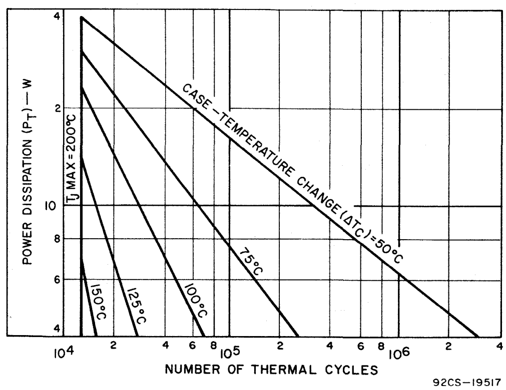


Fig.3 — Thermal-cycle rating chart for type 2N6264.

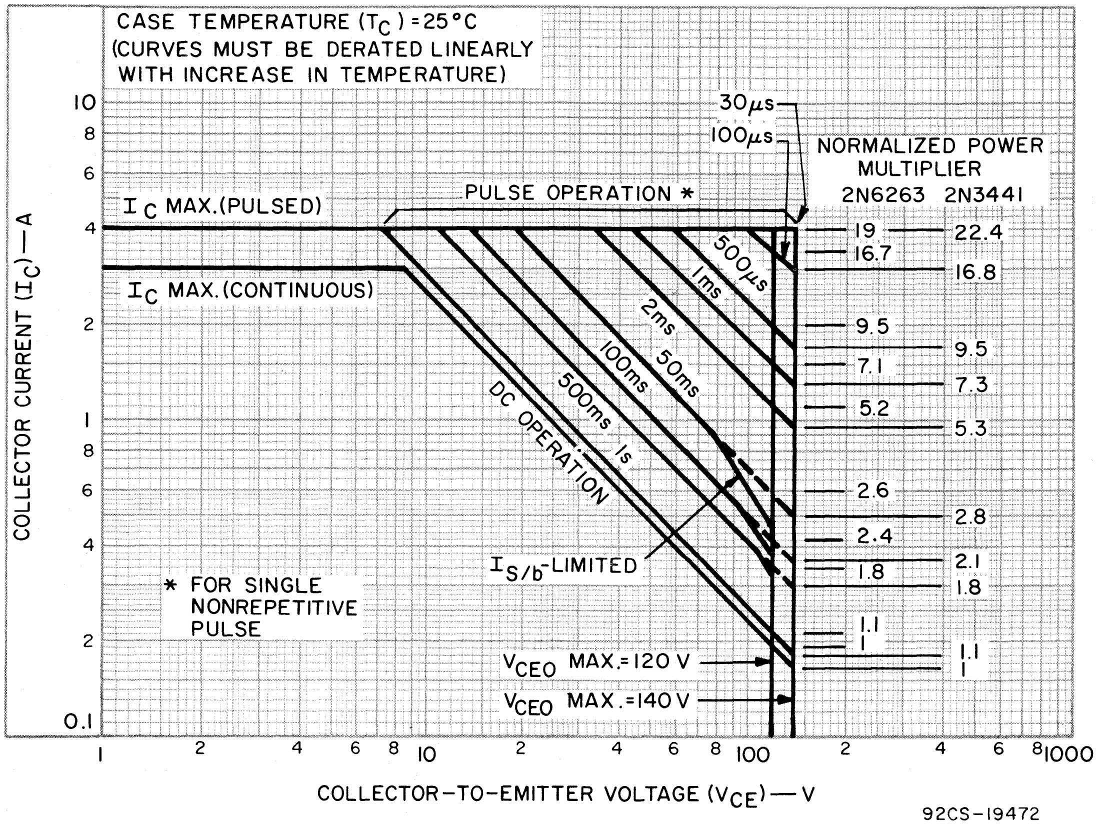


Fig.4—Maximum operating areas for type 2N6263 and 2N3441.

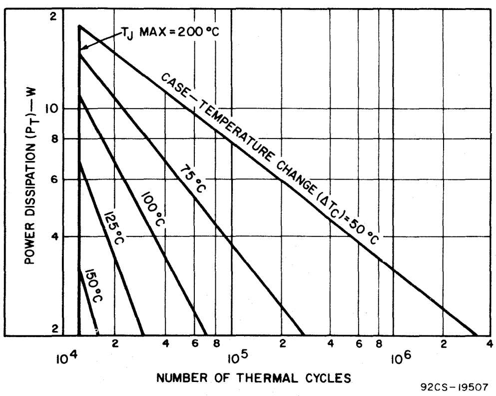


Fig.5—Thermal-cycle rating chart for type 2N3441.

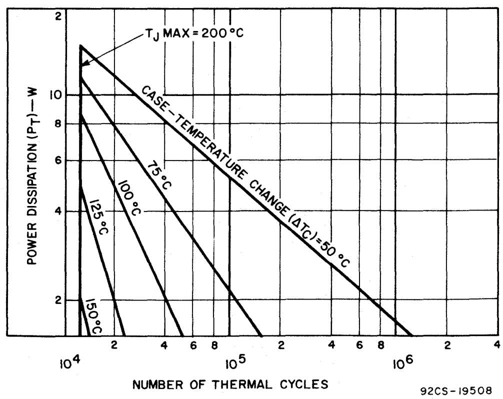


Fig.6—Thermal-cycle rating chart for type 2N6263.

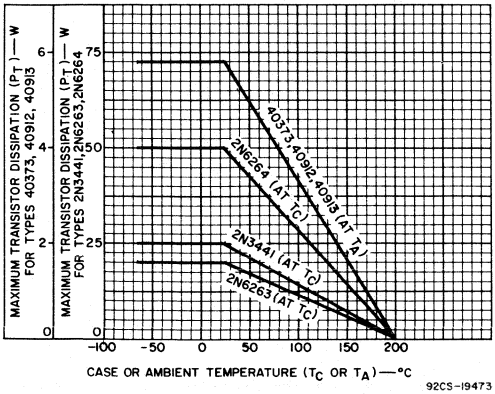


Fig.7—Dissipation derating curves for all types.

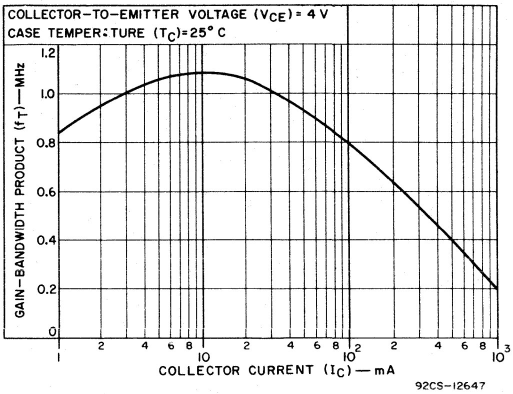


Fig.8—Typical gain-bandwidth product for all types.

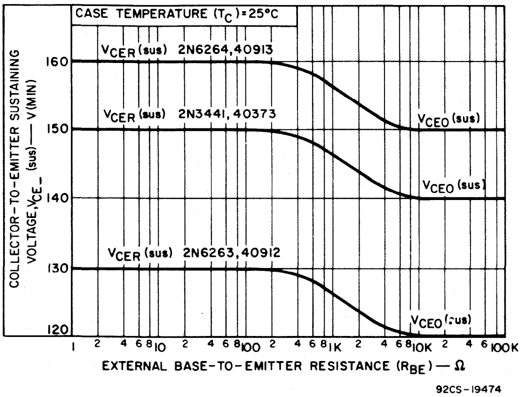


Fig.9—Sustaining voltage vs. base-to-emitter resistance for all types.

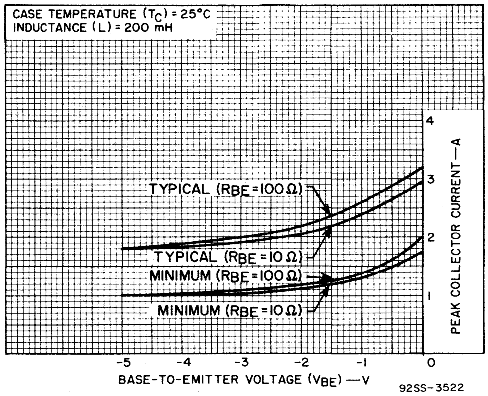


Fig.10—Reverse-bias second-breakdown characteristics for all types.

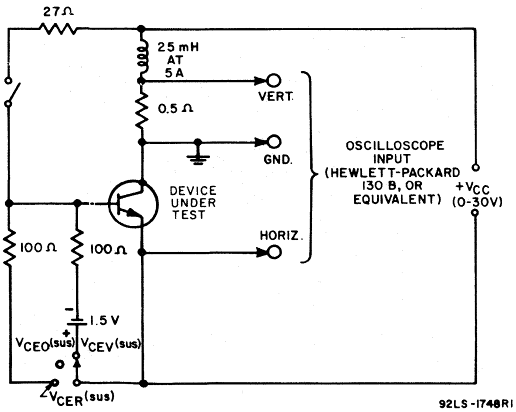
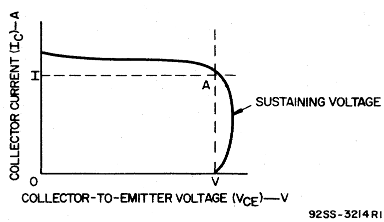


Fig.11—Circuit used to measure sustaining voltages, V_{CEO}(sus), V_{CER}(sus), and V_{CEV}(sus) for all types.



Note: The sustaining voltage, V_{CEO}(sus), V_{CER}(sus), or or V_{CEV}(sus) is acceptable when the trace falls to the right and above point "A" for all types. (For values of current and voltage, see *Electrical Characteristics)*

Fig.12—Oscilloscope display for measurement of sustaining voltages (test circuit shown in Fig. 11).

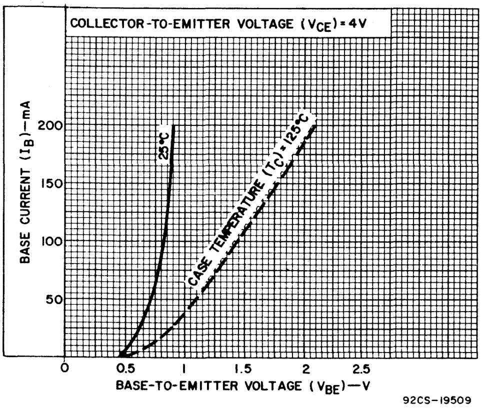


Fig.13—Typical input characteristics for types 2N6264 and 40913.

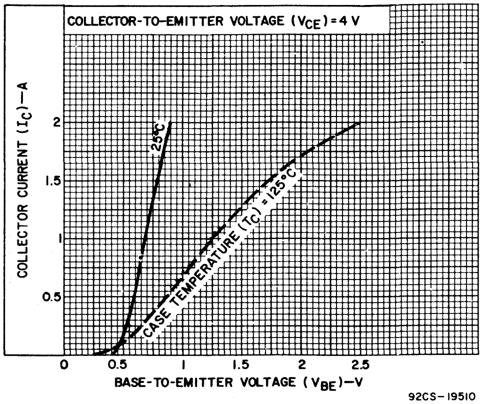


Fig.14—Typical transfer characteristics for types 2N6264 and 40913.

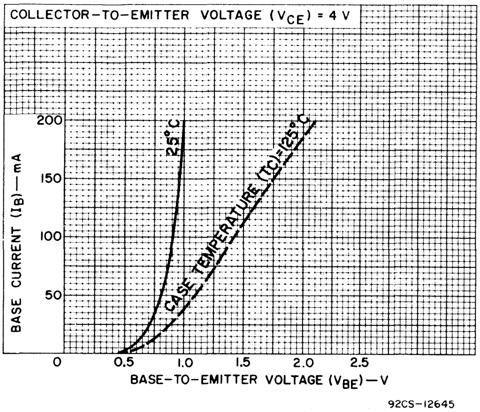


Fig.15—Typical input characteristics for types 2N3441 and 40373.

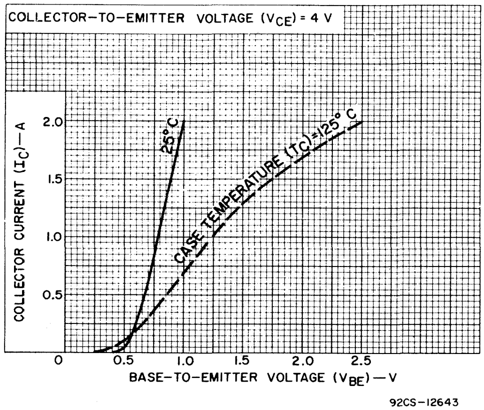


Fig.16—Typical transfer characteristics for types 2N3441 and 40373.

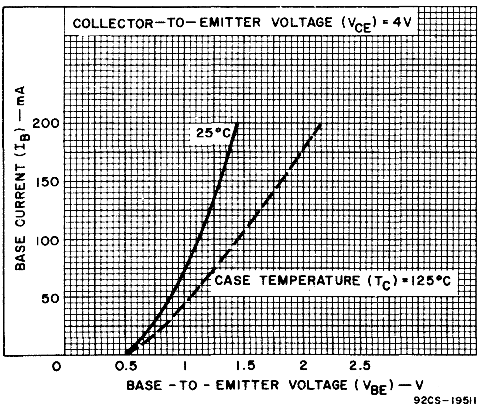


Fig.17—Typical input characteristics for types 2N6263 and 40912.

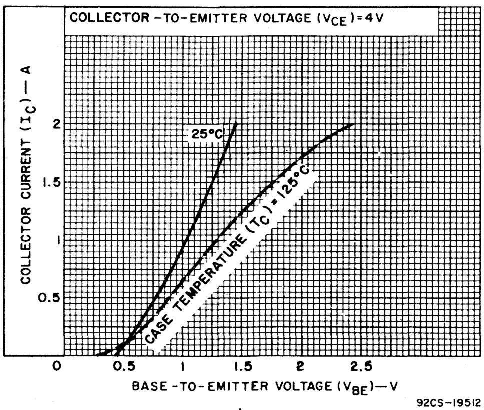


Fig.18—Typical transfer characteristics for types 2N6263 and 40912.

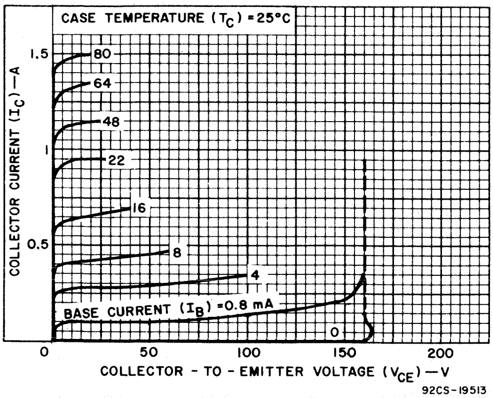


Fig. 19—Typical output characteristics for types 2N6264 and 40913.

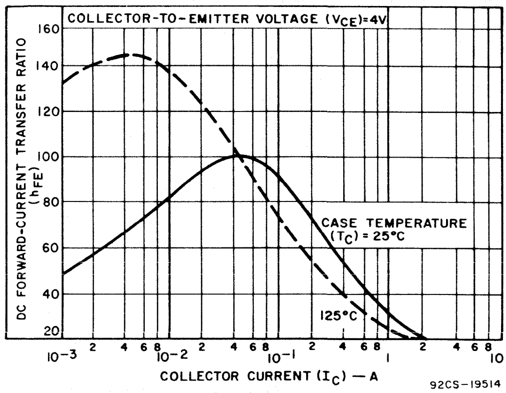


Fig. 20—Typical dc-beta characteristics for types 2N6264 and 40913.

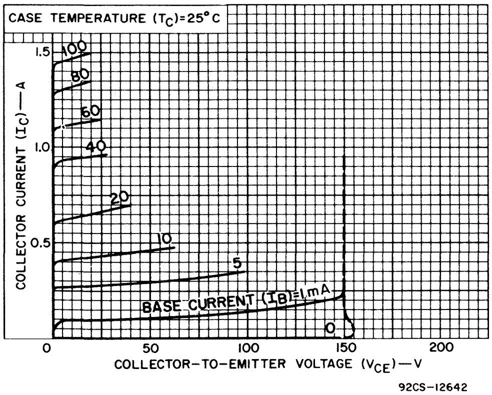


Fig. 21—Typical output characteristics for types 2N3441 and 40373.

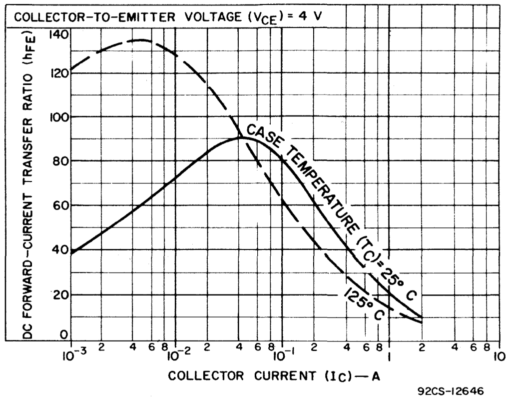


Fig. 22—Typical dc-beta characteristics for types 2N3441 and 40373.

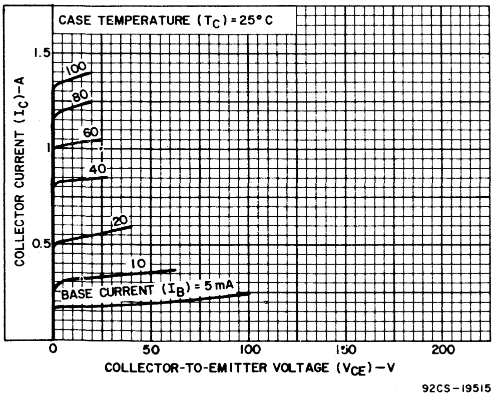


Fig. 23—Typical output characteristics for types 2N6263 and 40912.

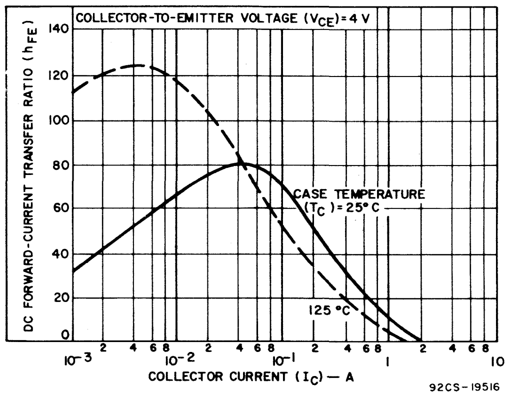
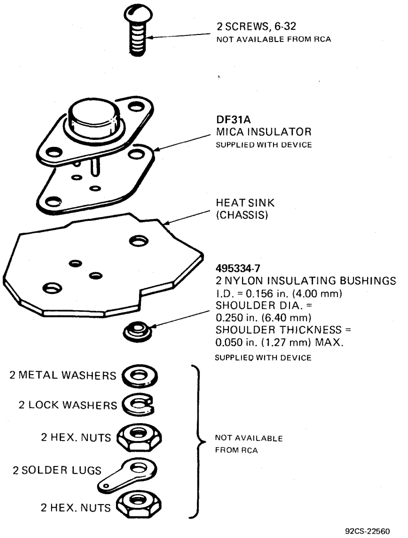


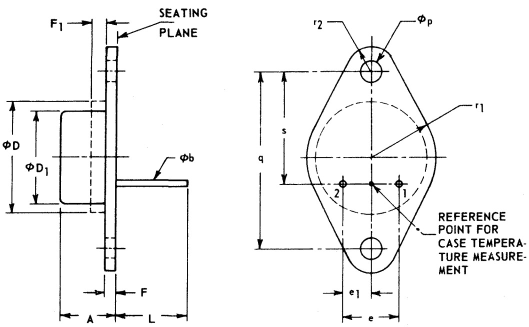
Fig. 24—Typical dc-beta characteristics for types 2N6263 and 40912.



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.25 — Suggested hardware for 2N3441, 2N6263, and 2N6264.

DIMENSIONAL OUTLINE FOR 2N3441, 2N6263, and 2N6264 JEDEC TO-66



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	0.250	0.340	6.35	8.64	
φb	0.028	0.034	0.711	0.863	
φD	—	0.620	—	15.75	
φD1	0.470	0.500	11.94	12.70	
e	0.190	0.210	4.83	5.33	
e1	0.093	0.107	2.36	2.72	
F	0.050	0.075	1.27	1.91	2
F1	—	0.050	—	1.27	1
L	0.360	—	9.14	—	
φp	0.142	0.152	3.61	3.86	
q	0.958	0.962	24.33	24.43	
r1	—	0.350	—	8.89	
r2	—	0.145	—	3.68	
s	0.570	0.590	14.48	14.99	

NOTES:

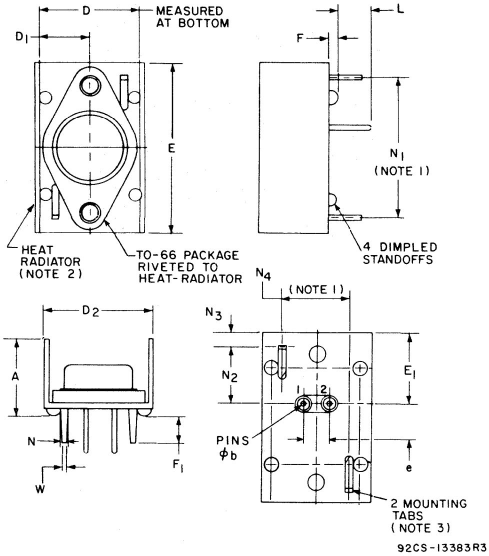
1. The outline contour is optional within zone defined by φD and F1.
2. Dimensions does not include seating flanges.

92SS-3738

TERMINAL CONNECTIONS FOR 2N3441, 2N6263, & 2N6264

Pin 1 - Base
Pin 2 - Emitter
Case, Mounting Flange - Collector

DIMENSIONAL OUTLINE FOR JEDEC TO-66 WITH HEAT RADIATOR



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A		0.595		15.11	
φb	0.028	0.034	0.711	0.864	
D	0.750	0.760	19.05	19.30	
D1	0.375	0.380	9.52	9.65	
D2	0.820	0.920	20.83	23.37	
E	1.297	1.327	32.94	33.70	
E1	0.551	0.561	13.99	14.25	
e	0.190	0.210	4.83	5.33	
F	0.040	0.055	1.02	1.40	
F1	0.175	0.210	4.44	5.33	
L	0.270		0.686		
N	0.052	0.065	1.32	1.65	
N1	1.098	1.102	27.89	27.99	1
N2	0.448	0.452	11.38	11.47	
N3	0.099	0.113	0.25	0.29	
N4	0.498	0.502	12.65	12.75	
W	0.048	0.060	1.22	1.52	

NOTES:

1. Measured at bottom of heat radiator.
2. 0.035 in. (0.889) C.R.S., tin plated.
3. Recommended hole size for printed-circuit board is 0.070 in. (1.778) dia.

TERMINAL CONNECTIONS FOR 40373, 40912, & 40913

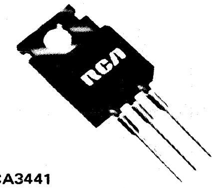
Pin 1 - Base
Pin 2 - Emitter
Heat-Radiator - Collector

RCA

Solid State Division

Power Transistors

RCA3441 RCA6263



RCA3441
RCA6263

JEDEC TO-220AB H-1535R1

Hometaxial-Base Silicon N-P-N VERSAWATT Transistors

Designed for Medium-Power Linear and Switching Service in Consumer, Automotive, and Industrial Applications

Features:

- Maximum safe-area-of-operation curves
- Low saturation voltages
- High dissipation ratings
- Thermal-cycling rating curves

Applications:

- Series and shunt regulators
- High-fidelity amplifiers
- Power-switching circuits
- Solenoid drivers

RCA3441 and RCA6263 are silicon n-p-n transistors intended for a wide variety of high-current applications. The hometaxial-base construction of these devices renders them highly resistant to second breakdown over a wide range of operating conditions.

The VERSAWATT case has a proven thermal-cycling capability. This capability is assured by real-time quality controls in our manufacturing locations. The RCA3441 and RCA6263 are supplied in the JEDEC TO-220AB straight-lead version of the package. They are also available on special order in a variety of lead-form configurations. Two popular variations have leads formed to fit TO-66 sockets (specify formed lead No. 6201) or printed-circuit boards (specify formed lead No. 6207). Detailed information on these and other VERSAWATT outlines is contained in "RCA's Lineup of Power Transistors" (PSP-704).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		RCA6263	RCA3441	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	140	160	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:				
With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$	130	150	V
With base open	$V_{CEO}(sus)$	120	140	V
With base reverse-biased V_{BE} = −1.5 V	$V_{CEV}(sus)$	140	160	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	7	7	V
CONTINUOUS COLLECTOR CURRENT	I_C	3	3	A
PEAK COLLECTOR CURRENT		4	4	A
CONTINUOUS BASE CURRENT	I_B	2	2	A
TRANSISTOR DISSIPATION:	P_T			
At case temperatures up to 25°C		36	36	W
At case temperatures above 25°C		See Fig. 4		
TEMPERATURE RANGE:				
Storage and Operating (Junction)		−65 to +150		°C
PIN TEMPERATURE (During Soldering):				
At distances ≥ 1/32 in. (0.8 mm) from seating plane for 10 s max.		235		°C

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ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS				UNITS
		VOLTAGE V dc			CURRENT A dc		RCA6263		RCA3441		
		V_{CE}	V_{EB}	V_{BE}	I_C	I_B	MIN.	MAX.	MIN.	MAX.	
Collector-Cutoff Current: With base open	I_{CEO}	100 120				0 0	– –	5 –	– –	– 5	mA
With base-emitter junction reverse-biased	I_{CEX}	120 140		–1.5 –1.5			– –	5 –	– –	– 5	mA
At T_C = 150°C	I_{CEX}	120 140		–1.5 –1.5			– –	10 –	– –	– 10	mA
Emitter-Cutoff Current	I_{EBO}		5		0		–	2	–	2	mA
Collector-to-Emitter Sustaining Voltage: With base open	V_{CEO}(sus)				0.1^a	0	120	–	140	–	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}(sus)				0.1^a		130	–	150	–	V
With base-emitter junction reverse-biased	V_{CEV}(sus)			–1.5	0.1^a		140	–	160	–	V
DC Forward-Current Transfer Ratio	h_{FE}	4			0.5^a		20	150	20	150	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)				0.5^a	0.05^a	–	1.2	–	1.2	V
Base-to-Emitter Voltage	V_{BE}	4			0.5^a		–	2	–	2	V
Gain-Bandwidth Product	f_T	4			0.2		200	–	200	–	kHz
Common-Emitter, Small-Signal, Short-Circuit Forward-Current Transfer Ratio (f = 1 kHz)	h_{fe}	4			0.1		25	–	25	–	
Forward-Bias Second Breakdown Collector Current[b] (t ≥ 1 s)	$I_{S/b}$	120					0.3	–	0.3	–	A
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$						–	3.5	–	3.5	°C/W
Junction-to-Ambient	$R_{\theta JA}$						–	70	–	70	°C/W

[a]Pulsed: Pulse duration = 300 μs, duty factor = 1.8%.

[b]Pulsed: 1-second non-repetitive pulse.

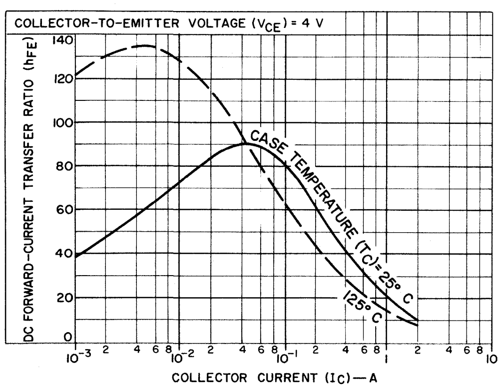


Fig. 1— Typical dc beta characteristics for RCA3441.

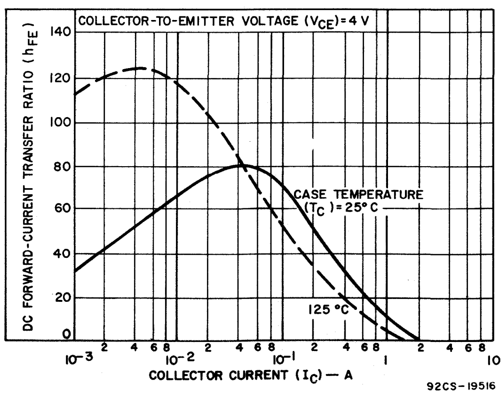


Fig. 2— Typical dc beta characteristics for RCA6263.

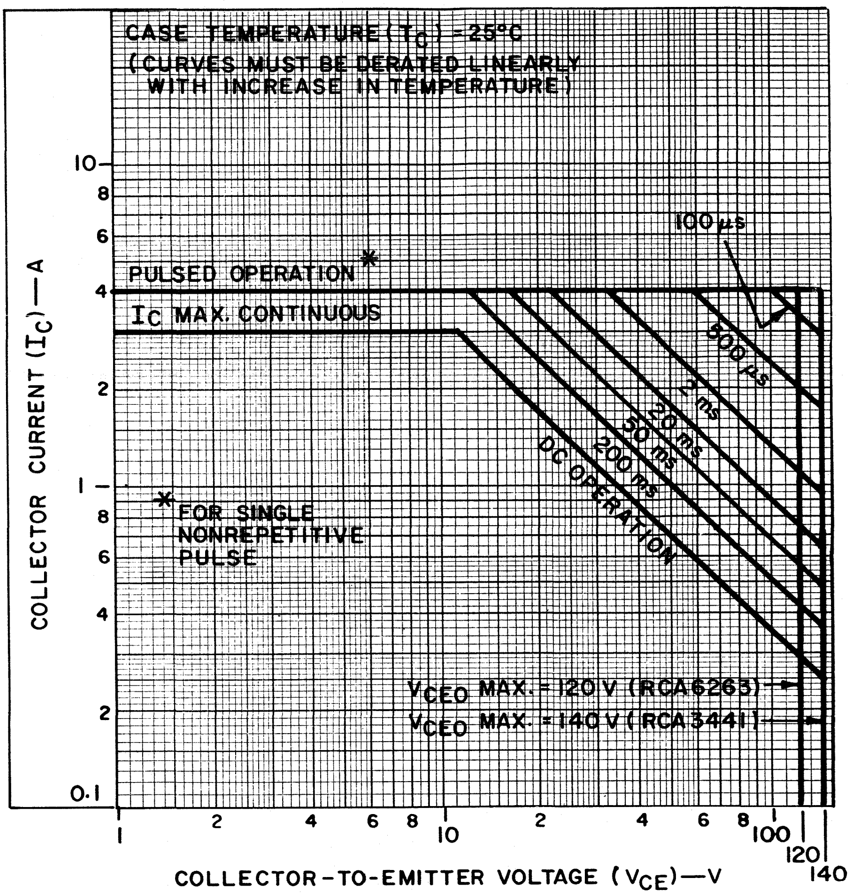


Fig. 3— Maximum operating areas for both types.

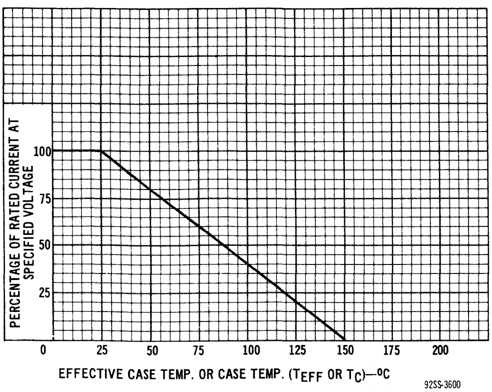


Fig. 4— Current derating curve for both types.

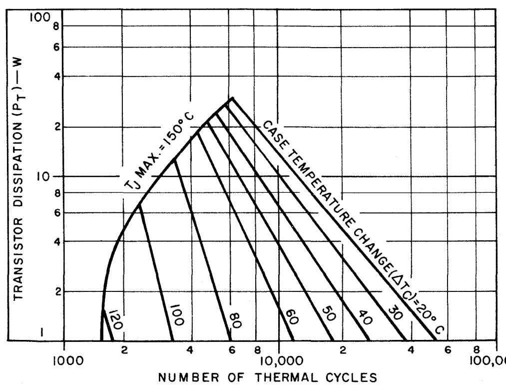


Fig. 5— Thermal-cycling rating chart for both types.

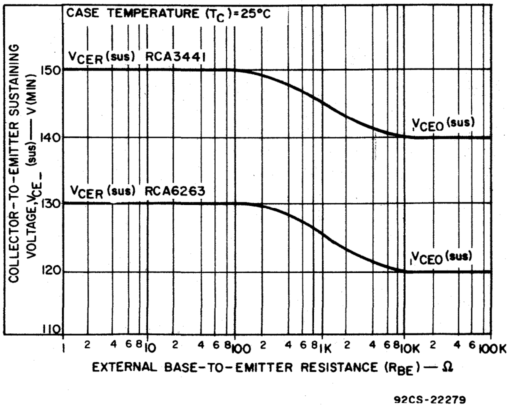


Fig. 6– Sustaining voltage vs. base-to-emitter resistance for both types.

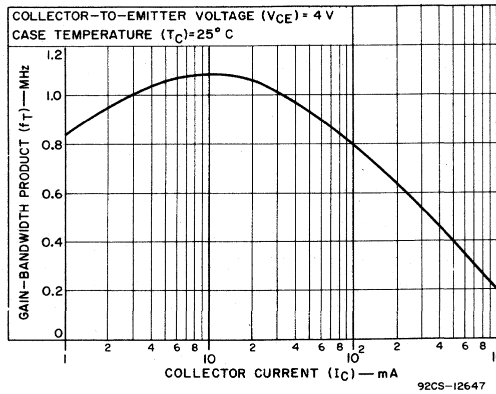


Fig. 7– Typical gain-bandwidth product for both types.

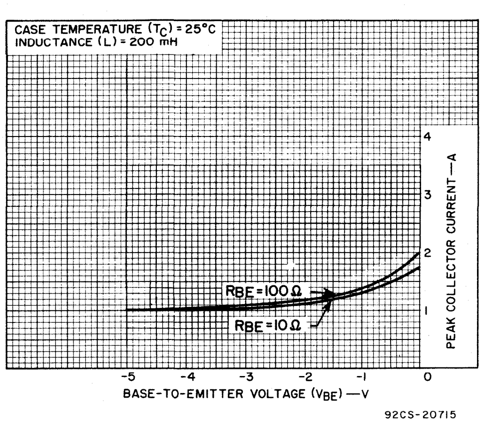


Fig. 8– Minimum reverse-bias second-breakdown characteristics for both types.

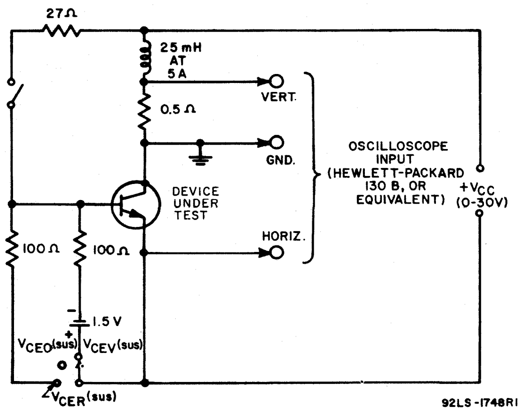
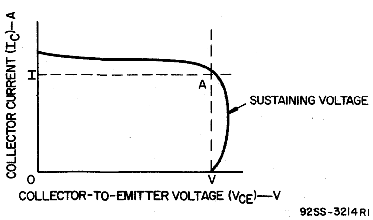


Fig. 9– Circuit used to measure sustaining voltages, $V_{CEO}(sus)$, $V_{CER}(sus)$, and $V_{CEV}(sus)$ for both types.



NOTE:
THE SUSTAINING VOLTAGE V_{CEO}(sus) OR V_{CEV}(sus) IS ACCEPTABLE WHEN THE TRACE FALLS TO THE RIGHT AND ABOVE POINT "A" FOR TYPES 2N4347 AND 2N3442.
(FOR VALUES OF I & V, SEE ELECTRICAL CHARACTERISTICS)

Fig. 10– Oscilloscope display for measurement of sustaining voltages (test circuit shown in Fig. 9).

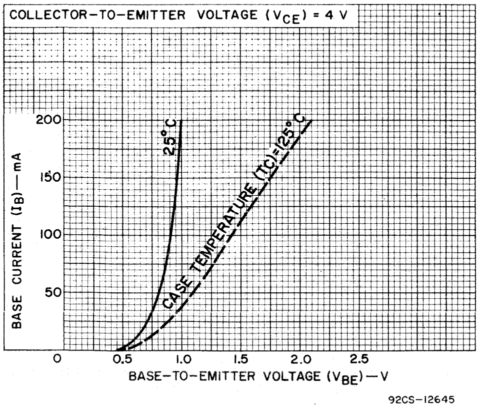


Fig. 11— Typical input characteristics for RCA3441.

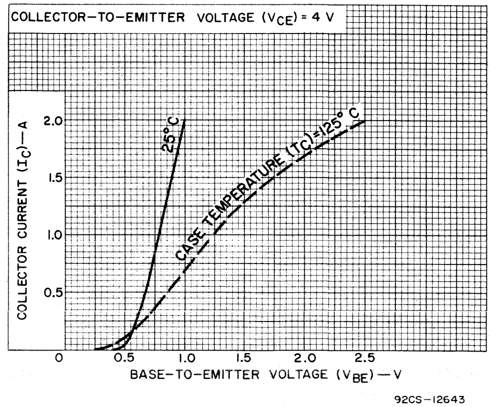


Fig. 12— Typical transfer characteristics for RCA3441.

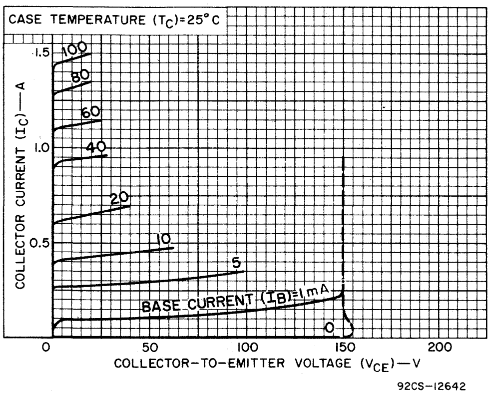


Fig. 13— Typical output characteristics for RCA3441.

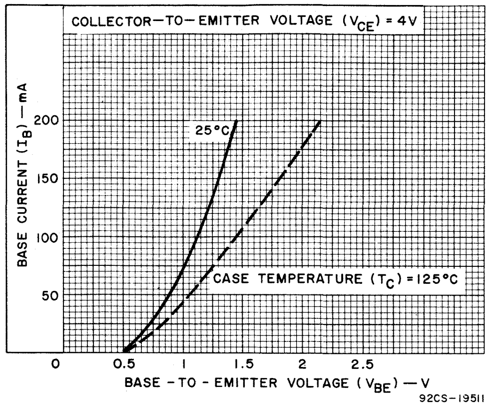


Fig. 14— Typical input characteristics for RCA6263.

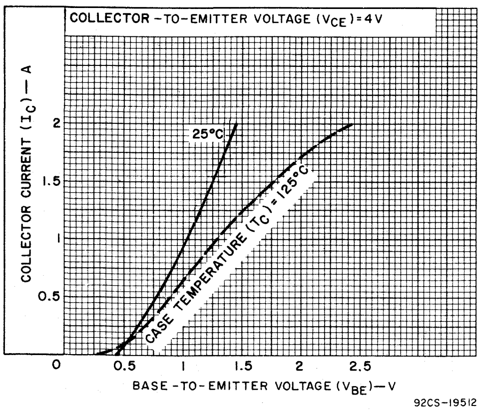


Fig. 15— Typical transfer characteristics for RCA6263.

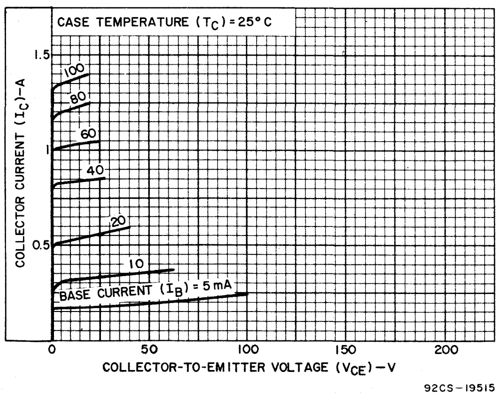
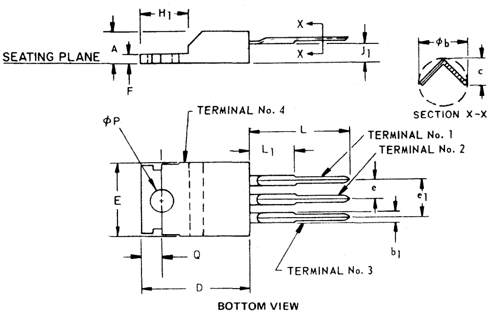


Fig. 16— Typical output characteristics for RCA6263.

DIMENSIONAL OUTLINE
JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
ϕb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
ϕP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 (6.35 – 6.48 mm) from case.

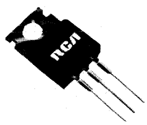
TERMINAL CONNECTIONS
JEDEC TO-220AB

Terminal No. 1 – Base
Terminal No. 2 – Collector
Terminal No. 3 – Emitter
Terminal No. 4 – Collector

RCA
Solid State
Division

Power Transistors

2N6477
2N6478



JEDEC TO-220AB H-1535R1

Hometaxial-Base, Medium-Power Silicon N-P-N Transistors

Rugged Devices for Intermediate Power Applications in Industrial and Commercial Equipment

Features:

- **Maximum safe-area-of-operation curves for dc and pulse operation**
- **High voltage ratings**
- **Low saturation voltages**
- **Thermal-cycling rating curves**

Applications:

- **Series and shunt regulators**
- **High-fidelity amplifiers**
- **Power switching circuits**
- **Solenoid drivers**
- **Vertical output stages in color and B/W TV**

RCA 2N6477 and 2N6478▲ are hometaxial-base silicon n-p-n transistors intended for a wide variety of medium-to-high power, high-voltage applications. These devices, which are voltage extensions of the 2N5298 family, are especially useful in vertical output stages in color and black-and-white TV. The units differ in voltage ratings and in the currents at which parameters are controlled.

The 2N6477 and 2N6478 are supplied in the JEDEC TO-220AB straight-lead version of the package. They are also available on special order in a variety of lead-form configurations. Two popular variations have leads formed to fit TO-66 sockets (specify formed lead No. 6201) or printed-circuit boards (specify formed lead No. 6207). Detailed information on these and other VERSAWATT outlines is contained in "RCA's Line-up of Power Transistors" (PSP-704).

▲ Formerly RCA Dev. Nos. TA8405 and TA8343.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N6477	2N6478	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	140	160	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:				
With base open	$V_{CEO}(sus)$	120	140	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$	130	150	V
* With base reverse-biased (V_{BE} = −1.5 V)	$V_{CEV}(sus)$	140	160	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	5	V
*CONTINUOUS COLLECTOR CURRENT	I_C	2.5	2.5	A
PEAK COLLECTOR CURRENT		4	4	A
*CONTINUOUS BASE CURRENT	I_B	1	1	A
TRANSISTOR DISSIPATION:	P_T			
* At case temperature up to 25°C		50	50	W
* At case temperatures above 25°C		See Fig. 2		
At ambient temperatures up to 25°C		1.8	1.8	W
At ambient temperatures above 25°C		Derate linearly at 0.0144		W/°C
*TEMPERATURE RANGE:				
Storage and Operating (Junction)		−65 to 150		°C
*PIN TEMPERATURE (During Soldering):				
At distances ⩾ 1/32 in. (0.8 mm) from seating plane for 10 s max.		235		°C

*In accordance with JEDEC registration data format JS-6 RDF-2.

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ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS				UNITS
		VOLTAGE V dc			CURRENT A dc		2N6477		2N6478		
		V_{CE}	V_{EB}	V_{BE}	I_C	I_B	MIN.	MAX.	MIN.	MAX.	
* Collector-Cutoff Current: With base open	I_{CEO}	80				0	–	2	–	–	mA
		100				0	–	–	–	2	
With base-emitter junction reverse-biased	I_{CEV}	130		−1.5			–	2	–	–	
		150		−1.5			–	–	–	2	
At T_C = 150°C	I_{CEV}	120		−1.5			–	10	–	–	
		140		−1.5			–	–	–	10	
* Emitter-Cutoff Current	I_{EBO}		5		0		–	2	–	2	mA
* Collector-to-Emitter Sustaining Voltage: With base open	$V_{CEO}(sus)$				0.1[a]	0	120	–	140	–	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$				0.1[a]		130	–	150	–	
With base-emitter junction reverse-biased	$V_{CEV}(sus)$			−1.5	0.1[a]		140	–	160	–	
* DC Forward-Current Transfer Ratio	h_{FE}	4			1[a]		25	150	25	150	
		4			2.5[a]		5	–	5	–	
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				1[a]	0.1	–	1	–	1	V
					2.5[a]	0.5	–	2	–	2	
* Base-to-Emitter Voltage	V_{BE}	4			1[a]		–	1.8	–	1.8	V
		4			2.5[a]		–	3	–	3	
* Magnitude of Common-Emitter, Small-Signal, Short-Circuit Forward-Current Transfer Ratio (f = 40 kHz)	$\|h_{fe}\|$	4			0.5		5	–	5	–	
Gain-Bandwidth Product	f_T	4			0.5		200	–	200	–	kHz
* Common-Emitter, Small-Signal, Short-Circuit Forward-Current Transfer Ratio (f = 1 kHz)	h_{fe}	4			0.1		25	–	25	–	
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$						–	2.5	–	2.5	°C/W
Junction-to-Ambient	$R_{\theta JC}$						–	70	–	70	

* In accordance with JEDEC registration data format (JS-6 RDF-2).

[a] Pulsed: Pulse duration = 300 μs, duty factor = 1.8%.

CAUTION: The sustaining voltage $V_{CEO}(sus)$, $V_{CER}(sus)$, and $V_{CEV}(sus)$ MUST NOT be measured on a curve tracer. These sustaining voltages should be measured by means of the test circuit shown in Fig. 10.

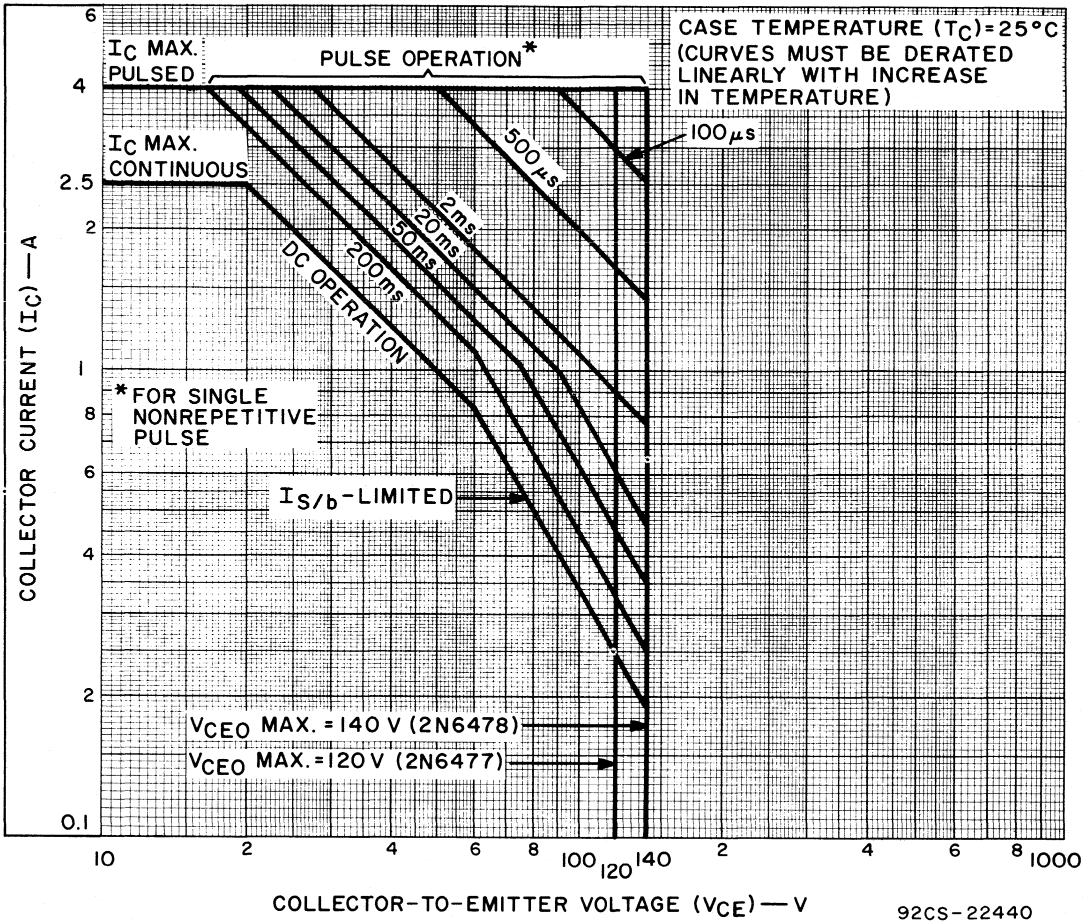


Fig.1 — Maximum operating areas for both types.

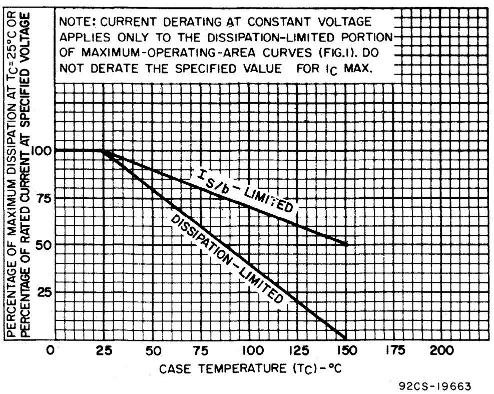


Fig.2 — Current derating curve for both types.

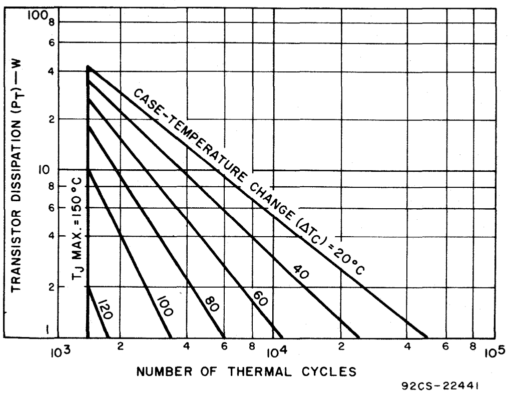


Fig.3 — Thermal-cycling rating chart for both types.

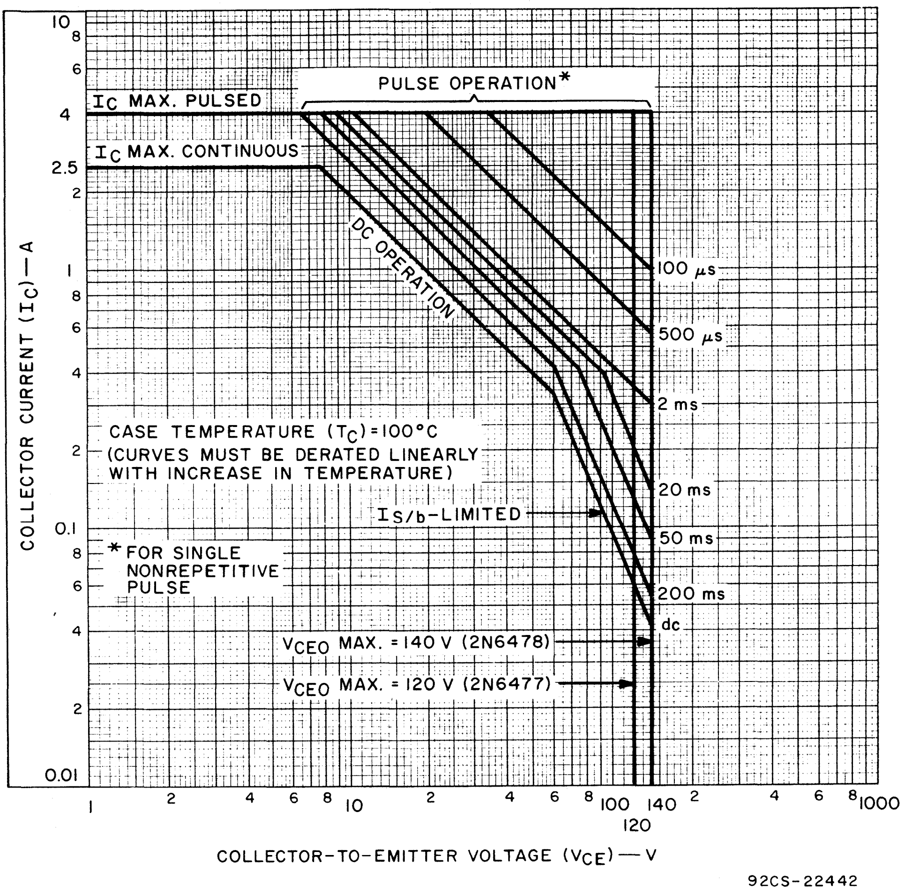


Fig.4 – Maximum operating areas for both types.

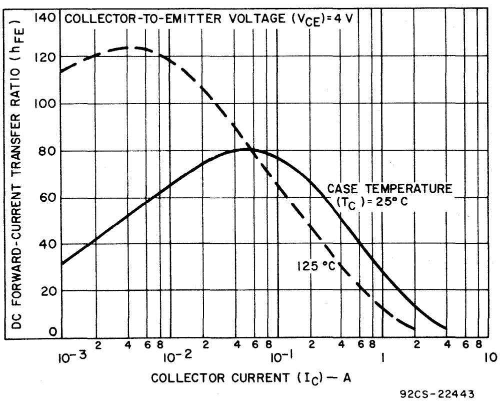


Fig.5 – Typical dc beta characteristics for 2N6477.

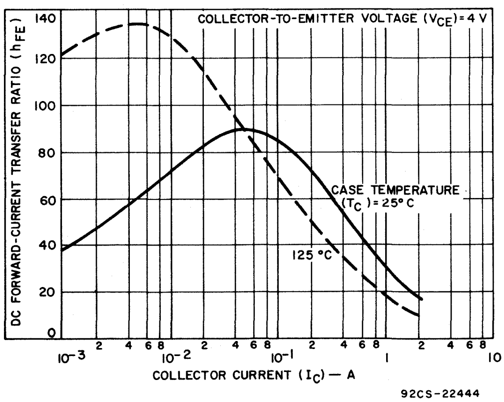


Fig.6 – Typical dc beta characteritics for 2N6478.

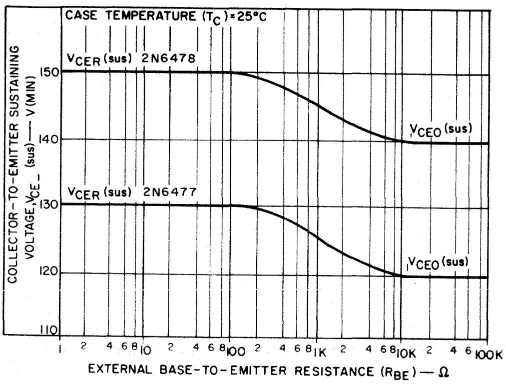


Fig.7 – Sustaining voltage vs. base-to-emitter resistance for both types.

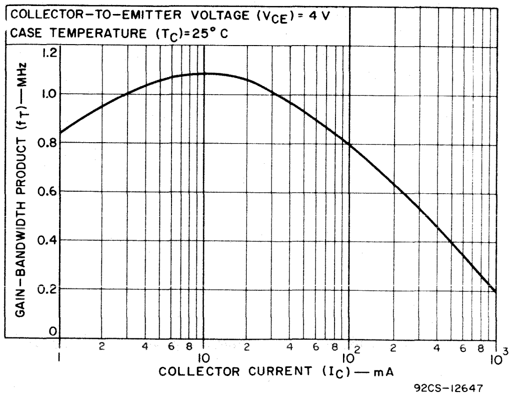


Fig.8 – Typical gain-bandwidth product for both types.

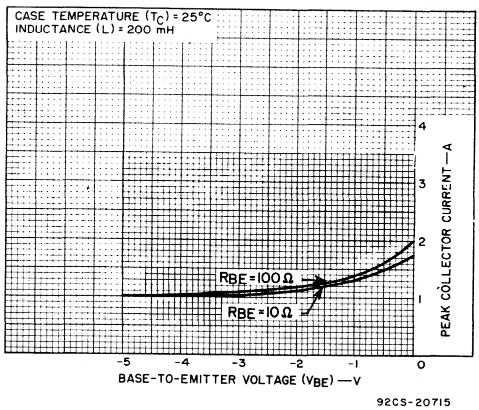


Fig.9 – Minimum reverse-bias second-breakdown characteristics for both types.

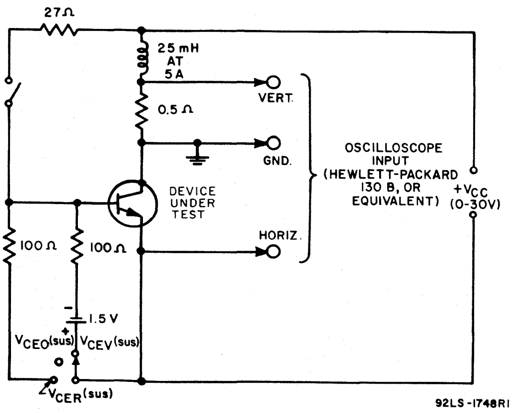
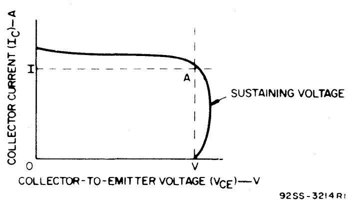


Fig.10 – Circuit used to measure sustaining voltages, V_{CEO}(sus), V_{CER}(sus), and V_{CEV}(sus) for both types.



Note:
The sustaining voltage, V_{CEO}(sus), V_{CER}(sus), or V_{CEV}(sus) is acceptable when the trace falls to the right and above point "A" for all types. (For values of current and voltage, see *Electrical Characteristics*)

Fig.11 – Oscilloscope display for measurement of sustaining voltages (test circuit shown in Fig. 10).

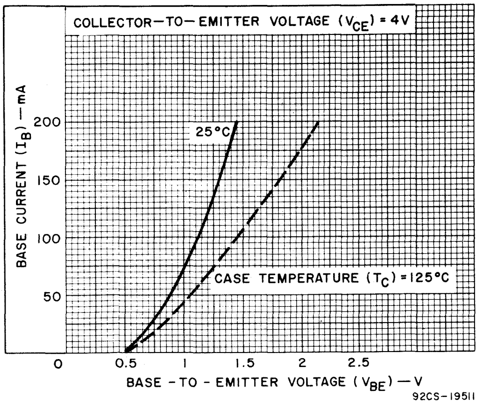


Fig. 12 — Typical input characteristics for 2N6477.

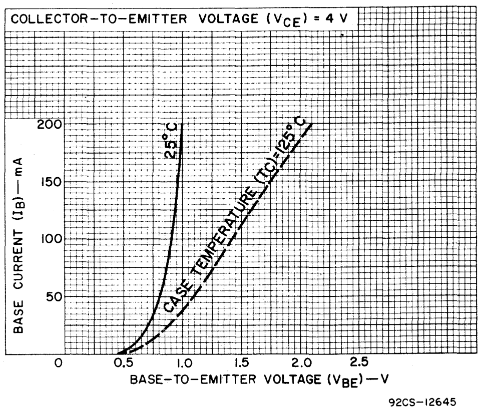


Fig. 13 — Typical input characteristics for 2N6478.

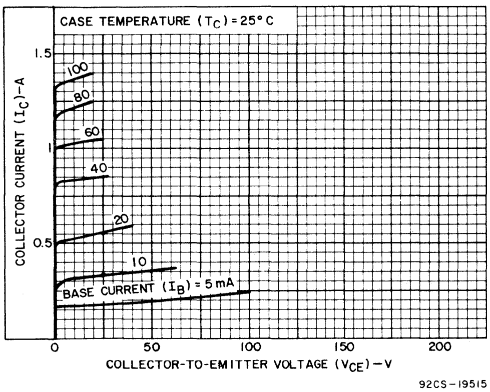


Fig. 14 — Typical output characteristics for 2N6477.

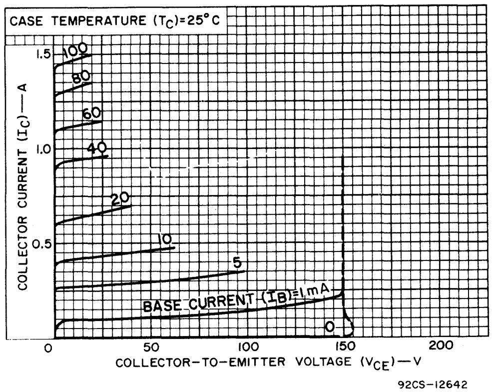


Fig. 15 — Typical output characteristics for 2N6478.

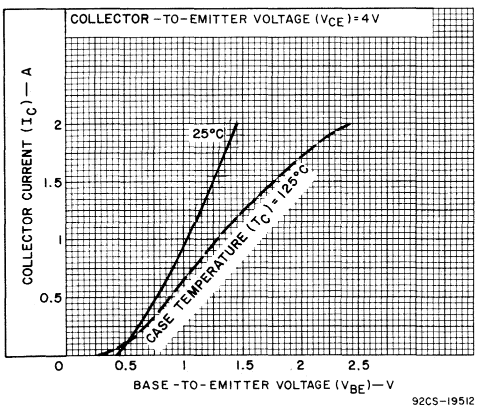


Fig. 16 — Typical transfer characteristics for 2N6477.

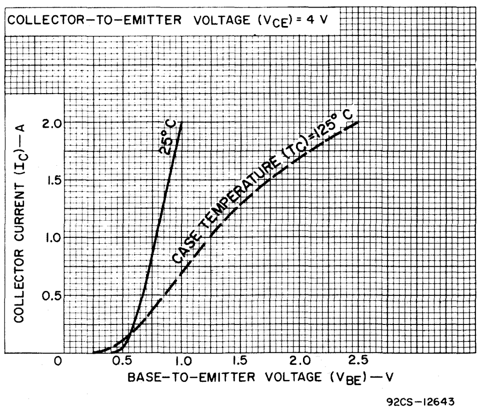
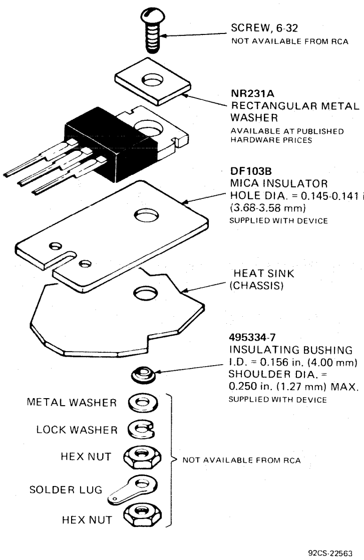


Fig. 17 — Typical transfer characteristics for 2N6478.



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.18 – Suggested mounting hardware for JEDEC TO-220AB.

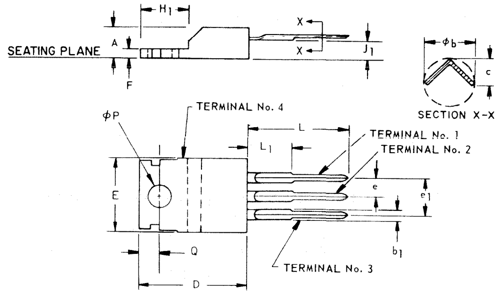
VERSAWATT PACKAGE MOUNTING . . . . .

For complete discussion on handling and mounting of RCA molded-plastic power devices, refer to RCA application note AN-4124.

Please submit requirements for optional lead configurations to your RCA Technical Sales Representative, or write to
RCA Solid State Division,
Power Transistor Marketing,
Somerville, N. J. 08876

For basic transistor theory, circuits, and application information, refer to "RCA Solid-State Power Circuits Designer's Handbook", SP-52, or "RCA Transistor, Thyristor, & Diode Manual", SC-15.

DIMENSIONAL OUTLINE
JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
ϕb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	.0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
ϕP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

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NOTES:
1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 IN. (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS
JEDEC TO-220AB

Terminal No.1 – Base
Terminal No. 2 – Collector
Terminal No. 3 – Emitter
Terminal No. 4 – Collector

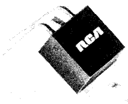
Solid State
Division

Power Transistors

2N5490 2N5492 2N5495
2N5491 2N5493 2N5496
2N5494 2N5497

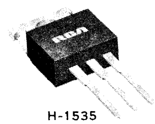
SILICON N-P-N POWER TRANSISTORS

General-Purpose Types For Medium-Power Switching and Amplifier Applications in Military, Industrial, and Commercial Equipment



H-1534

2N5491, 2N5493, 2N5495, 2N5497
For TO-66 Sockets



H-1535

2N5490, 2N5492, 2N5494, 2N5496
For Printed-Circuit Boards

RCA-2N5490, 2N5491, 2N5492, 2N5493, 2N5494, 2N5495, 2N5496 and 2N5497* are hometaxial-base silicon n-p-n transistors. They are intended for a wide variety of medium-power switching and amplifier applications, such as series and shunt regulators and driver and output stages of high-fidelity amplifiers.

Types 2N5491, 2N5493, 2N5495, and 2N5497 have formed emitter and base leads for insertion into TO-66 sockets. Types 2N5490, 2N5492, 2N5494, and 2N5496 are electrically identical to the 2N5491, 2N5493, 2N5495, and 2N5497 but have straight leads for mounting on printed circuit boards.

These new plastic power transistors differ in voltage ratings and in the currents at which the parameters are controlled.

* Formerly RCA Dev. Nos. TA7317, TA7318, TA7315, TA7316, TA7313, TA7314, TA7311, TA7312, respectively.

FEATURES

- **Low saturation voltage—**
  $V_{CE}(sat)$ = 1 V max. at I_C = 2 A (2N5490, 2N5491)
  = 1 V max. at I_C = 2.5 A (2N5492, 2N5493)
  = 1 V max. at I_C = 3 A (2N5494, 2N5495)
  = 1 V max. at I_C = 3.5 A (2N5496, 2N5497)
- **Molded silicone-plastic package**
- **Maximum safe-area-of-operation curves specified for DC and pulse operation**

Maximum Ratings, *Absolute-Maximum Values:*

		2N5490 2N5491 2N5494 2N5495	2N5492 2N5493	2N5496 2N5497	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	60	75	90	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:					
With -1.5 volts (V_{BE}) of reverse bias	$V_{CEV}(sus)$	60	75	90	V
With external base-to-emitter resistance (R_{BE}) = 100Ω	$V_{CER}(sus)$	50	65	80	V
With base open	$V_{CEO}(sus)$	40	55	70	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	5	5	V
COLLECTOR CURRENT	I_C	7	7	7	A
BASE CURRENT	I_B	3	3	3	A
TRANSISTOR DISSIPATION:	P_T				
At case temperatures up to 25°C		50	50	50	W
At ambient temperatures up to 25°C		1.8	1.8	1.8	W
At case temperatures above 25°C		Derate linearly at 0.4 W/°C or see Figs. 2 & 3.			
At ambient temperatures above 25°C		Derate linearly at 0.0144 W/°C			
TEMPERATURE RANGE:					
Storage & Operating (Junction)		← -65 to 150 →			°C
LEAD TEMPERATURE (During Soldering):					
At distance ≥ 1/8 in. (3.17 mm) from case for 10 s max		← 235 →			°C

ELECTRICAL CHARACTERISTICS *Case Temperature (T_C) = 25° C Unless Otherwise Specified*

Characteristics	Symbols	TEST CONDITIONS					LIMITS								Units
		DC Collector Voltage (V)	DC Emitter or Base Voltage (V)		DC Current (A)		Types 2N5496 2N5497		Types 2N5494 2N5495		Types 2N5492 2N5493		Types 2N5490 2N5491		
		V_{CE}	V_{EB}	V_{BE}	I_C	I_B	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Collector-Cutoff Current With base-emitter junction reverse biased	I_{CEV}	85		-1.5			-	1	-	-	-	-	-	-	mA
		55		-1.5			-	-	-	1	-	-	-	-	
		70		-1.5			-	-	-	-	-	1	-	-	
	I_{CEV} (T_C = 150°C)	85		-1.5			-	5	-	-	-	-	-	-	mA
		55		-1.5			-	-	-	5	-	-	-	-	
		70		-1.5			-	-	-	-	-	5	-	-	
Collector-Cutoff Current With external base-to-emitter resistance (R_{BE}) = 100 Ω	I_{CER}	70					-	0.5	-	-	-	-	-	-	mA
		40					-	-	-	0.5	-	-	-	2	
		55					-	-	-	-	-	0.5	-	-	
	I_{CER} (T_C = 150°C)	70					-	3.5	-	-	-	-	-	-	mA
		40					-	-	-	3.5	-	-	-	5	
		55					-	-	-	-	-	3.5	-	-	
Emitter-Cutoff Current	I_{EBO}		5				-	1	-	1	-	1	-	1	mA
DC Forward-Current Transfer Ratio	h_{FE}[c]	4			3.5		20	100	-	-	-	-	-	-	
		4			3		-	-	20	100	-	-	-	-	
		4			2.5		-	-	-	-	20	100	-	-	
		4			2		-	-	-	-	-	-	20	100	
Collector-to-Emitter Sustaining Voltage: With base open	$V_{CEO}(sus)$[c]				0.1	0	70	-	40	-	55	-	40	-	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$[c]				0.1		80	-	50	-	65	-	50	-	V
With base-emitter junction reverse biased	$V_{CEV}(sus)$[c]			-1.5	0.1		90	-	60	-	75	-	60	-	V
Base-to-Emitter Voltage	V_{BE}[c]	4			3.5		-	1.7	-	-	-	-	-	-	V
		4			3		-	-	-	1.5	-	-	-	-	
		4			2.5		-	-	-	-	-	1.3	-	-	
		4			2		-	-	-	-	-	-	-	1.1	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$[c]				3.5	0.35	-	1	-	-	-	-	-	-	V
					3	0.3	-	-	-	1	-	-	-	-	
					2.5	0.25	-	-	-	-	-	1	-	-	
					2	0.2	-	-	-	-	-	-	-	1	
Gain-Bandwidth Product	f_T	4			0.5		0.8	-	0.8	-	0.8	-	0.8	-	MHz
Sat. Switching Time: Turn-On (See Figs.15 and 17)	t_{on}	V_{CC} = 30			3.5	0.35[a]	-	5	-	-	-	-	-	-	µs
					3	0.3[a]	-	-	-	5	-	-	-	-	
					2.5	0.25[a]	-	-	-	-	-	5	-	-	
					2	0.2	-	-	-	-	-	-	-	5	
Turn-Off (See Figs.15 and 17)	t_{off}	V_{CC} = 30			3.5	0.35[b]	-	15	-	-	-	-	-	-	µs
					3	0.3[b]	-	-	-	15	-	-	-	-	
					2.5	0.25[b]	-	-	-	-	-	15	-	-	
					2	0.2	-	-	-	-	-	-	-	15	
Thermal Resistance: Junction-to-Case	θ_{J-C}						-	2.5	-	2.5	-	2.5	-	2.5	°C/W
Junction-to-Ambient	θ_{J-A}						-	70	-	70	-	70	-	70	°C/W

[a] I_{BI} value (turn-on base current). [b] I_{B2} value (turn-off base current). [c] Pulsed, pulse duration = 300 µs, duty factor = .018.

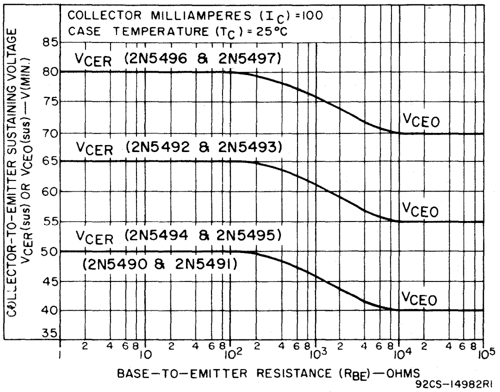


Fig.1 - Collector-to-emitter sustaining voltage characteristics for types 2N5490 through 2N5497 inclusive.

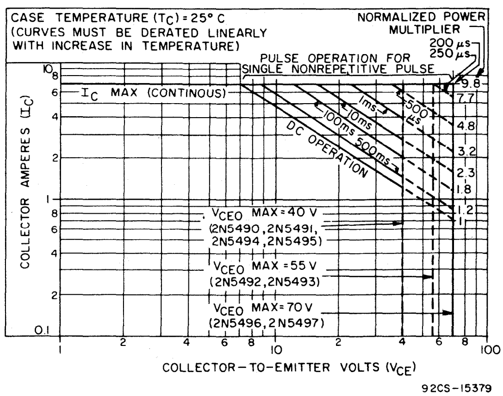


Fig.2 - Maximum operating areas for types 2N5490 through 2N5497 inclusive.

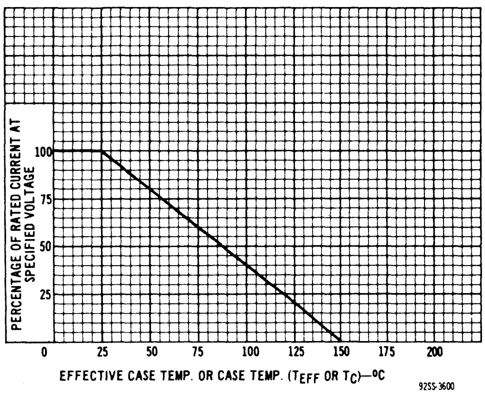


Fig.3 - Dissipation derating curve for types 2N5490 through 2N5497 inclusive.

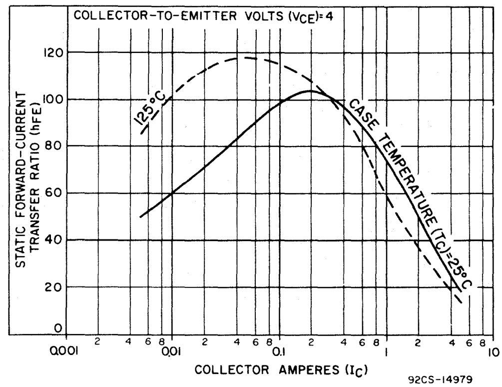


Fig.4 - Typical static beta characteristics for types 2N5496 and 2N5497.

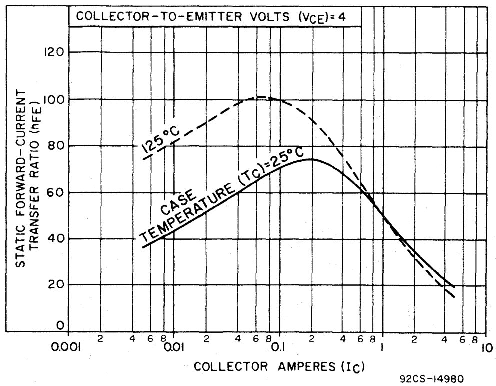


Fig.5 - Typical static beta characteristics for types 2N5494 and 2N5495.

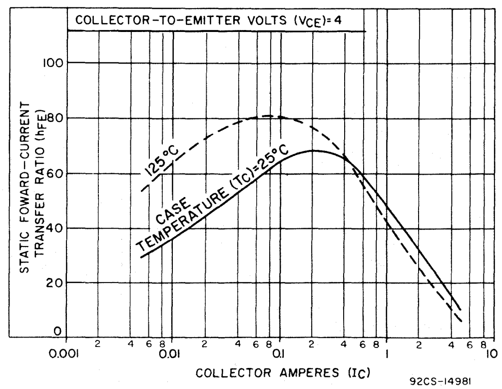


Fig.6 - Typical static beta characteristics for types 2N5490 through 2N5493 inclusive.

REVERSE-BIAS OPERATION

The energy required to induce second breakdown when the transistor is turned off depends on the current during the "on" condition, the emitter-to-base voltage and resistance when the transistor is turned off, and the amount of inductance in series with the collector. The curves shown in Fig.7 should prove useful in the design of circuits having inductive loads (such as solenoid- or relay-control circuits, magnetic-circuits, magnetic-deflection circuits, and switching regulators) without protective zener diodes across the collector-emitter junction. Also, these curves can be used in the design of circuits in which some leakage inductance is present (such as inverters, converters, and transformer-coupled power amplifiers.)

The curves shown in Fig.2 are based on the premise that the junction temperature must not exceed the maximum allowable junction temperature. Also, this limit must not be exceeded in the reverse-bias mode. After it is established that the operation of the unit lies within the capability shown in Fig.7, a computation is required to insure that the reverse bias energy will not exceed the derated power time as shown in Fig.2. Derating is accomplished as described in the preceding discussion of forward-bias operation.

In general, reverse-bias second-breakdown energy ($E_{S/b}$) capability increases with a decrease in inductance. Therefore, the allowable energy shown in the above-mentioned curves (calculated from $E_{S/b} = ½LI^2$, where L is a series load or leakage inductance and I is the peak collector current from the curves) will be conservative for smaller inductive loads. For further information on second breakdown, consult RCA "SILICON POWER CIRCUITS MANUAL." Form No. SP-50.

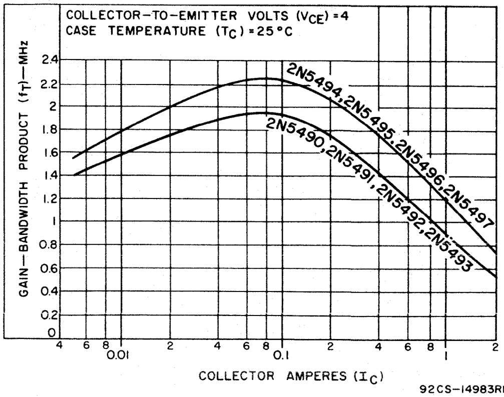


Fig.8 - Typical gain-bandwidth product for types 2N5490 through 2N5497 inclusive.

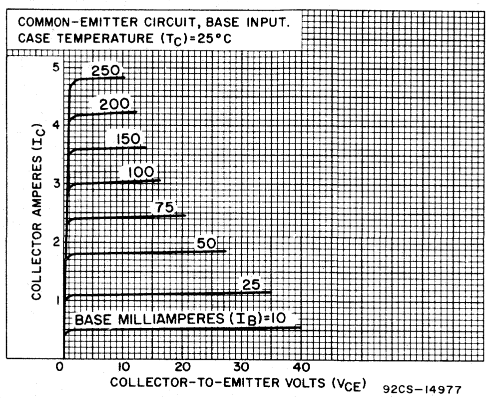


Fig.9 - Typical output characteristics for types 2N5494 through 2N5497 inclusive.

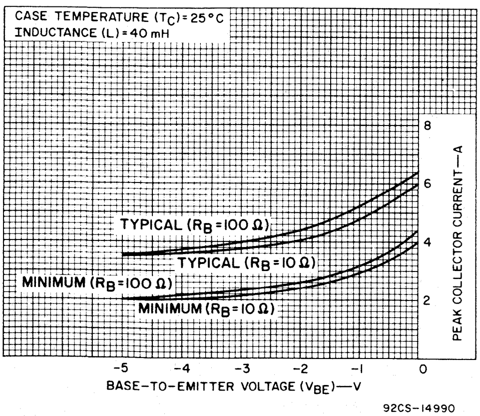


Fig.7 - Reverse-Bias, Second-Breakdown Characteristics for Types 2N5490 through 2N5497 inclusive.

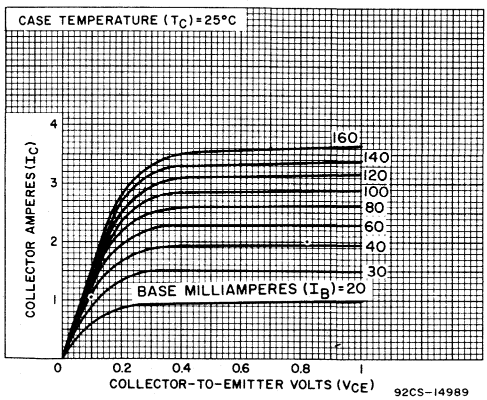


Fig.10 - Typical output characteristics for types 2N5494 and 2N5495.

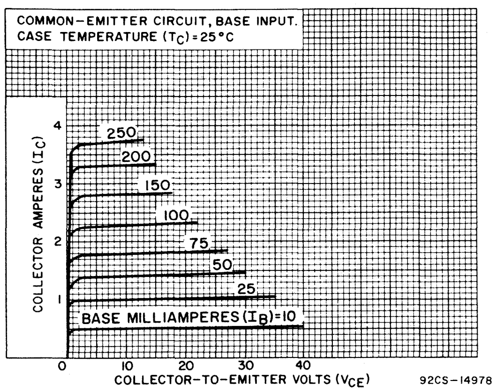


Fig.11 - Typical output characteristics for types 2N5490 through 2N5493 inclusive.

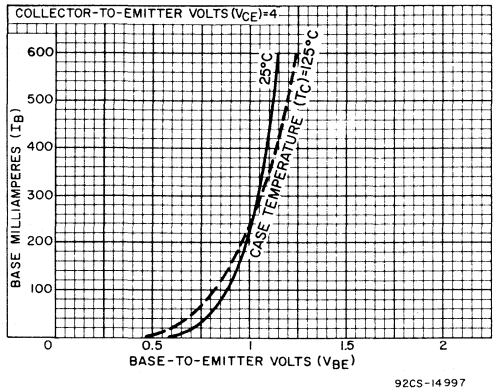


Fig.12 - Typical input characteristics for types 2N5494 through 2N5497 inclusive.

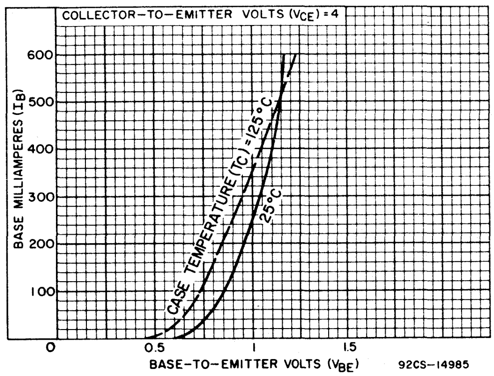


Fig.13 - Typical input characteristics for types 2N5490 through 2N5493 inclusive.

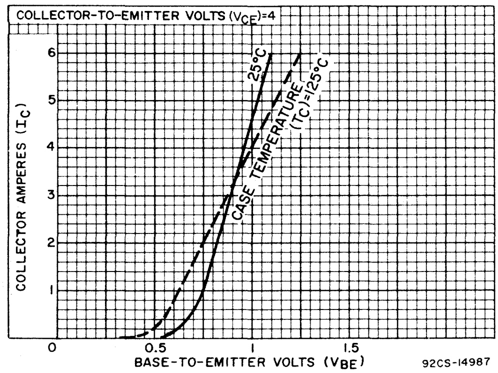


Fig.14 - Typical transfer characteristics for types 2N5494 through 2N5497 inclusive.

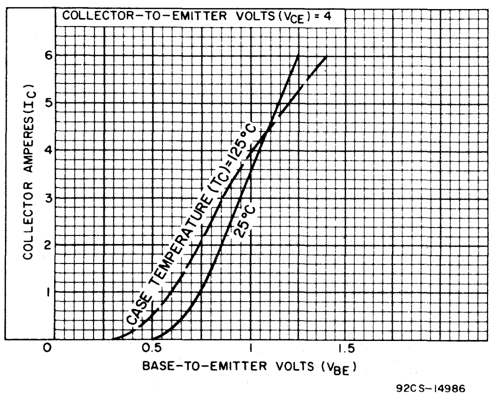


Fig.15 - Typical transfer characteristics for types 2N5490 through 2N5493 inclusive.

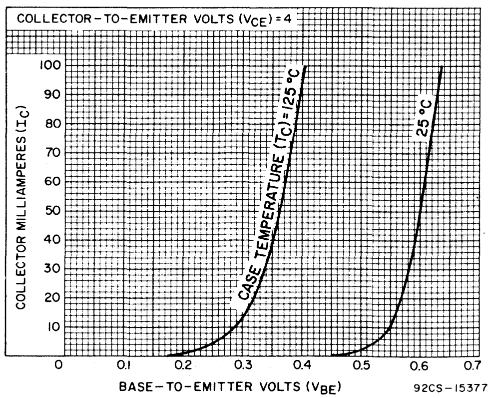


Fig.16 - Typical transfer characteristics for types 2N5490 through 2N5497 inclusive.

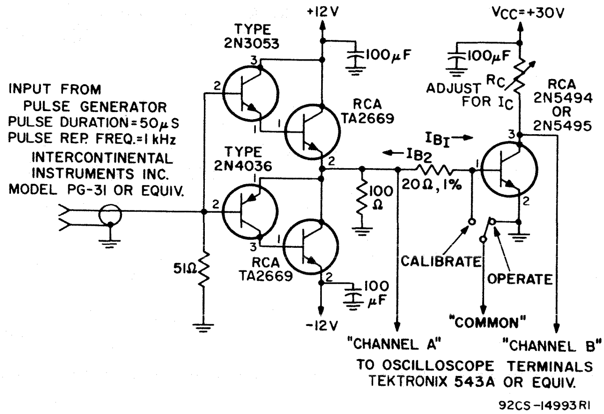


Fig.17 - Circuit used to measure switching times for types 2N5494 and 2N5495.

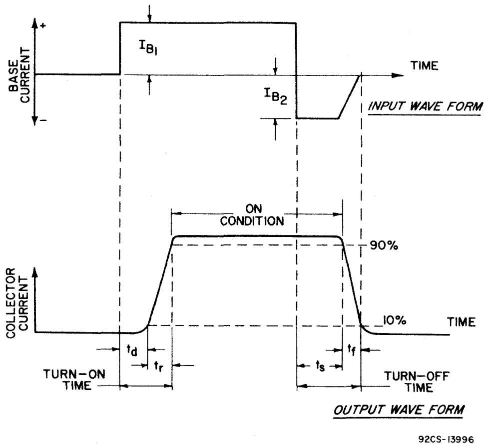


Fig.18 - Oscilloscope display for measurement of switching times (test circuit shown in Fig.17).

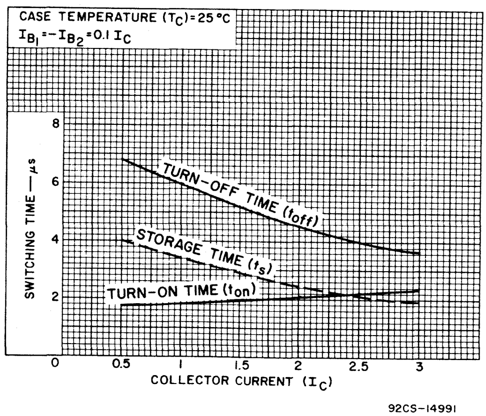
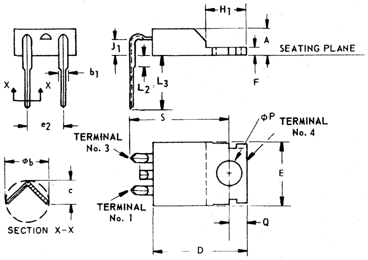


Fig.19 - Typical saturated switching characteristics for types 2N5494 and 2N5495.

DIMENSIONAL OUTLINE FOR TYPES 2N5490, 2N5492, 2N5494, & 2N5496



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.02	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e_2	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L_2	–	0.050	–	1.27	–
L_3	0.360	0.422	9.15	10.71	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–
S	0.580	0.610	14.74	15.49	–

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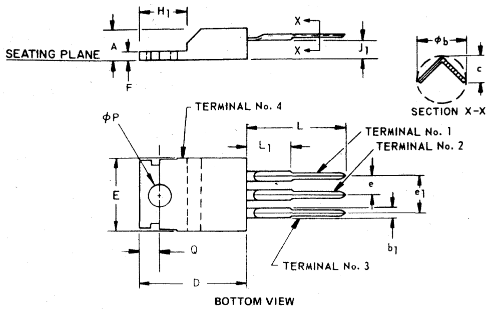
NOTES:

1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.050 – 0.055 (1.27 – 1.40 mm) below seating plane.

TERMINAL CONNECTIONS

Terminal No. 1-Base
Terminal No. 3-Emitter
Terminal No. 4-Collector

DIMENSIONAL OUTLINE FOR TYPES 2N5491, 2N5493, 2N5495, & 2N5497



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

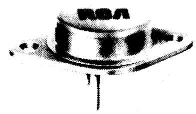
TERMINAL CONNECTIONS

Terminal No. 1-Base
Terminal No. 2-Collector
Terminal No. 3-Emitter
Terminal No. 4-Collector

RCA
Solid State
Division

Power Transistors

2N6371



JEDEC TO-3

H-1570

Hometaxial II* High-Power Silicon N-P-N Transistors

Rugged General-Purpose Device
For Industrial and Commercial Uses

Features:

- **Maximum-safe-area-of-operation curves**
- **Low saturation voltage**
- **High dissipation rating**
- **Thermal-cycle rating curve**

Applications:

- **Series and shunt regulators**
- **High-fidelity amplifiers**
- **Power-switching circuits**
- **Solenoid drivers**
- **12-V audio and inverter circuits**

The RCA-2N6371▲ is a hometaxial-base● diffused-junction silicon n-p-n transistor intended for a wide variety of intermediate-power and high-power applications. It is especially suited for use in audio and inverter circuits at 12 volts.

▲RCA-2N6371 is the direct replacement for RCA-40251.

●"Hometaxial" was coined by RCA from "homogeneous" and "axial" to describe a single-diffused transistor with a base region of homogeneous-resistivity silicon in the axial direction (emitter-to-collector). "Hometaxial II" is a term used to describe RCA's expanded line of transistors produced by the hometaxial process.

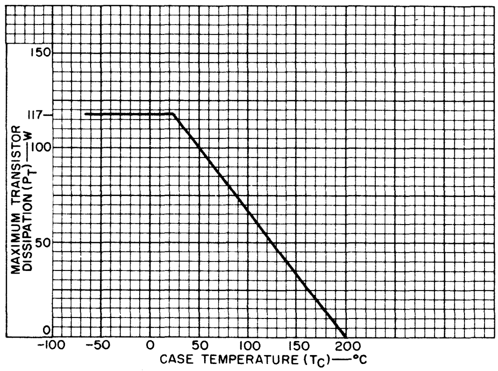


Fig. 1—Dissipation derating curve.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:			
* With external base-to-emitter resistance R_{BE} = 100 Ω	$V_{CER}(sus)$	45	V
* With base open	$V_{CEO}(sus)$	40	V
With base reverse bias V_{BE} = −1.5 V	$V_{CEX}(sus)$	50	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	V
*CONTINUOUS COLLECTOR CURRENT	I_C	16	A
*CONTINUOUS BASE CURRENT	I_B	7	A
*TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25°C		117	W
At case temperatures above 25°C		See Fig. 1	
*TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to +200	°C
*PIN TEMPERATURE (During Soldering):			
At distances ≥ 1/32 in. (0.8 mm) from seating plane for 10 s max.		235	°C

*In accordance with JEDEC registration data format JS-6 RDF-2.

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: VOLTAGE V dc V_{CE}	VOLTAGE V dc V_{EB}	VOLTAGE V dc V_{BE}	CURRENT A dc I_C	CURRENT A dc I_B	LIMITS MIN.	LIMITS MAX.	UNITS
* Collector Cutoff Current: With base open	I_{CEO}	25				0	–	1.5	mA
With base-emitter junction reverse-biased	I_{CEV}	45		−1.5			–	2	mA
At T_C = 150°C	I_{CEV}	40		−1.5			–	10	mA
* Emitter Cutoff Current	I_{EBO}		5				–	10	mA
Collector-to-Emitter Sustaining Voltage: * With base open	$V_{CEO}(sus)$				0.2	0	40	–	V
* With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$				0.2		45	–	V
With base-emitter junction reverse-biased	$V_{CEX}(sus)$			−1.5	0.1		50	–	V
* DC Forward Current Transfer Ratio	h_{FE}	4			8[a]		15	60	
		4			16[a]		4	–	
* Base-to-Emitter Voltage	V_{BE}	4			16[a]		–	4	V
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				16[a]	4	–	4	V
					8[a]	0.8	–	1.5	V
* Common-Emitter, Small-Signal, Short-Circuit Forward Current Transfer Ratio (f = 1 kHz)	h_{fe}	4			1		10	–	
* Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 0.4 MHz)	$\|h_{fe}\|$	4			1		2	–	
Gain-Bandwidth Product	f_T				1		800	–	kHz
Forward-Bias Second Breakdown Collector Current	$I_{S/b}$	40					2.9	–	A
Thermal Resistance Junction-to-Case	$R_{\theta JC}$						–	1.5	°C/W

[a] Pulsed: Pulse duration = 300 μs, duty factor = 2%.
* In accordance with JEDEC registration data format JS-6 RDF-2.

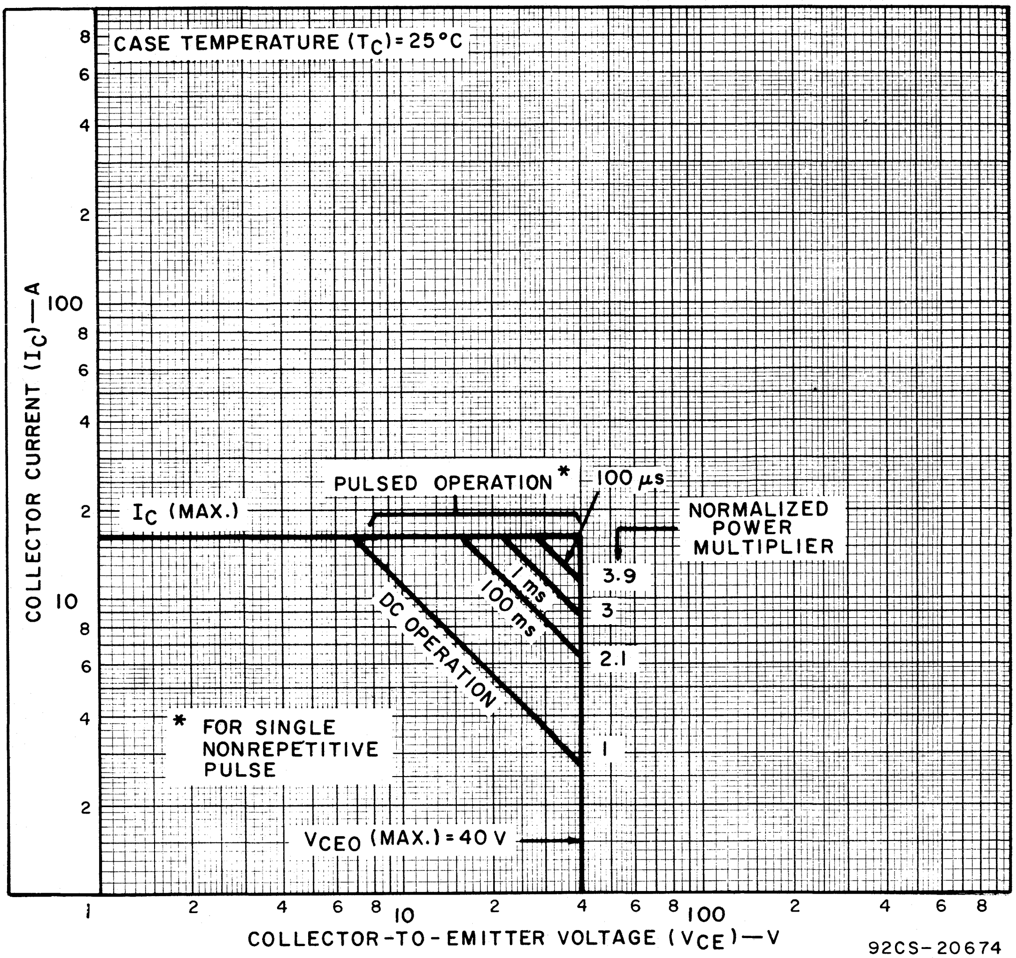


Fig. 2—Maximum safe area of operation at case temperature of 25°C.

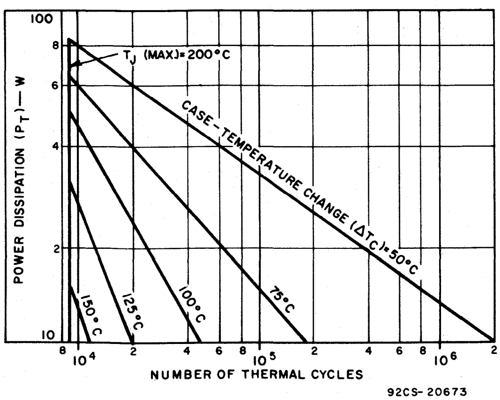


Fig. 3—Thermal-cycle rating chart.

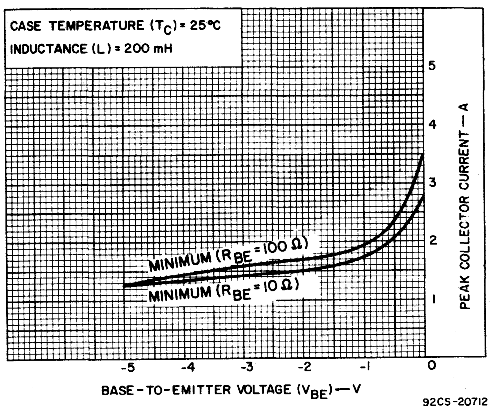


Fig. 4—Reverse-bias second-breakdown characteristics.

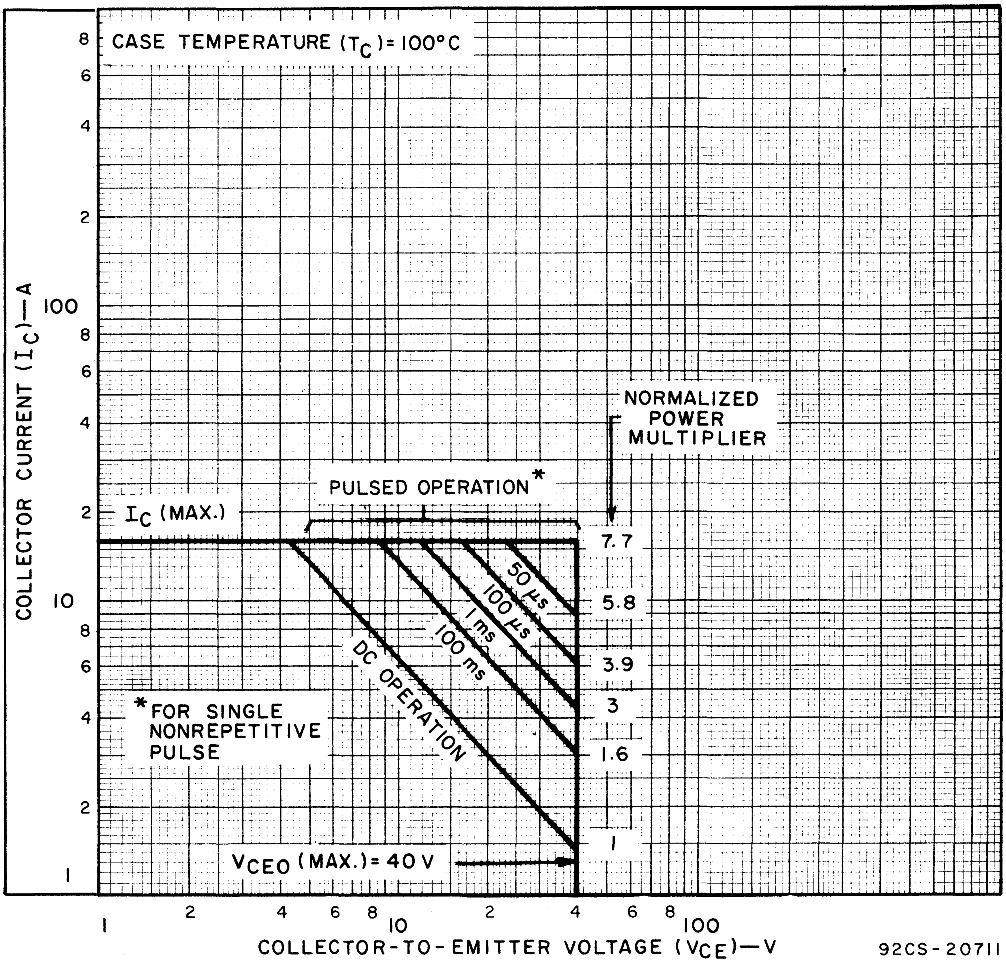


Fig. 5—Maximum safe area of operation at case temperature of 100°C.

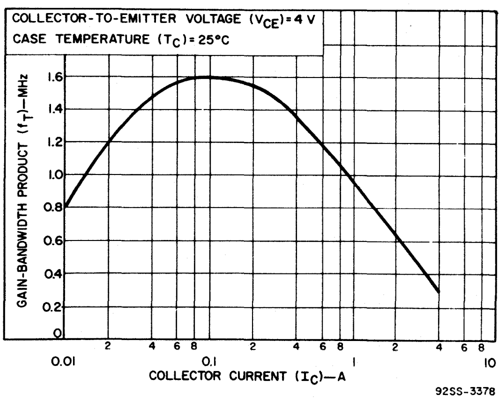


Fig. 6—Typical gain-bandwidth product.

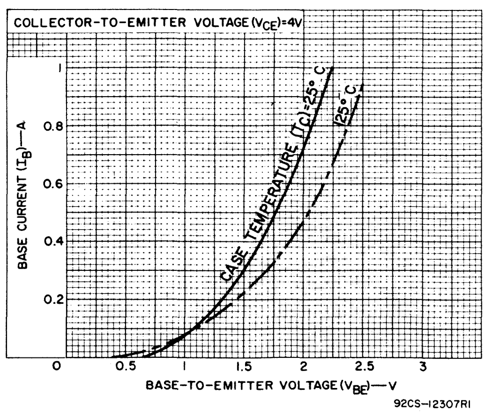


Fig. 7—Typical input characteristics.

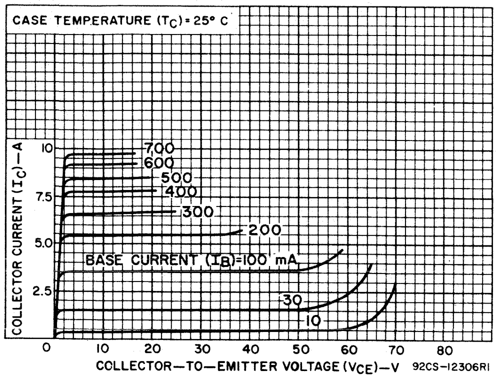


Fig. 8—Typical output characteristics.

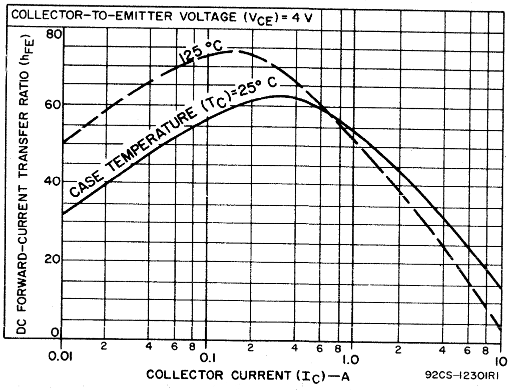
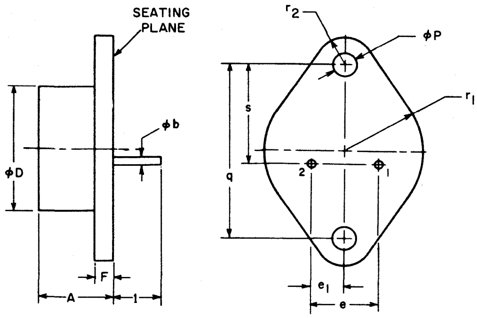


Fig. 9—Typical dc beta characteristics.

DIMENSIONAL OUTLINE JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
ϕb	0.038	0.043	0.97	1.09	2
ϕD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e_1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
1	0.312		7.92		2
ϕP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r_1		0.525		13.34	
r_2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS–15222

TERMINAL CONNECTIONS

Pin 1 — Base
Pin 2 — Emitter
Case — Collector
Mounting Flange — Collector

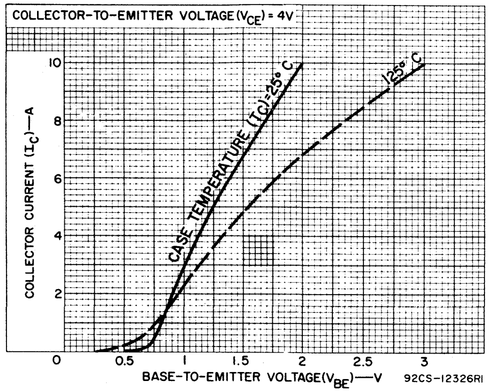
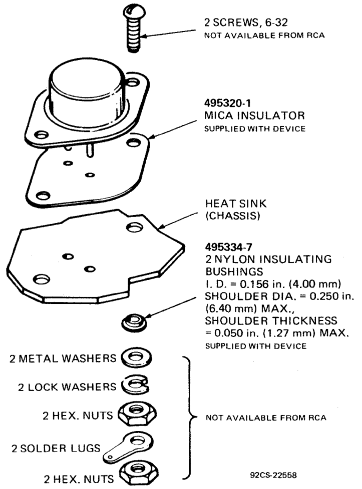


Fig. 10—Typical transfer characteristics.



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 11—Suggested mounting hardware.

For basic transistor theory, circuits, and application information, refer to "RCA Solid State Power Circuits Designer's Handbook", SP-52, or "RCA Transistor, Thyristor, & Diode Manual", SC-15.

RCA

Solid State
Division

Power Transistors
2N6254
2N3055
2N6253

JEDEC TO-3

H-1570

Hometaxial II• High-Power Silicon N-P-N Transistors

Rugged, Broadly Applicable Devices
For Industrial and Commercial Use

Features:

- **2N6254: premium type from 2N3055 family**
- **Maximum safe-area-of-operation curves**
- **Low saturation voltages**
- **High dissipation ratings**
- **Thermal-cycle rating curves**

Applications:

- **Series and shunt regulators**
- **High-fidelity amplifiers**
- **Power-switching circuits**
- **Solenoid drivers**

RCA 2N3055, 2N6253 and 2N6254 are silicon n-p-n transistors intended for a wide variety of high-power applications. The hometaxial•-base construction of these devices renders them highly resistant to second breakdown over a wide range of operating conditions.

•"Hometaxial" was coined by RCA from "homogeneous" and "axial" to describe a single-diffused transistor with a base region of homogeneous-resistivity silicon in the axial direction (emitter-to-collector).

"Hometaxial II" is a term used to describe RCA's expanded line of transistors produced by the hometaxial process.

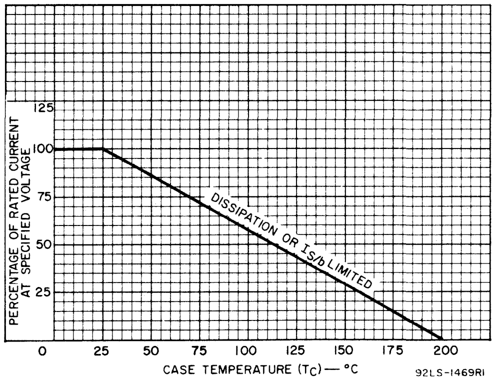


Fig. 1—Current derating curve.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N6253	2N3055	2N6254	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	55	100	100	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:					
* With external base-to-emitter resistance (R_{BE}) = 100Ω	$V_{CER}(sus)$	55	70	85	V
* With base open	$V_{CEO}(sus)$	45	60	80	V
With base reverse-biased V_{BE} = -1.5 V	$V_{CEV}(sus)$	55	90	90	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	7	7	V
*CONTINUOUS COLLECTOR CURRENT	I_C	15	15	15	A
*CONTINUOUS BASE CURRENT	I_B	7	7	7	A
*TRANSISTOR DISSIPATION	P_T				
At case temperatures up to 25°C		115	115	150	W
At case temperatures above 25°C		← See Fig. 1 →			
*TEMPERATURE RANGE:					
Storage and Operating (Junction)		← -65 to +200 →			°C
*PIN TEMPERATURE (During Soldering):					
At distances ≥1/32 in. (0.8 mm) from seating plane for 10 s max.		← 235 →			°C

*In accordance with JEDEC registration data formats (2N3055:JS-9 RDF-10/2N6253-4: JS-6 RDF-2).

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ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified.*

CHARACTERISTIC	SYMBOL	DC COLLECTOR VOLTAGE V	DC EMITTER OR BASE VOLTAGE V		DC CURRENT A		LIMITS						UNITS
							2N6253		2N3055		2N6254		
		V_{CE}	V_{EB}	V_{BE}	I_C	I_B	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
* Collector-Cutoff Current: With base open	I_{CEO}	25				0	–	1.5	–	–	–	–	mA
		30				0	–	–	–	0.7	–	–	
		60				0	–	–	–	–	–	1	
With base-emitter junction reverse-biased	I_{CEX}	55		-1.5			–	2	–	–	–	–	
		100		-1.5			–	–	–	5	–	0.5	
At T_C = 150°C	I_{CEX}	50		-1.5			–	10	–	–	–	–	
		100		-1.5			–	–	–	30	–	5	
* Emitter-Cutoff Current	I_{EBO}		5				–	10	—	–	–	–	mA
			7				–	–	–	5	–	0.5	
Collector-to-Emitter Sustaining Voltage: * With base open	$V_{CEO}(sus)$				0.2[a]	0	45	–	60	–	80	–	V
* With external base-to-emitter resistance (R_{BE}) = 100Ω	$V_{CER}(sus)$				0.2[a]		55	–	70	–	85	–	
With base-emitter junction reverse-biased	$V_{CEV}(sus)$			-1.5	0.1[a]		55	–	90	–	90	–	
* DC Forward Current Transfer Ratio	h_{FE}	4			15[a]		3	–	–	–	5	–	
		4			10[a]		–	–	5	–	–	–	
		2			5[a]		–	–	–	–	20	70	
		4			4[a]		–	–	20	70	–	–	
		4			3[a]		20	70	–	–	–	–	
* Base-to-Emitter Volatge	V_{BE}	4			3[a]		–	1.7	–	–	–	–	V
		4			4[a]		–	–	–	1.8	–	–	
		2			5[a]		–	–	–	–	–	1.5	
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				3[a]	0.3[a]	–	1	–	–	–	–	V
					4[a]	0.4[a]	–	–	–	1.1	–	–	
					5[a]	0.5[a]	–	–	–	–	–	0.5	
					10[a]	3.3[a]	–	–	–	8	–	–	
					15[a]	3[a]	–	–	–	–	–	4	
					15[a]	5[a]	–	4	–	–	–	–	
* Common-Emitter, Small-Signal, Short-Circuit Forward Current Transfer Ratio (f = 1 kHz)	h_{fe}	4			1		10	–	15	120	10	–	
* Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 0.4 MHz)	$\|h_{fe}\|$	4			1		2	–	–	–	2	–	
Gain-Bandwidth Product	f_T				1		–	–	800	–	–	–	kHz
* Common-Emitter, Short-Circuit, Small-Signal, Forward Current Transfer Ratio Cutoff Frequency	f_{hfe}	4			1		10	–	10	–	10	–	kHz
Forward-Bias Second Breakdown Collector Current	$I_{S/b}$	80			1.87		–	–	–	–	1	–	s
		60			1.95		–	–	1	–	–	–	
		45			2.55		1	–	–	–	–	–	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$						–	1.5	–	1.5	–	1.17	°C/W

[a] Pulsed: Pulse duration = 300 μs, duty factor = 1.8%.
* In accordance with JEDEC registration data formats JS-9 RDF-10 (2N3055) and JS-6 RDF-2 (2N6253–4).

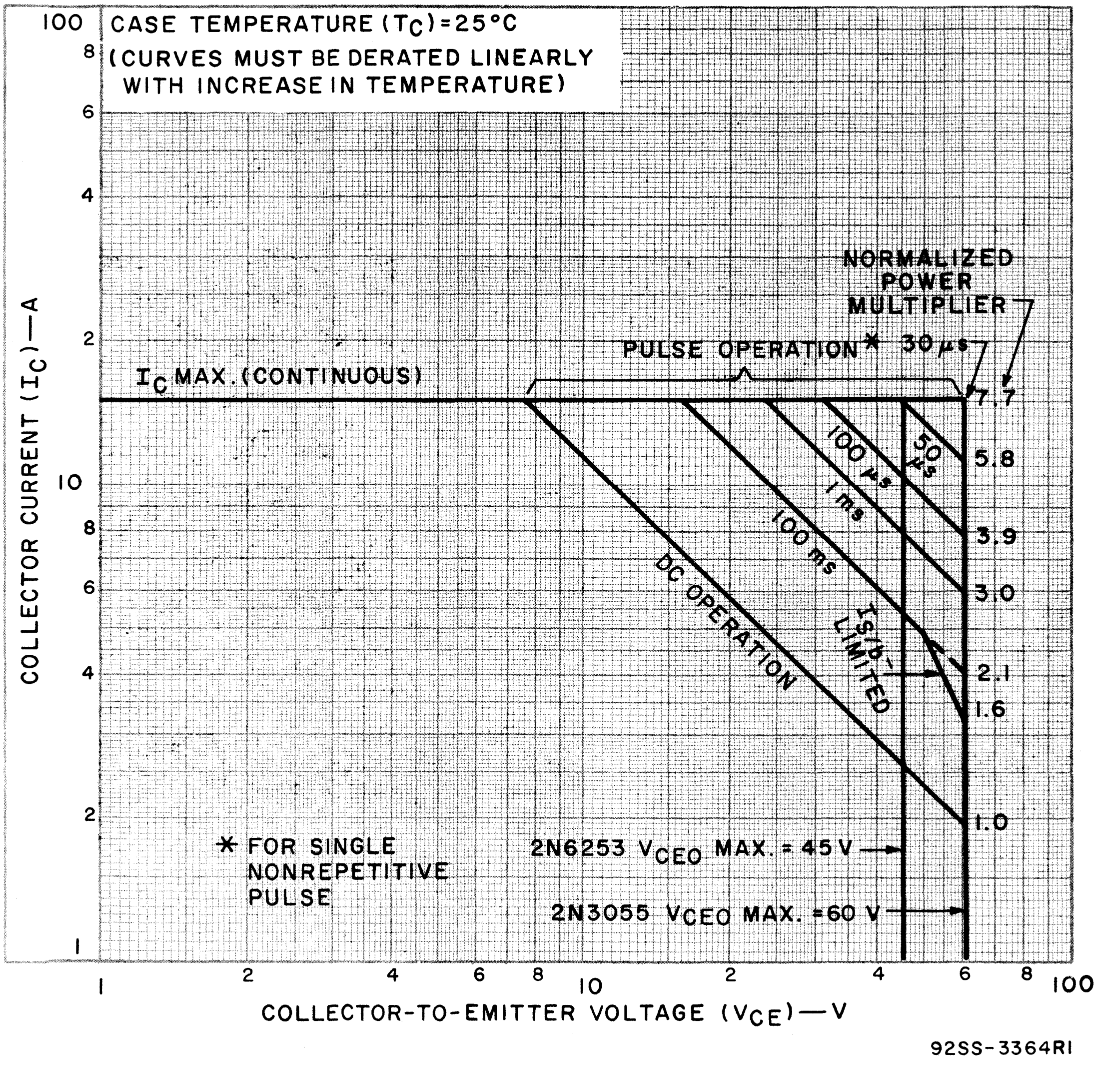


Fig.2—Maximum operating areas for types 2N6253 and 2N3055.

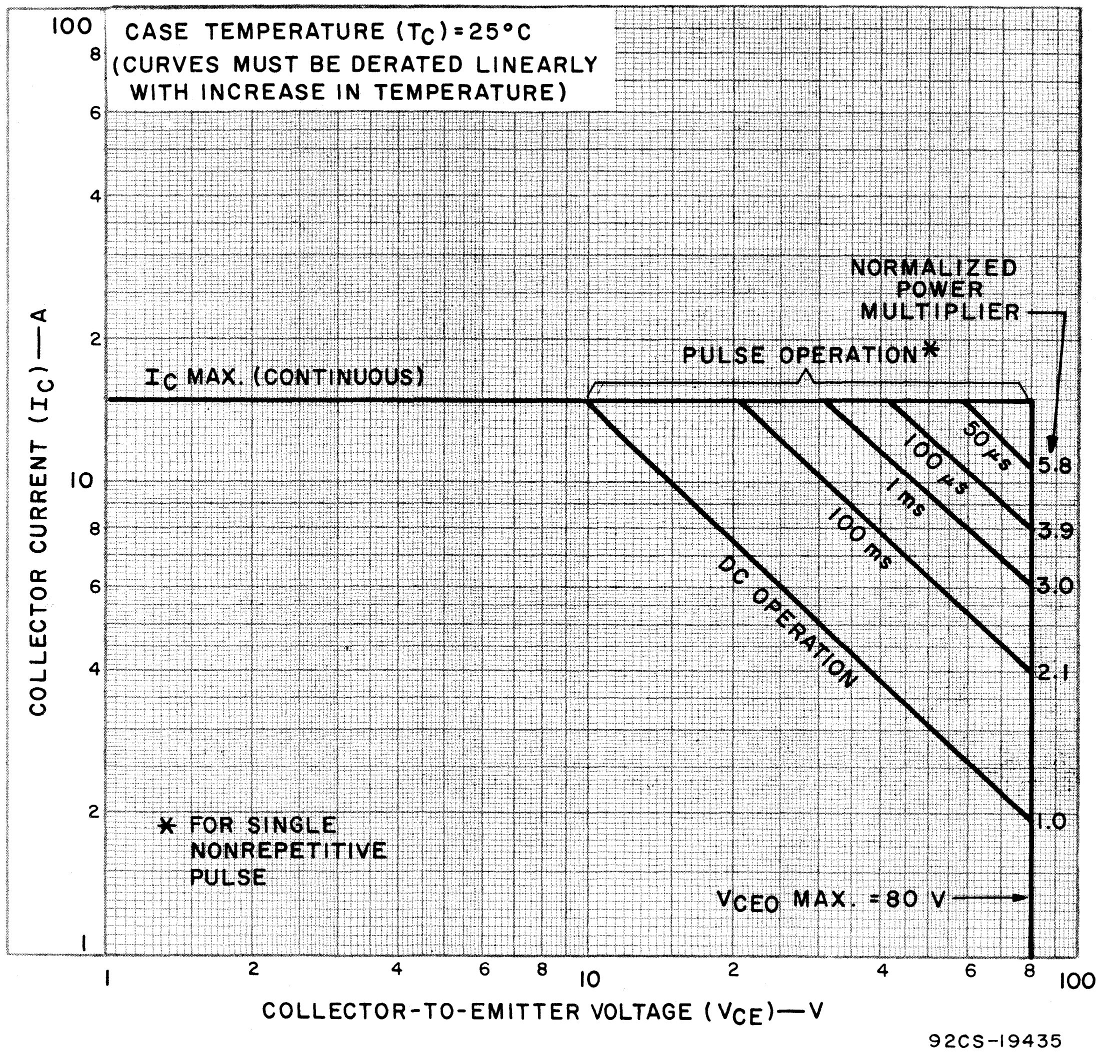


Fig.3—Maximum operating areas for 2N6254.

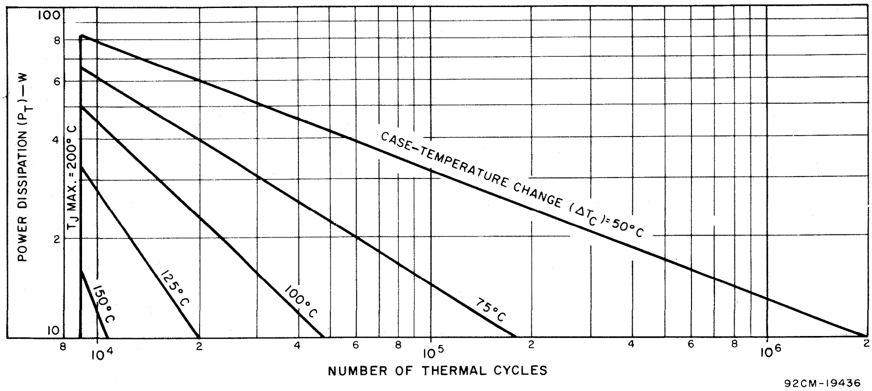


Fig.4—Thermal-cycle rating chart for types 2N3055 and 2N6253.

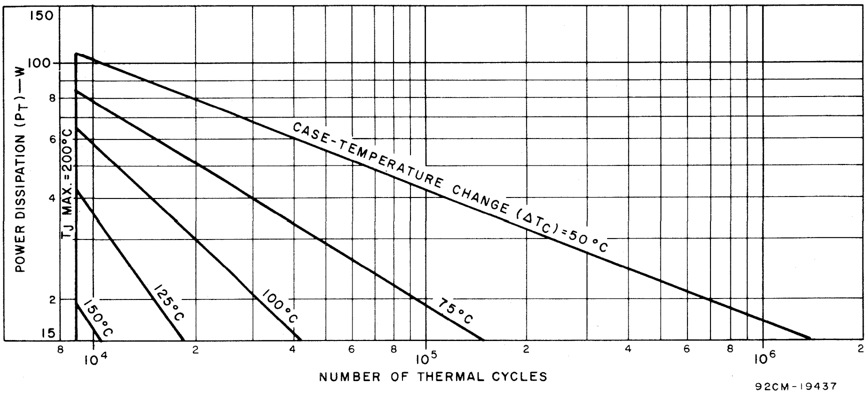


Fig.5—Thermal-cycle rating chart for type 2N6254.

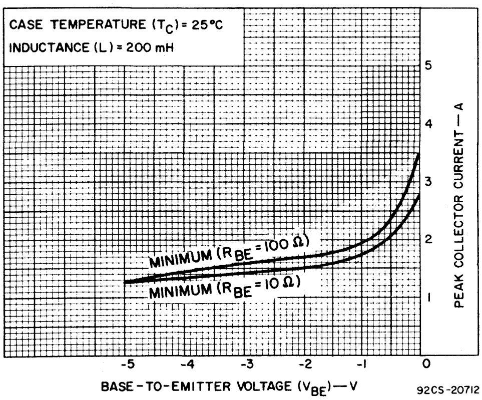


Fig.6—Reverse-bias, second-breakdown characteristics for all types.

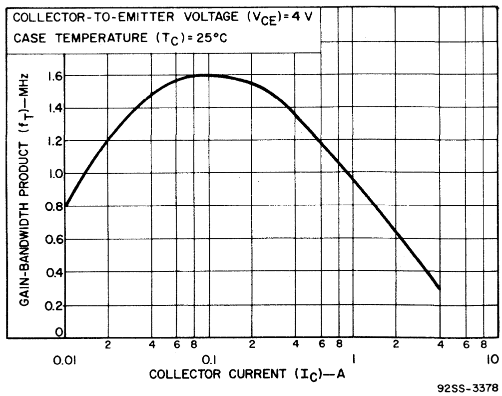


Fig.7—Typical gain-bandwidth product for all types.

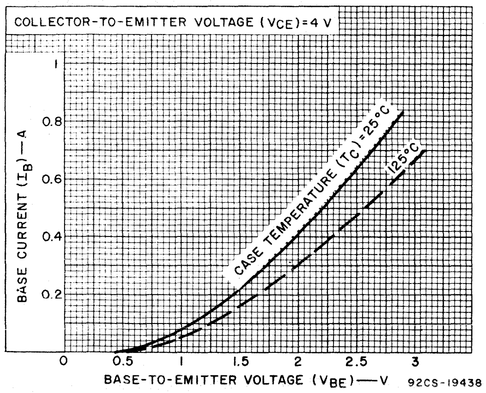


Fig.8—Typical input characteristics for type 2N6254.

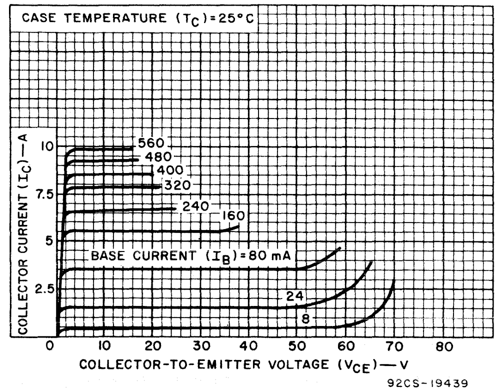


Fig.9—Typical output characteristics for type 2N6254.

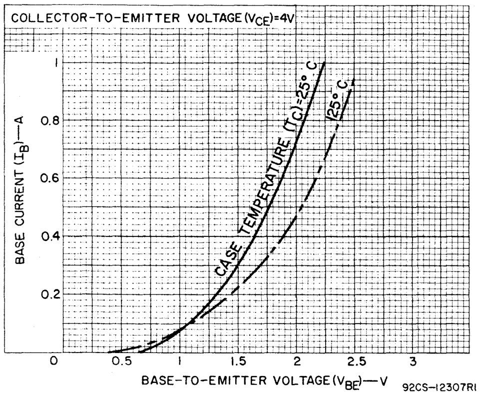


Fig.10—Typical input characteristics for type 2N3055.

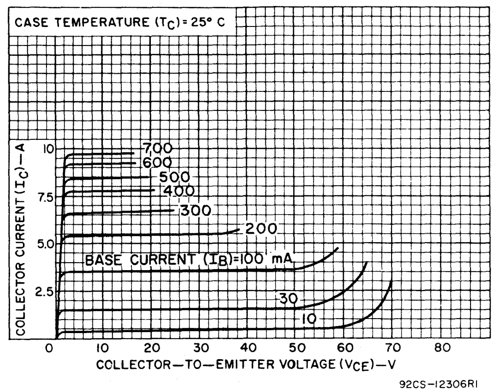


Fig.11—Typical output characteristics for type 2N3055.

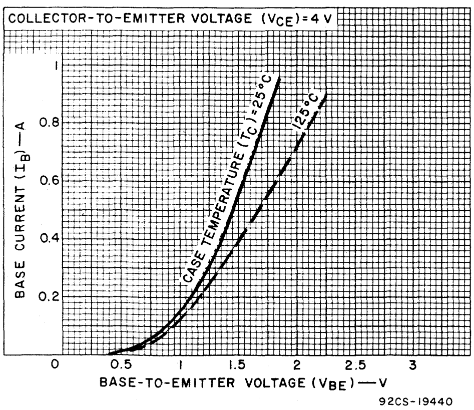


Fig.12—Typical input characteristics for type 2N6253.

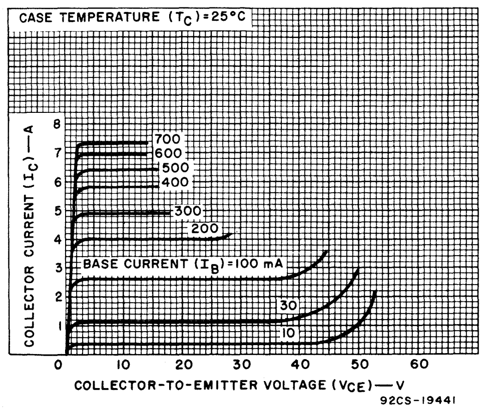


Fig.13—Typical output characteristics for type 2N6253.

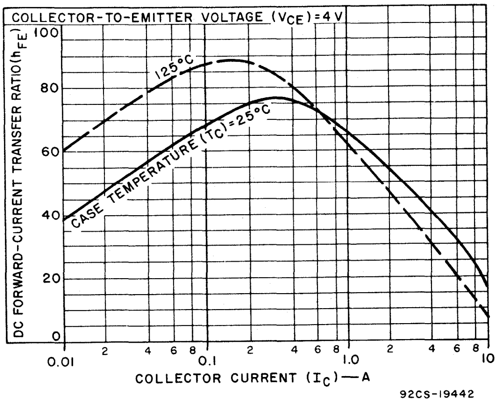


Fig.14—Typical dc-beta characteristics for type 2N6254.

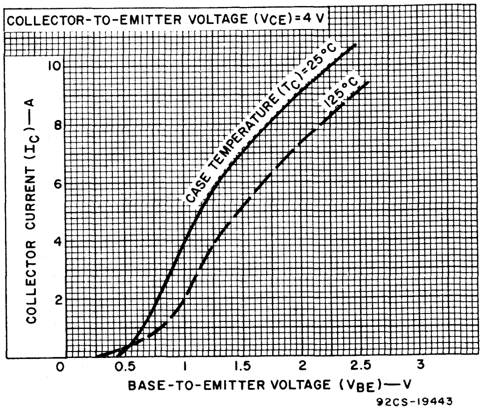


Fig.15—Typical transfer characteristics for type 2N6254.

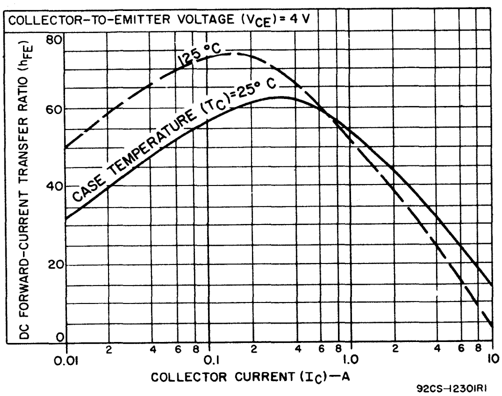


Fig.16—Typical dc-beta characteristics for type 2N3055.

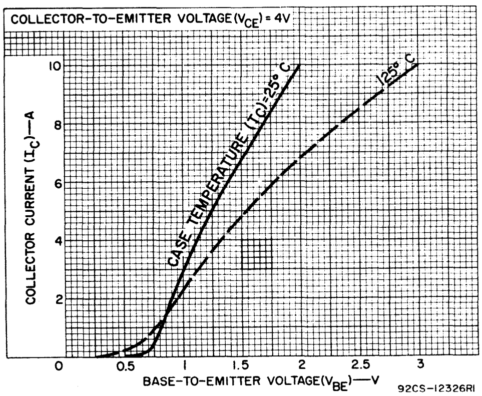


Fig.17—Typical transfer characteristics for types 2N6253 and 2N3055.

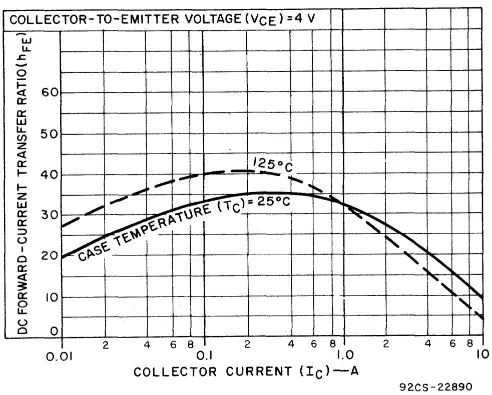


Fig.18—Typical dc-beta characteristics for type 2N6253.

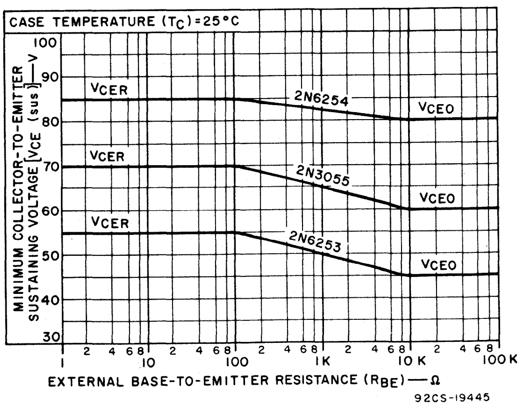
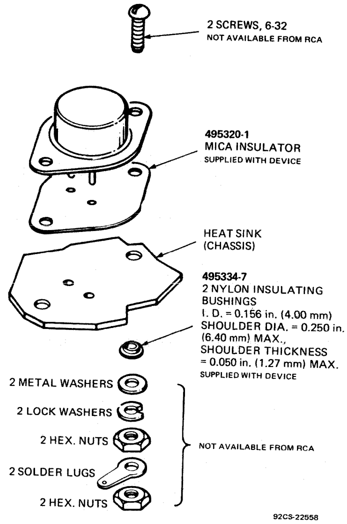


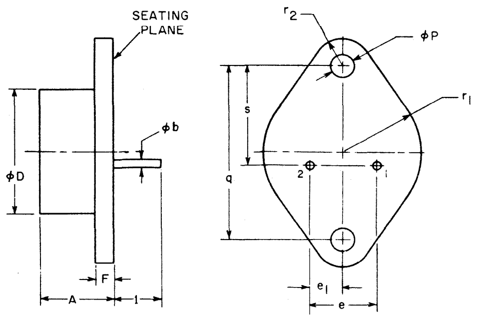
Fig.19—Sustaining voltage vs. base-to-emitter resistance for all types.



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.20—Suggested mounting hardware.

DIMENSIONAL OUTLINE JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
φb	0.038	0.043	0.97	1.09	2
φD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
1	0.312		7.92		2
φP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r1		0.525		13.34	
r2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

TERMINAL CONNECTIONS

Pin 1 – Base
Pin 2 – Emitter
Case – Collector
Mounting Flange – Collector

NOTES:

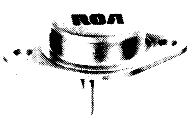
1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS–15222

RCA
Solid State Division

Power Transistors

BD142



JEDEC TO-3

H-1570

Hometaxial-Base, High-Power Silicon N-P-N Transistor

Rugged General-Purpose Device
For Commercial Use

Features:

- **Maximum-safe-area-of-operation curves**
- **Low saturation voltage**
- **High dissipation rating**
- **Thermal-cycling rating curve**

The RCA-BD142 is a hometaxial-base diffused-junction silicon n-p-n transistor intended for a wide variety of intermediate-power and high-power applications. It is especially suited for use in audio and inverter circuits at 12 volts.

Applications:

- **Series and shunt regulators**
- **High-fidelity amplifiers**
- **Power-switching circuits**
- **Solenoid drivers**
- **12-V audio and inverter circuits**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:			
With base open	$V_{CEO}(sus)$	45	V
With base reverse bias $V_{BE} = -1.5$ V	$V_{CEV}(sus)$	50	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	7	V
CONTINUOUS COLLECTOR CURRENT	I_C	15	A
CONTINUOUS BASE CURRENT	I_B	7	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25°C		117	W
At case temperatures above 25°C		See Figs. 1 & 2	
TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to +200	°C
PIN TEMPERATURE (During Soldering):			
At distances ≥ 1/32 in. (0.8 mm) from seating plane for 10 s max.		235	°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
		VOLTAGE V dc			CURRENT A dc				
		V_{CE}	V_{EB}	V_{BE}	I_C	I_B	MIN.	MAX.	
Collector Cutoff Current: With base-emitter junction reverse-biased	I_{CEV}	40		−1.5			–	2	mA
Emitter Cutoff Current	I_{EBO}		7				–	1	mA
Collector-to-Emitter Sustaining Voltage: With base open	$V_{CEO}(sus)$				0.2	0	45	–	V
With base-emitter junction reverse-biased	$V_{CEV}(sus)$			−1.5	0.1		50	–	
DC Forward Current Transfer Ratio	h_{FE}	4			4[a]		12.5	160	
Base-to-Emitter Voltage	V_{BE}	4			4[a]		–	1.5	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				4[a]	0.4	–	1.1	V
Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 1 kHz)	h_{fe}	4			1		10	–	
Magnitude of Common-Emitter, Small-Signal Short-Circuit, Forward Current Transfer Ratio (f = 0.4 MHz)	$\|h_{fe}\|$	4			1		2	–	
Gain-Bandwidth Product	f_T				1		800	–	kHz
Forward-Bias Second-Breakdown Collector Current (t ⩾ 1 s)	$I_{S/b}$	39					3	–	A
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$						–	1.5	°C/W

[a] Pulsed: Pulse duration = 300 μs, duty factor = 2%.

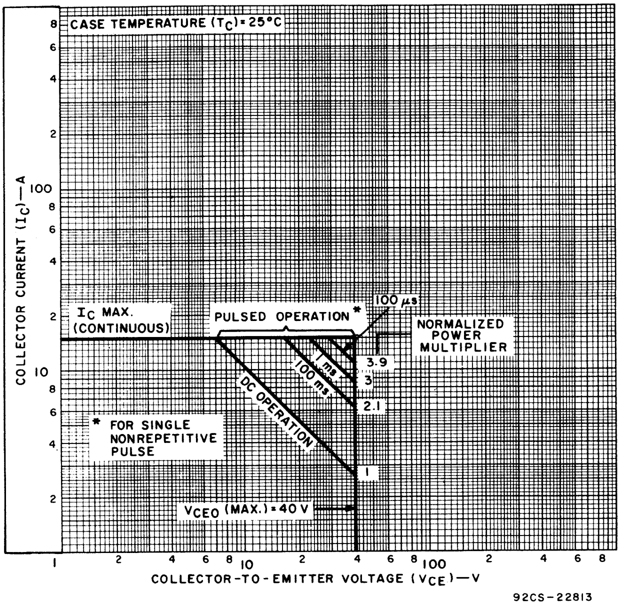


Fig. 1— Maximum safe area of operation.

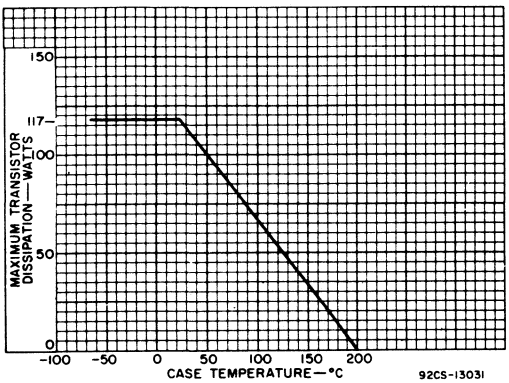


Fig. 2— Dissipation derating curve.

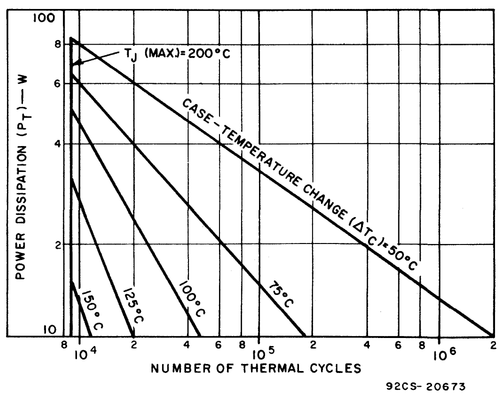


Fig. 3— Thermal-cycling rating chart.

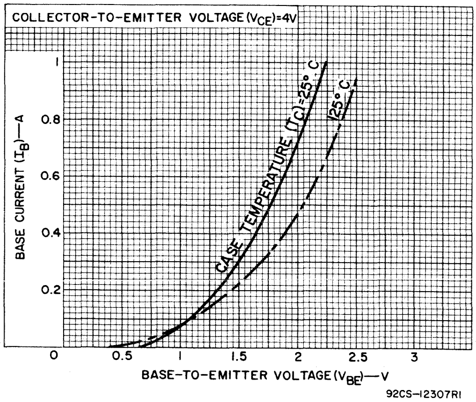


Fig. 4— Typical input characteristics.

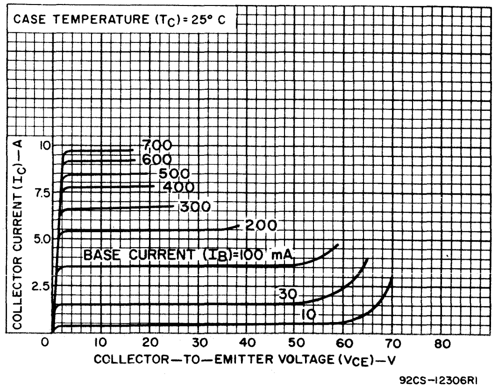


Fig. 5— Typical output characteristics.

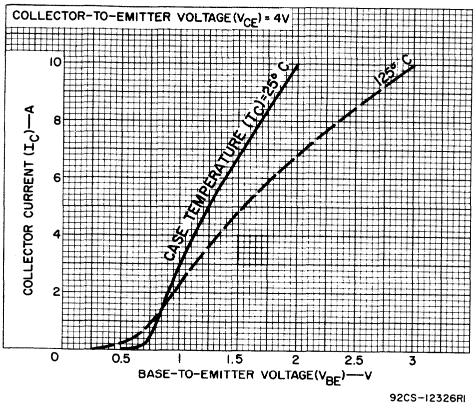


Fig. 6— Typical transfer characteristics.

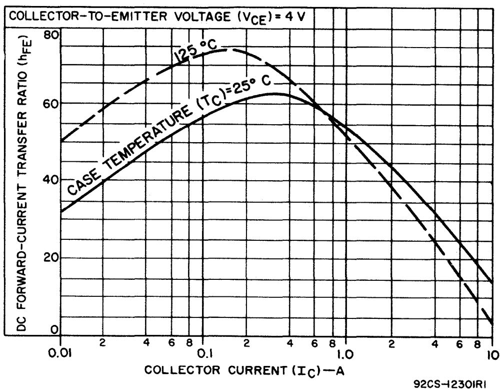


Fig. 7— Typical dc beta characteristics.

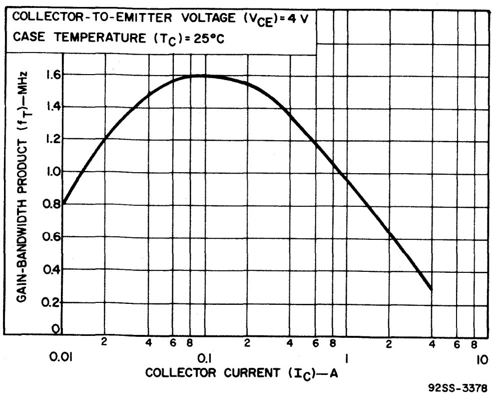


Fig. 8— Typical gain-bandwidth product.

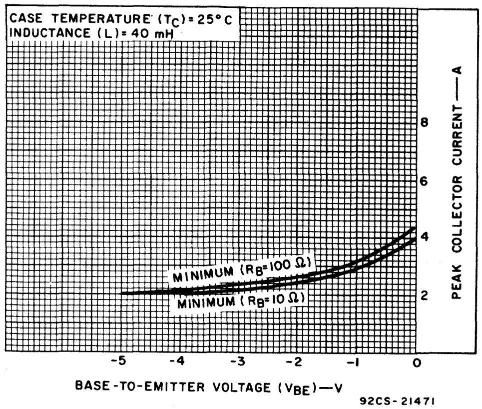


Fig. 9— Minimum reverse-bias second-breakdown characteristics.

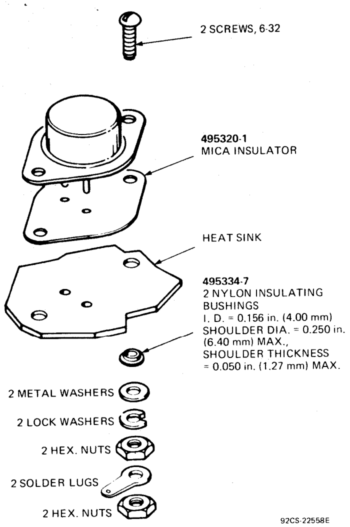
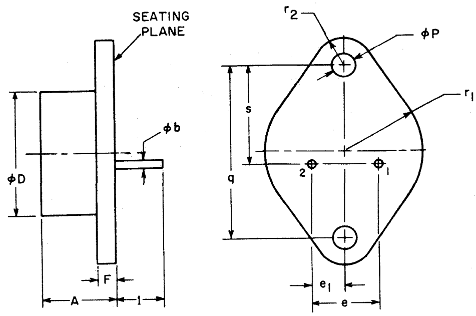


Fig. 10— Suggested mounting hardware.

For basic transistor theory, circuits, and application information, refer to "RCA Solid State Power Circuits Designer's Handbook", SP-52, or "RCA Transistor, Thyristor, & Diode Manual", SC-15.

DIMENSIONAL OUTLINE JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
φb	0.038	0.043	0.97	1.09	2
φD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
1	0.312		7.92		2
φP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r1		0.525		13.34	
r2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

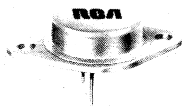
92CS–15222

TERMINAL CONNECTIONS

Pin 1 — Base
Pin 2 — Emitter
Case — Collector
Mounting Flange — Collector

RCA
Solid State
Division

Power Transistors
BD181
BD182
BD183



JEDEC TO-3

H-1570

Hometaxial-Base, High-Power Silicon N-P-N Transistors

Rugged, Broadly Applicable Devices
For Commercial Use

Features:

- **Maximum safe-area-of-operation curves**
- **Low saturation voltages**
- **High dissipation ratings**
- **Thermal-cycling rating curves**

RCA-BD181, BD182 and BD183 are silicon n-p-n transistors intended for a wide variety of high-power applications. The hometaxial-base construction of these devices renders them highly resistant to second breakdown over a wide range of operating conditions.

Applications:

- **Series and shunt regulators**
- **High-fidelity amplifiers**
- **Power-switching circuits**
- **Solenoid drivers**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		BD181	BD182	BD183	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	55	70	85	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:					
With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$	55	70	85	V
With base open	$V_{CEO}(sus)$	45	60	80	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	7	7	7	V
CONTINUOUS COLLECTOR CURRENT	I_C	15	15	15	A
CONTINUOUS BASE CURRENT	I_B	7	7	7	A
TRANSISTOR DISSIPATION:	P_T				
At case temperatures up to 25°C		117	117	117	W
At case temperatures above 25°C		← See Fig. 2 →			
TEMPERATURE RANGE:					
Storage and Operating (Junction)		← −65 to +200 →			°C
PIN TEMPERATURE (During Soldering):					
At distances ⩾ 1/32 in. (0.8 mm) from seating plane for 10 s max.		← 235 →			°C

10-73

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS						LIMITS						UNITS
		VOLTAGE V dc				CURRENT A dc		BD181		BD182		BD183		
		V_{CB}	V_{CE}	V_{EB}	V_{BE}	I_C	I_B	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Collector-Cutoff Current: With emitter open and T_C = 200°C	I_{CBO}	45 60 80					0 0 0	– – –	2 – –	– – –	– 5 –	– – –	– – 5	mA
With base-emitter junction reverse-biased	I_{CEX}		45 60 80		−1.5 −1.5 −1.5			 – –	1 – –	– – –	– 1 –	– – –	– – 1	
Emitter-Cutoff Current	I_{EBO}			7				–	5	–	5	–	5	mA
Collector-to-Emitter Sustaining Voltage: With base open	$V_{CEO}(sus)$					0.2[a]	0	45	–	60	–	80	–	
With external base-to-emitter resistance (R_{BE})=100 Ω	$V_{CER}(sus)$					0.2[a]		55	–	70	–	85	–	V
DC Forward Current Transfer Ratio	h_{FE}		4 4			4[a] 3[a]		– 20	– 70	20 –	70 –	– 20	– 70	
Base-to-Emitter Voltage	V_{BE}		4 4			3[a] 4[a]		– –	1.5 –	– –	– 1.5	– –	1.5 –	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					4[a] 3[a]	0.4[a] 0.3[a]	– –	– 1	– –	1 –	– –	– 1	V
Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 0.4 MHz)	$\|h_{fe}\|$		4			1		2	–	2	–	2	–	
Gain-Bandwidth Product	f_T					1		800	–	800	–	800	–	kHz
Common-Emitter, Short-Circuit, Small-Signal, Forward Current Transfer Ratio Cutoff Frequency	f_{hfe}		4			0.3		15	–	15	–	15	–	kHz
Forward-Bias Second Breakdown Collector Current (t ⩾ 1 s)	$I_{S/b}$		30					3.95	–	3.95	–	3.95	–	A
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$							–	1.5	–	1.5	–	1.5	°C/W

[a] Pulsed: Pulse duration = 300 μs, duty factor = 1.8%.

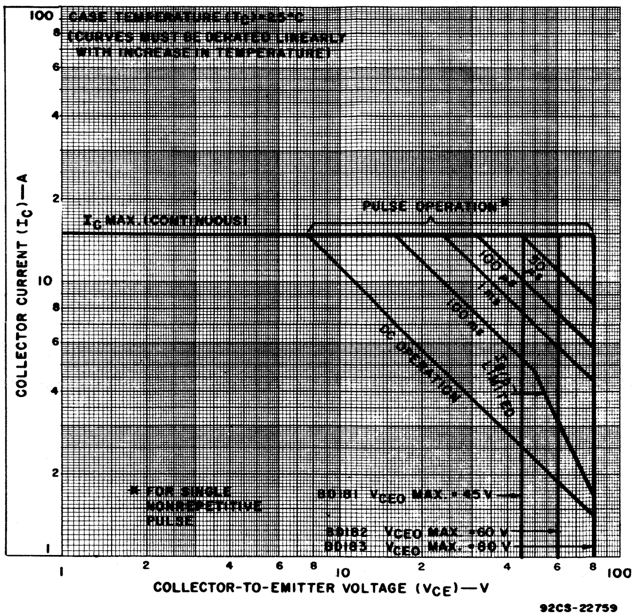


Fig. 1 — Maximum operating areas for all types.

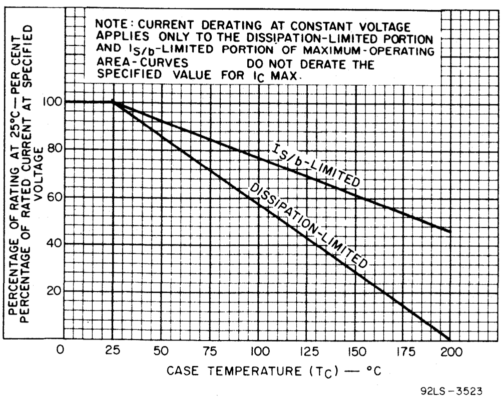


Fig. 2 — Dissipation and $I_{S/b}$ derating of all types.

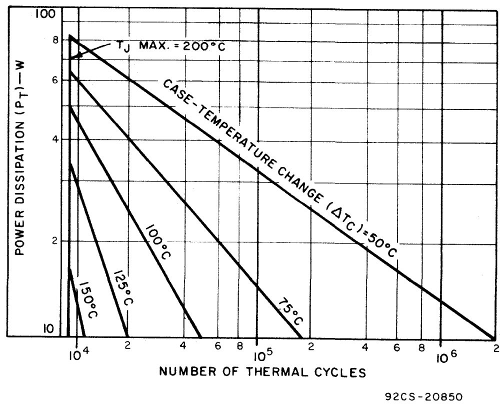


Fig. 3 — Thermal cycling rating chart for all types.

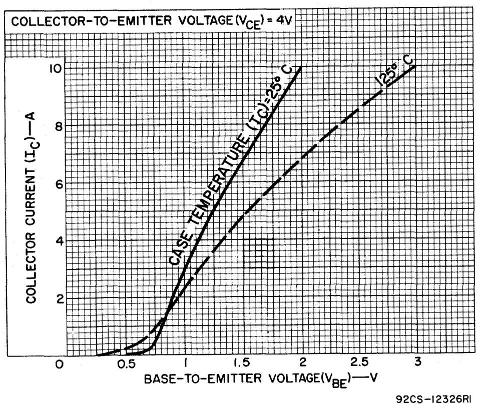


Fig. 4 — Typical transfer characteristics for all types.

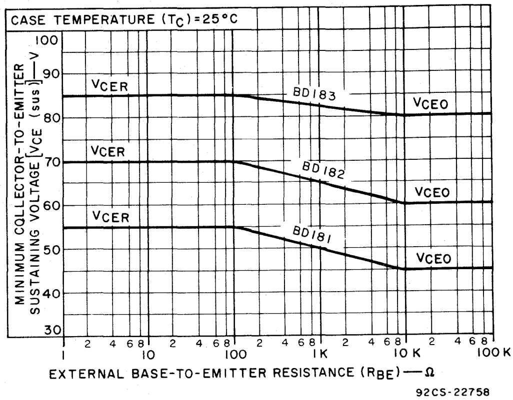


Fig. 5 — Sustaining voltage vs. base-to-emitter resistance for all types.

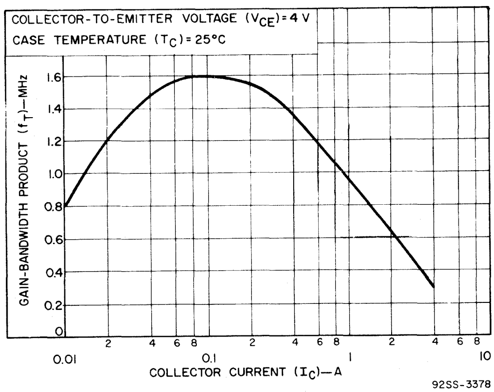


Fig. 6 — Typical gain-bandwidth product for all types.

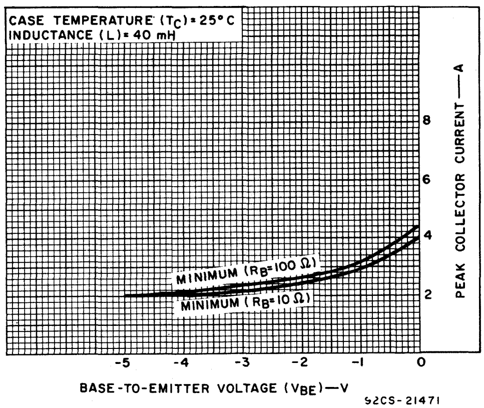


Fig. 7 — Minimum reverse-bias second-breakdown characteristics for all types.

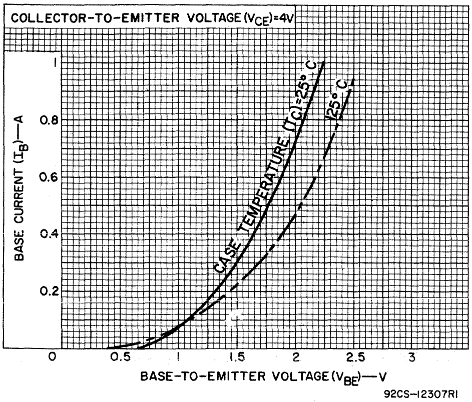


Fig. 8 – Typical input characteristics for BD182.

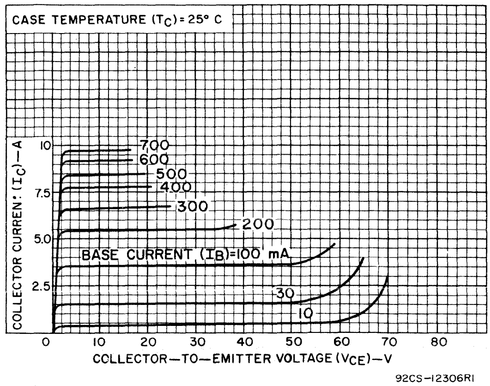


Fig. 9 – Typical output characteristics for BD182.

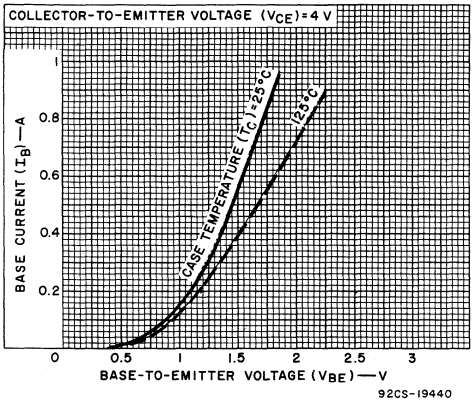


Fig. 10 – Typical input characteristics for BD181 and BD183.

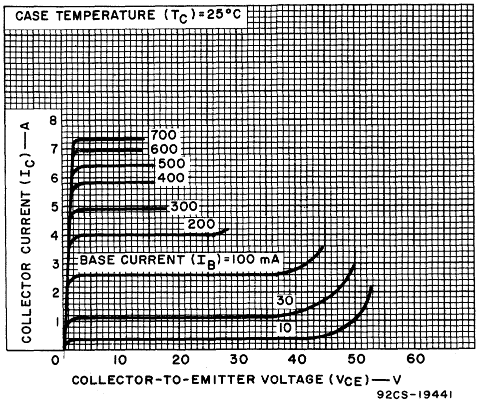


Fig. 11 – Typical output characteristics for BD181 and BD183.

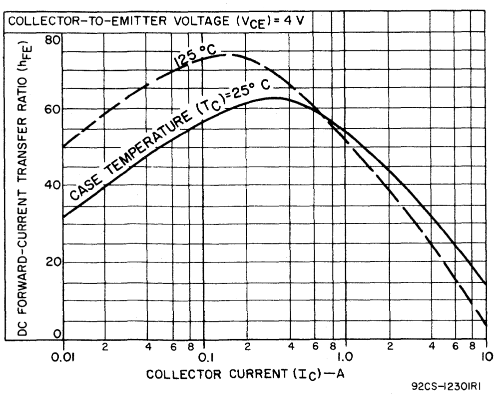


Fig. 12 – Typical dc-beta characteristics for BD182.

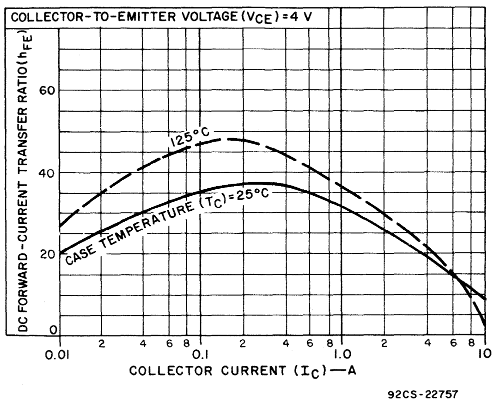
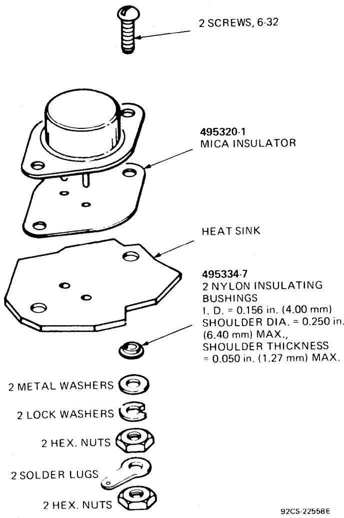


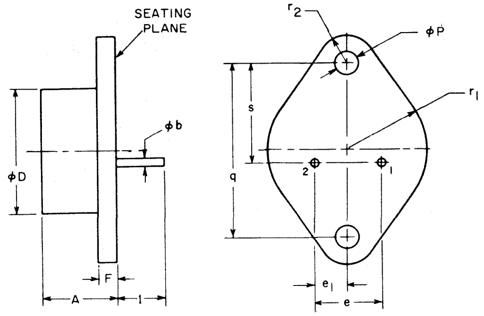
Fig. 13 – Typical dc-beta characteristics for BD181 and BD183.



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 14 — Suggested mounting hardware.

DIMENSIONAL OUTLINE JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
φb	0.038	0.043	0.97	1.09	2
φD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e_1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
l	0.312		7.92		2
φP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r_1		0.525		13.34	
r_2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS—15222

For basic transistor theory, circuits, and application information, refer to "RCA Solid State Power Circuits Designer's Handbook", SP-52, or "RCA Transistor, Thyristor, & Diode Manual", SC-15.

TERMINAL CONNECTIONS

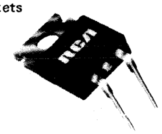
Pin 1 — Base
Pin 2 — Emitter
Case — Collector
Mounting Flange — Collector

RCA
Solid State
Division

Power Transistors

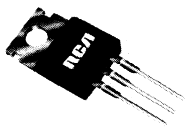
2N6098 2N6099 2N6100 2N6101 2N6102 2N6103

For TO-66 Sockets



2N6098
2N6100
2N6102

JEDEC TO-220AA H1534R1



2N6099
2N6101
2N6103

JEDEC TO-220AB H1535R1

High-Current, Silicon N-P-N VERSAWATT Transistors

Designed for Medium-Power Linear and Switching Service in Consumer, Automotive, and Industrial Applications

Features:

- **Low saturation voltage —**
  V_{CE}(sat) = 1 V max. at I_C = 4 A (2N6098, 2N6099)
  = 1 V max. at I_C = 5 A (2N6100, 2N6101)
  = 1 V max. at I_C = 8 A (2N6102, 2N6103)
- **VERSAWATT package (molded-silicone plastic)**
- **Maximum safe-area-of-operation curves**
- **Thermal-cycle rating curve**

These RCA types are hometaxial-base silicon n-p-n transistors. Types 2N6098, 2N6100, and 2N6102 have formed emitter and base leads for easy insertion into TO-66 sockets. Types 2N6099, 2N6101, and 2N6103 are electrically identical to the 2N6098, 2N6100, and 2N6102, respectively.

These new VERSAWATT-package transistors differ in voltage ratings and in the currents at which the parameters are controlled. They are intended for a wide variety of medium-power switching and linear applications, such as series and shunt regulators, solenoid drivers, motor-speed controls, inverters, and driver and output stages of high-fidelity amplifiers.

*Formerly RCA Dev. Nos. TA7381-86, inclusive.

OPTIONAL LEAD CONFIGURATION

An additional lead forming for printed-circuit board mounting is also available. (See page 8).
Please submit requirements to your RCA Technical Sales Representative, or write to RCA Linear Power Marketing, Somerville, N.J. 08876.

Maximum Ratings, *Absolute-Maximum Values:*

		2N6102 2N6103	2N6098 2N6099	2N6100 2N6101	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	45	70	80	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:					
With external base-to-emitter resistance (R_{BE}) = 100Ω	V_{CER}(sus)	45	65	75	V
* With base open	V_{CEO}(sus)	40	60	70	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	8	8	V
*COLLECTOR CURRENT (Continuous)	I_C	16	10	10	A
*BASE CURRENT	I_B	4	4	4	A
TRANSISTOR DISSIPATION:	P_T				
* At case temperatures up to 25°C		75	75	75	W
At ambient temperatures up to 25°C		1.8	1.8	1.8	W
* At case temperatures above 25°C, derate linearly		← 0.6 →			W/°C
At ambient temperatures above 25°C, derate linearly		← 0.0144 →			W/°C
*TEMPERATURE RANGE:					
Storage & Operating (Junction)		← -65 to 150 →			°C
*LEAD TEMPERATURE (During Soldering):					
At distance ≥ 1/8 in. (3.17 mm) from case of 10 s max		← 235 →			°C

*In accordance with JEDEC registration data format JS-6 RDF-2.

ELECTRICAL CHARACTERISTICS, Case Temperature (T_C) = 25°C Unless Otherwise Specified

Characteristic	Symbol	TEST CONDITIONS: DC Collector Voltage (V) V_{CE}	DC Emitter Voltage (V) V_{EB}	DC Current (A) I_C	DC Current (A) I_B	LIMITS 2N6102 2N6103 Min.	2N6102 2N6103 Max.	2N6098 2N6099 Min.	2N6098 2N6099 Max.	2N6100 2N6101 Min.	2N6100 2N6101 Max.	Units
* Collector-Cutoff Current	I_{CEX}	40	1.5			-	2	-	-	-	-	mA
		65	1.5			-	-	-	2	-	-	
		75	1.5			-	-	-	-	-	2	
With base-emitter junction reverse biased	I_{CEX} (T_C=150°C)	40	1.5			-	10	-	-	-	-	
		65	1.5			-	-	-	10	-	-	
		75	1.5			-	-	-	-	-	10	
With base open	I_{CEO}	30			0	-	2	-	-	-	-	mA
		50			0	-	-	-	2	-	-	
		60			0	-	-	-	-	-	2	
* Emitter-Cutoff Current	I_{EBO}		5			-	1	-	-	-	-	mA
			8			-	-	-	1	-	1	
Collector-to-Emitter Sustaining Voltage: With external base-to-emitter resistance (R_{BE}) = 100Ω[a]	$V_{CER}(sus)$			0.2		45	-	65	-	75	-	V
* With base open[a]	$V_{CEO}(sus)$			0.2	0	40	-	60	-	70	-	
* DC Forward-Current Transfer Ratio[a]	h_{FE}	4		4		-	-	20	80	-	-	
		4		5		-	-	-	-	20	80	
		4		8		15	60	-	-	-	-	
		4		10		–	-	5	-	5	-	
		4		16		5	-	-	-	-	-	
* Base-to-Emitter Voltage[a]	V_{BE}	4		4		-	-	-	1.7	-	-	V
		4		5		-	-	-	-	-	1.7	
		4		8		-	1.7	-	-	-	-	
* Collector-to-Emitter Saturation Voltage[a]	$V_{CE}(sat)$			10	2	-	-	-	2.5	-	2.5	V
				16	3.2	-	2.5	-	-	-	-	
* Common-Emitter, small-signal short-circuit, forward current transfer ratio	h_{fe}	4	f=1kHz	0.5		15	-	15	-	15	-	
* Magnitude of common-emitter, small-signal, short circuit, forward current transfer ratio	$\|h_{fe}\|$	4	f=0.1MHz	0.5		8	28	8	28	8	28	
Thermal Resistance: Junction-to-Case	$\theta_{J\text{-}C}$					-	1.67	-	1.67	-	1.67	°C/W
Junction-to-Ambient	$\theta_{J\text{-}A}$					-	70	-	70	-	70	

*In accordance with JEDEC registration data format (JS-6, RDF-2)

[a]Pulsed, pulse duration = 300 μs, duty factor = 0.018

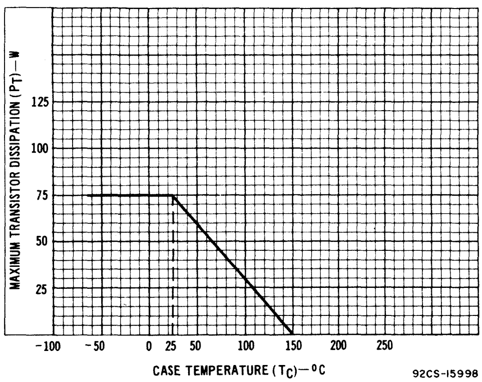


Fig.1—Derating curve for all types.

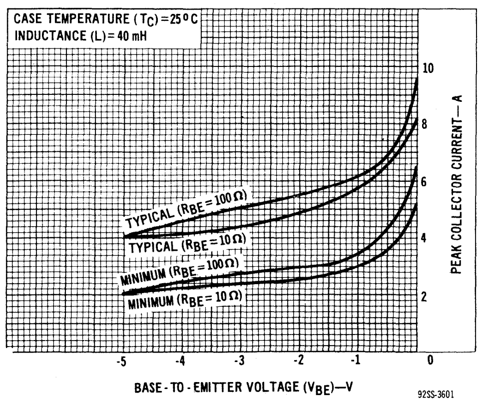


Fig.2—Reverse-bias, second-breakdown characteristics for all types.

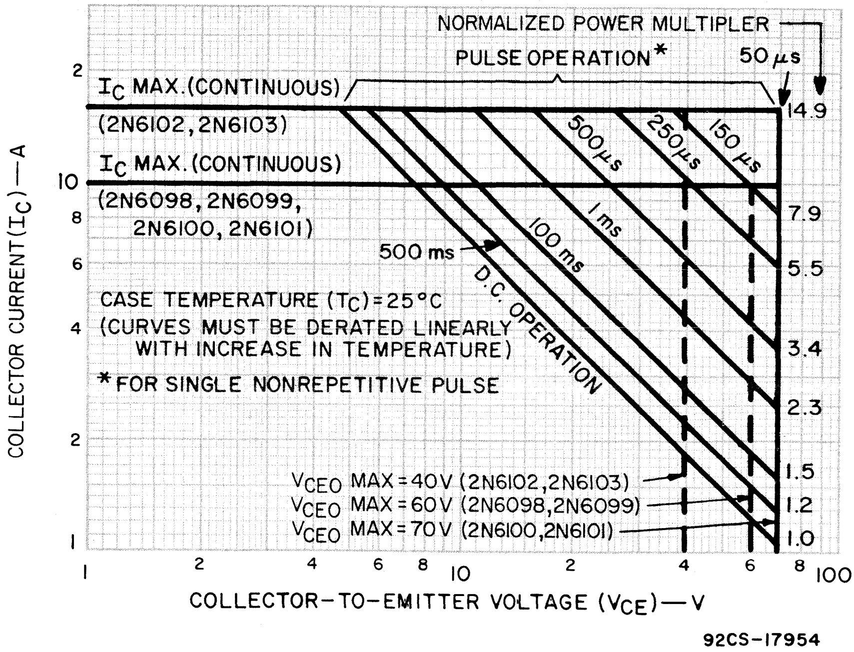


Fig.3—Maximum safe operating areas for all types.

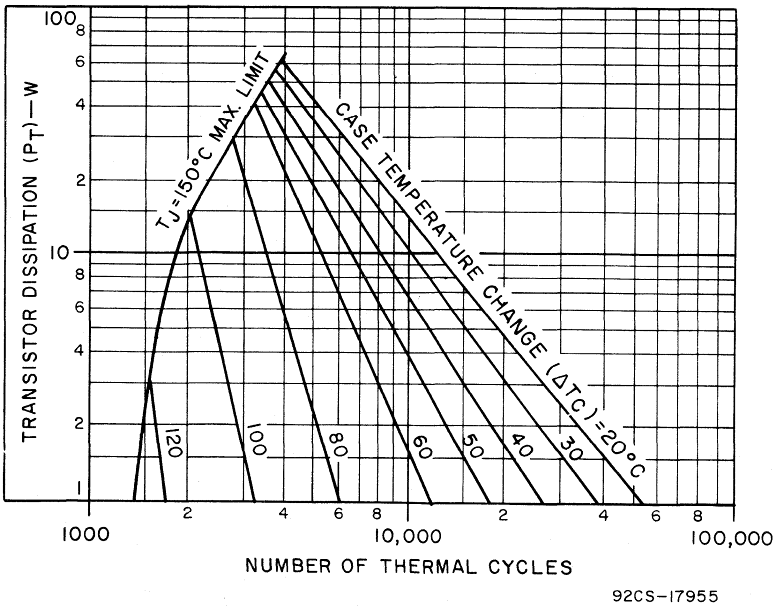


Fig.4—Thermal-cycling rating for all types.

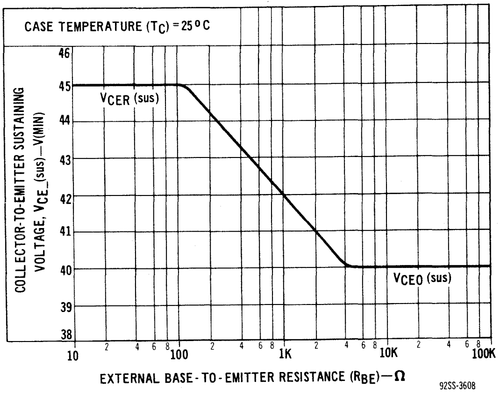


Fig.5—Sustaining voltage vs. base-to-emitter resistance for types 2N6102 & 2N6103.

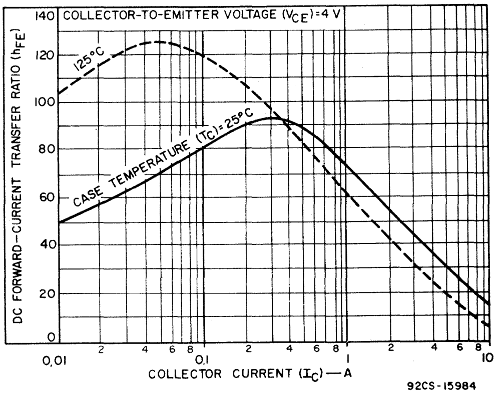


Fig.6—Typical dc beta characteristics for types 2N6102 & 2N6103.

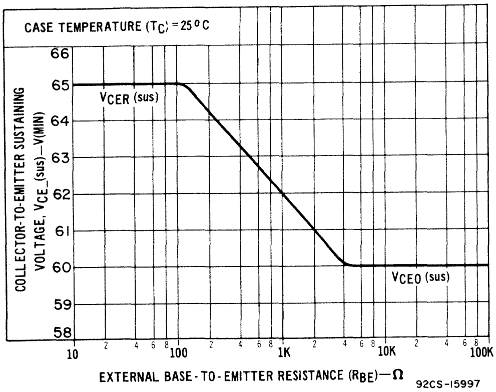


Fig.7—Sustaining voltage vs. base-to-emitter resistance for types 2N6098 & 2N6099.

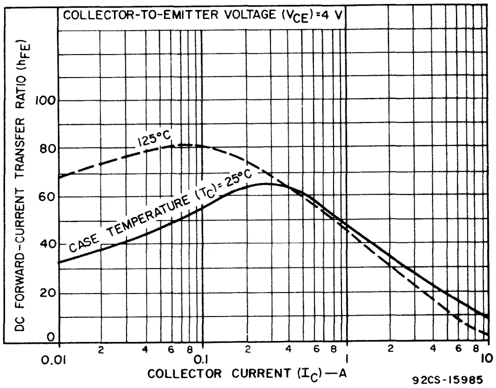


Fig.8—Typical dc-beta characteristics for types 2N6098 & 2N6099.

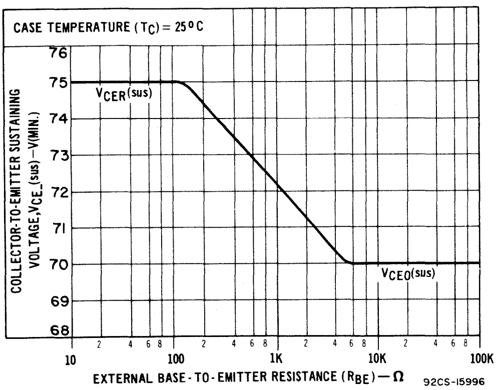


Fig.9—Sustaining voltage vs. base-to-emitter resistance for types 2N6100 & 2N6101.

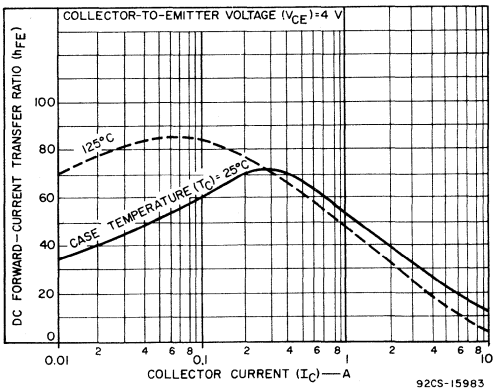


Fig.10—Typical dc beta characteristics for types 2N6100 & 6101.

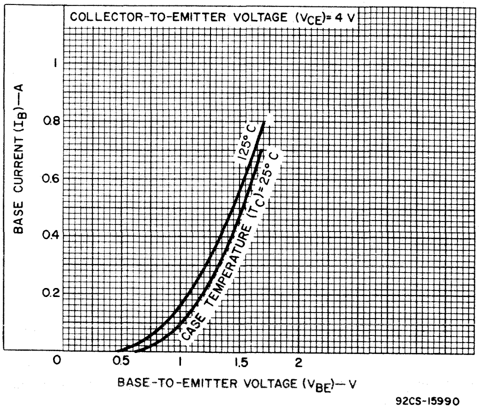


Fig. 11—Typical input characteristics for types 2N6102 & 2N6103.

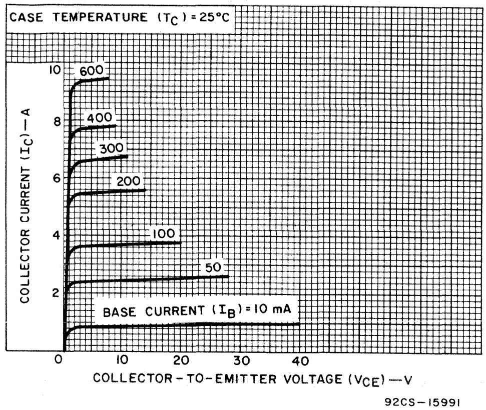


Fig. 12—Typical output characteristics for types 2N6102 & 2N6103.

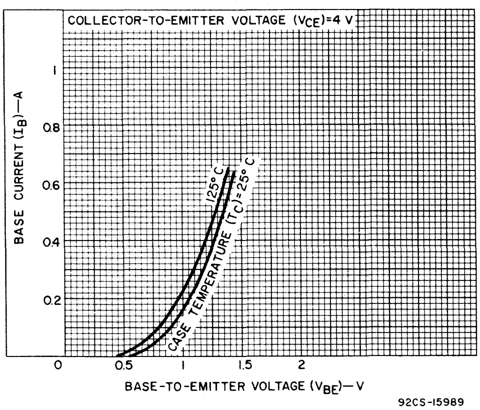


Fig. 13—Typical input characteristics for types 2N6098 & 2N6099.

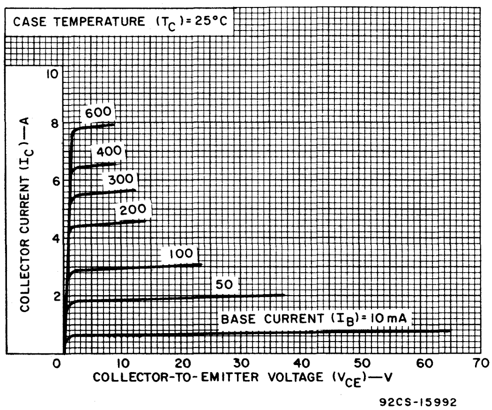


Fig. 14—Typical output characteristics for types 2N6098 & 2N6099.

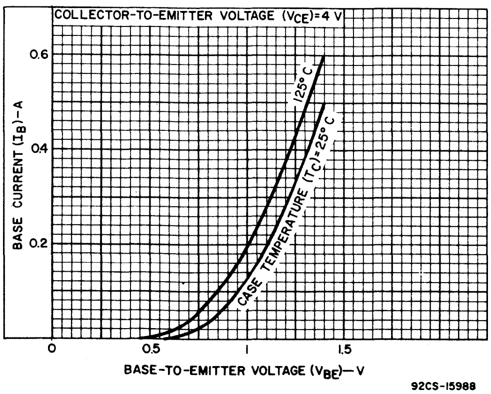


Fig. 15—Typical input characteristics for types 2N6100 & 2N6101.

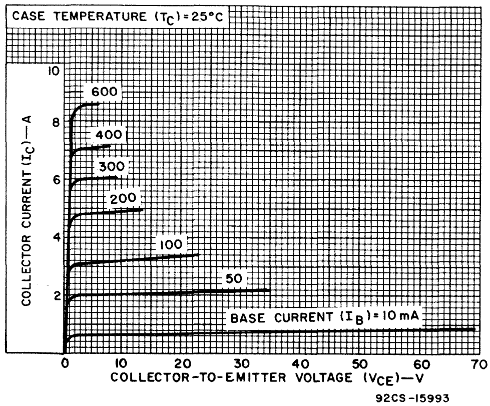


Fig. 16—Typical output characteristics for types 2N6100 & 2N6101.

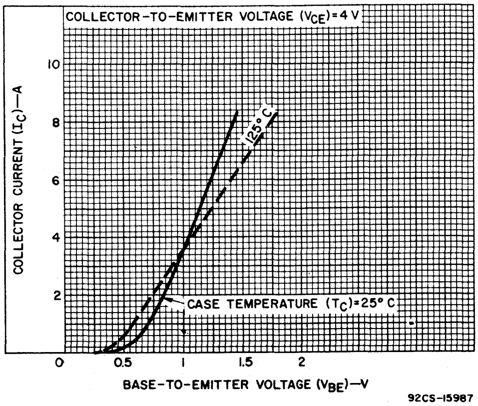


Fig. 17—Typical transfer characteristics for all types.

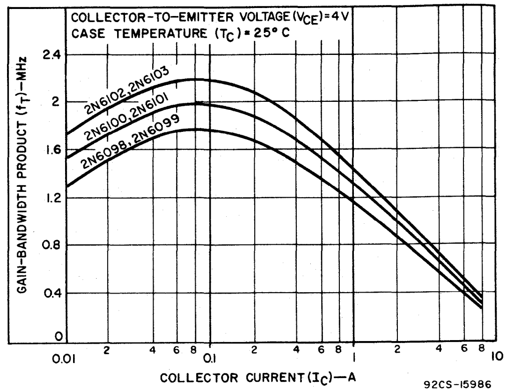


Fig. 18—Typical gain-bandwidth product for all types.

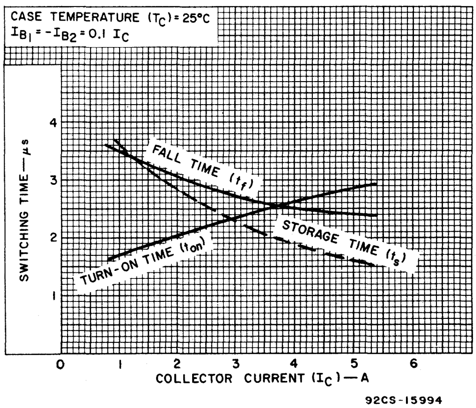
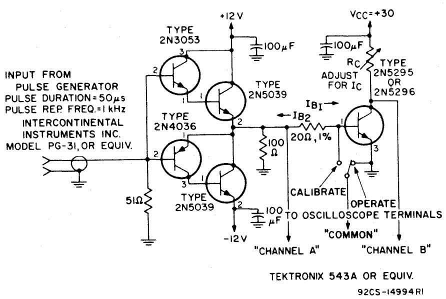


Fig. 19—Typical saturated switching characteristics for all types.



NOTE: Collector-terminal connection for transistor under test is mounting-flange (2N6098, 2N6100, 2N6102), lead No. 3 (2N6099, 2N6101, 2N6103).

Fig. 20—Circuit used to measure switching times for all types.

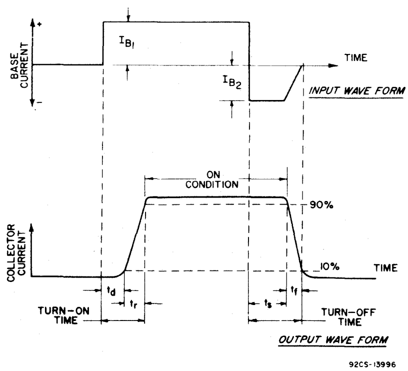
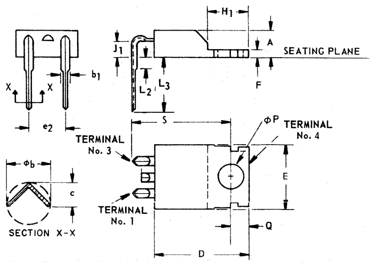


Fig. 21—Phase relationship between input current and output current showing reference points for specification of switching times. (Test circuit shown in Fig. 20).

DIMENSIONAL OUTLINE FOR TYPES 2N6098, 2N6100, 2N6102



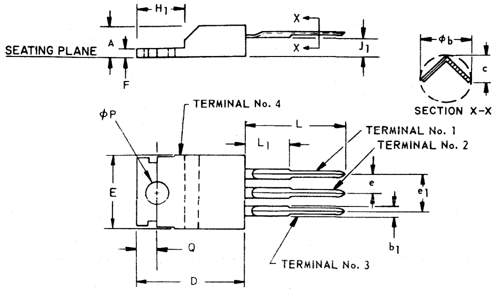
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
ϕb	0.02	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e_2	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L_2	–	0.050	–	1.27	–
L_3	0.360	0.422	9.15	10.71	–
ϕP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–
S	0.580	0.610	14.74	15.49	–

92CS-17990R1

NOTES:

1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.050 – 0.055 (1.27 – 1.40 mm) below seating plane.

DIMENSIONAL OUTLINE FOR TYPES 2N6099, 2N6101, 2N6103



BOTTOM VIEW

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
ϕb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
ϕP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

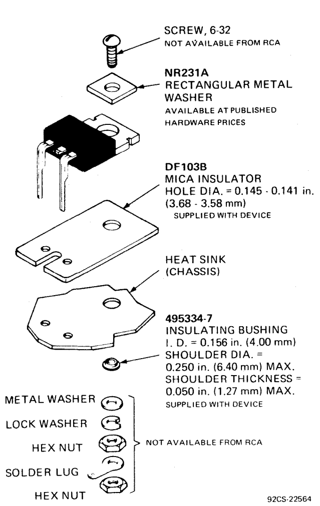
1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

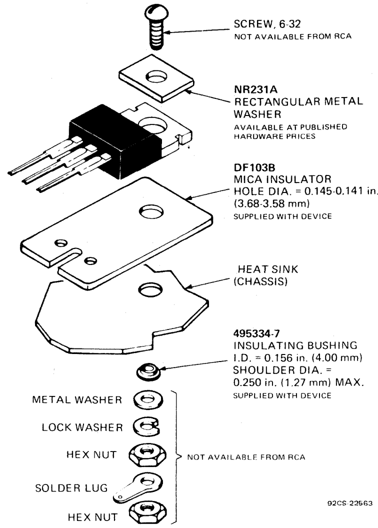
TERMINAL CONNECTIONS FOR TYPES 2N6098, 2N6100, 2N6102

Terminal No. 1-Base
Terminal No. 3-Emitter
Terminal No. 4-Collector

TERMINAL CONNECTIONS FOR TYPES 2N6099, 2N6101, 2N6103

Terminal No. 1-Base
Terminal No. 2-Collector
Terminal No. 3-Emitter
Terminal No. 4-Collector





In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.22—Suggested mounting hardware for types 2N6098, 2N6100 & 2N6102.

Fig.23—Suggested mounting hardware for types 2N6099, 2N6101 & 2N6103.

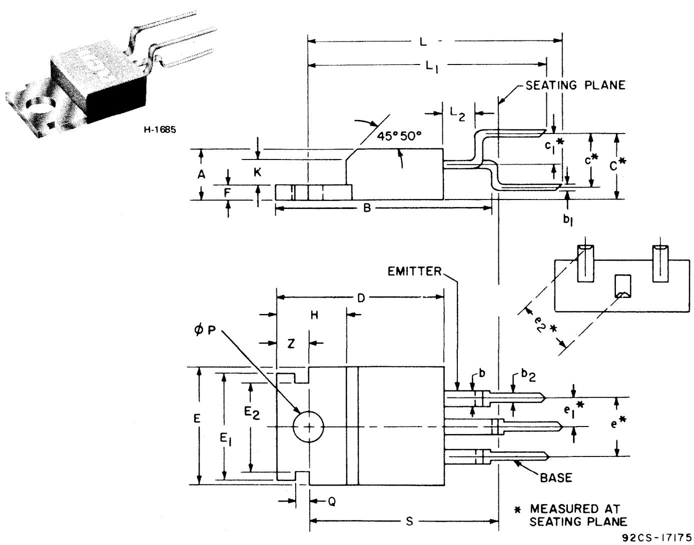


Fig.24—Dimensional outline of VERSAWATT transistor package designed for mounting on printed-circuit boards.

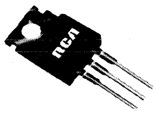
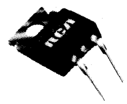
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.140	0.190	3.56	4.82
B	–	0.850	–	21.59
b	0.045	0.070	1.15	1.17
b_1	0.015	0.030	0.382	0.762
b_2	0.020	0.038	0.508	0.965
C	0.230	0.270	5.85	6.85
c	0.180	0.220	4.58	5.58
c_1	0.130	0.170	3.31	4.31
D	0.560	0.625	14.23	15.87
E	0.330	0.420	8.39	10.41
E_1	0.365	0.385	9.28	9.77
E_2	0.300	0.320	7.62	8.12
e	0.190	0.210	4.83	5.33
e_1	0.090	0.110	2.29	2.79

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
e_2	0.203	0.243	5.16	6.17
F	0.045	0.055	1.15	1.39
H	0.230	0.270	5.85	6.85
K	0.080	0.085	2.032	2.159
L	0.993	1.033	25.22	26.23
L_1	0.895	0.935	22.73	23.74
L_2	0.070	0.090	1.78	2.28
ϕP	0.139	0.147	3.531	3.734
Q	0.040	0.060	1.02	1.52
S	0.655	0.685	16.64	17.39
Z	0.100	0.120	2.54	3.04

RCA Solid State Division

Power Transistors

BD278

 BD278 TO-220AB	 Also Available TO-220AA

High-Current Silicon N-P-N VERSAWATT Transistor

For Medium-Power Linear and Switching Service in Consumer, Automotive, and Industrial Applications

Features:

- **Low saturation voltage:** $V_{CE}(sat)$ = 1 V max. at I_C = 4 A
- **VERSAWATT package (molded-silicone plastic)**
- **Maximum-safe-area-of-operation curve**
- **Thermal-cycling rating curve**

Type BD278 is a hometaxial-base silicon n-p-n transistor supplied in the JEDEC TO-220AB straight-lead VERSAWATT package. It is also available in the TO-220AA package (leads formed to fit a TO-66 socket); to order this version, specify formed lead No. 6201.

The BD278 is intended for a wide variety of medium-power switching and linear applications such as series regulators, shunt regulators, solenoid drivers, motor-speed controls, inverters, output stages for high-fidelity amplifiers, and power-supply and vertical-deflection circuits for monochrome and color TV.

Maximum Ratings, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	55	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:			
With external base-to-emitter resistance (R_{BE}) = 100Ω	$V_{CER}(sus)$	55	V
With base open	$V_{CEO}(sus)$	45	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	V
COLLECTOR CURRENT (Continuous)	I_C	10	A
BASE CURRENT	I_B	4	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25°C		75	W
At ambient temperatures up to 25°C		1.8	W
At case temperatures above 25°C, derate linearly		0.6	W/°C
At ambient temperatures above 25°C, derate linearly		0.0144	W/°C
TEMPERATURE RANGE:			
Storage & Operating (Junction)		−65 to 150	°C
LEAD TEMPERATURE (During Soldering):			
At distance ≥ 1/8 in. (3.17 mm) from case for 10 s max		235	°C

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25°C unless specified otherwise

CHARACTERISTIC	SYMBOL	TEST CONDITIONS VOLTAGE V dc		CURRENT A dc		LIMITS		UNITS
		V_{CE}	V_{EB}	I_C	I_B	MIN.	MAX.	
Collector Cutoff Current: With base-to-emitter junction reverse-biased	I_{CEX}	55	1.5			–	2	mA
With base-to-emitter junction reverse-biased and T_C = 150°C	I_{CEX}	50	1.5			–	10	mA
With base open	I_{CEO}	30			0	–	2	mA
Emitter Cutoff Current	I_{EBO}		5			–	5	mA
Collector-to-Emitter Sustaining Voltage: With external base-to-emitter resistance (R_{BE}) = 100 Ω[a]	V_{CER}(sus)			0.2		55	–	V
With base open[a]	V_{CEO}(sus)			0.2	0	45	–	V
DC Forward-Current Transfer Ratio[a]	h_{FE}	4		4		15	75	
Base-to-Emitter Voltage[a]	V_{BE}	4		4		–	1.8	V
Collector-to-Emitter Saturation Voltage[a]	V_{CE}(sat)			4	0.4	–	1.0	V
Common-Emitter Small-Signal Short-Circuit Forward-Current Transfer Ratio (f = 1 kHz)	h_{fe}	4		0.5		15	–	
Magnitude of Common-Emitter Small-Signal Short-Circuit Forward-Current Transfer Ratio (f = 0.1 MHz)	$\|h_{fe}\|$	4		0.5		8	28	
Forward-Bias Second-Breakdown Collector Current (t = 0.5 s)	$I_{S/b}$	40				1.87	–	A
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$					–	1.67	°C/W
Junction-to-Ambient	$R_{\theta JA}$					–	70	°C/W

[a] Pulsed, pulse duration = 300 μs, duty factor = 0.018.

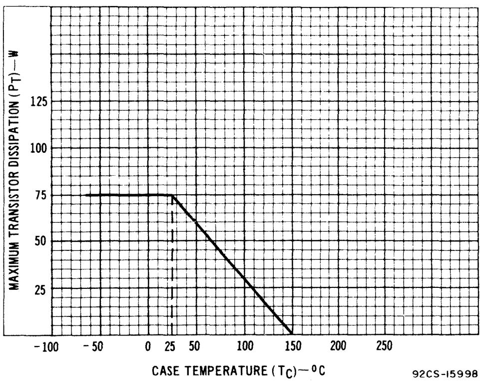


Fig.1 — Derating curve.

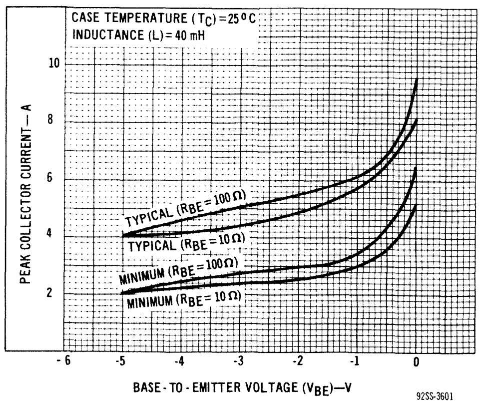


Fig.2 — Reverse-bias second-breakdown characteristics.

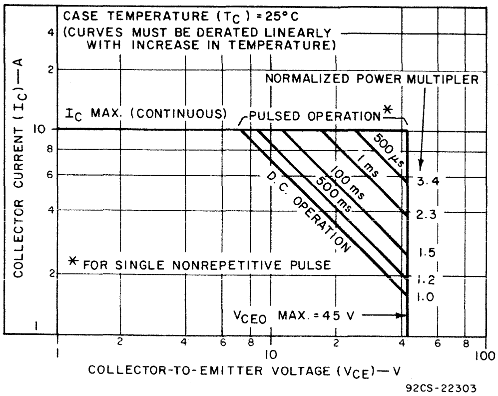


Fig.3 — Maximum safe operating area.

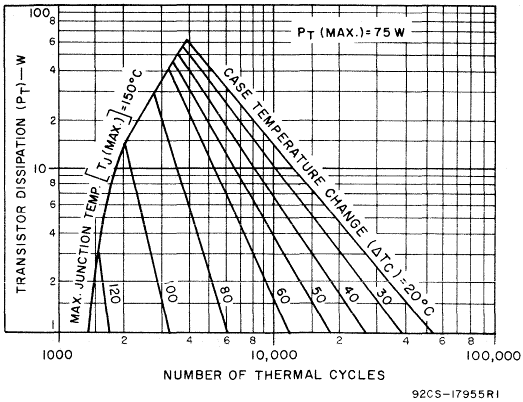


Fig.4 — Thermal-cycling ratings.

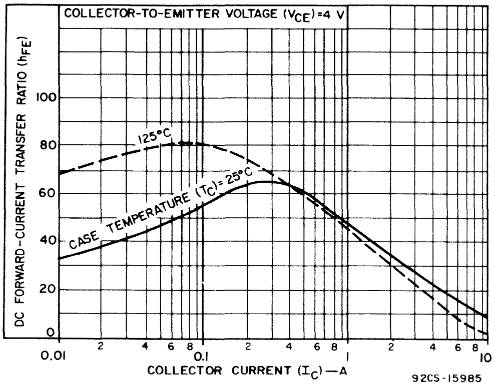


Fig.5 — Typical dc beta characteristics.

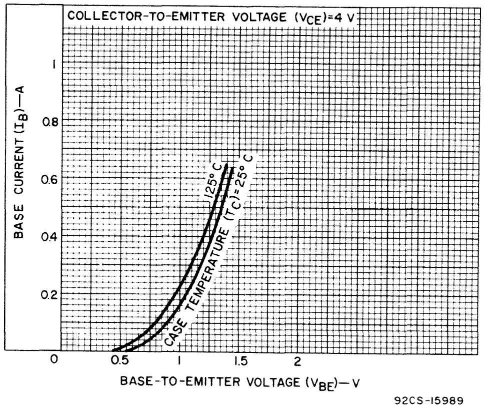


Fig.6 — Typical input characteristics.

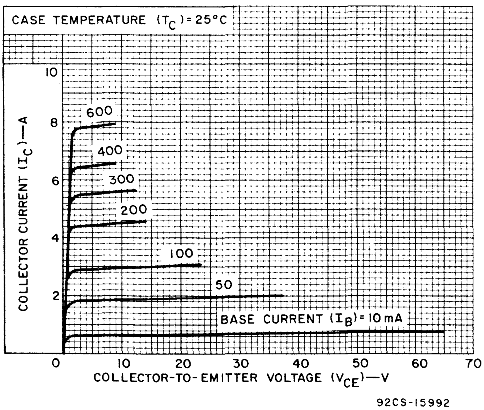


Fig.7 — Typical output characteristics.

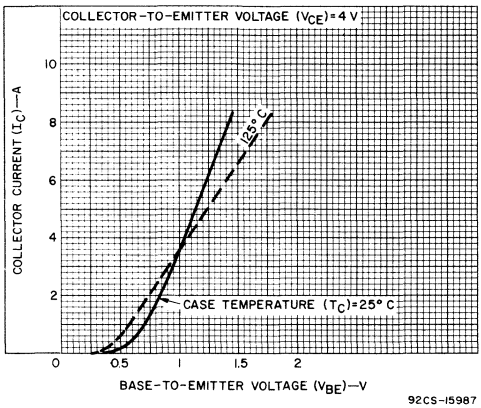
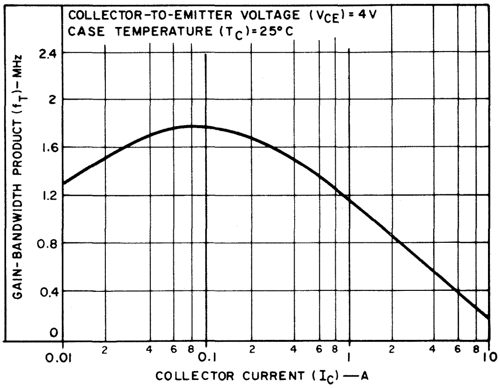


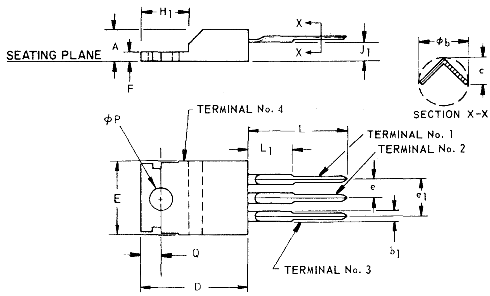
Fig.8 — Typical transfer characteristics.



92CS-21469

Fig.9 — Typical gain-bandwidth product.

DIMENSIONAL OUTLINE JEDEC TO-220AB



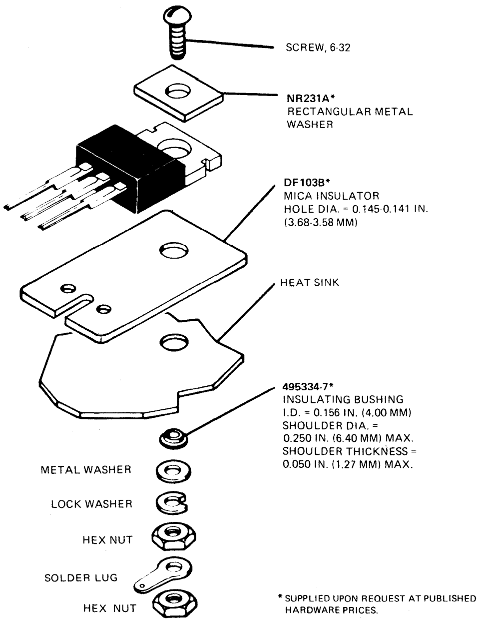
Bottom View

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
ϕb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
ϕP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in.(6.35 – 6.48 mm) from case.



92CS-17182R3

Fig.10 — Suggested mounting hardware for JEDEC TO-220AB.

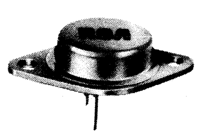
TERMINAL CONNECTIONS

Terminal No.1 — Base
Terminal No.2 — Collector
Terminal No.3 — Emitter
Terminal No.4 — Collector

RCA

Solid State
Division

Power Transistors 2N6262 2N4347 2N3442



JEDEC TO-3 H-1570

Hometaxial II• High-Voltage Silicon N-P-N Transistors

Rugged High-Power Devices for Applications in Industrial and Commercial Equipment

Features:

- **Low saturation voltages**
- **Thermal-cycle rating charts**
- **High dissipation capability – 100 W (2N4347)**
  – 117 W (2N3442)
  – 150 W (2N6262)
- **Maximum area-of-operation curves for dc and pulse operation.**

RCA 2N3442, 2N4347, and 2N6262 are hometaxial-base●, silicon n-p-n transistors intended for a wide variety of high-power, high-voltage applications. Typical applications for these transistors include power-switching circuits, audio amplifiers, series- and shunt-regulator driver and output stages, dc-to-dc converters, inverters, and solenoid (hammer)/relay driver service.

These devices employ the popular JEDEC TO-3 package; they differ in maximum ratings for voltage, current, and power.

Applications:

- **Series and shunt regulators**
- **High-fidelity amplifiers**
- **Power-switching circuits**

● "Hometaxial" was coined by RCA from "homogeneous" and "axial" to describe a single-diffused transistor with a base region of homogeneous-resistivity silicon in the axial direction (emitter-to-collector). "Hometaxial II" is a term used to describe RCA's expanded line of transistors produced by the hometaxial process.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N4347	2N3442	2N6262	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	140	160	170	V
COLLECTOR-TO-EMITTER VOLTAGE:					
* With base open	V_{CEO}	120	140	150	V
With reverse bias (V_{BE}) of –1.5 V	V_{CEX}	140*	160	170	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	7	7	7	V
*COLLECTOR CURRENT:	I_C				
Continuous		5	10	10	A
Peak		10*	15	15	A
*BASE CURRENT:	I_B				
Continuous		3	7	7	A
Peak		8*	–	–	A
*TRANSISTOR DISSIPATION:	P_T				
At case temperature up to 25°C		100	117	150	W
At case temperatures above 25°C		← See Figs. 1, 4, 7, & 22 →			
*TEMPERATURE RANGE:					
Storage & Operating (Junction)		← –65 to +200 →			°C
*PIN TEMPERATURE (During Soldering):					
At distances ≥1/32 in. (0.8 mm) from case for 10 s max.		235	235	235	°C

*In accordance with JEDEC registration data format (JS-6, RDF-2).

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ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS							LIMITS						UNITS
		DC Collector Voltage (V)		DC Emitter or Base Voltage (V)		DC Current (A)			Type 2N4347		Type 2N3442		Type 2N6262		
		V_{CB}	V_{CE}	V_{EB}	V_{BE}	I_C	I_E	I_B	Min.	Max.	Min.	Max.	Min.	Max.	
Collector-Cutoff Current: With emitter open	I_{CBO}	140					0		–	–	–	1*	–	1	mA
* With base-emitter junction reverse-biased	I_{CEX}		120		−1.5				–	2	–	–	–	–	mA
			140		−1.5				–	–	–	5	–	–	
			150		−1.5				–	–	–	–	–	0.1	
* With base-emitter junction reverse-biased and T_C = 150°C	I_{CEX}		125		−1.5				–	10	–	–	–	–	mA
			140		−1.5				–	–	–	30	–	–	
			150		−1.5				–	–	–	–	–	2	
* With base open	I_{CEO}		100						–	200	–	–	–	–	mA
			110						–	–	–	–	–	1	
			140						–	–	–	200	–	–	
* Emitter-Cutoff Current	I_{EBO}			7		0			–	5	–	5	–	0.2	mA
* DC Forward Current Transfer Ratio	h_{FE}		2			3^a			–	–	–	–	20	70	
			2			10^a			–	–	–	–	5	–	
			4			2^a			15	60	–	–	–	–	
			4			3^a			–	–	20	70	–	–	
			4			5^a			10	–	–	–	–	–	
			4			10^a			–	–	7.5	–	–	–	
Collector-to-Emitter Sustaining Voltage: With base-emitter junction reverse-biased	$V_{CEV}(sus)$				−1.5	0.1			140	–	160	–	–	–	V
					−1.5	0.2			–	–	–	–	170	–	
With external base-to-emitter resistance (R_{BE}) = 100Ω	$V_{CER}(sus)$					0.1			130	–	–	–	–	–	V
						0.2			–	–	150	–	160	–	
* With base open	$V_{CEO}(sus)$					0.2^a		0	120	–	140	–	–	–	V
						0.2^a		0	–	–	–	–	150	–	
* Base-to-Emitter Voltage	V_{BE}		2			3^a			–	–	–	–	–	1	V
			4			3^a			–	–	–	1.7	–	–	
			4			2^a			–	2	–	–	–	–	
			4			5^a			–	3	–	–	–	–	
			4			10^a			–	–	–	5.7	–	–	
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					2^a		0.2	–	1	–	–	–	–	V
						3^a		0.3	–	–	–	1	–	0.5	
						5^a		0.63	–	2	–	–	–	–	
						10^a		2	–	–	–	5	–	–	
Power Rating Test	PRT		67			1.5			1	–	–	–	–	–	s
			78			1.5			–	–	1	–	–	–	
			100			1.5			–	–	–	–	1	–	
* Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio: f = 50 kHz	$\|h_{fe}\|$		4			0.5			40	–	–	–	–	–	
f = 40 kHz	$\|h_{fe}\|$		4			1			–	–	–	–	2	–	
			4			2			–	–	2	–	–	–	
* Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 1 kHz)	h_{fe}		4			0.5			40	–	–	–	–	–	
			4			1			–	–	–	–	10	–	
			4			2			–	–	12	72	–	–	
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$								–	1.75	–	1.5	–	1.17	°C/W

*In accordance with JEDEC registration data format JS-6 RDF-2.

[a] Pulse test; pulse duration = 300 μs, rep. rate = 60 Hz

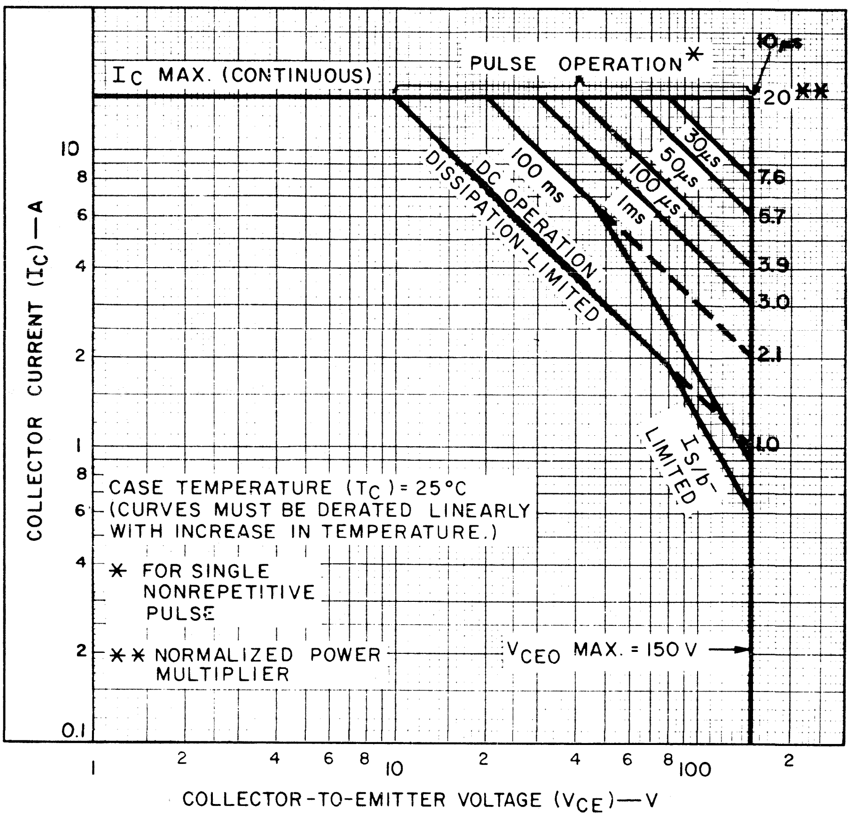


Fig. 1—Maximum operating areas for type 2N6262.

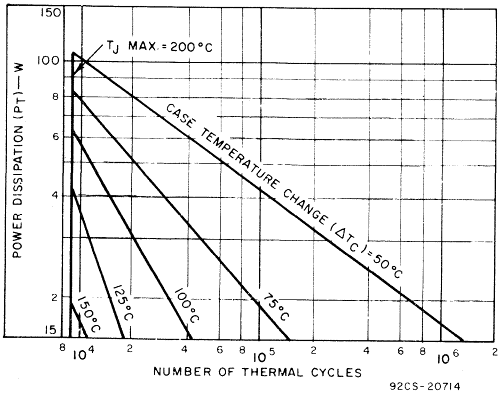


Fig.2—Thermal-cycle rating chart for type 2N6262.

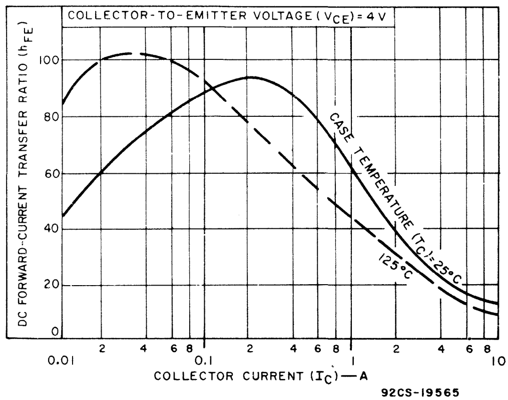


Fig.3—Typical dc beta characteristics for type 2N6262.

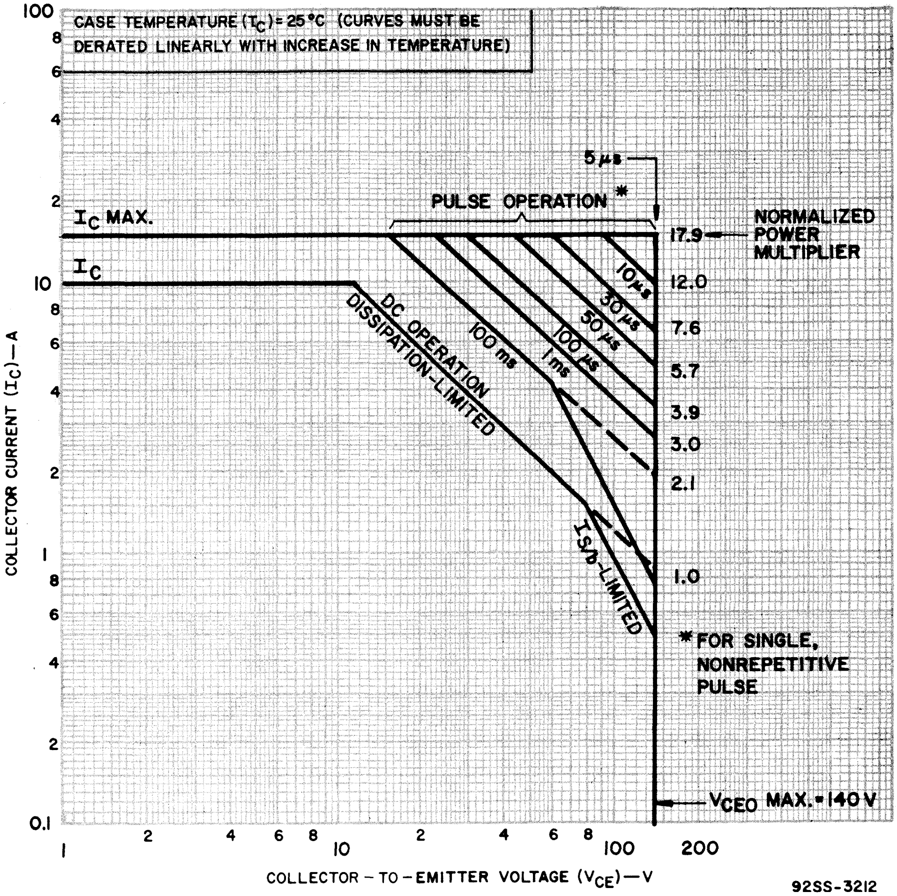


Fig.4— Maximum operating areas for type 2N3442.

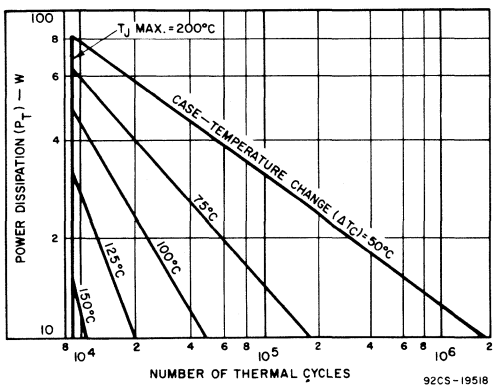


Fig.5— Thermal-cycle rating chart for type 2N3442.

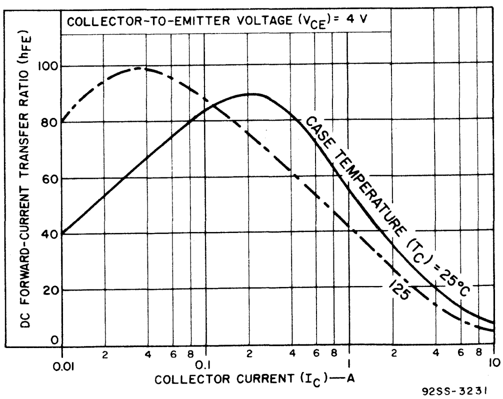


Fig.6— Typical dc beta characteristics for type 2N3442.

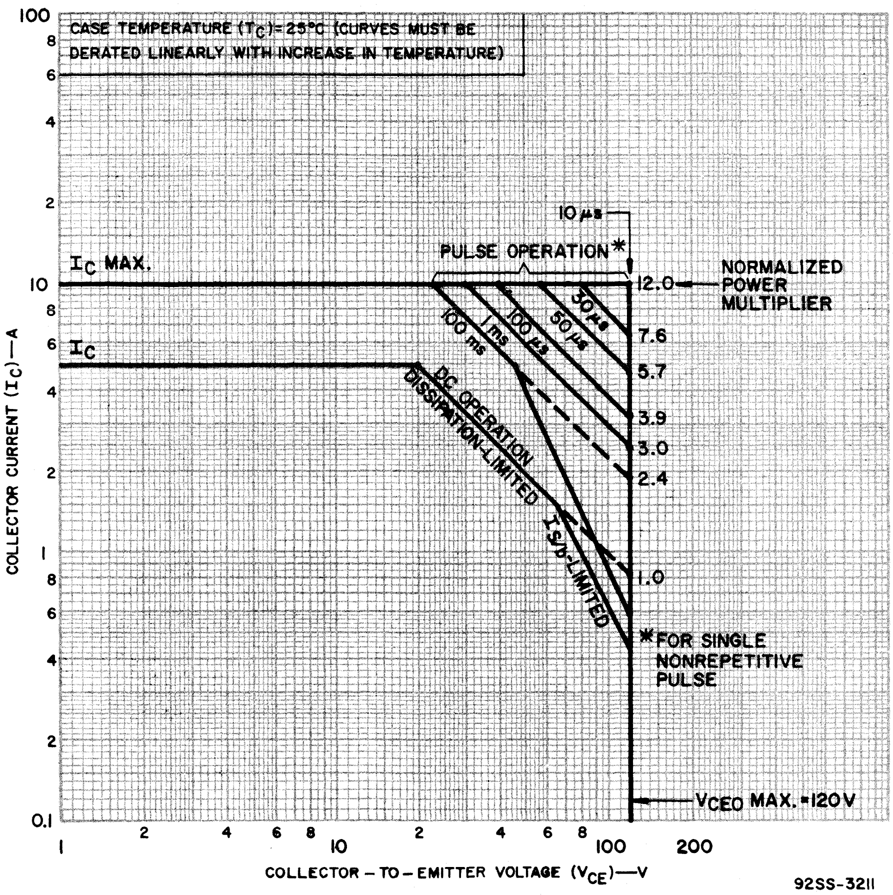


Fig.7– Maximum operating areas for type 2N4347.

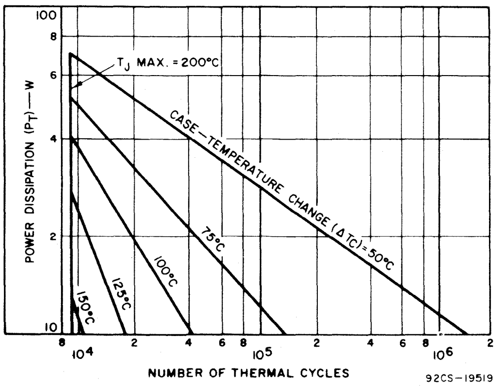


Fig.8– Thermal-cycle rating chart for type 2N4347.

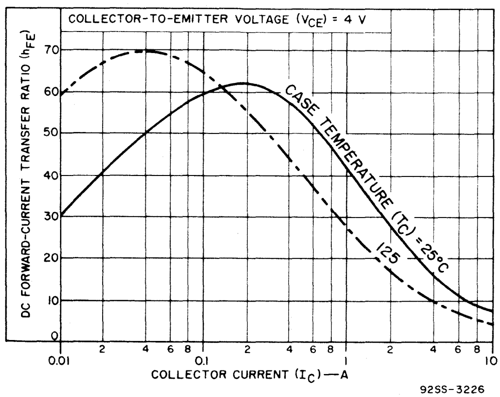


Fig.9– Typical dc beta characteristics for type 2N4347.

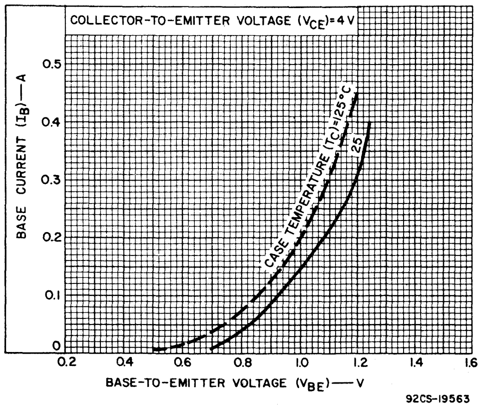


Fig. 10—Typical input characteristics for type 2N6262.

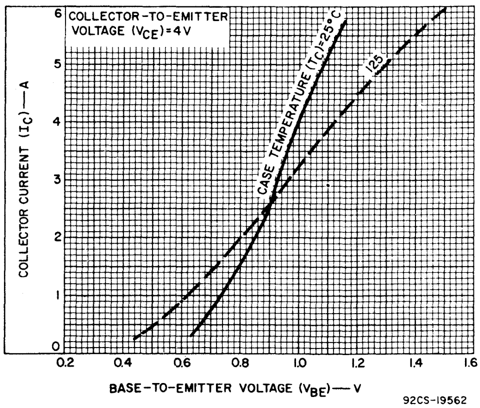


Fig. 11—Typical transfer characteristics for type 2N6262.

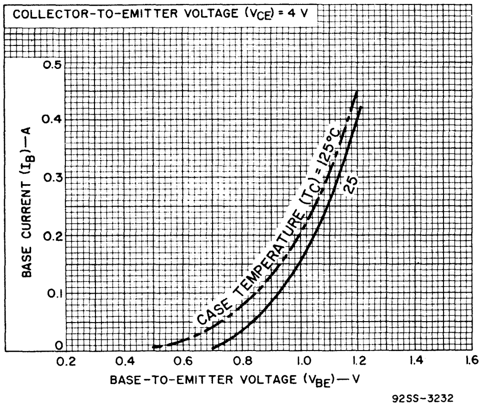


Fig. 12—Typical input characteristics for type 2N3442.

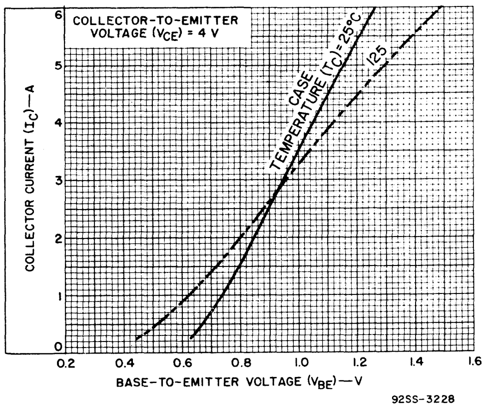


Fig. 13—Typical transfer characteristics for types 2N3442 and 2N4347.

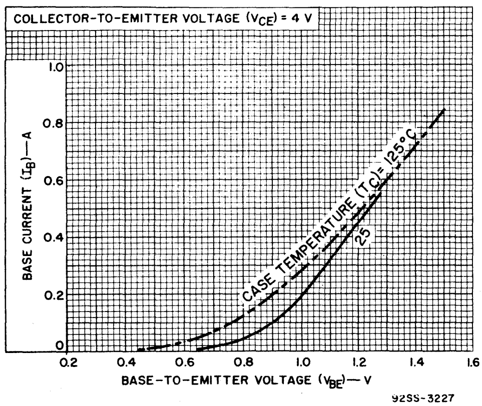


Fig. 14—Typical input characteristics for type 2N4347.

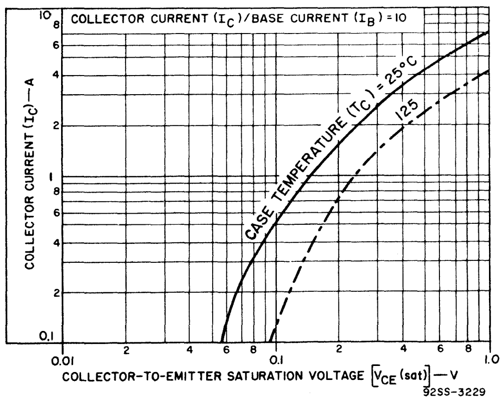


Fig. 15—Typical saturation-voltage characteristics for all types.

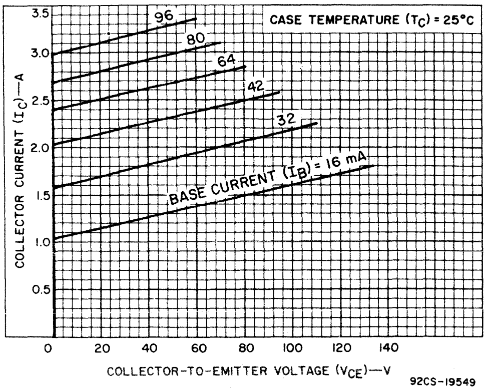


Fig.16—Typical large-signal output characteristics for type 2N6262.

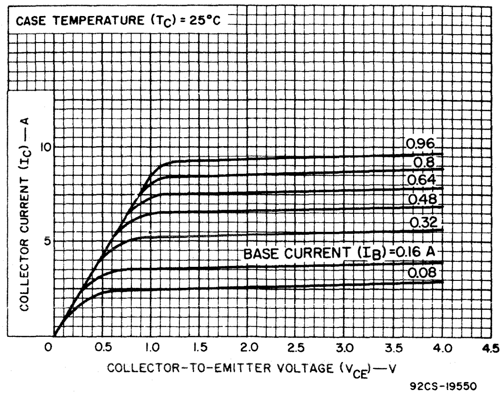


Fig.17—Typical small-signal output characteristics for type 2N6262.

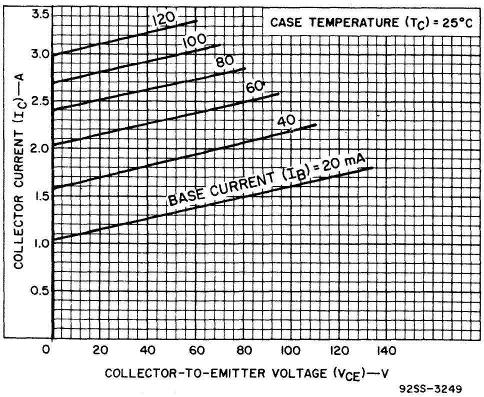


Fig.18—Typical large-signal output characteristics for type 2N3442.

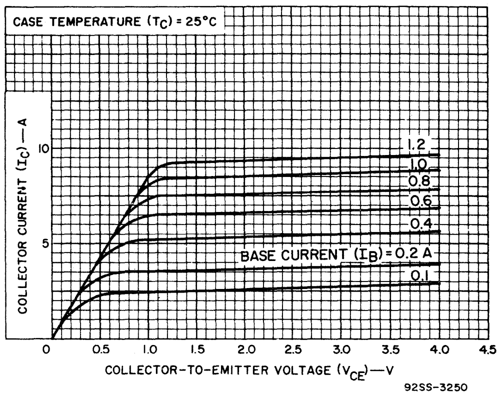


Fig.19—Typical small-signal output characteristics for type 2N3442.

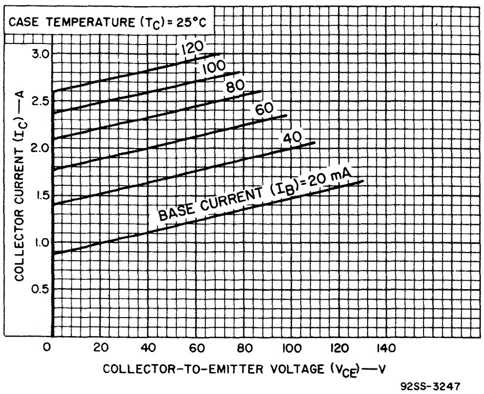


Fig.20—Typical large-signal output characteristics for type 2N4347.

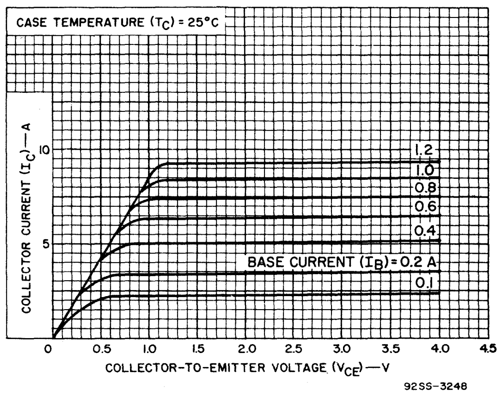


Fig.21—Typical small-signal output characteristics for type 2N4347.

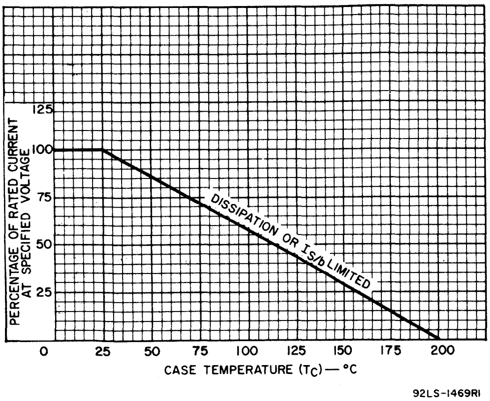


Fig.22—Current derating curve for all types.

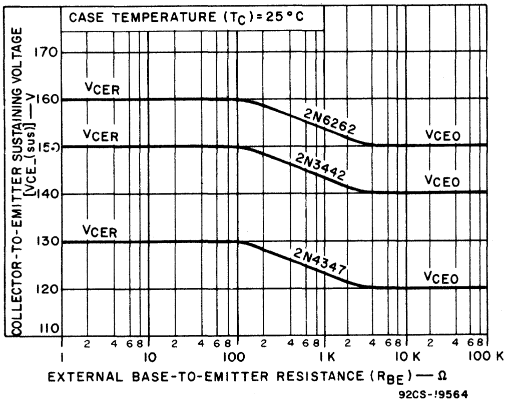


Fig.23—Sustaining voltage vs. base-to-emitter resistance for all types.

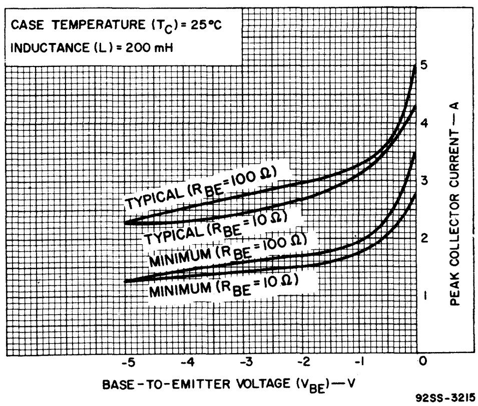
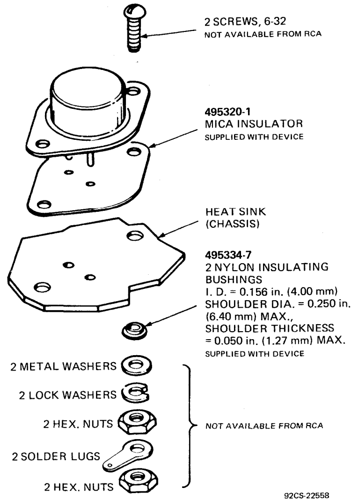


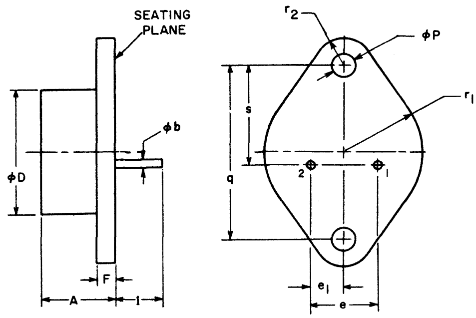
Fig.24—Reverse-bias, second-breakdown characteristics for all types.



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.25—Suggested mounting hardware.

DIMENSIONAL OUTLINE — JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
φb	0.038	0.043	0.97	1.09	2
φD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
1	0.312		7.92		2
φP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r1		0.525		13.34	
r2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. **These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.**
2. Two pins.

92CS—15222

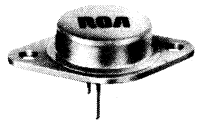
TERMINAL CONNECTIONS

Pin 1 - Base
Pin 2 - Emitter
Case - Collector
Mounting Flange - Collector

RCA
Solid State
Division

Power Transistors

2N3771 2N6257
2N3772 2N6258



JEDEC TO-3

H-1570

Hometaxial II• High-Power High-Current Transistors

Rugged Silicon N-P-N Devices for Applications in Industrial and Commercial Equipment

Features:

- **High dissipation capability**
- **V_{CEX}(sus) at 3 A = 50 V min. (2N3771, 2N6257); = 90 V min. (2N3772, 2N6258)**
- **15-A specification for: h_{FE}, V_{BE}, & V_{CE}(sat) (2N3771, 2N6257)**
- **10-A specification for: h_{FE}, V_{BE}, & V_{CE}(sat) (2N3772, 2N6258)**
- **Low saturation voltage with high beta**

RCA-2N3771, 2N3772, 2N6257, and 2N6258 are hometaxial-base•, silicon n-p-n transistors intended for a wide variety of high-power, high-current applications. Typical applications for these transistors include power-switching circuits, audio amplifiers, series- and shunt-regulator driver and output stages, dc-to-dc converters, inverters, and solenoid (hammer)/relay driver service.

All devices employ the popular JEDEC TO-3 package; they differ in maximum ratings for voltage, current, and power.

• "Hometaxial" was coined by RCA from "homogeneous" and "axial" to describe a single-diffused transistor with a base region of homogeneous-resistivity silicon in the axial direction (emitter-to-collector). "Hometaxial II" is a term used to describe RCA's expanded line of transistors produced by the hometaxial process.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N3771	2N3772	2N6257	2N6258	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	100	50	100	V
*COLLECTOR-TO-EMITTER VOLTAGE:						
With −1.5 V (V_{BE}) & R_{BE} = 100 Ω	V_{CEX}	50	80	50	90	V
With base open	V_{CEO}	40	60	40	80	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	7	5	7	V
*CONTINUOUS COLLECTOR CURRENT	I_C	30	20	20	30	A
*PEAK COLLECTOR CURRENT		30	30	30	30	A
*CONTINUOUS BASE CURRENT	I_B	7.5	5	5	7.5	A
*PEAK BASE CURRENT		15	15	15	15	A
*TRANSISTOR DISSIPATION:	P_T					
At case temperatures up to 25°C		150	150	150	250	W
At case temperatures above 25°C		← See Figs. 1, 6, & 7 →				
*TEMPERATURE RANGE:						
Storage & Operating (Junction)		← −65 to 200 →				°C
*PIN TEMPERATURE (During soldering):						
At distance ≥ 1/32 in. (0.8 mm) from seating plane for 10 s max.		← 230 →				°C

*In accordance with JEDEC registration data format JS-6 RDF-2.

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

Characteristic	Symbol	TEST CONDITIONS							LIMITS								Units
		DC Collector Voltage (V)		DC Emitter or Base Voltage (V)		DC Current (A)			Type 2N3771		Type 2N3772		Type 2N6257		Type 2N6258		
		V_{CB}	V_{CE}	V_{EB}	V_{BE}	I_C	I_E	I_B	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
* Collector-Cutoff Current: With emitter open	I_{CBO}	50					0		–	2*	–	–	–	4	–	–	mA
		100					0		–	–	–	5*	–	–	–	1	
With base-emitter junction reverse-biased	I_{CEX}		45		−1.5				–	–	–	–	–	4	–	–	mA
			50		−1.5				–	2	–	–	–	–	–	–	
			100		−1.5				–	–	–	5	–	–	–	1	
With base-emitter junction reverse-biased & T_C = 150°C	I_{CEX}		30		−1.5				–	10	–	10	–	–	–	–	mA
			45		−1.5				–	–	–	–	–	20	–	–	
			100		−1.5				–	–	–	–	–	–	–	10	
With base open	I_{CEO}		25					0	–	–	–	–	–	10	–	–	mA
			30					0	–	10	–	–	–	–	–	–	
			50					0	–	–	–	10	–	–	–	–	
			60					0	–	–	–	–	–	–	–	2	
* Emitter-Cutoff Current	I_{EBO}			5		0			–	5	–	–	–	10	–	–	mA
				7		0			–	–	–	5	–	–	–	2	
* DC Forward Current Transfer Ratio	h_{FE}		4			30[a]			5	–	–	–	–	–	5	–	
			4			20[a]			–	–	5	–	5	–	–	–	
			2			15[a]			–	–	–	–	–	–	20	60	
			4			15[a]			15	60	–	–	–	–	–	–	
			4			10[a]			–	–	15	60	–	–	–	–	
			4			8[a]			–	–	–	–	15	75	–	–	
Collector-to-Emitter Sustaining Voltage (*See Fig. 5*) With base-emitter junction reverse-biased (R_{BE} = 100Ω)	$V_{CEX}(sus)$			−1.5		0.2			50	–	80	–	50	–	90	–	V
With external base-to-emitter resistance (R_{BE}) = 100Ω	$V_{CER}(sus)$					0.2			45	–	70	–	45	–	85	–	V
* With base open	$V_{CEO}(sus)$					0.2		0	40	–	60	–	40	–	80	–	V
* Base-to-Emitter Voltage	V_{BE}		2			20[a]			–	–	–	–	–	–	–	2	V
			4			15[a]			–	2.7	–	–	–	–	–	–	
			4			10[a]			–	–	–	2.2	–	–	–	–	
			4			8[a]			–	–	–	–	–	2.2	–	–	
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					30[a]		6	–	4	–	–	–	–	–	3	V
						20[a]		4	–	–	–	4	–	4	–	–	
						15[a]		1.5	–	2	–	–	–	–	–	0.75	
						10[a]		1	–	–	–	1.4	–	–	–	–	
						8[a]		0.8	–	–	–	–	–	1.5	–	–	
Second-Breakdown Collector Current With base forward-biased & 1–s, nonrepetitive pulse	$I_{S/b}$[b]		80						–	–	–	–	–	–	3.1	–	A
			60						–	–	2.5	–	–	–	–	–	
			40						3.75	–	–	–	3.75	–	–	–	
Second-Breakdown Energy With base reverse biased & L = 40 mH, R_{BE} = 100 Ω	$E_{S/b}$[c]			−1.5		5			500	–	500	–	500	–	500	–	mJ
* Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 0.05 MHz)	$\|h_{fe}\|$		4			1			4*	16 (Typ.)	4*	16 (Typ.)	4*	16 (Typ.)	4*	16 (Typ.)	
* Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 1 kHz)	h_{fe}		4			1			40	–	40	–	40	–	40	–	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$								–	1.17	–	1.17	–	1.17	–	0.7	°C/W

* In accordance with JEDEC registration data format JS-6 RDF-2.

[a] Pulsed; pulse duration = 300 μs, rep. rate = 60 Hz.

[b] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward biased for transistor operation in the active region.

[c] $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse-bias conditions. $E_{S/b} = ½LI^2$, where L is a series load or leakage inductance and I is the peak collector current.

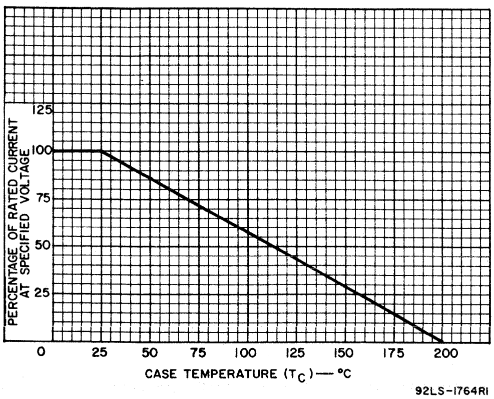


Fig.1—Derating curve for all types.

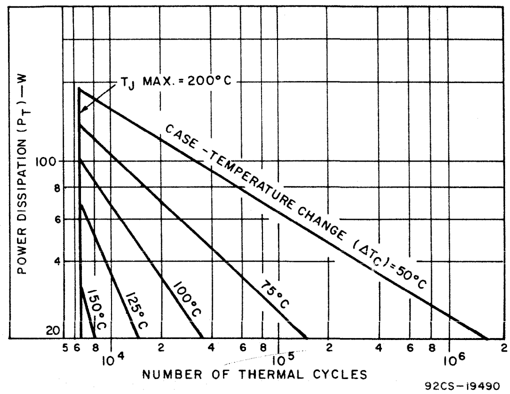


Fig.2—Thermal-cycle rating chart for type 2N6258.

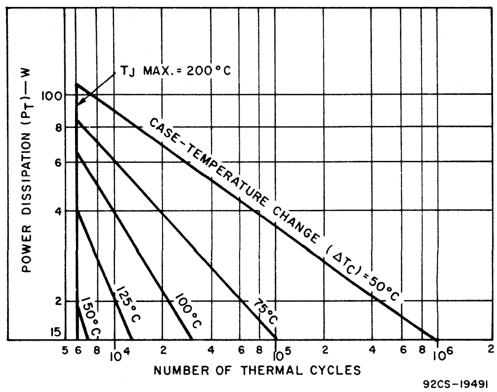


Fig.3—Thermal-cycle rating chart for types 2N3771, 2N3772, and 2N6257.

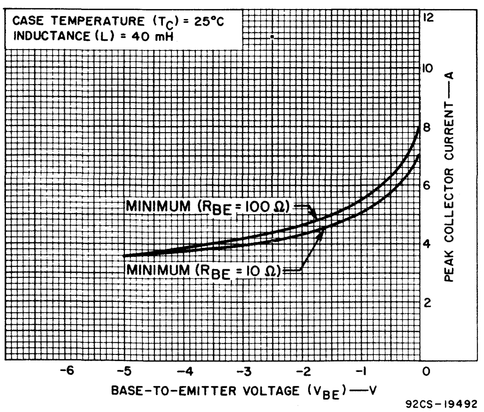


Fig.4—Reverse-bias second-breakdown characteristics for all types.

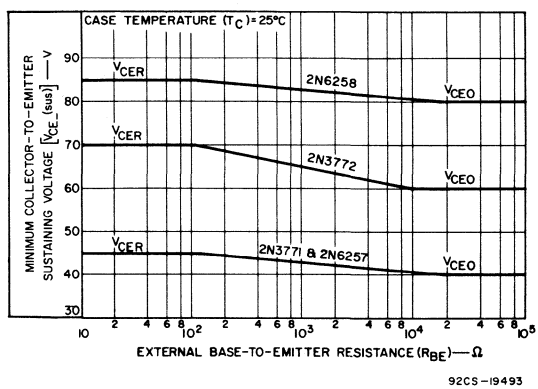


Fig.5—Sustaining voltage vs. base-to-emitter resistance for all types.

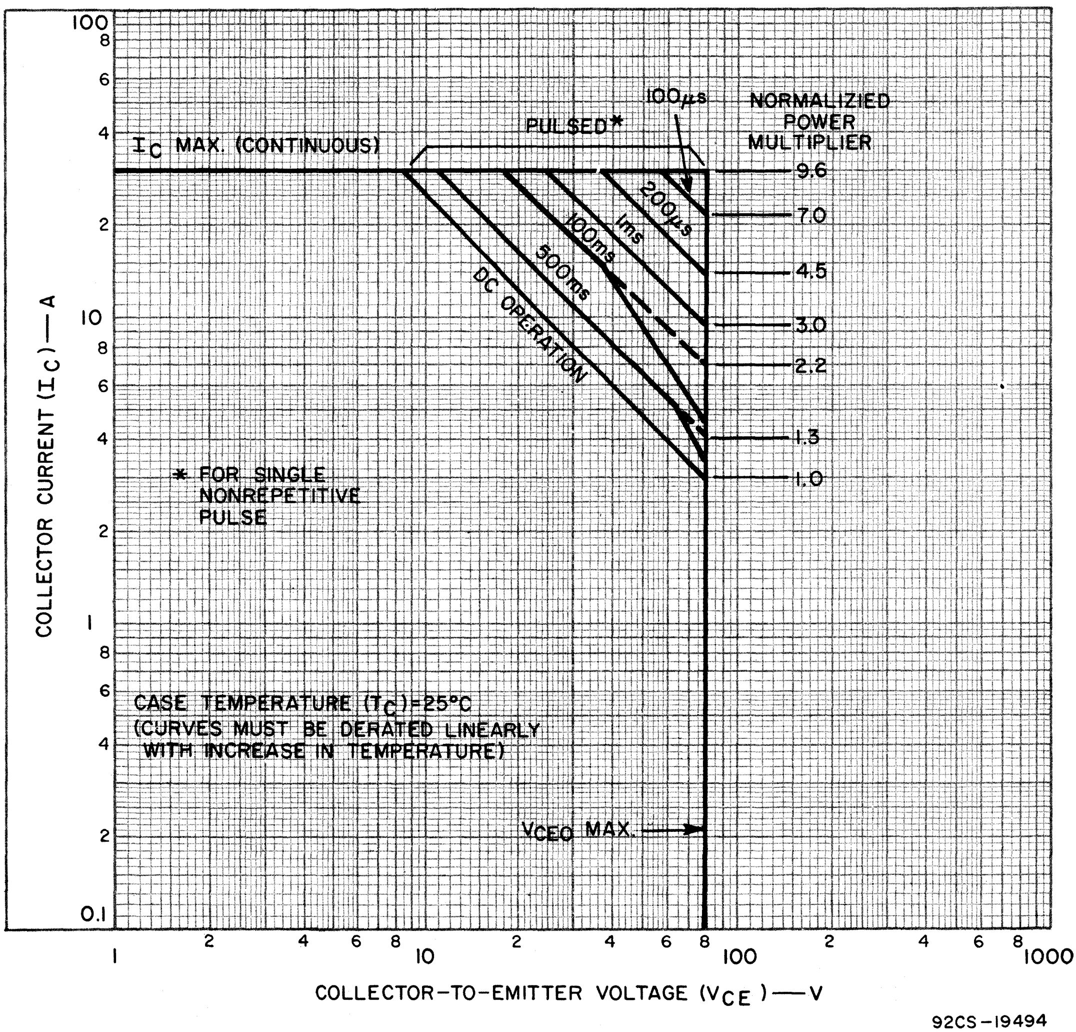


Fig.6—Maximum operating areas for types 2N6258.

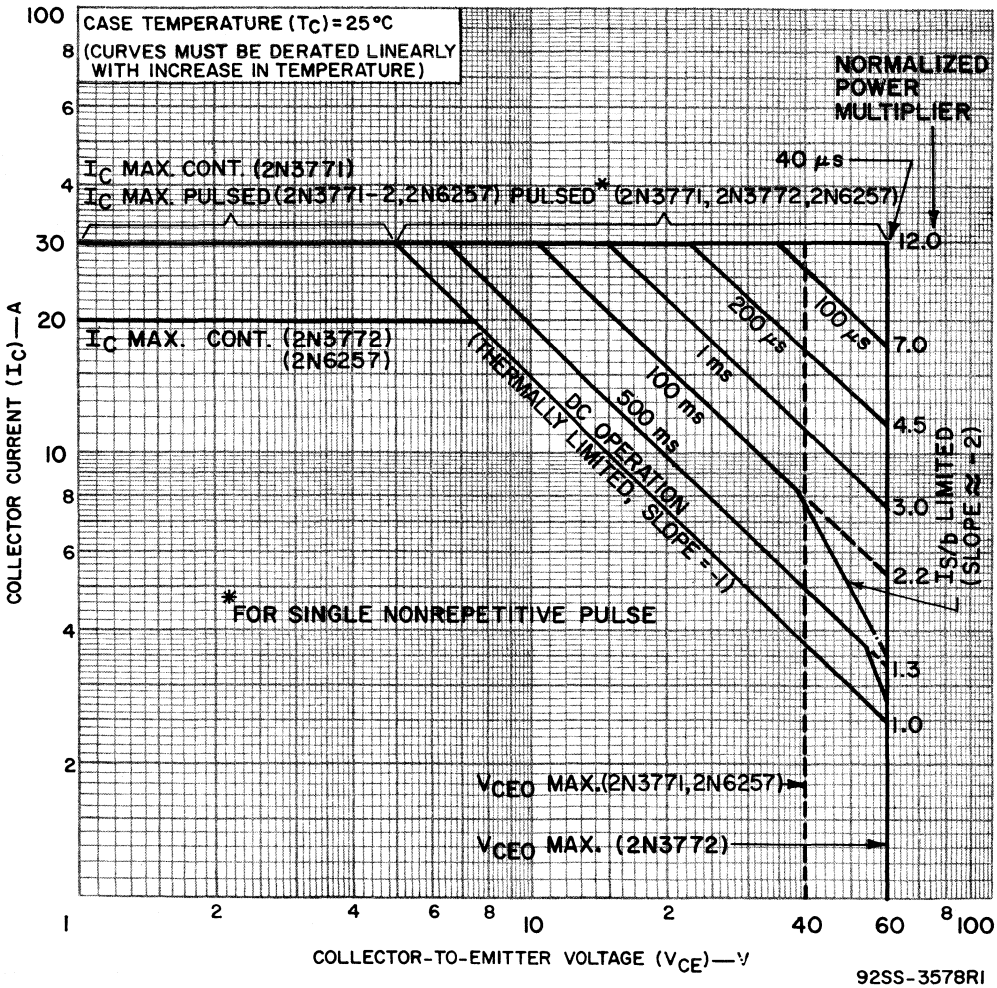


Fig.7—Maximum operating areas for types 2N3771, 2N3772, and 2N6257.

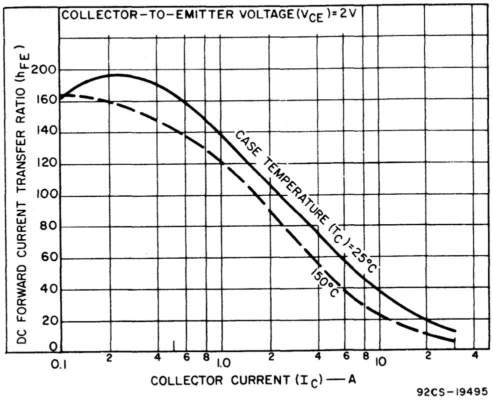


Fig.8—Typical dc beta characteristics for type 2N6258.

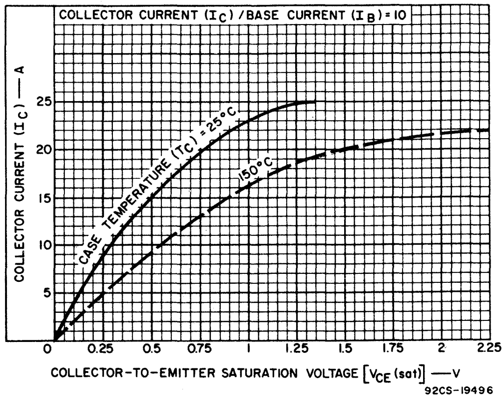


Fig.9—Typical saturation-voltage characteristics for type 2N6258.

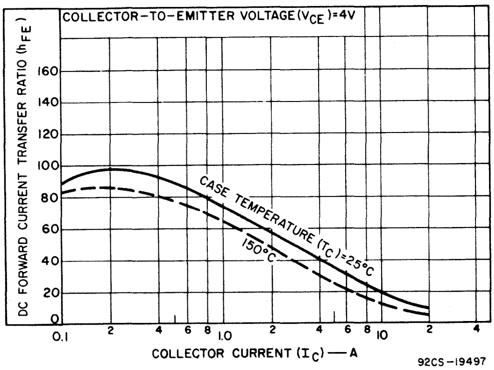


Fig.10—Typical dc beta characteristics for type 2N3772 and 2N6257.

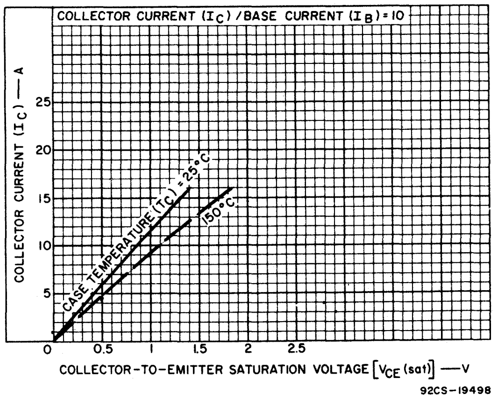


Fig.11—Typical saturation-voltage characteristics for types 2N3772 and 2N6257.

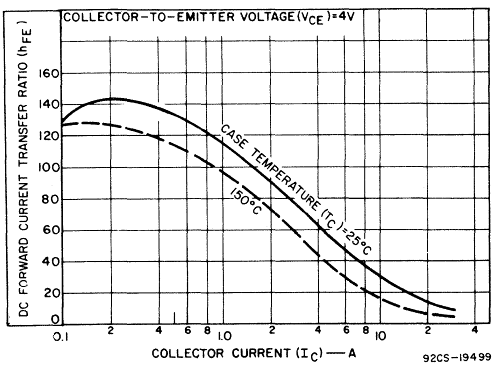


Fig.12—Typical dc beta characteristics for type 2N3771.

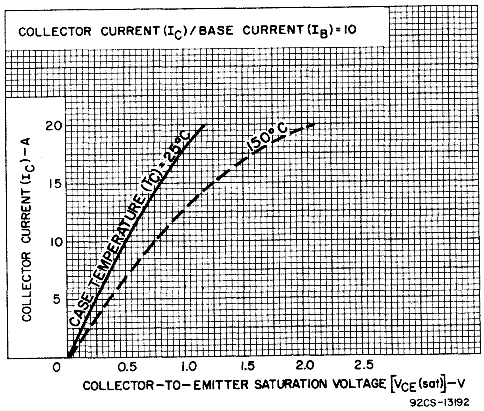


Fig.13—Typical saturation-voltage characteristics for type 2N3771.

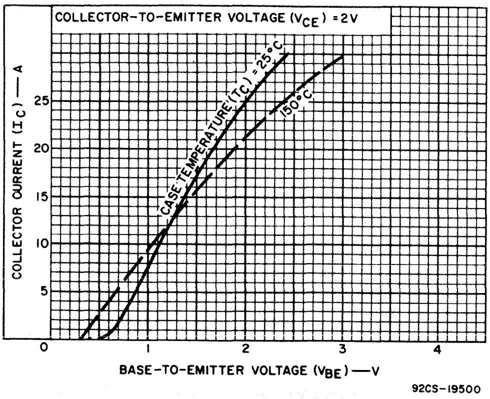


Fig.14—Typical transfer characteristics for type 2N6258.

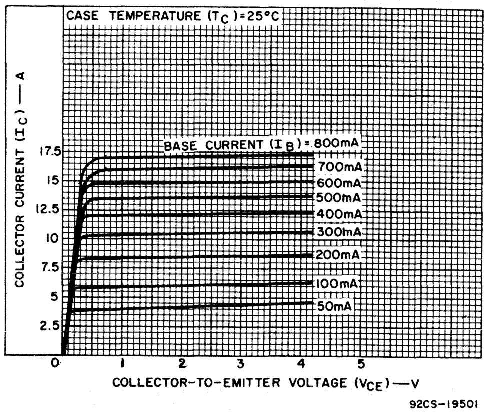


Fig.15—Typical output characteristics for type 2N6258.

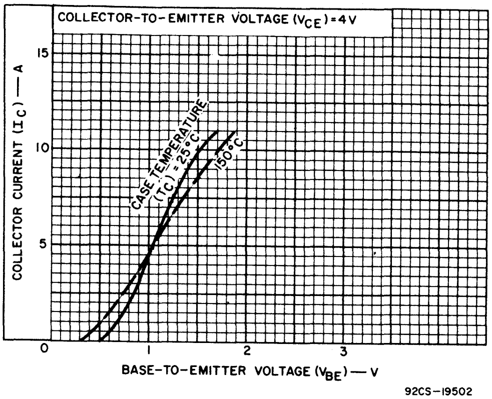


Fig.16—Typical transfer characteristics for types 2N3772 and 2N6257.

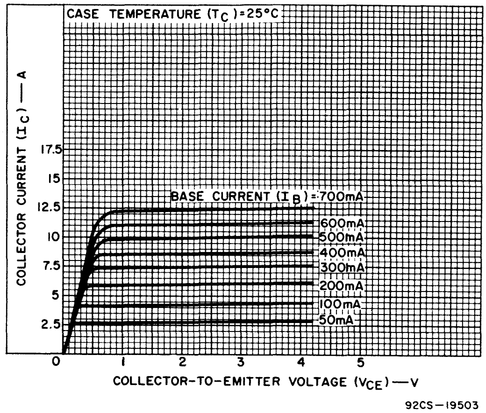


Fig.17—Typical output characteristics for types 2N3772 and 2N6257.

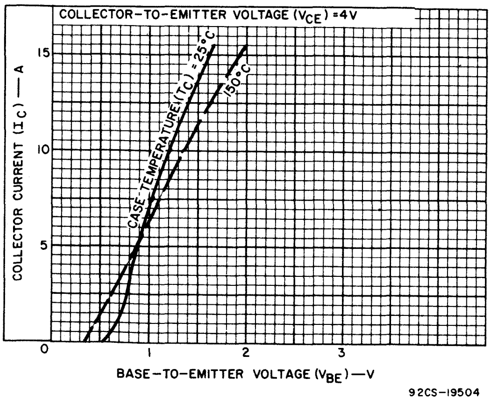


Fig.18—Typical transfer characteristics for type 2N3771.

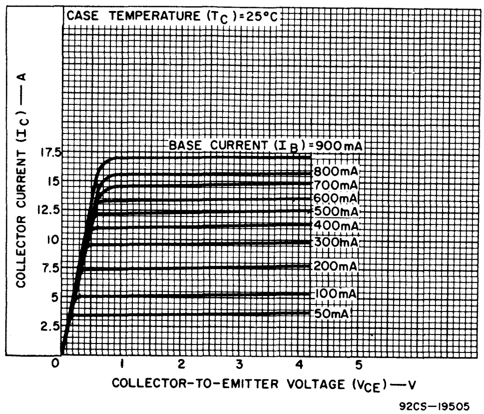


Fig.19—Typical output characteristics for type 2N3771.

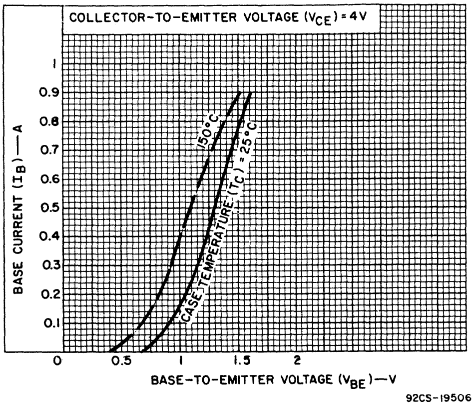


Fig.20—Typical input characteristics for type 2N6258.

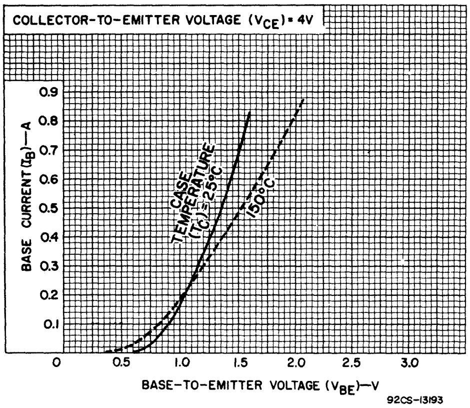


Fig.21—Typical input characteristics for types 2N3771 and 2N6257.

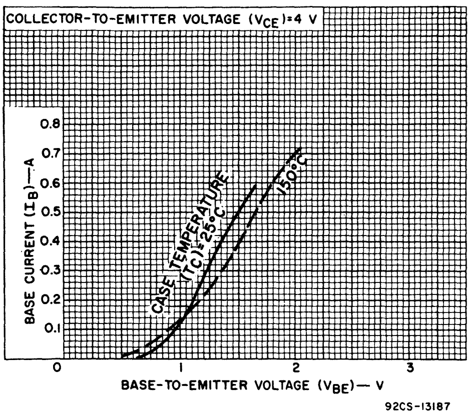
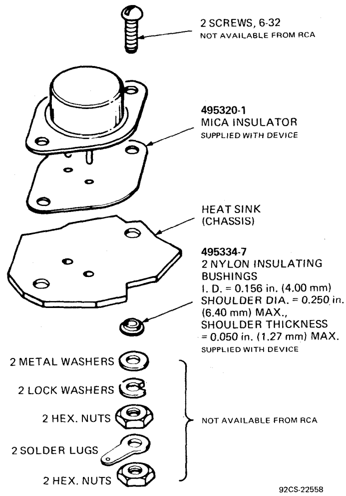


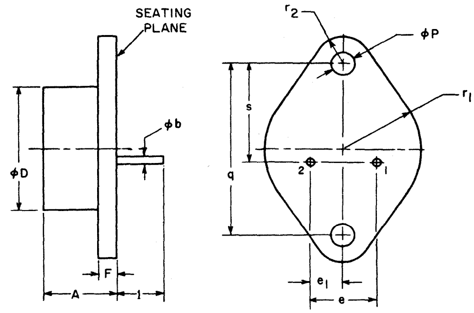
Fig.22—Typical input characteristics for type 2N3772.



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.23—Suggested mounting hardware.

DIMENSIONAL OUTLINE – JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
ϕb	0.038	0.043	0.97	1.09	2
ϕD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e_1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
1	0.312		7.92		2
ϕP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r_1		0.525		13.34	
r_2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:
1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

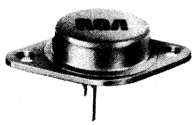
92CS–15222

TERMINAL CONNECTIONS

Pin 1 – Base
Pin 2 – Emitter
Case – Collector
Mounting Flange – Collector

RCA Solid State Division

Power Transistors
2N6259 2N4348 2N3773



JEDEC TO-3

H-1570

Hometaxial II• High-Current Silicon N-P-N Transistors

Rugged High-Voltage Devices for Applications in Industrial and Commercial Equipment

Features:

- High dissipation capability — 120 W (2N4348), 150 W (2N3773), 250 W (2N6259)
- 5-A specification for h_{FE}, V_{BE}, & $V_{CE}(sat)$ (2N4348)
- 8-A specification for h_{FE}, V_{BE}, & $V_{CE}(sat)$ (2N3773, 2N6259)
- V_{CEX} — 140 V min (2N4348), 160 V min (2N3773), 170 V min (2N6259)
- Low saturation voltage with high beta

RCA-2N3773, 2N4348, and 2N6259 are hometaxial-base• silicon n-p-n transistors intended for a wide variety of high-voltage high-current applications. Typical applications for these transistors include power-switching circuits, audio amplifiers, series- and shunt-regulator driver and output stages, dc-to-dc converters, inverters, and solenoid (hammer)/relay driver service.

These devices employ the popular JEDEC TO-3 package; they differ in maximum ratings for voltage, current, and power.

• "Hometaxial" was coined by RCA from "homogeneous" and "axial" to describe a single-diffused transistor with a base region of homogeneous-resistivity silicon in the axial direction (emitter-to-collector). "Hometaxial II" is a term used to describe RCA's expanded line of transistors produced by the hometaxial process.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N4348	2N3773	2N6259	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	140	160	170	V
COLLECTOR-TO-EMITTER VOLTAGE:					
* With base open	V_{CEO}	120	140	150	V
With reverse bias (V_{BE}) of −1.5 V	V_{CEX}	140	160	170	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	7	7	7	V
*COLLECTOR CURRENT:	I_C				
Continuous		10	16	16	A
Peak		30	30	30	A
*BASE CURRENT:	I_B				
Continuous		4	4	4	A
Peak		15	15	15	A
*TRANSISTOR DISSIPATION:	P_T				
At case temperatures up to 25°C		120	150	250	W
At case temperatures above 25°C		← See Figs. 1, 4, 7, & 22 →			
*TEMPERATURE RANGE:					
Storage & Operating (Junction)		← −65 to +200 →			°C
*PIN TEMPERATURE (During Soldering):					
At distances ≥1/32 in. (0.8 mm) from case for 10 s max.		← 230 →			°C

* In accordance with JEDEC registration data format (JS-6, RDF-2).

11-73

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: DC Collector Voltage (V) V_{CB}	V_{CE}	DC Emitter or Base Voltage (V) V_{EB}	V_{BE}	DC Current (A) I_C	I_E	I_B	LIMITS: Type 2N4348 Min.	Max.	Type 2N3773 Min.	Max.	Type 2N6259 Min.	Max.	UNITS
* Collector-Cutoff Current: With emitter open	I_{CBO}	140					0		–	–	–	2	–	–	mA
With base-emitter junction reverse-biased	I_{CEX}		120		−1.5				–	2	–	–	–	–	mA
			140		−1.5				–	–	–	2	–	–	
			150		−1.5				–	–	–	–	–	0.2	
With base-emitter junction reverse-biased and T_C = 150°C	I_{CEX}		120		−1.5				–	10	–	–	–	–	mA
			140		−1.5				–	–	–	10	–	–	
			150		−1.5				–	–	–	–	–	4	
With base open	I_{CEO}		100						–	200	–	–	–	–	mA
			120						–	–	–	10	–	2	
* Emitter-Cutoff Current	I_{EBO}			7		0			–	5	–	5	–	2	mA
* DC Forward Current Transfer Ratio	h_{FE}		4			5[a]			15	60	–	–	–	–	
			4			8[a]			–	–	15	60	–	–	
			2			8[a]			–	–	–	–	15	60	
			4			10[a]			10	–	–	–	–	–	
			4			16[a]			–	–	5	–	10	–	
Collector-to-Emitter Sustaining Voltage: With base-emitter junction reverse-biased (R_{BE} = 100Ω)	V_{CEX}(sus)				−1.5	0.1			140	–	160	–	170	–	V
With external base-to-emitter resistance (R_{BE}) = 100Ω	V_{CER}(sus)					0.2[a]			140	–	150	–	160	–	V
* With base open	V_{CEO}(sus)					0.2[a]		0	120	–	140	–	150	–	V
* Base-to-Emitter Voltage	V_{BE}		4			5[a]			–	2	–	–	–	–	V
			4			8[a]			–	–	–	2.2	–	–	
			2			8[a]			–	–	–	–	–	2	
			4			10[a]			–	3	–	–	–	–	
* Collector-to-Emitter Saturation Voltage	V_{CE}(sat)					5[a]		0.5	–	1	–	–	–	–	V
						8[a]		0.8	–	–	–	1.4	–	1	
						10[a]		1.25	–	2	–	–	–	–	
						16[a]		3.2	–	–	–	4	–	2.5	
Second-Breakdown Collector Current With base forward-biased and 1-s, nonrepetitive pulse	$I_{S/b}$[b]		80						1.5	–	–	–	–	–	A
			100						–	–	1.5	–	2.5	–	
Second-Breakdown Energy With base reverse-biased and L = 40 mH, R_{BE} = 100Ω	$E_{S/b}$[c]				−1.5	2.5			0.125	–	0.125	–	0.125	–	J
* Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 50 kHz)	$\|h_{fe}\|$		4			1			4	–	4	–	4	–	
* Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 1 kHz)	h_{fe}		4			1			40	–	40	–	40	–	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$								–	1.46	–	1.17	–	0.7	°C/W

*In accordance with JEDEC registration data format JS-6 RDF-2.

[a] Pulsed; pulse duration = 300μs, rep. rate = 60 Hz.

[b] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward-biased for transistor operation in the active region.

[c] $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse-bias conditions. $E_{S/b} = 1/2 L I^2$ where L is a series load or leakage inductance and I is the peak collector current.

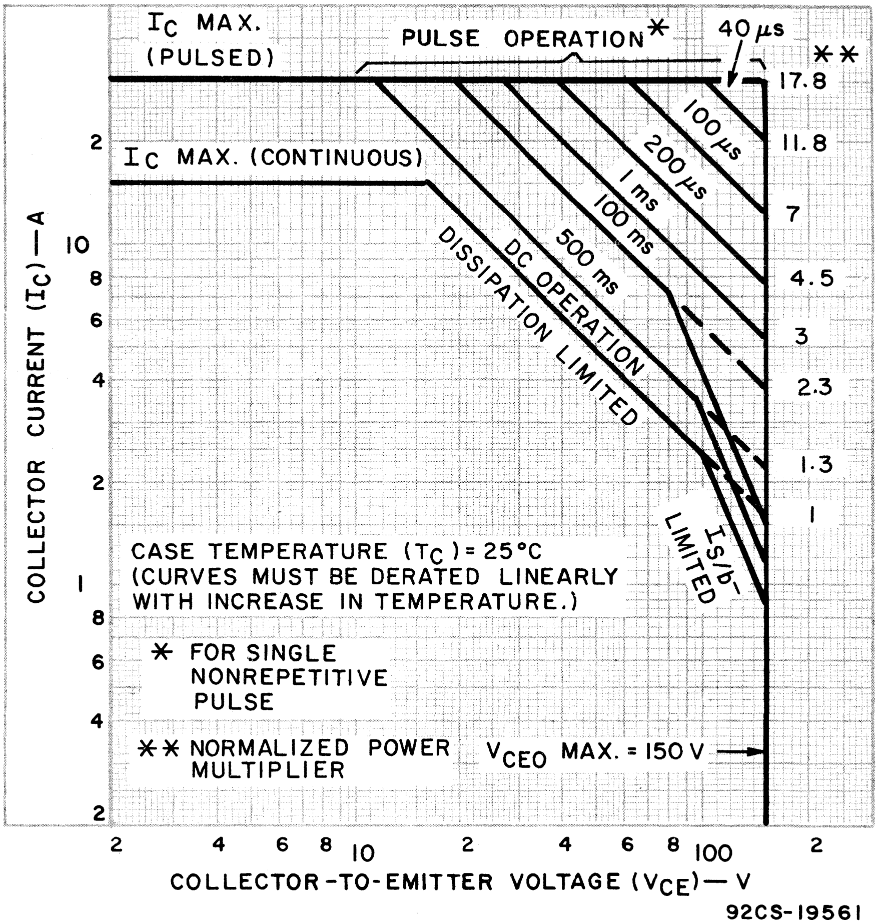


Fig.1—Maximum operating areas for type 2N6259.

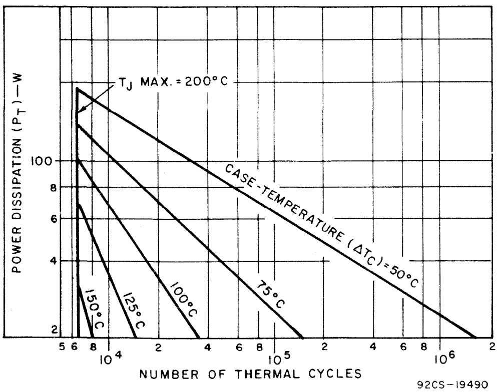


Fig.2—Thermal-cycle rating chart for type 2N6259.

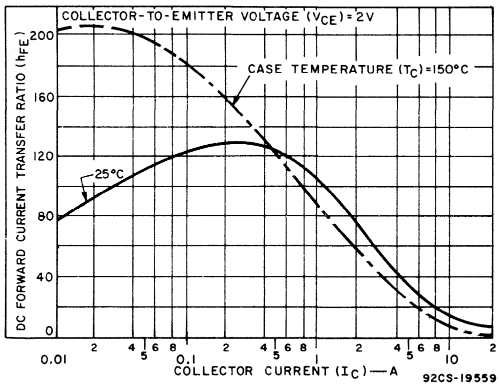


Fig.3—Typical dc beta characteristics for type 2N6259.

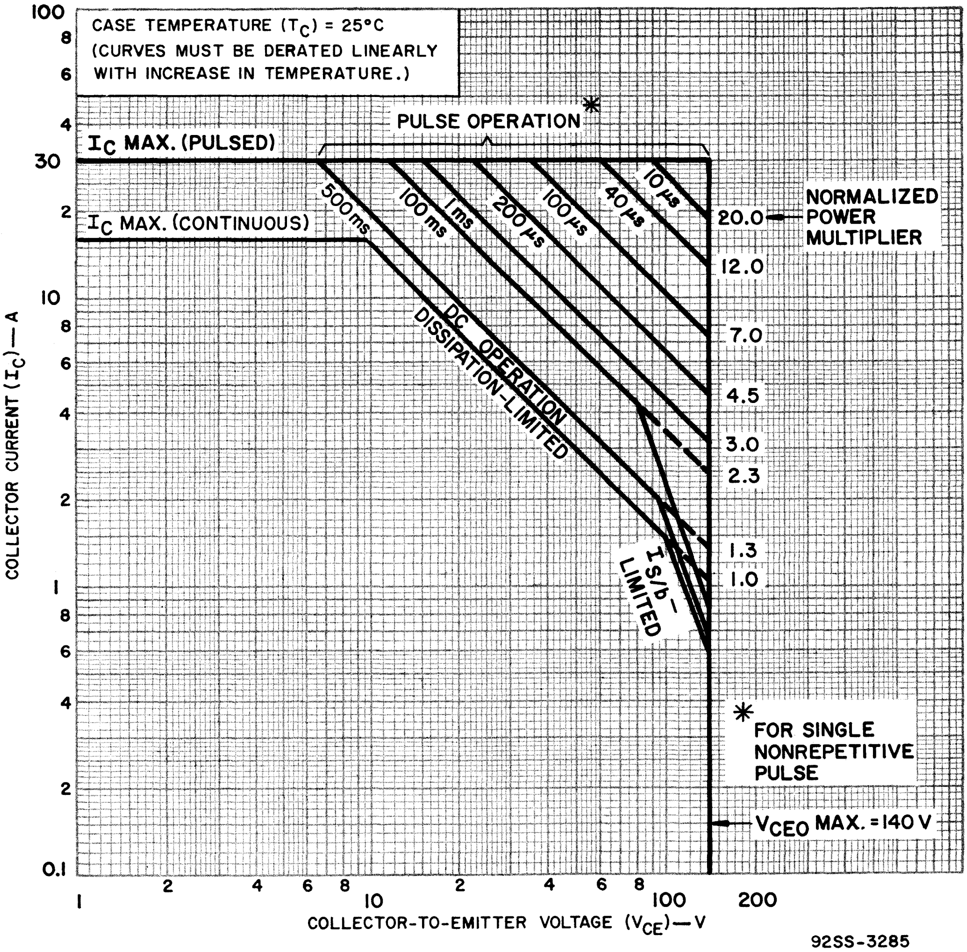


Fig.4—Maximum operating areas for type 2N3773.

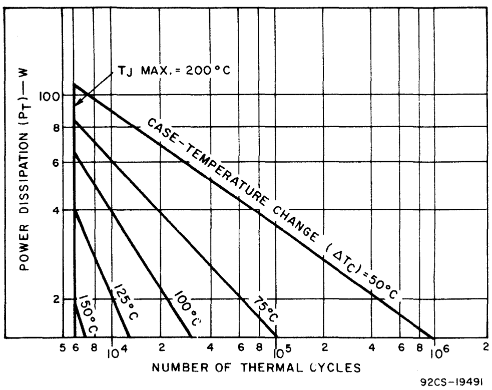


Fig.5—Thermal-cycle rating chart for type 2N3773.

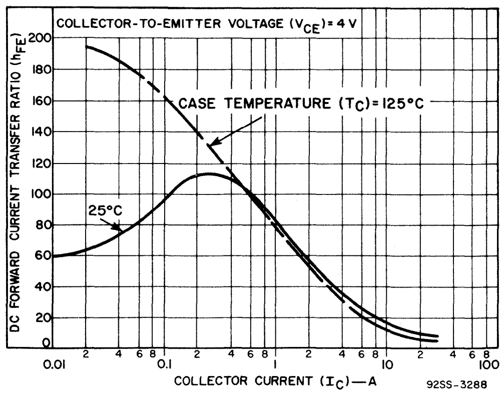


Fig.6—Typical dc beta characteristics for type 2N3773.

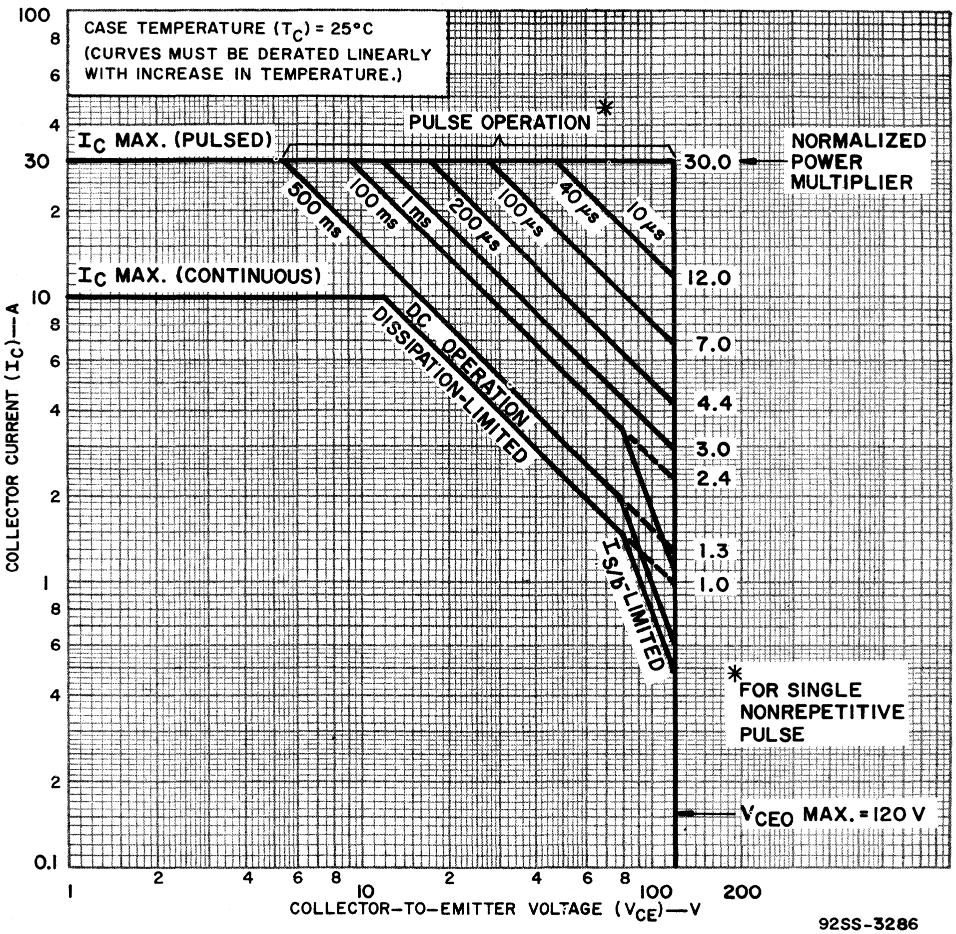


Fig.7—Maximum operating areas for type 2N4348.

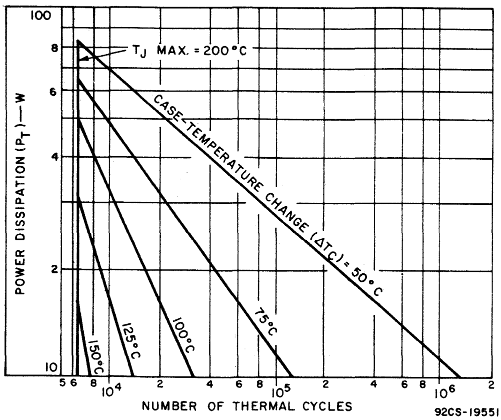


Fig.8—Thermal-cycle rating chart for type 2N4348.

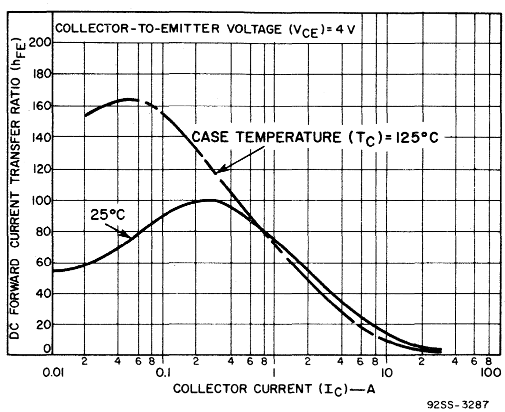


Fig.9—Typical dc beta characteristics for type 2N4348.

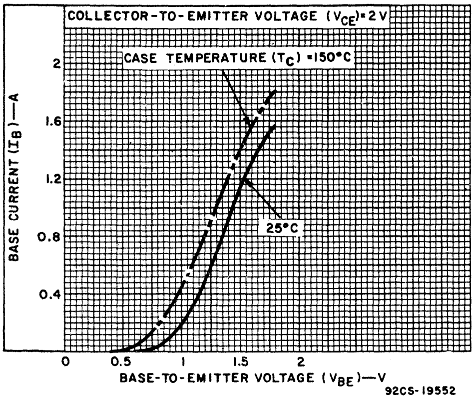


Fig.10—Typical input characteristics for type 2N6259.

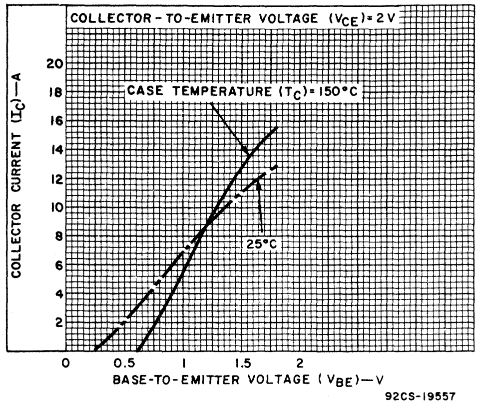


Fig.11—Typical transfer characteristics for type 2N6259.

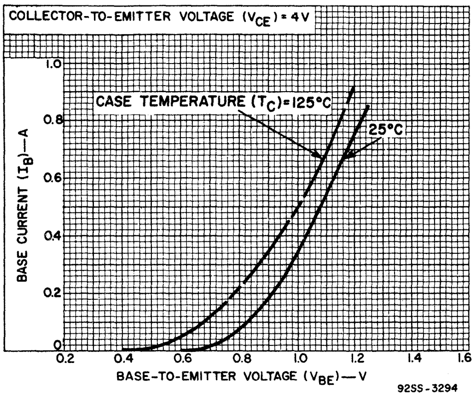


Fig.12—Typical input characteristics for type 2N3773.

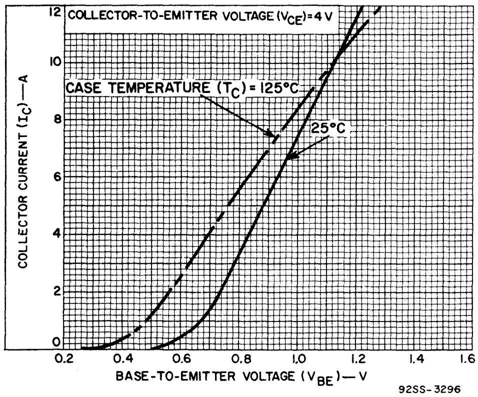


Fig.13—Typical transfer characteristics for type 2N3773.

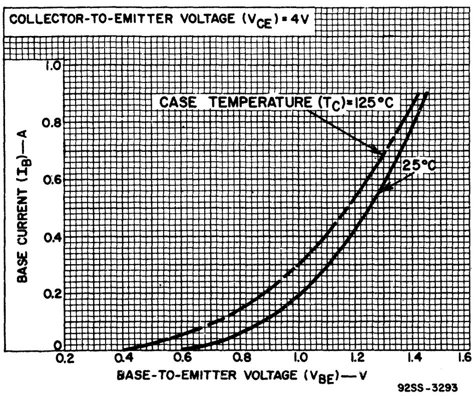


Fig.14—Typical input characteristics for type 2N4348.

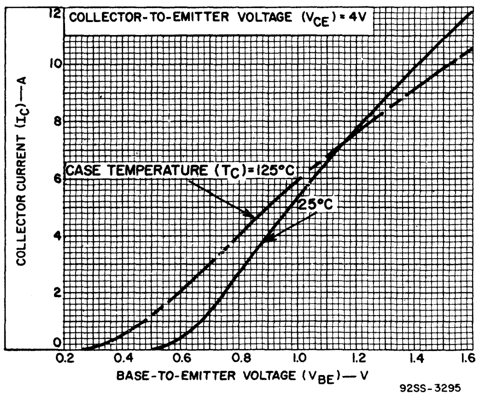


Fig.15—Typical transfer characteristics for type 2N4348.

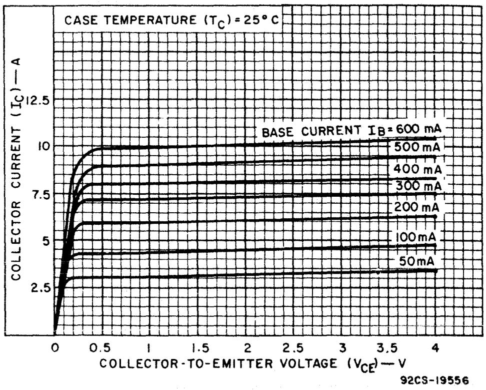


Fig. 16—Typical output characteristics for type 2N6259.

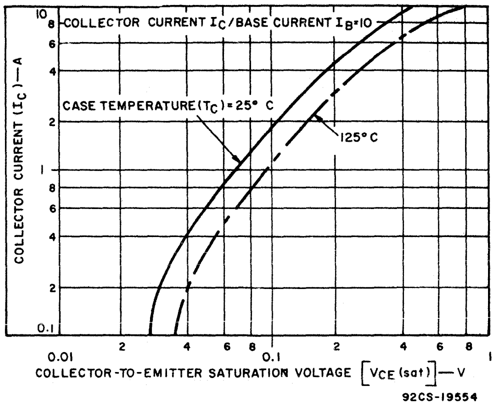


Fig. 17—Typical saturation-voltage characteristics for type 2N6259.

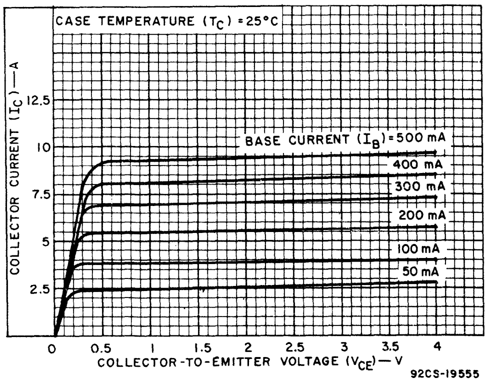


Fig. 18—Typical output characteristics for type 2N3773.

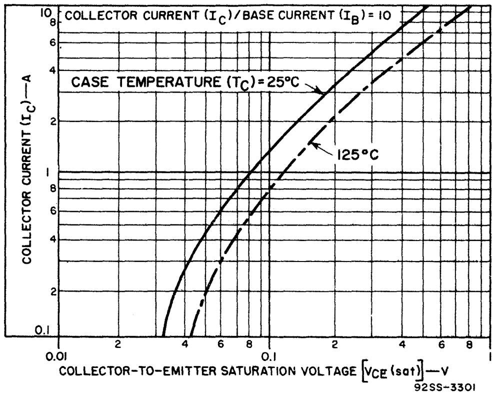


Fig. 19—Typical saturation-voltage characteristics for type 2N3773.

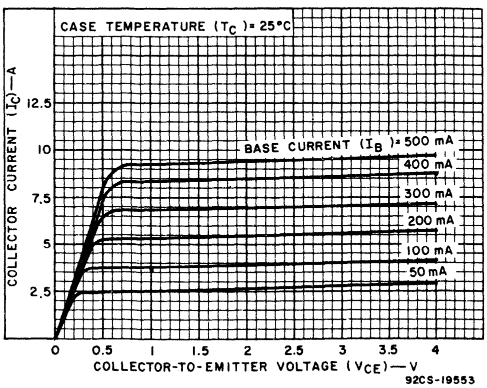


Fig. 20—Typical output characteristics for type 2N4348.

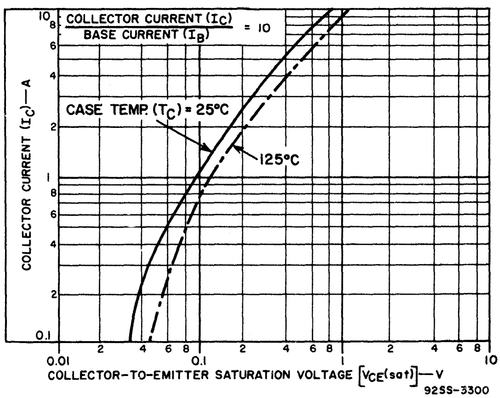


Fig. 21—Typical saturation-voltage characteristics for type 2N4348.

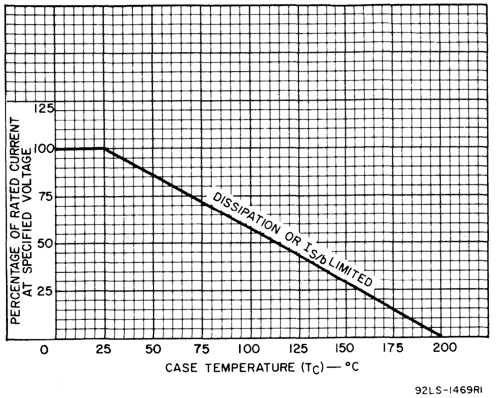


Fig.22—Dissipation derating curve for all types.

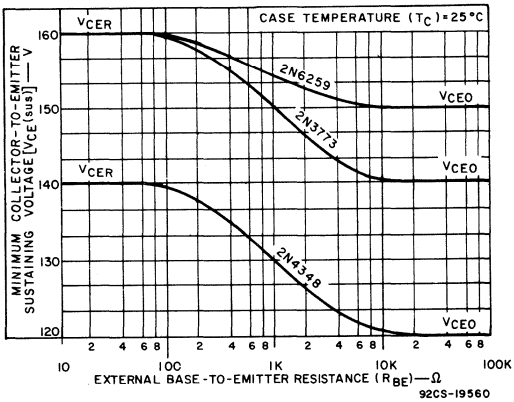


Fig.23—Sustaining voltage vs. base-to-emitter resistance for all types.

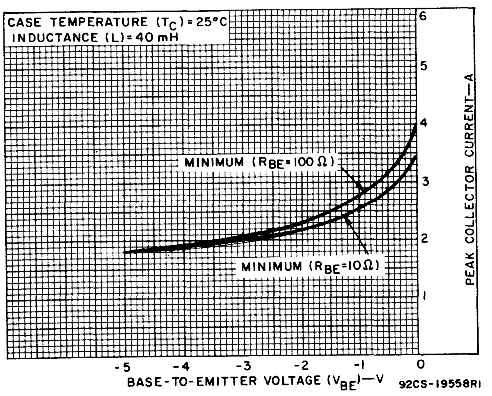
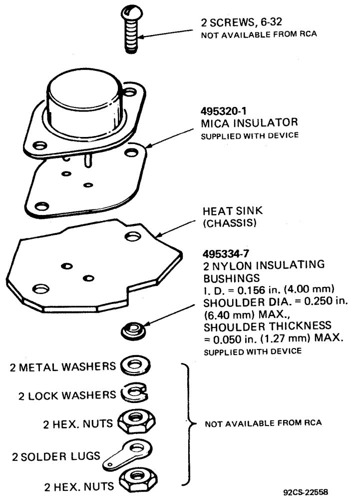


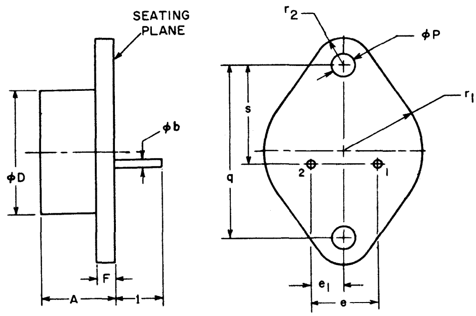
Fig.24—Reverse-bias, second-breakdown characteristics for all types.



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.25—Suggested mounting hardware.

DIMENSIONAL OUTLINE — JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
φb	0.038	0.043	0.97	1.09	2
φD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
l	0.312		7.92		2
φP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r1		0.525		13.34	
r2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS-15222

TERMINAL CONNECTIONS

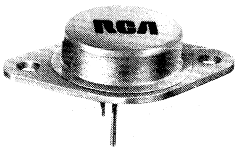
Pin 1 — Base
Pin 2 — Emitter
Case — Collector
Mounting Flange — Collector

RCA

Solid State
Division

Power Transistors

41508



JEDEC TO-3

H-1570

Hometaxial-Base High-Current Silicon N-P-N Transistor

Rugged High-Voltage Device for Applications in Industrial and Commercial Equipment

Features:

- **High dissipation capability — 150 W**
- **8-A specification for h_{FE}, V_{BE}, and V_{CE}(sat)**
- **V_{CEX} — 160 V min.**
- **Low saturation voltage with high beta**

RCA-41508 is a hometaxial-base silicon n-p-n transistor intended for a wide variety of high-voltage high-current applications. Typical applications include power-switching circuits, audio amplifiers, series- and shunt-regulator driver and output stages, dc-to-dc converters, inverters, and solenoid (hammer)/relay driver service. The 41508 employs the popular JEDEC TO-3 package.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	160	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With base open	V_{CEO}	140	V
With reverse bias (V_{BE}) of −1.5 V	V_{CEX}	160	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	7	V
COLLECTOR CURRENT:	I_C		
Continuous		16	A
Peak		30	A
BASE CURRENT:	I_B		
Continuous		4	A
Peak		15	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25°C		150	W
At case temperatures above 25°C		*See Fig. 2*	
TEMPERATURE RANGE:			
Storage & Operating (Junction)		−65 to +200	°C
PIN TEMPERATURE (During Soldering):			
At distances $\geq$1/32 in. (0.8 mm) from case for 10 s max.		230	°C

11-73

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS							LIMITS		UNITS
		VOLTAGE V dc				CURRENT A dc			41508		
		V_{CB}	V_{CE}	V_{EB}	V_{BE}	I_C	I_E	I_B	Min.	Max.	
Collector-Cutoff Current: With emitter open	I_{CBO}	140					0		–	2	mA
With base-emitter junction reverse-biased	I_{CEX}		140		−1.5				–	2	mA
With base-emitter junction reverse-biased and T_C = 150°C	I_{CEX}		140		−1.5				–	10	mA
With base open	I_{CEO}		120					0	–	10	mA
Emitter-Cutoff Current	I_{EBO}			7		0			–	5	mA
DC Forward Current Transfer Ratio	h_{FE}		4			8[a]			15	60	
			4			16[a]			5	–	
Collector-to-Emitter Sustaining Voltage: With base-emitter junction reverse-biased (R_{BE} = 100Ω)	$V_{CEX}(sus)$				−1.5	0.1			160	–	V
With external base-to-emitter resistance (R_{BE}) = 100Ω	$V_{CER}(sus)$					0.2[a]			150	–	V
With base open	$V_{CEO}(sus)$					0.2[a]		0	140	–	V
Base-to-Emitter Voltage	V_{BE}		4			8[a]			–	2.2	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					8[a]		0.8	–	1.4	V
						16[a]		3.2	–	4	
Second-Breakdown Collector Current With base forward-biased and 1-s nonrepetitive pulse	$I_{S/b}$[b]		60						2.5	—	A
Second-Breakdown Energy With base reverse-biased and L = 40 mH, R_{BE} = 100Ω	$E_{S/b}$[c]				−1.5	2.5			0.125	–	J
Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 50 kHz)	$\|h_{fe}\|$		4			1			4	–	
Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 1 kHz)	h_{fe}		4			1			40	–	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$								–	1.17	°C/W

[a] Pulsed; pulse duration = 300 μs, rep. rate = 60 Hz.

[b] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward-biased for transistor operation in the active region.

[c] $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse-bias conditions. $E_{S/b} = 1/2 L I^2$ where L is a series load or leakage inductance and I is the peak collector current.

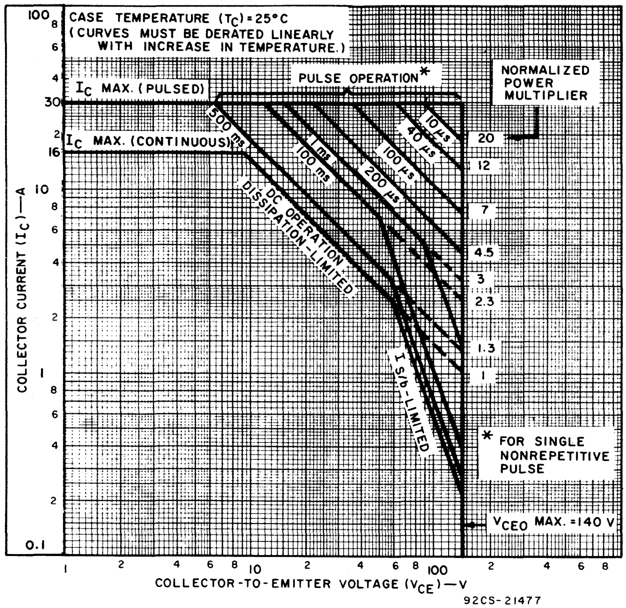


Fig. 1 — Maximum operating areas.

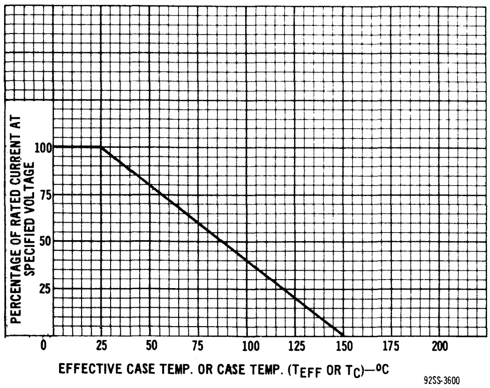


Fig. 2— Current derating curve.

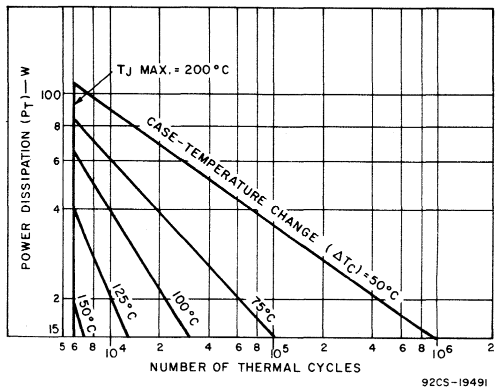


Fig. 3— Thermal-cycling chart.

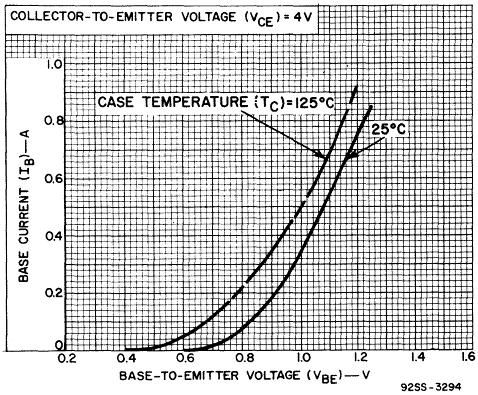


Fig. 4 — Typical input characteristics.

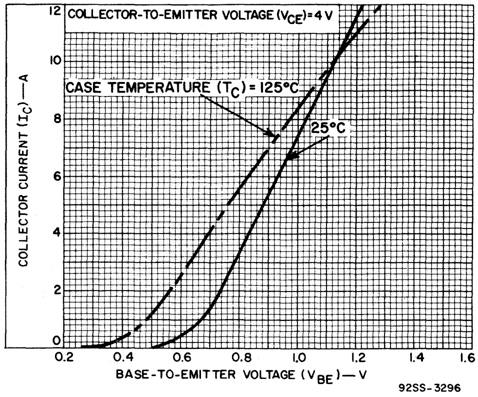


Fig. 5 — Typical transfer characteristics.

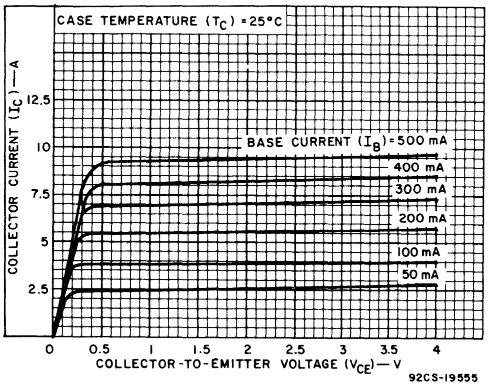


Fig. 6 — Typical output characteristics.

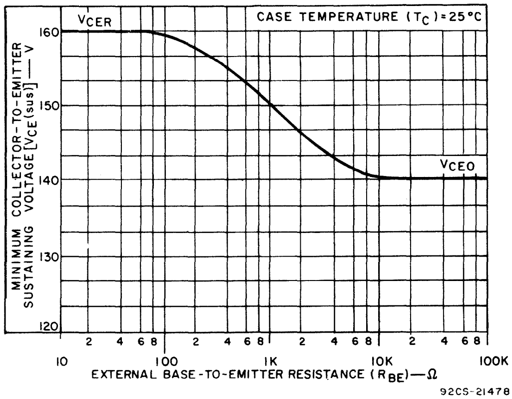


Fig. 7 — Sustaining voltage vs. base-to-emitter resistance.

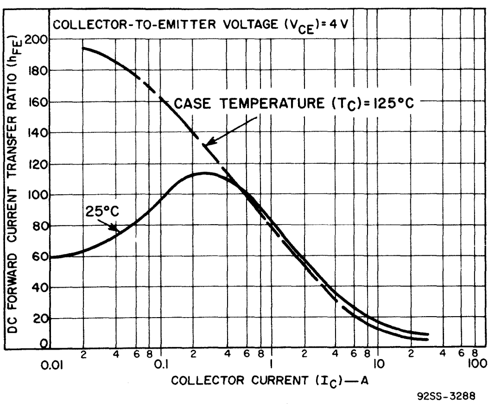


Fig. 8 — Typical dc beta characteristics.

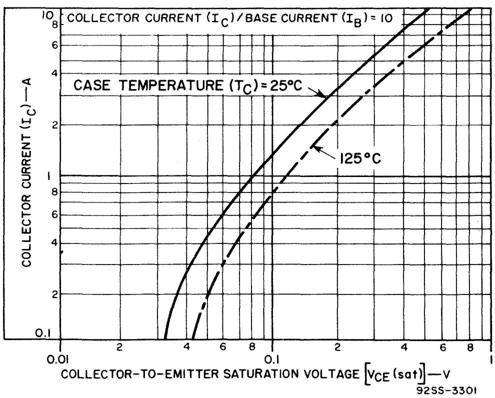


Fig. 9 — Typical saturation-voltage characteristics.

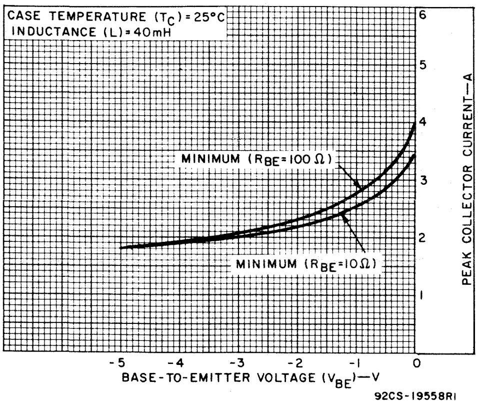
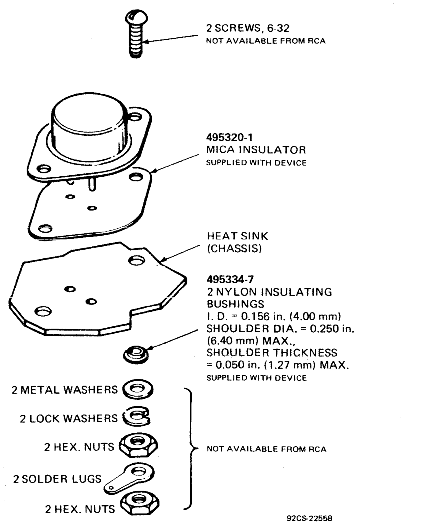


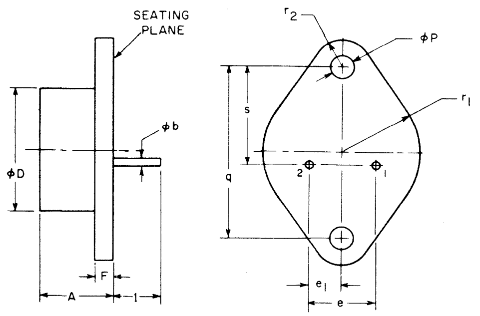
Fig. 10 — Reverse-bias second-breakdown characteristics.



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 11— Suggested mounting hardware.

DIMENSIONAL OUTLINE JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
φb	0.038	0.043	0.97	1.09	2
φD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e_1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
l	0.312		7.92		2
φP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r_1		0.525		13.34	
r_2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

TERMINAL CONNECTIONS

Pin 1 — Base
Pin 2 — Emitter
Case — Collector
Mounting Flange — Collector

NOTES:

1. **These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.**
2. **Two pins.**

92CS—15222

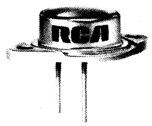
When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.

For basic transistor theory, circuits, and application information, refer to "RCA Solid State Power Circuits Designer's Handbook", SP-52, or "RCA Transistor, Thyristor, & Diode Manual", SC-15.

RCA Solid State Division

Power Transistors

2N5575 2N5578



Modified JEDEC TO-3
(0.060-In.-Dia. Pins)

H-1811

High-Current, High-Power, Hometaxial-Base Silicon N-P-N Transistors

For Linear and Switching Applications in Military, Commercial, and Industrial Equipment

Features:

- **Maximum safe-area-of operation curves**
- **$I_{S/b}$-limit line beginning at 25 V**
- **High-current capability**
- **Low saturation voltage at high beta**
- **High-dissipation capability**
- **Low thermal resistance**

RCA-2N5575 and 2N5578● are high-current, high-power, hometaxial-base silicon n-p-n transistors. They differ in maximum voltage and current ratings.

These power transistors are intended for a wide variety of high-current, high-power linear and switching applications such as low- to medium-frequency amplifiers, switching and linear regulators, power-switching circuits, series- or shunt-regulator driver and output stages, dc-to-dc converters, inverters, control circuits, and solenoid (hammer)/relay drivers.

The high-current capability (100-A peak) makes these types particularly suitable for circuit designs that now require several low-current types connected in parallel.

● Formerly RCA Dev. Nos. TA7016 and TA7017, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N5575	2N5578	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	70	90	V
*COLLECTOR-TO-EMITTER VOLTAGE:				
With base open, sustaining	$V_{CEO}(sus)$	50	70	V
With external base-to-emitter resistance (R_{BE}) = 10 Ω & V_{BE} = −1.5 V	V_{CEX}	70	90	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	8	8	V
*COLLECTOR CURRENT (Continuous)	I_C	80	60	A
*COLLECTOR CURRENT (Peak)		100	80	A
*BASE CURRENT (Continuous)	I_B	20	15	A
*TRANSISTOR DISSIPATION:	P_T			
At case temperatures up to 25°C and V_{CE} up to 25 V		300	300	W
At case temperatures of 100°C and V_{CB} of 25 V		150	150	W
At case temperatures up to 25°C and V_{CE} above 25 V		See Fig. 1		
At case temperatures above 25°C and V_{CE} above 25 V		See Figs. 1 & 2		
*TEMPERATURE RANGE:				
Operating (Junction)		−65 to 175		°C
Storage		−65 to 200		°C
*PIN TEMPERATURE (During Soldering):				
At distance ≥ 1/32 in. (0.8 mm) from case for 10 s max.		230		°C

* In accordance with JEDEC registration data format JS-6 RDF-1.

11-73

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Voltage V dc				Current A dc			LIMITS 2N5575		2N5578		UNITS
		V_{CE}	V_{CB}	V_{EB}	V_{BE}	I_C	I_B	I_E	Min.	Max.	Min.	Max.	
* Collector Cutoff Current: With base-emitter junction reverse-biased	I_{CEV}	60 80			−1.5 −1.5				– –	10 –	– –	– 10	mA
With external base-emitter resistance (R_{BE})=10 Ω	I_{CER}	50 70							– –	5 –	– –	– 5	mA
* With base-emitter junction reverse-biased	I_{CEV} (T_C=150°C)	60 80			−1.5 −1.5				– –	20 –	– –	– 20	mA
* Emitter Cutoff Current	I_{EBO}			8					–	10	–	10	mA
* Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$					0.2	0		50	–	70	–	
* DC Forward Current Transfer Ratio	h_{FE}[a]	3 4				40 60			– 10	– 40	10 –	40 –	
Collector-to-Emitter Sustaining Voltage: (See Figs. 5 & 6) With base open	$V_{CEO}(sus)$					0.2			50[b]	–	70[b]	–	V
With base-emitter junction reverse-biased & R_{BE}=10 Ω	$V_{CEX}(sus)$				−1.5	0.2			70[b]	–	90[b]	–	V
Base-to-Emitter Voltage	V_{BE}[a]	4 4				40 60			– –	– 3	– –	2.5 –	V
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$[a]					40 60	4 6		– –	– 2	– –	1.5 –	V
* Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$[a]					40 60	4 6		– –	– 3	– –	2.5 –	V
Output Capacitance	C_{ob}		10					0	–	2000	–	2000	pF
Input Capacitance	C_{ib}			0.5		0			–	4000	–	4000	pF
* Magnitude of Common-Emitter, Small-Signal, Short-Circuit Forward Current Transfer Ratio (f=0.2 MHz)	$\|h_{fe}\|$	4				10			2	–	2	–	
* Saturated Switching Time: Turn-on time	t_{ON}	V_{CC}= 30 V				40 60	4 6		– –	– 15	– –	10 –	µs
Turn-off time	t_{OFF}	V_{CC}= 30 V				40 60	4 6		– –	– 15	– –	10 –	µs
Second-Breakdown Collector Current (With base forward-biased)	$I_{S/b}$[c]	25							12[d]	–	12[d]	–	A
Second Breakdown Energy (With base reverse-biased, R_{BE}=10 Ω, L=33 mH)	$E_{S/b}$[e]				−1.5	7			0.8	–	0.8	–	J
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$								–	0.5	–	0.5	°C/W

[a]Pulsed; pulse duration ≤ 350 µs, duty factor=0.02.

[b]CAUTION: The sustaining voltages $V_{CEO}(sus)$ and $V_{CEX}(sus)$ MUST NOT be measured on a curve tracer. These sustaining voltages should be measured by means of the test circuit shown in Fig. 5.

[c]$I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward-biased for transistor operation in the active region.

[d]Pulsed; 1-s, non-repetitive pulse.

[e]$E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse-bias conditions. $E_{S/b}=1/2LI^2$ where L is a series load or leakage inductance and I is the peak collector current.

*In accordance with JEDEC registration data format JS-6 RDF-1.

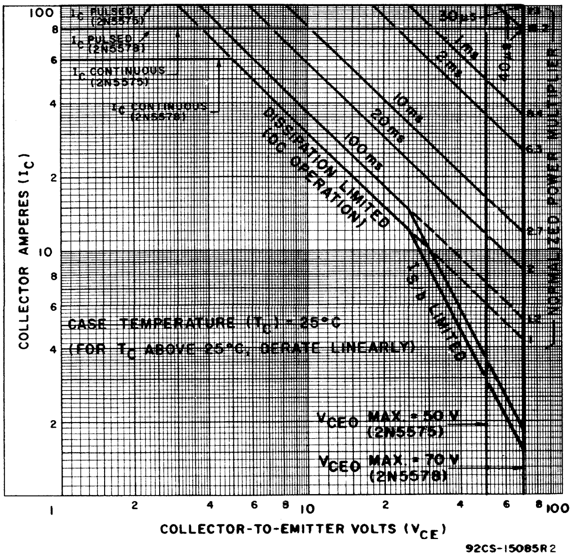


Fig. 1—Maximum operating areas for both types.

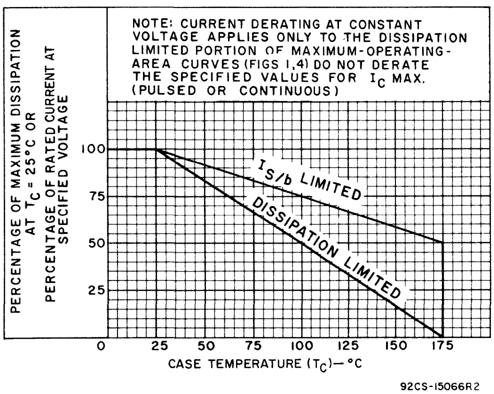


Fig. 2—Dissipation derating curves for both types.

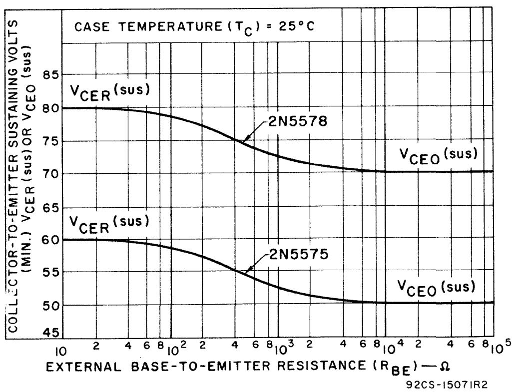


Fig. 3—Collector-to-emitter sustaining voltage characteristics for both types.

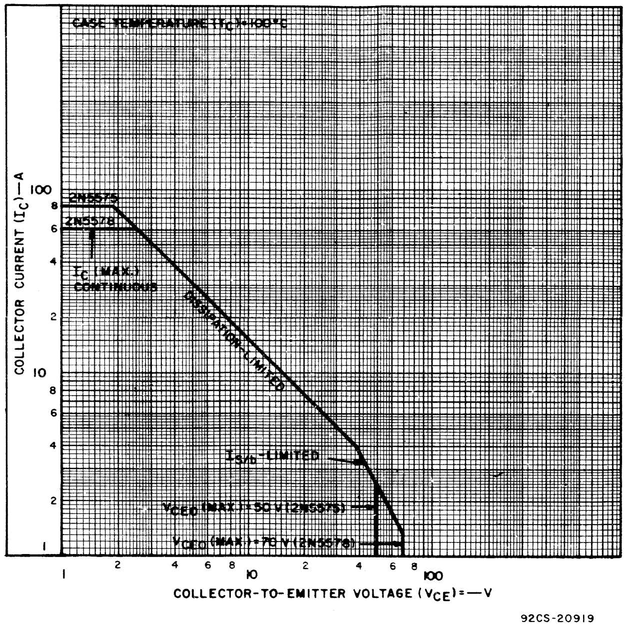


Fig. 4—Maximum operating areas for both types.

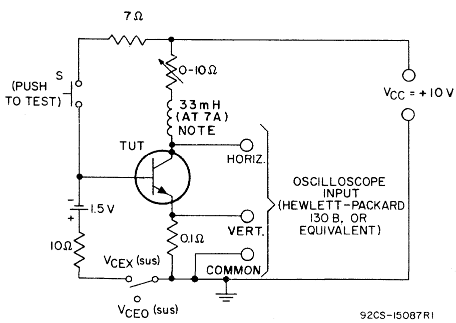
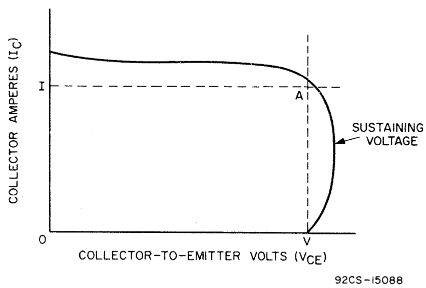


Fig. 5—Circuit used to measure sustaining voltages $V_{CEO}(sus)$ and $V_{CEX}(sus)$ for both types.



NOTE:
The sustaining Voltage $V_{CEO}(sus)$ or $V_{CEX}(sus)$ is acceptable when the trace falls to the right and above point "A". (For values of current and voltage, see *Electrical Characteristics.*)

Fig. 6—Oscilloscope display for measurement of sustaining voltages (test circuit shown in Fig. 5).

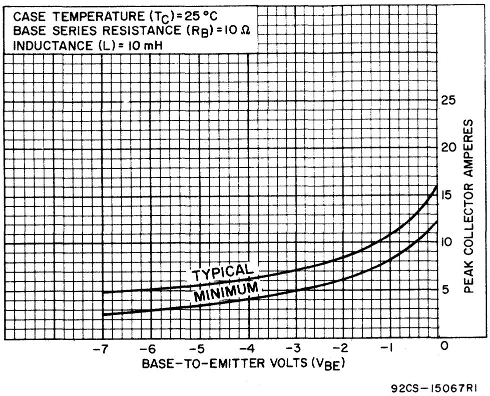


Fig. 7—Reverse-bias second-breakdown characteristics for both types.

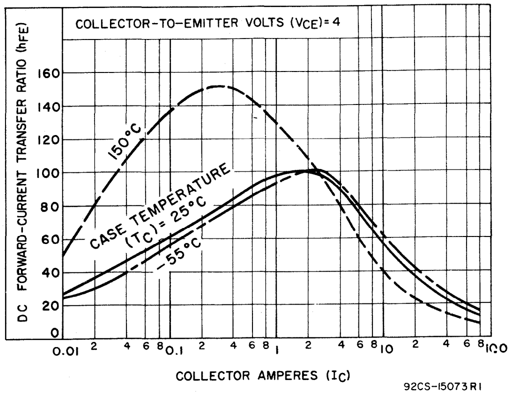


Fig. 8—Typical dc beta characteristics for type 2N5575.

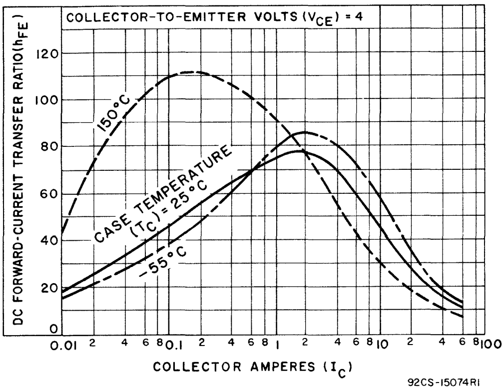


Fig. 9—Typical dc beta characteristics for type 2N5578.

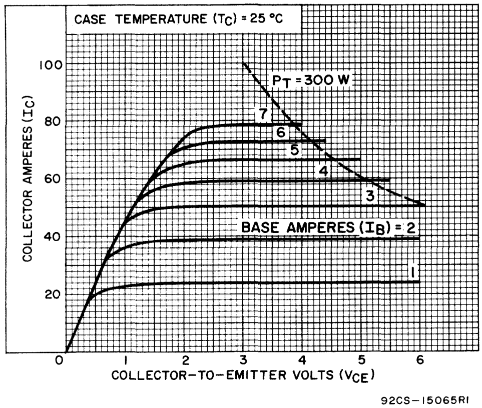


Fig. 10—Typical output characteristics for type 2N5575.

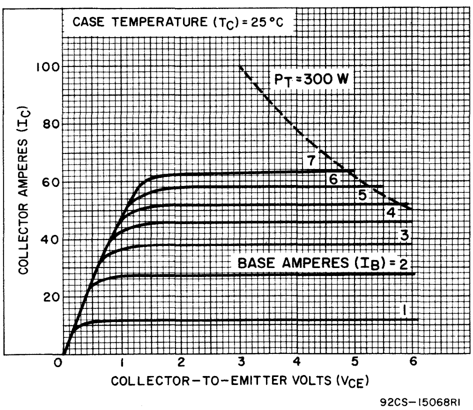


Fig. 11—Typical output characteristics for type 2N5578.

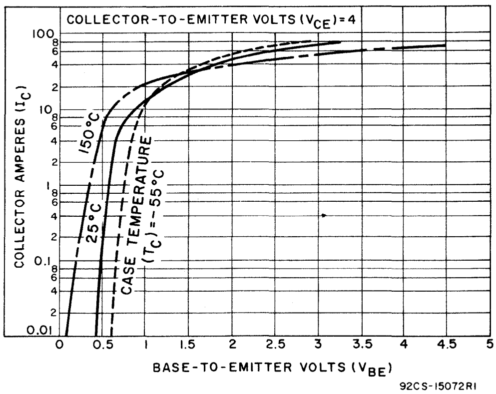


Fig. 12—Typical transfer characteristics for type 2N5575.

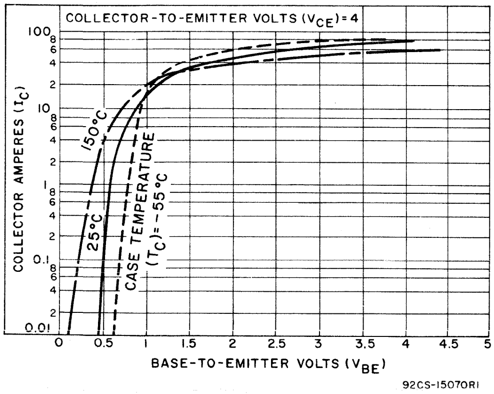


Fig. 13—Typical transfer characteristics for type 2N5578.

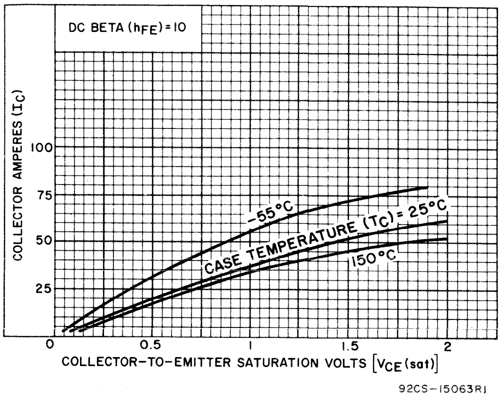


Fig. 14—Typical saturation voltage characteristics for type 2N5575.

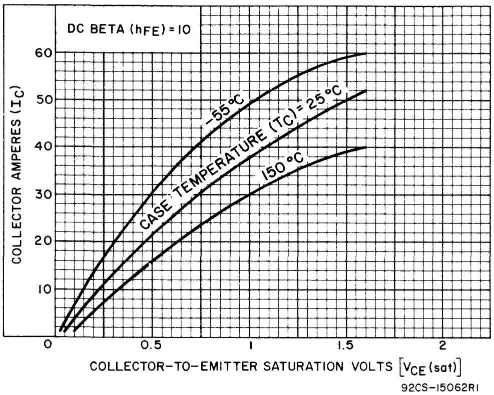


Fig. 15—Typical saturation voltage characteristics for type 2N5578.

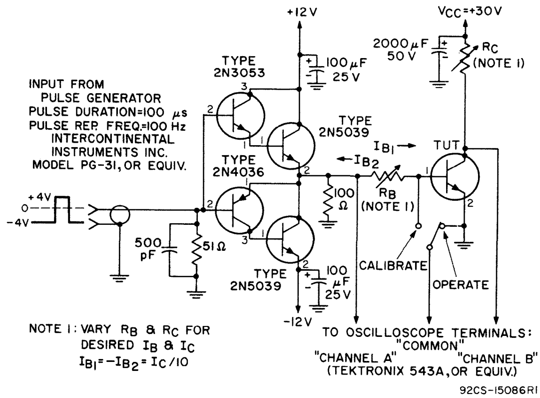


Fig. 16—Circuit used to measure switching times for both types.

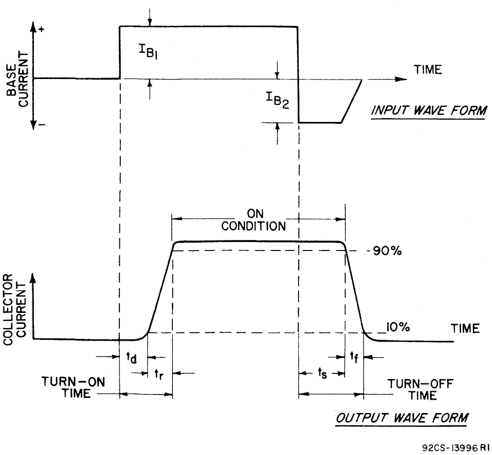


Fig. 17—Oscilloscope display for measurement of switching times (test circuit shown in Fig. 16).

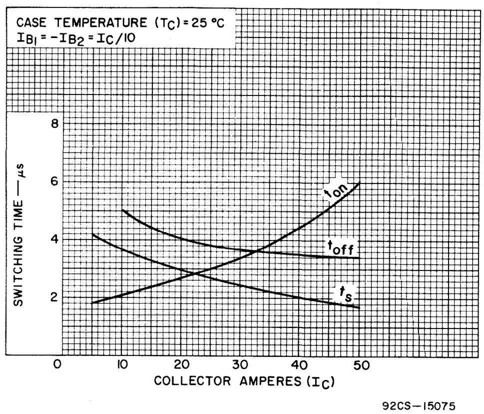
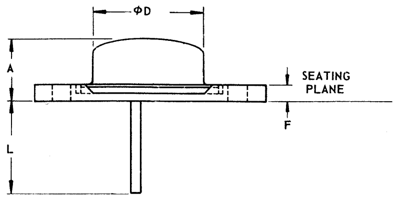
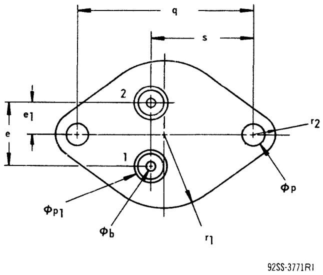


Fig. 18—Typical saturated switching characteristics for both types.





SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.416	0.450	10.57	11.43	
φb	0.059	0.62	1.499	1.575	
φD	0.750	0.771	19.05	19.583	
e	0.420	0.440	10.67	11.18	
e_1	0.205	0.225	5.21	5.72	
F	0.100	0.114	2.54	2.89	
L	0.595	0.625	15.12	15.87	1
φp	0.151	0.161	3.84	4.09	
ϕp_1	0.200	0.285	5.08	7.239	2
q	1.177	1.197	29.90	30.40	
r_1	–	0.525	–	13.34	
r_2	–	0.188	–	4.78	
s	0.655	0.675	16.64	17.15	

NOTES:

1. Two pins.
2. Clearance holes for both pins should be 0.285 in. (7.24 mm) min. dia.

TERMINAL CONNECTIONS

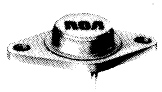
Pin 1 – Base
Pin 2 – Emitter
Case – Collector
Mounting Flange – Collector

Epitaxial-Base Power Transistors

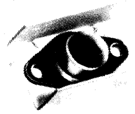
Solid State Division

Power Transistors

2N5954 2N6372 2N6467 40829
2N5955 2N6373 2N6468 40830
2N5956 2N6374 40831



JEDEC TO-66 H-1340



JEDEC TO-66
With Integral Heat Radiator H-1470A

Silicon N-P-N and P-N-P Medium-Power Transistors

General-Purpose Types for
Switching Applications in Military,
Industrial, and Commercial Equipment

Features

- **2N5954, 2N5955, 2N5956 complements to 2N6372, 2N6373, 2N6374**
- **Low saturation voltages**
- **Maximum-safe-area-of-operation curves**
- **Thermal-cycle ratings**
- **Hermetically-sealed JEDEC TO-66 package**
- **High gain at high current**

RCA-2N5954, 2N5955, 2N5956, 2N6467, and 2N6468▲ are multiple-epitaxial p-n-p transistors. RCA-2N6372, 2N6373, and 2N6374● are multiple-epitaxial n-p-n transistors. They are complements to 2N5954, 2N5955, and 2N5956. These devices differ in voltage ratings and in the currents at which the parameters are controlled. All are supplied in the JEDEC TO-66 package.

Types 2N5954, 2N5955, and 2N5956 are available with factory-attached heat radiators as RCA types 40829, 40830, and 40831, respectively. The other devices may be obtained with heat radiators on special order. Radiator versions are intended for printed-circuit-board applications, and differ electrically from their basic counterparts only in device dissipation (5.8 W up to 25°C ambient) and thermal resistance (30°C/W max. at T_A = 25°C).

▲ Formerly RCA Dev. Nos. TA7264, TA7265, TA7266, TA8710, and TA8709, respectively.

● Formerly RCA Dev. Nos. TA8352, TA8353, and TA8354, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	N-P-N	2N6374	2N6373	2N6372			
	P-N-P	2N5956◆ 40831◆	2N5955◆ 40830◆	2N5954◆ 40829◆	2N6467◆	2N6468◆	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	70	90	110	130	V
COLLECTOR-TO-EMITTER VOLTAGE:							
* With 1.5 volts (V_{BE}) of reverse bias, and external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CEX}	50	70	90	110	130	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}	45	65	85	105	125	V
With base open	V_{CEO}	40	60	80	100	120	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	5	5	5	5	V
*CONTINUOUS COLLECTOR CURRENT	I_C	6	6	6	4	4	A
*CONTINUOUS BASE CURRENT	I_B	2	2	2	2	2	A
TRANSISTOR DISSIPATION:							
At case temperatures up to 25°C		40 (2N6374) (2N5956)	40 (2N6373) (2N5955)	40 (2N6372) (2N5954)	40 (2N6467)	40 (2N6468)	W
At ambient temperatures up to 25°C		5.8 (40831)	5.8 (40830)	5.8 (40829)	–	–	
At case temperatures above 25°C			See Figs. 1, 2, and 3.				
*TEMPERATURE RANGE:							
Storage and Operating (Junction)		←		–65 to +200		→	°C
*PIN TEMPERATURE (During Soldering):							
At distances ≥ 1/32 in. (0.8 mm) from seating plane for 10 s max.		←		+235		→	°C

* In accordance with JEDEC registration data format JS-6-RDF-2 (all types except 40829, 40830, and 40831)

◆ For p-n-p devices, voltage and current values are negative.

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ELECTRICAL CHARACTERISTICS FOR N-P-N TYPES, *At Case Temperature (T_C) = 25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS VOLTAGE V dc V_{CE}	V_{BE}	CURRENT A dc I_C	I_B	LIMITS 2N6374 Min.	Max.	2N6373 Min.	Max.	2N6372 Min.	Max.	UNITS
* Collector Cutoff Current: With external base-to-emitter resistance (R_{BE}) = 100 Ω	I_{CER}	35				–	100	–	–	–	–	μA
		55				–	–	–	100	–	–	
		75				–	–	–	–	–	100	
* With base-emitter junction reverse-biased and external base-to-emitter resistance (R_{BE}) = 100 Ω	I_{CEX}	45	−1.5			–	100	–	–	–	–	μA
		65	−1.5			–	–	–	100	–	–	
		85	−1.5			–	–	–	–	–	100	
* With base-emitter junction reverse-biased, R_{BE} = 100 Ω, and T_C = 150°C	I_{CEX}	45	−1.5			–	2	–	–	–	–	mA
		65	−1.5			–	–	–	2	–	–	
		85	−1.5			–	–	–	–	–	2	
* With base open	I_{CEO}	25				–	1	–	–	–	–	mA
		45				–	–	–	1	–	–	
		65				–	–	–	–	–	1	
* Emitter Cutoff Current	I_{EBO}		−5			–	0.1	–	0.1	–	0.1	mA
* DC Forward-Current Transfer Ratio	h_{FE}	4		3[a]		20	100	–	–	–	–	
		4		2.5[a]		–	–	20	100	–	–	
		4		2[a]		–	–	–	–	20	100	
		4		6[a]		5	–	5	–	5	–	
* Collector-to-Emitter Sustaining Voltage (see Figs. 12 and 13); With base open	$V_{CEO}(sus)$			0.1[a]		40[b]	–	60[b]	–	80[b]	–	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$			0.1[a]		45[b]	–	65[b]	–	85[b]	–	V
With base-emitter junction reverse-biased and external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CEX}(sus)$		−1.5	0.1[a]		50[b]	–	70[b]	–	90[b]	–	V
* Base-to-Emitter Voltage	V_{BE}	4		3[a]		–	2	–	–	–	–	V
		4		2.5[a]		–	–	–	2	–	–	
		4		2[a]		–	–	–	–	–	2	
		4		6[a]		–	3	–	3	–	3	
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$			3[a]	0.3	–	1	–	–	–	–	V
				2.5[a]	0.25	–	–	–	1	–	–	
				2[a]	0.2	–	–	–	–	–	1	
* Magnitude of Common Emitter, Small-Signal Short Circuit, Forward-Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	4		1		4	–	4	–	4	–	
* Common-Emitter, Small-Signal, Short-Circuit, Forward-Current Transfer Ratio (f = 1 kHz)	h_{fe}	4		0.5		25	–	25	–	25	–	
Thermal Resistance (Junction-to-case)	$R_{\theta JC}$					–	4.3	–	4.3	–	4.3	°C/W

[a] Pulsed, pulse duration = 300 μs, duty factor = 1.8%.

[b] *CAUTION: Sustaining voltages $V_{CEO}(sus)$, $V_{CER}(sus)$, and $V_{CEX}(sus)$ MUST NOT be measured on a curve tracer.*

* In accordance with JEDEC registration data format JS-6 RDF-2.

ELECTRICAL CHARACTERISTICS FOR P-N-P TYPES, *At Case Temperature (T_C) = 25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: VOLTAGE V dc V_{CE}	VOLTAGE V dc V_{BE}	CURRENT A dc I_C	CURRENT A dc I_B	LIMITS 2N5956 40831 Min.	2N5956 40831 Max.	2N5955 40830 Min.	2N5955 40830 Max.	2N5954 40829 Min.	2N5954 40829 Max.	2N6467 Min.	2N6467 Max.	2N6468 Min.	2N6468 Max.	UNITS
Collector-Cutoff Current: With external base-to-emitter resistance (R_{BE}) = 100 Ω	I_{CER}	–35				–	–100	–	–	–	–	–	–	–	–	µA
		–55				–	–	–	–100	–	–	–	–	–	–	
		–75				–	–	–	–	–	–100	–	–	–	–	
		–95				–	–	–	–	–	–	–	–100	–	–	
		–110				–	–	–	–	–	–	–	–	–	–100	
* With base-emitter junction reverse-biased, R_{BE} = 100 Ω	I_{CEX}	–45	1.5			–	–100	–	–	–	–	–	–	–	–	µA
		–65	1.5			–	–	–	–100	–	–	–	–	–	–	
		–85	1.5			–	–	–	–	–	–100	–	–	–	–	
		–100	1.5			–	–	–	–	–	–	–	–100	–	–	
		–120	1.5			–	–	–	–	–	–	–	–	–	–100	
* With base-emitter junction reverse-biased, R_{BE} = 100 Ω, and T_C = 150°C	I_{CEX}	–45	1.5			–	–2	–	–	–	–	–	–	–	–	mA
		–65	1.5			–	–	–	–2	–	–	–	–	–	–	
		–85	1.5			–	–	–	–	–	–2	–	–	–	–	
		–100	1.5			–	–	–	–	–	–	–	–2	–	–	
		–120	1.5			–	–	–	–	–	–	–	–	–	–2	
* With base open	I_{CEO}	–25				–	–1	–	–	–	–	–	–	–	–	mA
		–45				–	–	–	–1	–	–	–	–	–	–	
		–65				–	–	–	–	–	–1	–	–	–	–	
		–50				–	–	–	–	–	–	–	–1	–	–	
		–60				–	–	–	–	–	–	–	–	–	–1	
* Emitter-Cutoff Current	I_{EBO}		5			–	–0.1	–	–0.1	–	–0.1	–	–0.1	–	–0.1	mA
* DC Forward-Current Transfer Ratio	h_{FE}	–4		–3[a]		20	100	–	–	–	–	–	–	–	–	
		–4		–2.5[a]		–	–	20	100	–	–	–	–	–	–	
		–4		–2[a]		–	–	–	–	20	100	–	–	–	–	
		–4		–15[a]		–	–	–	–	–	–	15	150	15	150	
		–4		–6[a]		5	–	5	–	5	–	–	–	–	–	
		–4		–4[a]		–	–	–	–	–	–	5	–	5	–	
* Collector-to-Emitter Sustaining Voltage (See Figs. 12 and 13). With base open	$V_{CEO}(sus)$			–0.1[a]		–40[b]	–	–60[b]	–	–80[b]	–	–100[b]	–	–120[b]	–	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$			–0.1[a]		–45[b]	–	–65[b]	–	–85[b]	–	–105[b]	–	–125[b]	–	V
With base-emitter junction reverse biases and external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CEX}(sus)$		1.5	–0.1[a]		–50[b]	–	–70[b]	–	–90[b]	–	–110[b]	–	–130[b]	–	V
* Base-to-Emitter Voltage	V_{BE}	–4		–3[a]		–	–2	–	–	–	–	–	–	–	–	V
		–4		–2.5[a]		–	–	–	–2	–	–	–	–	–	–	
		–4		–2[a]		–	–	–	–	–	–2	–	–	–	–	
		–4		–1.5[a]		–	–	–	–	–	–	–	–2	–	–2	
		–4		–4[a]		–	–	–	–	–	–	–	–3.5	–	–3.5	
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$			–1.5[a]	–0.15	–	–	–	–	–	–	–	–1.2	–	–1.2	V
				–3[a]	–0.3	–	–1	–	–	–	–	–	–	–	–	
				–2.5[a]	–0.25	–	–	–	–1	–	–	–	–	–	–	
				–2[a]	–0.2	–	–	–	–	–	–1	–	–	–	–	
				–4[a]	–0.8	–	–	–	–	–	–	–	–4	–	–4	
* Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward-Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	–4		–1		5	–	5	–	5	–	5	–	5	–	
* Common-Emitter, Small-Signal, Short-Circuit, Forward-Current Transfer Ratio (f = 1 kHz)	h_{fe}	–4		–0.5		25	–	25	–	25	–	25	–	25	–	
Thermal Resistance: Junction-to-case	$R_{\theta JC}$					– (2N5956)	4.3 (2N5956)	– (2N5955)	4.3 (2N5955)	– (2N5954)	4.3 (2N5954)	–	4.3	–	4.3	°C/W
Junction-to-ambient	$R_{\theta JA}$					– (40831)	30 (40831)	– (40830)	30 (40830)	– (40829)	30 (40829)	–	–	–	–	°C/W

[a] Pulsed; pulse duration = 300 µs, duty factor = 1.8%.

[b] *CAUTION: Sustaining voltages $V_{CEO}(sus)$, $V_{CER}(sus)$, and $V_{CEX}(sus)$ MUST NOT be measured on a curve tracer.*

* In accordance with JEDEC registration data format JS-6-RDF-2 (all types except 40829, 40830, and 40831).

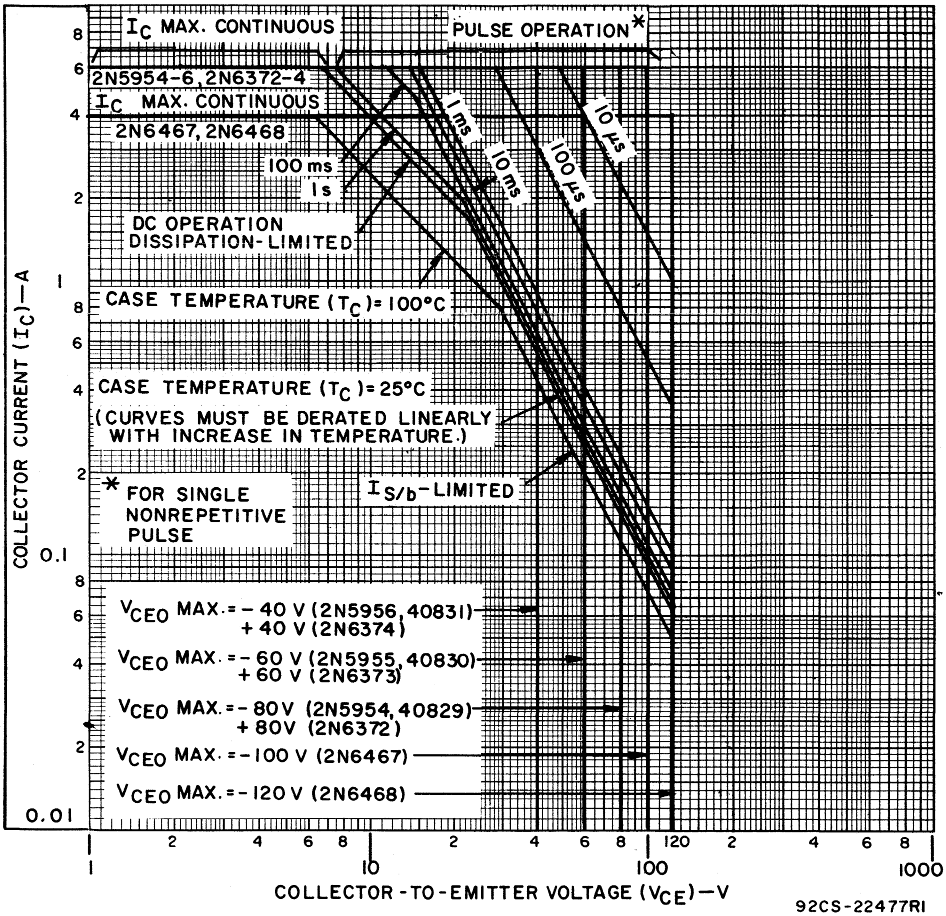


Fig.1 — Maximum operating areas for all types.

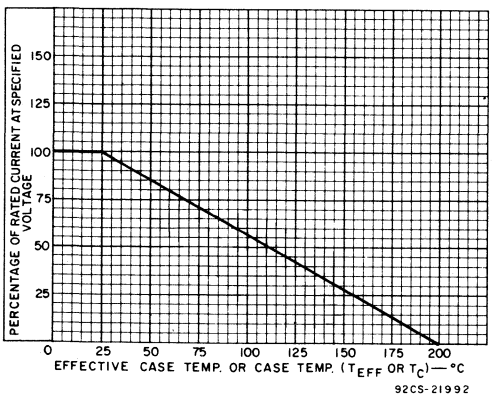


Fig.2 — Current derating curve for all types.

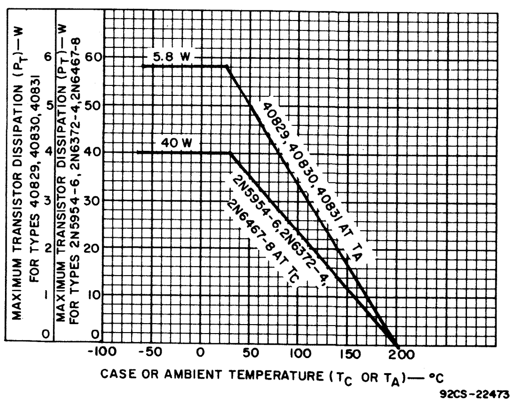


Fig.3 — Dissipation derating curve for all types.

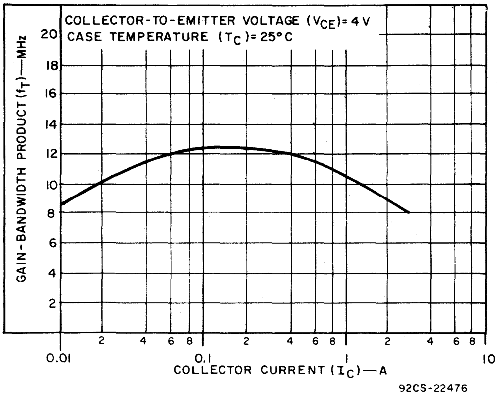


Fig.4 — Typical gain-bandwidth product for all types.♦

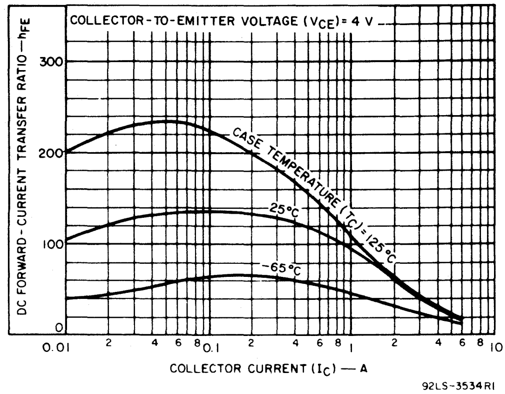


Fig.5 — Typical dc beta characteristics for all types.♦

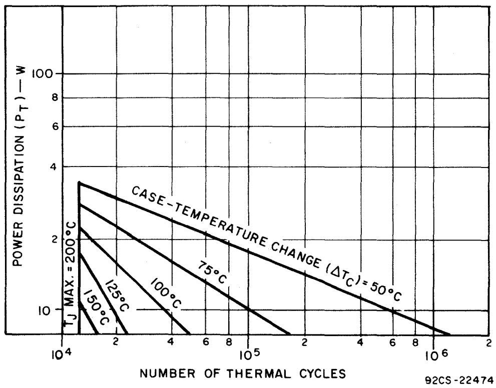


Fig.6 — Thermal-cycling rating chart for all types.

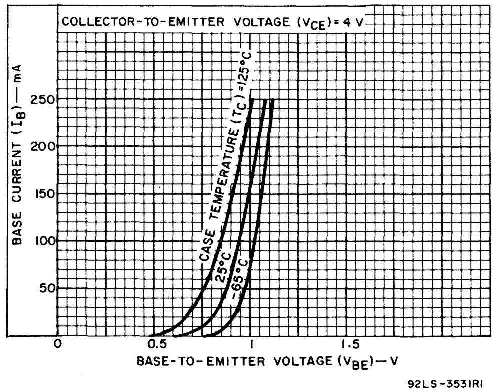


Fig.7 — Typical input characteristics for all types.♦

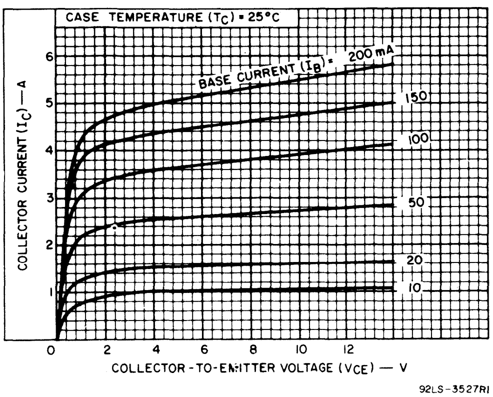


Fig.8 — Typical output characteristics for all types.♦

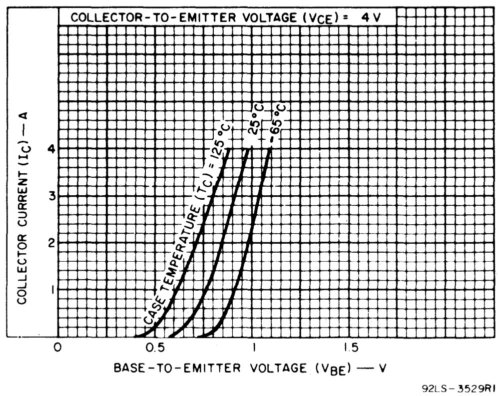


Fig.9 — Typical transfer characteristics for all types.♦

♦ For p-n-p devices, voltage and current values are negative.

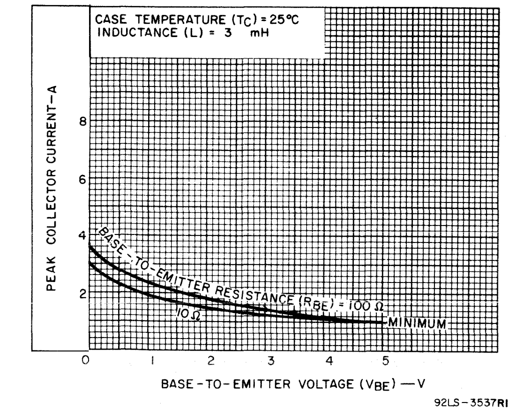


Fig.10 — Minimum reverse-bias second-breakdown characteristics for all types.♦

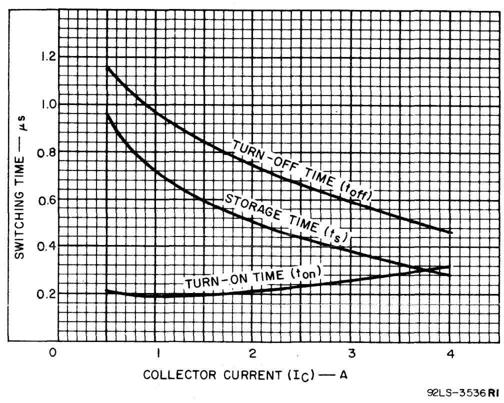
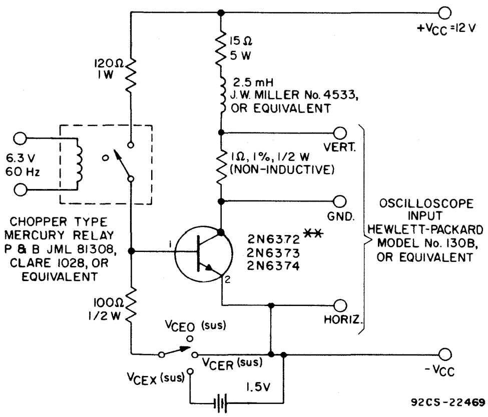
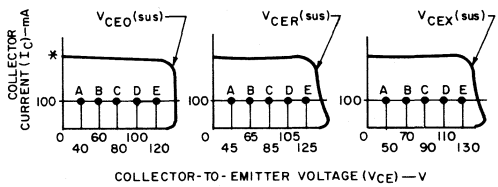


Fig.11 — Typical saturated switching characteristics for all types.♦



**FOR P-N-P TYPES 2N5954, 2N5955, 2N5956, 2N6467, AND 2N6468, 40829, 40830, AND 40831, REVERSE POLARITY OF V_{CC} AND BATTERY.

Fig.12 — Circuit used to measure sustaining voltages V_{CEO}(sus) V_{CER}(sus), and V_{CEX}(sus).

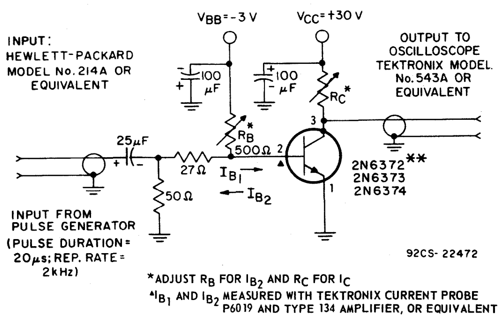


* PULSE CURRENT (I_P) RANGE MUST BE 0.2-0.4A

92CS-22475

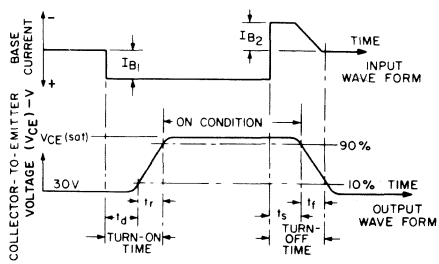
The sustaining voltages, V_{CEO}(sus), V_{CER}(sus), and V_{CEX}(sus), are acceptable when the traces fall to the right of point "A" for types 2N5956, 40831, and 2N6374; point "B" for types 2N5955, 40830, and 2N6373; point "C" for types 2N5954, 40829, and 2N6372; point "D" for type 2N6467, and point "E" for type 2N6468.

Fig.13 — Oscilloscope display for measurement for sustaining voltages (test circuit shown in Fig. 12).♦



** FOR P-N-P TYPES 2N5954, 2N5955, 2N5956, 2N6467, 2N6468, 40829, 40830, AND 40831, REVERSE DIRECTION OF I_{B1} AND I_{B2} AND REVERSE POLARITY OF CAPACITORS, V_{CC}, V_{BB}.

Fig.14 — Circuit used to measure saturated switching times.

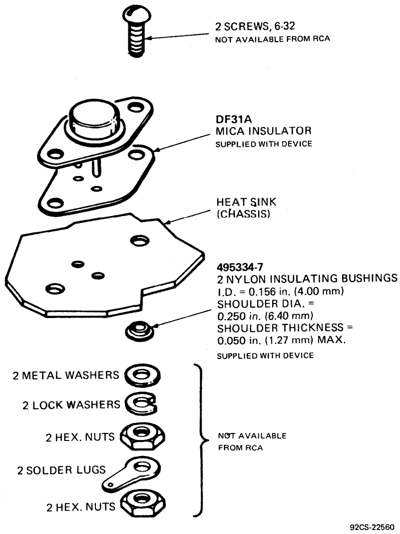


* FOR P-N-P TYPES 2N5954, 2N5955, 2N5956, 2N6467, 2N6468 40829, 40830, AND 40831, THE BASE-CURRENT WAVE FORM WILL BE INVERTED.

92CS-22470

Fig.15 — Oscilloscope display for measurement of switching times.

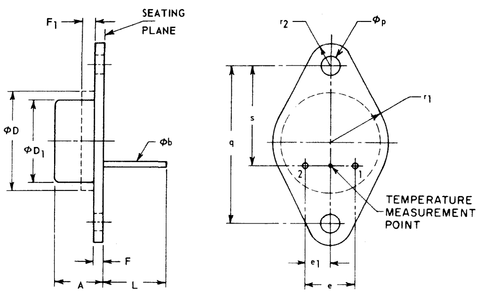
♦ For p-n-p devices, voltage and current values are negative.



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 16 — Suggested mounting hardware for JEDEC TO-66.

DIMENSIONAL OUTLINE
JEDEC TO-66



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.340	6.35	8.64	
φb	0.028	0.034	0.711	0.863	
φD	–	0.620	–	15.75	
φD1	0.470	0.500	11.94	12.70	
e	0.190	0.210	4.83	5.33	
e1	0.093	0.107	2.36	2.72	
F	0.050	0.075	1.27	1.91	2
F1	–	0.050	–	1.27	1
L	0.360	–	9.14	–	
φp	0.142	0.152	3.61	3.86	
q	0.958	0.962	24.33	24.43	
r1	–	0.350	–	8.89	
r2	–	0.145	–	3.68	
s	0.570	0.590	14.48	14.99	

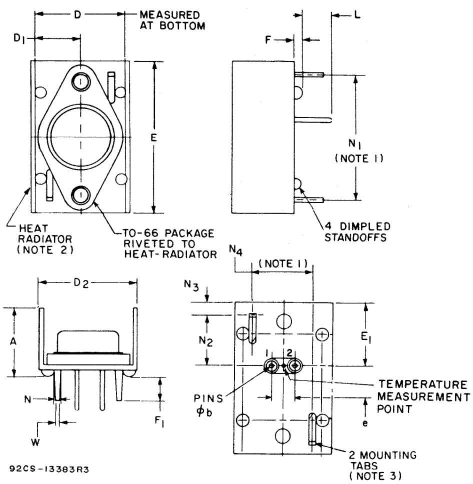
NOTES:
1. The outline contour is optional within zone defined by φD and F_1
2. Dimension does not include sealing flange.

92SS-3738

TERMINAL CONNECTIONS

Pin 1 — Base
Pin 2 — Emitter
Case, Mounting Flange — Collector

DIMENSIONAL OUTLINE
JEDEC TO-66 WITH HEAT RADIATOR



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	0.595	–	15.11	
φb	0.028	0.034	0.711	0.864	
D	0.750	0.760	19.05	19.30	
D1	0.375	0.380	9.52	9.65	
D2	0.820	0.920	20.83	23.37	
E	1.297	1.327	32.94	33.70	
E1	0.551	0.561	13.99	14.25	
e	0.190	0.210	4.83	5.33	
F	0.30	0.55	7.62	13.97	
F1	0.175	0.210	4.44	5.33	
L	0.170	–	4.31	–	
N	0.052	0.065	1.32	1.65	
N1	1.098	1.102	27.89	27.99	1
N2	0.448	0.452	11.38	11.47	
N3	0.099	0.113	0.25	0.29	
N4	0.498	0.502	12.65	12.75	1
W	0.048	0.060	1.22	1.52	

NOTES:
1. Measured at bottom of heat radiator.
2. 0.035 in. (0.889) C.R.S., tin plated.
3. Recommended hole size for printed-circuit board is 0.070 in. (1.778) dia.

TERMINAL CONNECTIONS

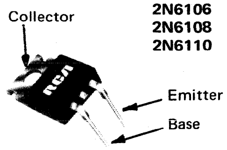
Pin 1 — Base
Pin 2 — Emitter
Heat Radiator — Collector

RCA
Solid State
Division

Power Transistors

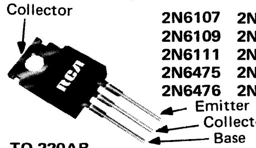
2N6288-2N6293 2N6473-2N6474
2N6106-2N6111 2N6475-2N6476

2N6106	2N6289
2N6108	2N6291
2N6110	2N6293



TO-220AA H-1534R1

2N6107	2N6288
2N6109	2N6290
2N6111	2N6292
2N6475	2N6473
2N6476	2N6474



TO-220AB H-1535R1

Epitaxial-Base, Silicon N-P-N and P-N-P VERSAWATT Transistors

General-Purpose Medium-Power Types for Switching and Amplifier Applications

Features

- **Low saturation voltages**
- **VERSAWATT package (molded silicone plastic)**
- **Complementary n-p-n and p-n-p types**
- **Thermal-cycling ratings**
- **Maximum safe-area-of-operation curves specified for dc operation**

RCA-2N6106–2N6111, 2N6288–2N6293, and 2N6473–2N6476 are epitaxial-base silicon transistors supplied in a VERSAWATT package. The 2N6288–2N6293, 2N6473, and 2N6474• are n-p-n complements of p-n-p types 2N6106–2N6111, 2N6475, and 2N6476▪ respectively. All these transistors are intended for a wide variety of medium-power switching and amplifier applications, such as series and shunt regulators and driver and output stages of high-fidelity amplifiers.

The 2N6289, 2N6291, and 2N6293 n-p-n types and 2N6106, 2N6108, and 2N6110 p-n-p devices fit into TO-66 sockets. The remaining types are supplied in the JEDEC TO-220AB straight-lead version of the VERSAWATT package. All of these devices are also available on special order in a variety of lead-form configurations. Detailed information on these and other VERSAWATT outlines is contained in "RCA's Lineup of Power Transistors" (PSP-704).

• Formerly RCA Dev. Nos. TA7784, TA8323, TA7783, TA8232, TA7782, TA8231, TA8444, and TA8723, respectively.

▪ Formerly RCA Dev. Nos. TA8210, TA7741, TA8211, TA7742, TA8212, TA7743, TA8445, and TA8722, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	N-P-N	2N6288 2N6289	2N6290 2N6291	2N6292 2N6293	2N6473	2N6474	
	P-N-P	2N6110♦ 2N6111♦	2N6108♦ 2N6109♦	2N6106♦ 2N6107♦	2N6475♦	2N6476♦	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	40	60	80	110	130	V
*COLLECTOR-TO-EMITTER VOLTAGE:							
With external base-supply resistance (R_{BB}) = 100Ω, and base supply voltage (V_{BB}) = 0	V_{CEX}	40	60	80	110	130	V
With base open	V_{CEO}	30	50	70	100	120	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	5	5	5	5	V
*COLLECTOR CURRENT (Continuous)							
At case temperature ⩽ 106°C	I_C	7	7	7	4	4	A
*BASE CURRENT (Continuous)							
At case temperature ⩽ 130°C	I_B	3	3	3	2	2	A
TRANSISTOR DISSIPATION:	P_T						
At case temperatures up to 25°C		40	40	40	40	40	W
* At case temperatures up to 100°C		16	16	16	16	16	W
At ambient temperatures up to 25°C		1.8	1.8	1.8	1.8	1.8	W
At case temperatures above 25°C		Derate linearly at 0.32 W/°C, or see Fig. 2.					
* At case temperatures above 100°C		Derate linearly at 0.32 W/°C					
At ambient temperatures above 25°C		Derate linearly at 0.0144 W/°C					
*TEMPERATURE RANGE:							
Storage and Operating (Junction)		←—— -65 to 150 ——→					°C
*LEAD TEMPERATURE (During Soldering):							
At distance ⩾ 1/8 in. (3.17 mm) from case for 10 s max.		←—— 235 ——→					°C

* In accordance with JEDEC registration data format (JS-6, RDF-2).

♦ For p-n-p devices, voltage and current values are negative.

10-73

ELECTRICAL CHARACTERISTICS FOR N-P-N TYPES, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: VOLTAGE V dc		CURRENT A dc		LIMITS: 2N6292 2N6293		2N6290 2N6291		2N6288 2N6289		2N6474		2N6473		UNITS
		V_{CE}	V_{BE}	I_C	I_B	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Collector-Cutoff Current: With external base-to-emitter resistance (R_{BE}) = 100 Ω	I_{CER}	75				–	0.1	–	–	–	–	–	–	–	–	mA
		55				–	–	–	0.1	–	–	–	–	–	–	
		35				–	–	–	–	–	0.1	–	–	–	–	
		120				–	–	–	–	–	–	–	0.1	–	–	
		100				–	–	–	–	–	–	–	–	–	0.1	
With (R_{BE}) = 100 Ω and T_C = 150°C		70				–	2	–	–	–	–	–	–	–	–	
		50				–	–	–	2	–	–	–	–	–	–	
		30				–	–	–	–	–	2	–	–	–	–	
T_C = 100°C		120				–	–	–	–	–	–	–	2	–	–	
		100				–	–	–	–	–	–	–	–	–	2	
* With base-emitter junction reverse-biased	I_{CEX}	75	−1.5			–	0.1	–	–	–	–	–	–	–	–	mA
		56	−1.5			–	–	–	0.1	–	–	–	–	–	–	
		37.5	−1.5			–	–	–	–	–	0.1	–	–	–	–	
		120	−1.5			–	–	–	–	–	–	–	0.1	–	–	
		100	−1.5			–	–	–	–	–	–	–	–	–	0.1	
* With base-emitter junction reverse-biased and T_C = 150°C		70	−1.5			–	2	–	–	–	–	–	–	–	–	
		50	−1.5			–	–	–	2	–	–	–	–	–	–	
		30	−1.5			–	–	–	–	–	2	–	–	–	–	
T_C = 100°C		120	−1.5			–	–	–	–	–	–	–	2	–	–	
		100	−1.5			–	–	–	–	–	–	–	–	–	2	
* With base open	I_{CEO}	20			0	–	–	–	–	–	1	–	–	–	–	mA
		40			0	–	–	–	1	–	–	–	–	–	–	
		60			0	–	1	–	–	–	–	–	1	–	–	
		50			0	–	–	–	–	–	–	–	–	–	1	
* Emitter-Cutoff Current	I_{EBO}		−5	0		–	1	–	1	–	1	–	1	–	1	mA
* Collector-to-Emitter Sustaining Voltage With base open	$V_{CEO}(sus)$			0.1[a]	0	70	–	50	–	30	–	120	–	100	–	V
With external base-to emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$			0.1		80	–	60	–	40	–	130	–	110	–	V
* DC Forward-Current Transfer Ratio	h_{FE}	4		2[a]		30	150	–	–	–	–	–	–	–	–	
		4		2.5[a]		–	–	30	150	–	–	–	–	–	–	
		4		3[a]		–	–	–	–	30	150	–	–	–	–	
		4		1.5[a]		–	–	–	–	–	–	15	150	15	150	
		2.5		4[a]		–	–	–	–	–	–	2	–	2	–	
		4		6.5[a]		5	–	5	–	5	–	–	–	–	–	
* Base-to-Emitter Voltage	V_{BE}	4		2[a]		–	1.5	–	–	–	–	–	–	–	–	V
		4		2.5[a]		–	–	–	1.5	–	–	–	–	–	–	
		4		3[a]		–	–	–	–	–	1.5	–	–	–	–	
		4		6.5[a]		–	3	–	3	–	3	–	–	–	–	
		4		1.5[a]		–	–	–	–	–	–	–	2	–	2	
		2.5		4[a]		–	–	–	–	–	–	–	3.5	–	3.5	
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$			2[a]	0.2	–	1	–	–	–	–	–	–	–	–	V
				2.5[a]	0.25	–	–	–	1	–	–	–	–	–	–	
				3[a]	0.3	–	–	–	–	–	1	–	–	–	–	
				6.5[a]	1.63	–	2	–	2	–	2	–	–	–	–	
				1.5[a]	0.15	–	–	–	–	–	–	–	1.2	–	1.2	
				4[a]	2	–	–	–	–	–	–	–	2.5	–	2.5	
* Common-Emitter, Small-Signal, Forward-Current Transfer Ratio (f = 50 kHz)	h_{fe}	4		0.5		20	–	20	–	20	–	20	–	20	–	
Gain-Bandwidth Product	f_T	4		0.5		4	–	4	–	4	–	4	–	4	–	MHz
* Magnitude of Common-Emitter, Small-Signal, Forward-Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	4		0.5		4	–	4	–	4	–	4	–	4	–	
* Collector-to-Base Capacitance (f = 1 MHz, V_{CB} = 10 V)	C_{obo}			0		–	250	–	250	–	250	–	250	–	250	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$					–	3.125	–	3.125	–	3.125	–	3.125	–	3.125	°C/W
Junction-to-Ambient	$R_{\theta JA}$					–	70	–	70	–	70	–	70	–	70	

[a] Pulsed: Pulse duration = 300 μs, duty factor = 0.018.
* In accordance with JEDEC registration data format (JS-6 RDF-2).
CAUTION: The sustaining voltage V_{CER}(sus) MUST NOT be measured on a curve tracer.

ELECTRICAL CHARACTERISTICS FOR P-N-P TYPES, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: VOLTAGE V dc		CURRENT A dc		LIMITS: 2N6106 2N6107		2N6108 2N6109		2N6110 2N6111		2N6476		2N6475		UNITS
		V_{CE}	V_{BE}	I_C	I_B	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Collector-Cutoff Current: With external base-to-emitter resistance (R_{BE}) = 100 Ω	I_{CER}	−75				—	−0.1	—	—	—	—	—	—	—	—	mA
		−55				—	—	—	−0.1	—	—	—	—	—	—	
		−35				—	—	—	—	—	−0.1	—	—	—	—	
		−120				—	—	—	—	—	—	—	−0.1	—	—	
		−100				—	—	—	—	—	—	—	—	—	−0.1	
With (R_{BE}) = 100 Ω and T_C = 150°C		−70				—	−2	—	—	—	—	—	—	—	—	
		−50				—	—	—	−2	—	—	—	—	—	—	
		−30				—	—	—	—	—	−2	—	—	—	—	
T_C = 100°C		−120				—	—	—	—	—	—	—	−2	—	—	
		−100				—	—	—	—	—	—	—	—	—	−2	
* With base-emitter junction reverse-biased	I_{CEX}	−75	1.5			—	−0.1	—	—	—	—	—	—	—	—	mA
		−56	1.5			—	—	—	−0.1	—	—	—	—	—	—	
		−37.5	1.5			—	—	—	—	—	−0.1	—	—	—	—	
		−120	1.5			—	—	—	—	—	—	—	−0.1	—	—	
		−100	1.5			—	—	—	—	—	—	—	—	—	−0.1	
* With base-emitter junction reverse-biased and T_C = 150°C		−70	1.5			—	−2	—	—	—	—	—	—	—	—	
		−50	1.5			—	—	—	−2	—	—	—	—	—	—	
		−30	1.5			—	—	—	—	—	−2	—	—	—	—	
T_C = 100°C		−120	1.5			—	—	—	—	—	—	—	−2	—	—	
		−100	1.5			—	—	—	—	—	—	—	—	—	−2	
* With base open	I_{CEO}	−20			0	—	—	—	—	—	−1	—	—	—	—	mA
		−40			0	—	—	—	−1	—	—	—	—	—	—	
		−60			0	—	−1	—	—	—	—	—	−1	—	—	
		−50			0	—	—	—	—	—	—	—	—	—	−1	
* Emitter-Cutoff Current	I_{EBO}		5	0		—	−1	—	−1	—	−1	—	−1	—	−1	mA
* Collector-to-Emitter Sustaining Voltage With base open	$V_{CEO}(sus)$			−0.1[a]	0	−70	—	−50	—	−30	—	−120	—	−100	—	V
With external base-to emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$			−0.1		−80	—	−60	—	−40	—	−130	—	−110	—	V
* DC Forward-Current Transfer Ratio	h_{FE}	−4		−2[a]		30	150	—	—	—	—	—	—	—	—	
		−4		−2.5[a]		—	—	30	150	—	—	—	—	—	—	
		−4		−3[a]		—	—	—	—	30	150	—	—	—	—	
		−4		−1.5[a]		—	—	—	—	—	—	15	150	15	150	
		−2.5		−4[a]		—	—	—	—	—	—	2	—	2	—	
		−4		−6.5[a]		5	—	5	—	5	—	—	—	—	—	
* Base-to-Emitter Voltage	V_{BE}	−4		−2[a]		—	−1.5	—	—	—	—	—	—	—	—	V
		−4		−2.5[a]		—	—	—	−1.5	—	—	—	—	—	—	
		−4		−3[a]		—	—	—	—	—	−1.5	—	—	—	—	
		−4		−1.5[a]		—	—	—	—	—	—	—	−2	—	−2	
		−2.5		−4[a]		—	—	—	—	—	—	—	−3.5	—	−3.5	
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$			−2[a]	−0.2	—	−1	—	—	—	—	—	—	—	—	V
				−2.5[a]	−0.25	—	—	—	−1	—	—	—	—	—	—	
				−3[a]	−0.3	—	—	—	—	—	−1	—	—	—	—	
				−6.5[a]	−1.63	—	−2	—	−2	—	−2	—	—	—	—	
				−1.5[a]	−0.15	—	—	—	—	—	—	—	−1.2	—	−1.2	
				−4[a]	−2	—	—	—	—	—	—	—	−2.5	—	−2.5	
* Common-Emitter, Small-Signal, Forward-Current Transfer Ratio (f = 50 kHz)	h_{fe}	−4		−0.5		20	—	20	—	20	—	20	—	20	—	
Gain-Bandwidth Product	f_T	−4		−0.5		10	—	10	—	10	—	10	—	10	—	MHz
* Magnitude of Common-Emitter, Small-Signal, Forward-Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	−4		−0.5		10	—	10	—	10	—	10	—	10	—	
* Collector-to-Base Capacitance (f = 1 MHz, V_{CB} = −10 V)	C_{obo}			0		—	250	—	250	—	250	—	250	—	250	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$					—	3.125	—	3.125	—	3.125	—	3.125	—	3.125	°C/W
Junction-to-Ambient	$R_{\theta JA}$					—	70	—	70	—	70	—	70	—	70	

[a] Pulsed: Pulse duration = 300 μs, duty factor = 0.018.
* In accordance with JEDEC registration data format (JS-6 RDF-2).
CAUTION: The sustaining voltage V_{CER}(sus) MUST NOT be measured on a curve tracer.

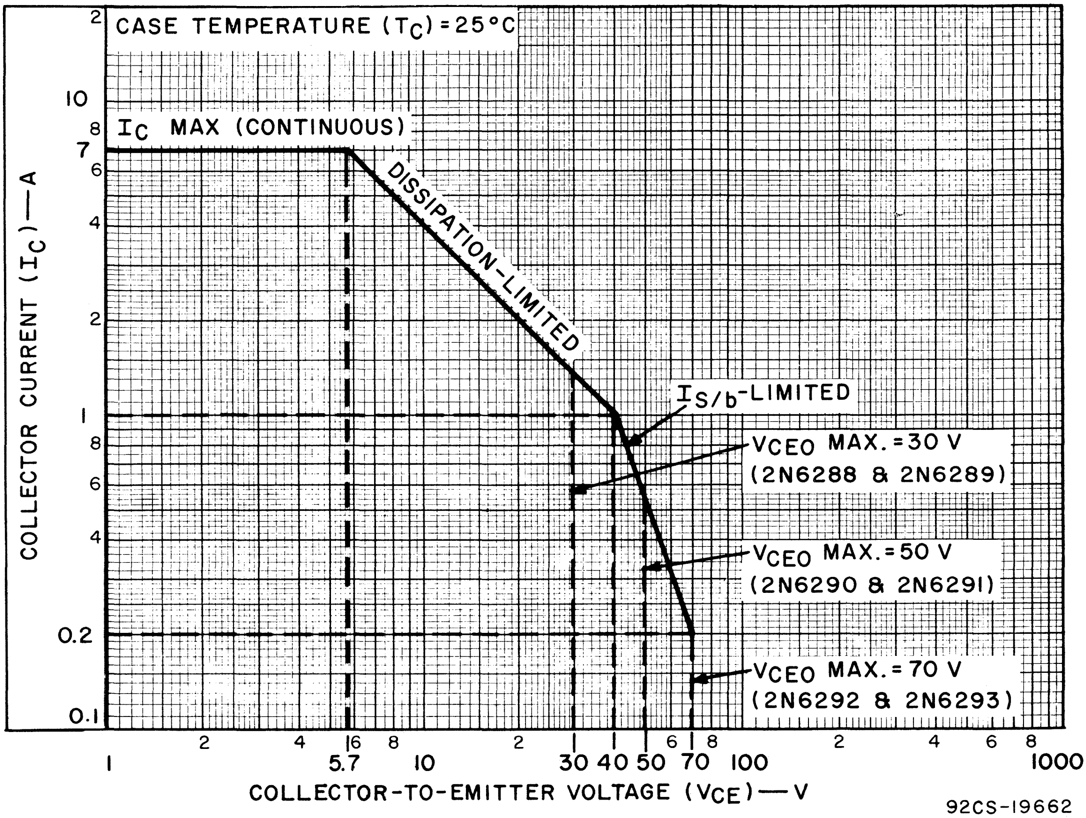


Fig. 1 — Maximum operating areas for 2N6288–2N6293.

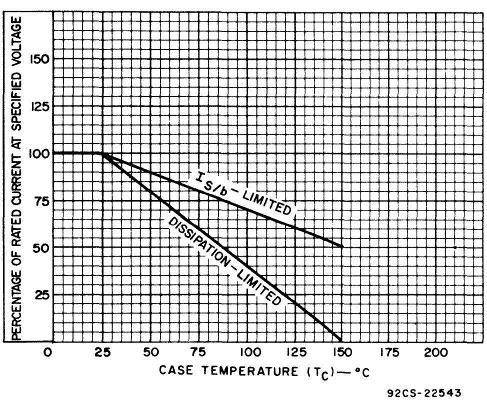


Fig. 2 — Current derating curves for all types.

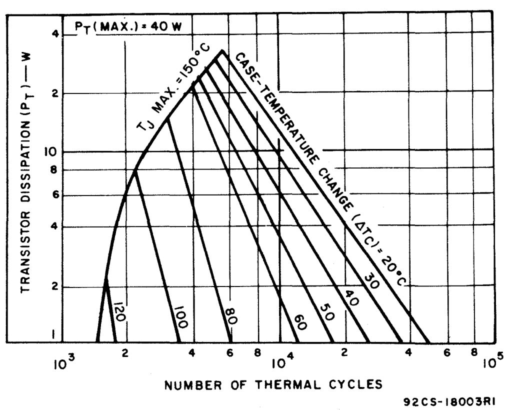


Fig. 3 — Thermal-cycling ratings for all types.

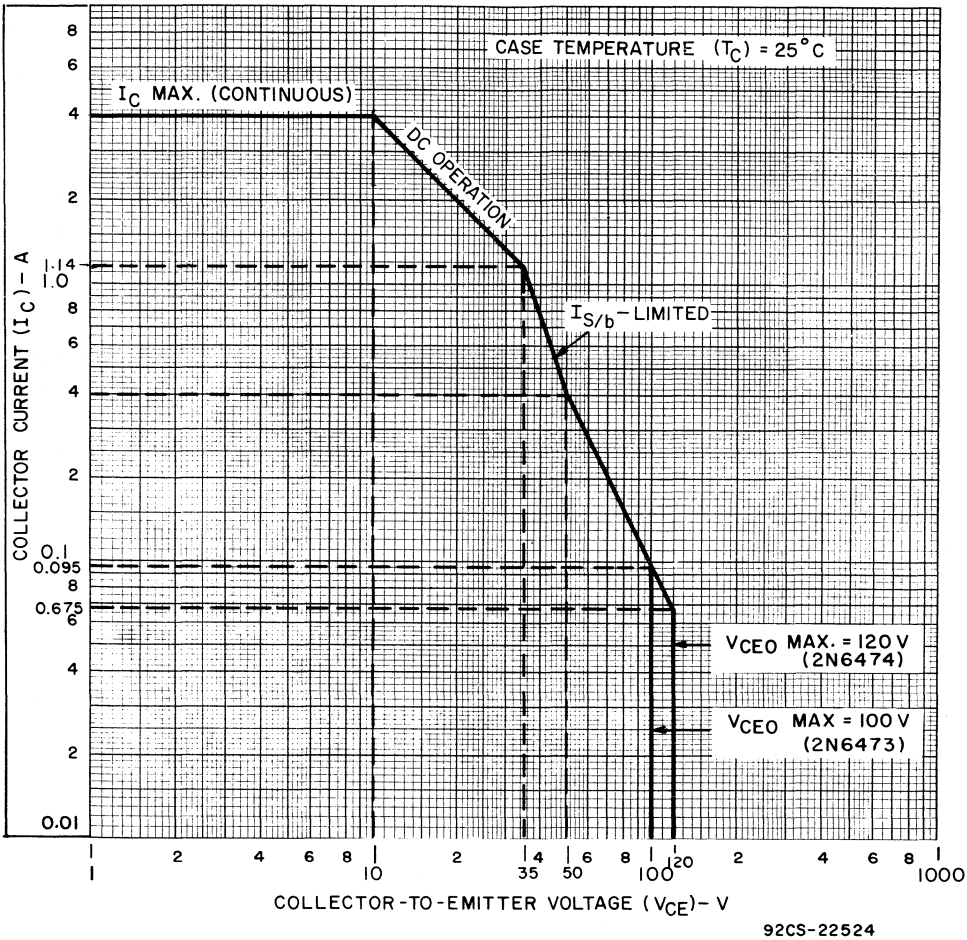


Fig. 4 — Maximum operating areas for 2N6473 and 2N6474.

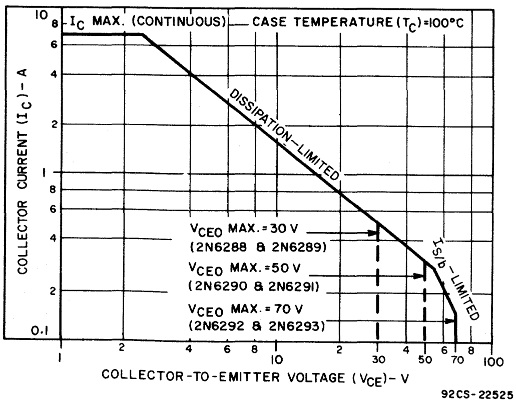


Fig. 5 — Maximum operating areas for 2N6288–2N6293.

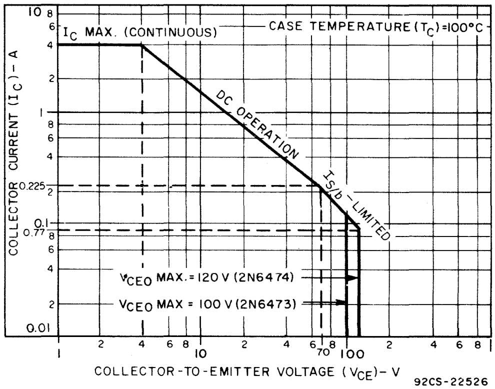


Fig. 6 — Maximum operating areas for 2N6473 – 2N6474.

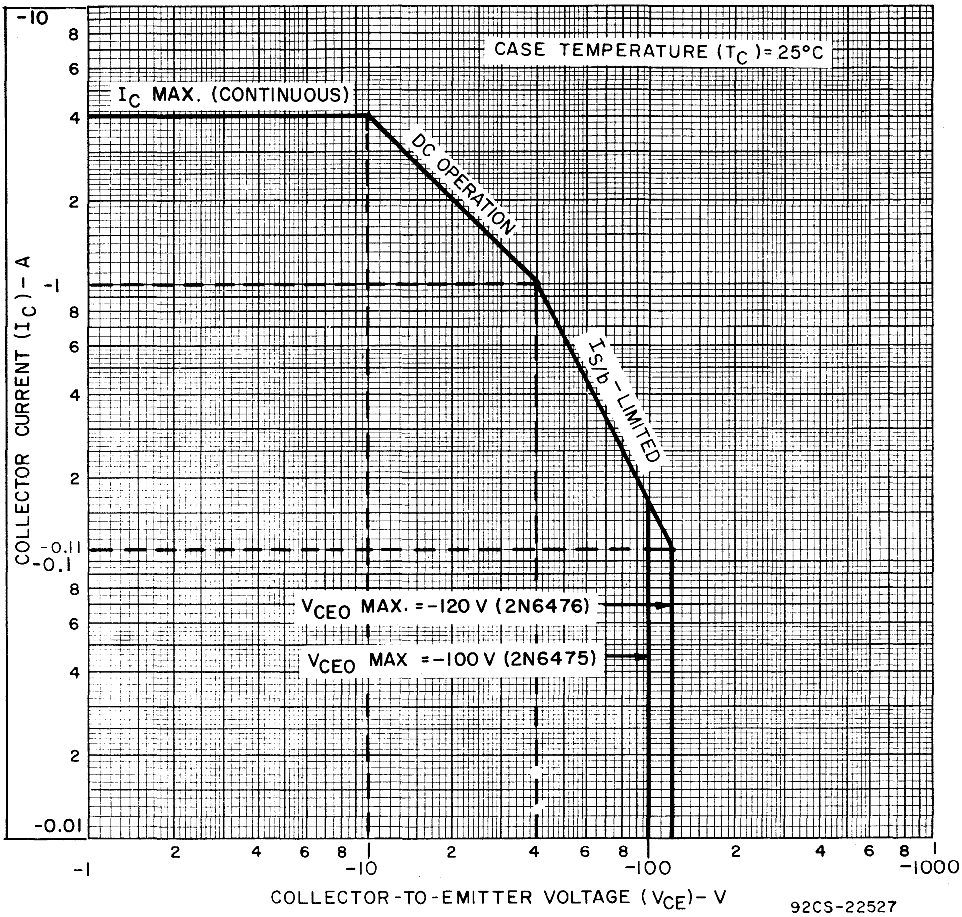


Fig. 7 — Maximum operating areas for 2N6475 — 2N6476.

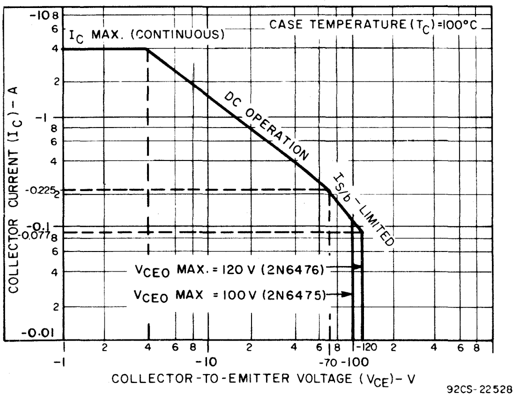


Fig. 8 — Maximum operating areas for 2N6475 and 2N6476.

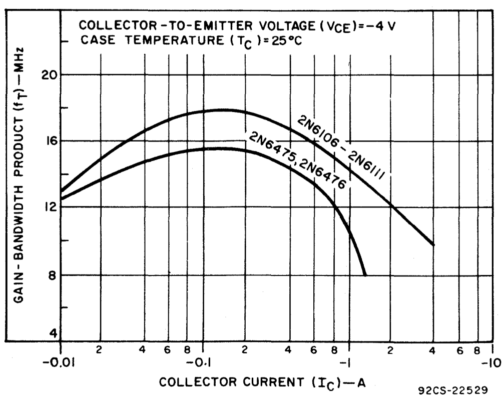


Fig. 9 — Typical gain-bandwidth product for 2N6106 — 2N6111, 2N6475, and 2N6476.

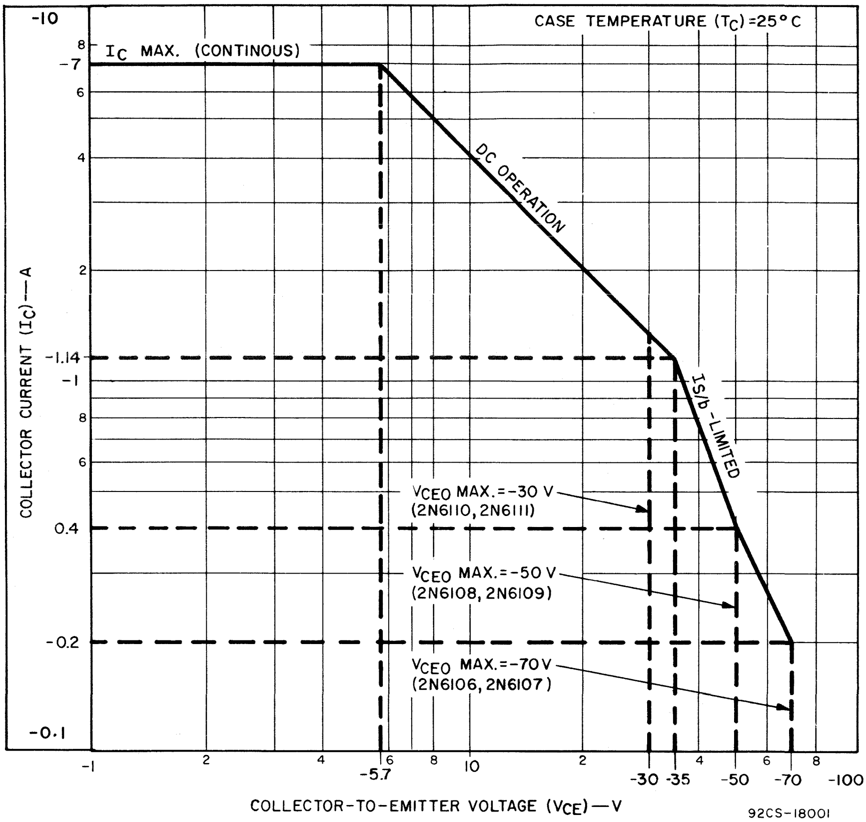


Fig. 10 — Maximum operating areas for types 2N6106 — 2N6111.

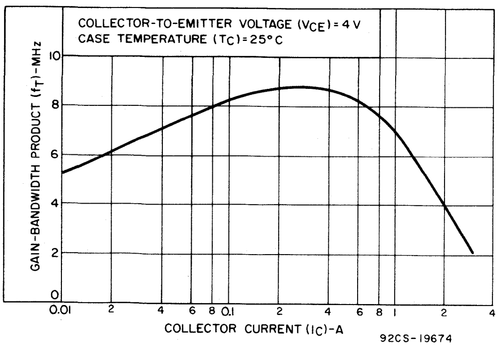


Fig. 11 — Typical gain-bandwidth product for 2N6288 — 2N6293.

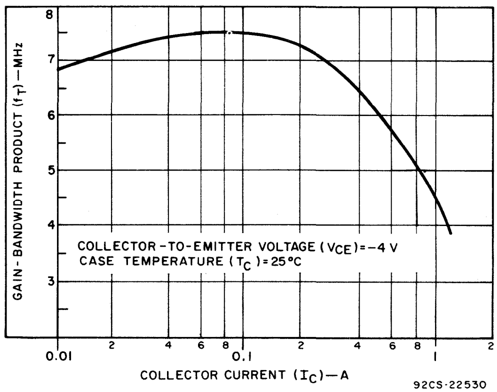


Fig. 12 — Typical gain-bandwidth product for 2N6473 and 2N6474.

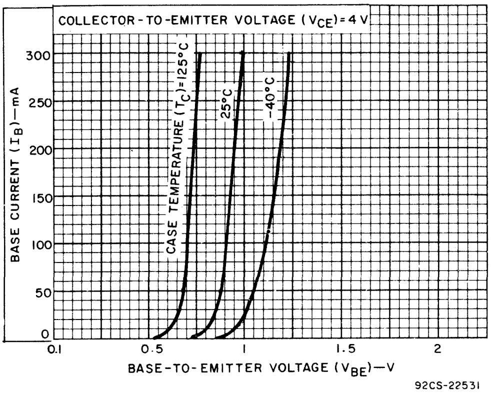


Fig. 13 – Typical input characteristics for 2N6288 – 2N6293.

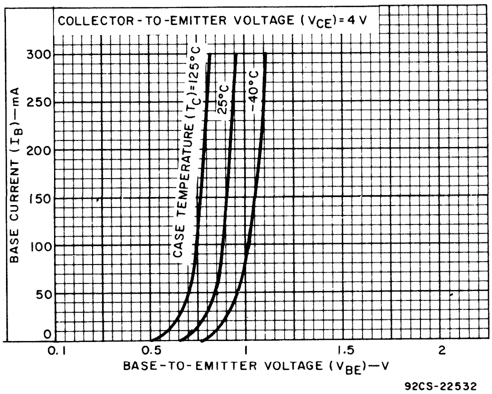


Fig. 14 – Typical input characteristics for 2N6473 and 2N6474.

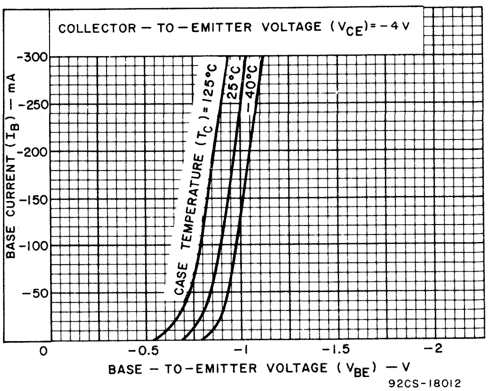


Fig. 15 – Typical input characteristics for 2N6106 – 2N6111, 2N6475, and 2N6476.

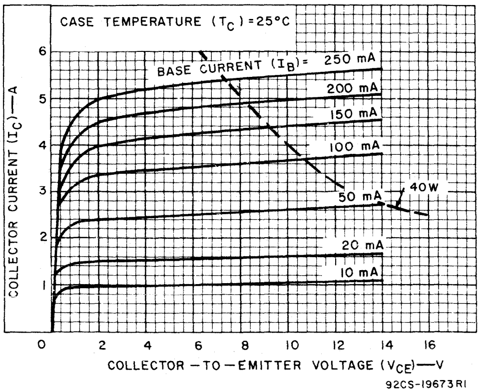


Fig. 16 – Typical output characteristics for 2N6288 – 2N6293.

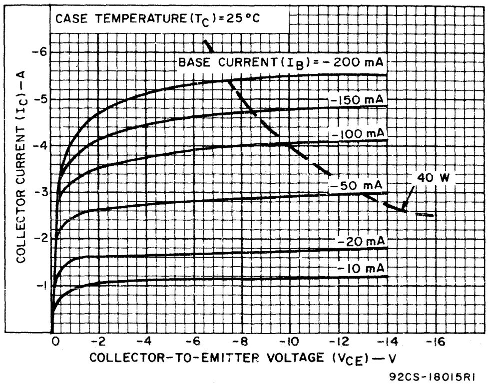


Fig. 17 – Typical output characteristics for 2N6106 – 2N6111.

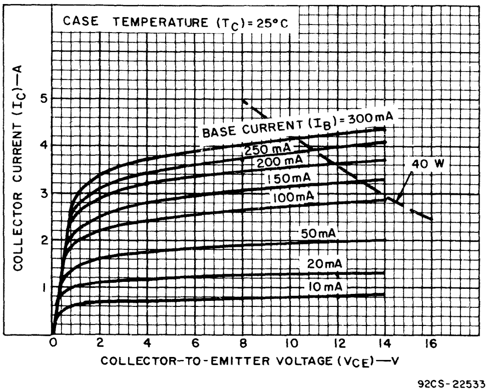


Fig. 18 – Typical output characteristics for 2N6473 and 2N6474.

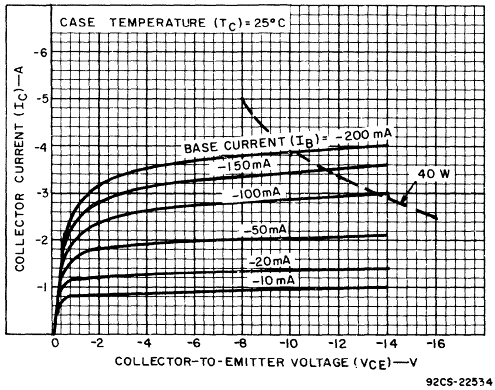


Fig. 19 – Typical output characteristics for 2N6475 and 2N6476.

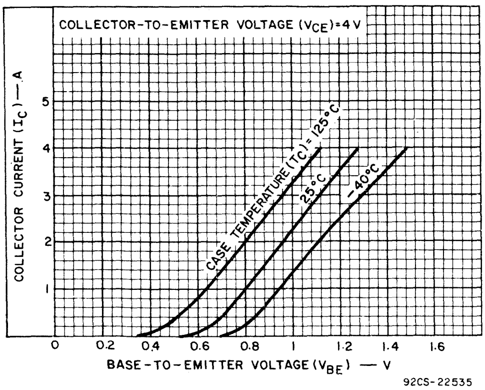


Fig. 20 – Typical transfer characteristics of types 2N6288 – 2N6293.

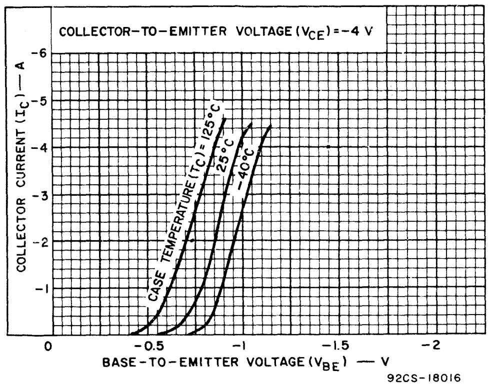


Fig. 21 – Typical transfer characteristics for types 2N6106 – 2N6111.

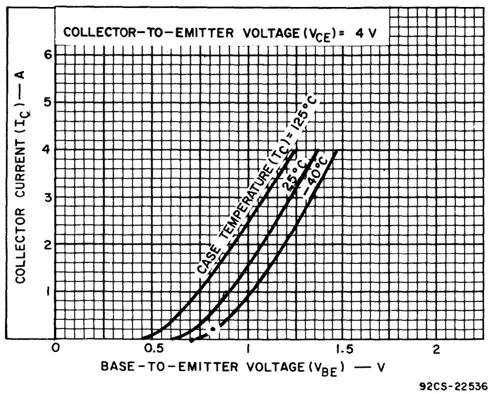


Fig. 22 — Typical transfer characteristics for 2N6473 and 2N6474.

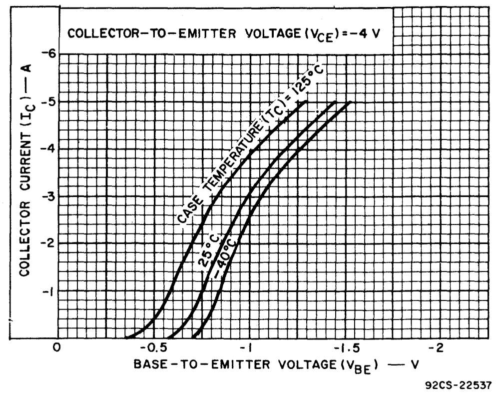


Fig. 23 — Typical transfer characteristics for 2N6475 and 2N6476.

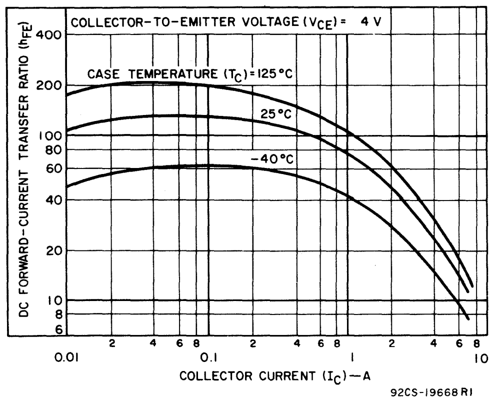


Fig. 24 — Typical dc beta characteristics for 2N6288 – 2N6293.

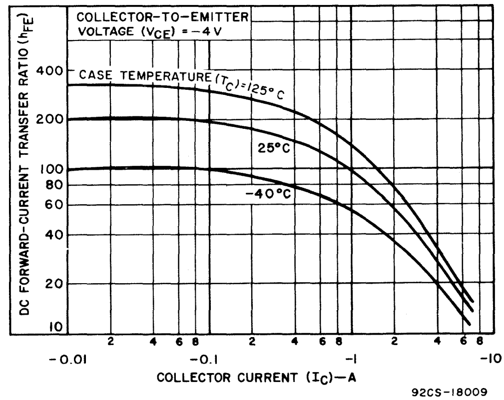


Fig. 25 — Typical dc beta characteristics for 2N6106 – 2N6111.

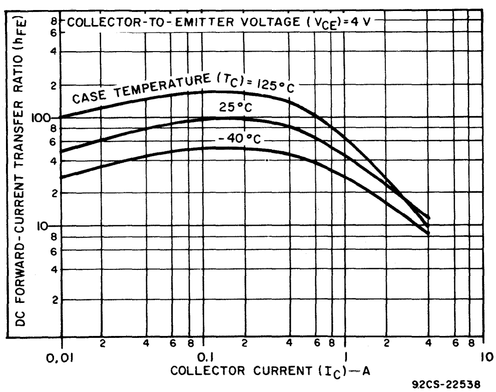


Fig. 26 — Typical dc beta characteristics for 2N6473 and 2N6474.

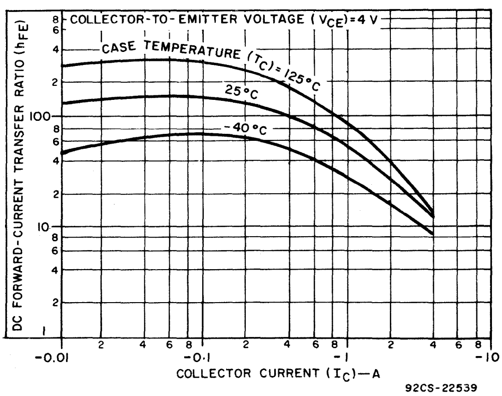


Fig. 27 — Typical dc beta characteristics for 2N6475 and 2N6476.

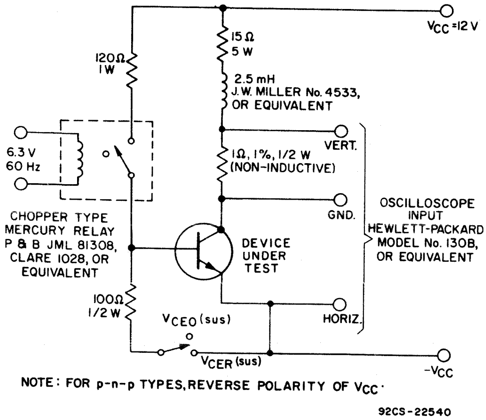
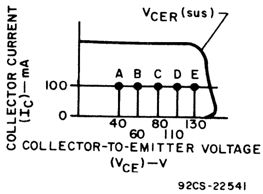


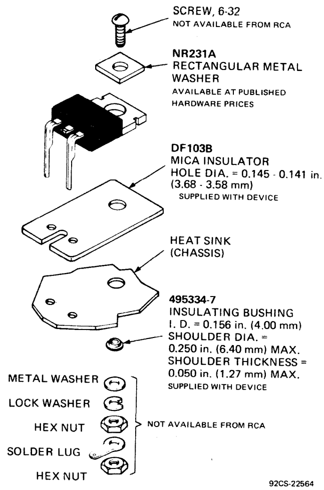
Fig. 28 — Circuit used to measure sustaining voltage $V_{CER}(sus)$ for all types.

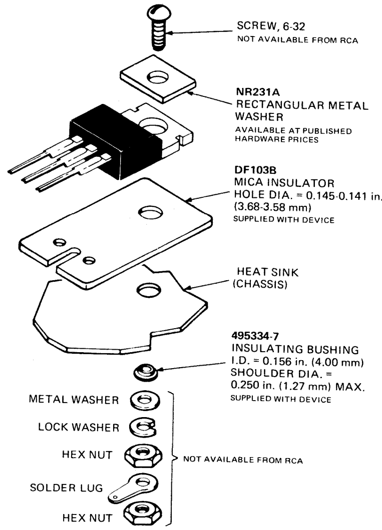


Note: Curve will be inverted and polarity reversed for p-n-p types. The sustaining voltage, V_{CER}(sus), is acceptable when the traces fall to the right and above the designated points:

Point A: 2N6110, 2N6111, 2N6288, 2N6289
Point B: 2N6108, 2N6109, 2N6290, 2N6291
Point C: 2N6106, 2N6107, 2N6292, 2N6293
Point D: 2N6475, 2N6473
Point E: 2N6476, 2N6474

Fig. 29 — Oscilloscope display for measurement of sustaining voltage (test circuit shown in Fig. 28).





In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

92CS-22563

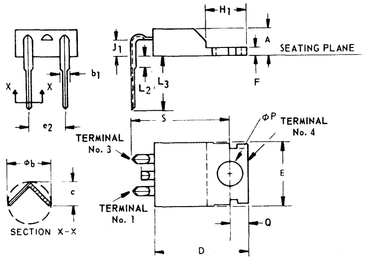
Fig. 30 — Suggested mounting hardware for JEDEC TO-220AA.

Fig. 31 — Suggested mounting hardware for JEDEC TO-220AB.

VERSAWATT PACKAGE MOUNTING

For complete discussion on handling and mounting of RCA molded-plastic power devices, refer to RCA application note AN-4124.

DIMENSIONAL OUTLINE FOR 2N6106, 2N6108, 2N6110, 2N6289, 2N6291, and 2N6293 JEDEC TO-220AA



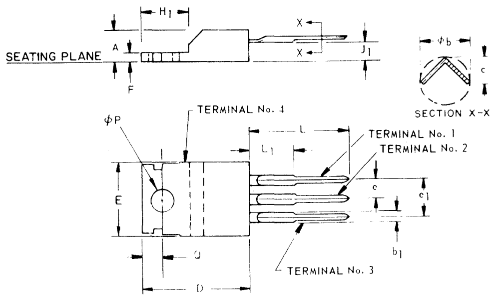
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
ϕb	0.02	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e_2	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L_2	–	0.050	–	1.27	–
L_3	0.360	0.422	9.15	10.71	–
ϕP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–
S	0.580	0.610	14.74	15.49	–

92CS-17990R1

NOTES:

1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.050 – 0.055 (1.27 – 1.40 mm) below seating plane.

DIMENSIONAL OUTLINE FOR 2N6107, 2N6109, 2N6111, 2N6288, 2N6290, 2N6473, 2N6474, 2N6475, and 2N6476 JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
ϕb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
ϕP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS JEDEC TO-220AA

Lead No.1 – Base*
Stub – Do not use stub as tie point.
Lead No.3 – Emitter*
Mounting Flange – Collector

TERMINAL CONNECTIONS JEDEC TO-220AB

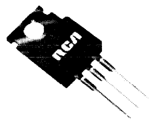
Lead No.1 – Base*
Lead No.2 – Collector
Lead No.3 – Emitter
Mounting Flange – Collector

*Types are available with base and emitter leads interchanged. Additional information is available from the nearest RCA Solid State Sales Office.

Solid State Division

Power Transistors

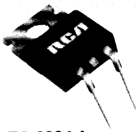
BD277



BD277

TO-220AB

H-1534R1



Also Available

TO-220AA

H-1535R1

7-A, 70-W, Epitaxial-Base, Silicon P-N-P VERSAWATT Transistor

For Applications in Series and Shunt Regulators

Features:

- Thermal-cycling ratings
- Maximum-safe-area-of-operation curve
- Low saturation voltage
- VERSAWATT package (molded silicone plastic)
- High power-dissipation capability

Type BD277 is an epitaxial-base silicon p-n-p transistor supplied in the JEDEC TO-220AB straight-lead VERSAWATT package. It is also available in the TO-220AA package (leads formed to fit a TO-66 socket); to order this version, specify formed lead No. 6201.

The BD277 is useful in series regulators and shunt regulators because of its low saturation voltage and high power-dissipation capability. It is also useful as a replacement for germanium p-n-p transistors in many applications.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE:			
With emitter open	V_{CBO}	−45	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With base open	V_{CEO}	−45	V
EMITTER-TO-BASE VOLTAGE:			
With collector open	V_{EBO}	−4	V
COLLECTOR CURRENT (Continuous)	I_C	−7	A
BASE CURRENT (Continuous)	I_B	−3	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25°C		70	W
At case temperatures above 25°C		Derate linearly at 0.56 W/°C or see Fig.2.	
TEMPERATURE RANGE:			
Storage & Operating (Junction)		−65 to 150	°C
LEAD TEMPERATURE (During Soldering):			
At distance ≥ 1/8 in. (3.17 mm) from case for 10 s max.		235	°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C unless specified otherwise*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS						LIMITS		UNITS
		VOLTAGE V dc			CURRENT A dc					
		V_{CE}	V_{CB}	V_{EB}	I_C	I_B	I_E	MIN.	MAX.	
Collector Cutoff Current: With emitter open	I_{CBO}		−45				0	–	−0.1	mA
With emitter open and T_C = 150°C	I_{CBO}		−40				0	–	−2.0	mA
With base open	I_{CEO}	−30				0		–	−1.0	mA
Emitter Cutoff Current: With collector open	I_{EBO}			−4	0			–	−1.0	mA
Collector-to-Emitter Breakdown Voltage: With base open	$V_{(BR)CEO}$				−0.1*	0		−45	–	V
Base-to-Emitter Voltage	V_{BE}	−2			−1.75*			–	1.2	V
DC Forward-Current Transfer Ratio	h_{FE}	−2			−1.75*			30	150	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				−1.75*	−0.1		–	−0.5	V
Gain-Bandwidth Product	f_T	−4			−0.5			10	–	MHz
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$							–	1.78	°C/W
Junction-to-Ambient	$R_{\theta JA}$							–	70	°C/W

* Pulsed: Pulse duration = 300 μs, duty factor ⩽ 2%.

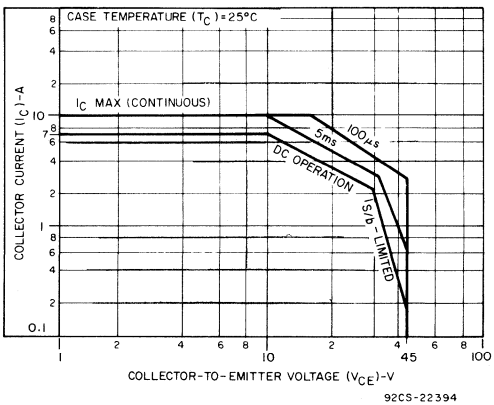


Fig.1 — Maximum operating area.

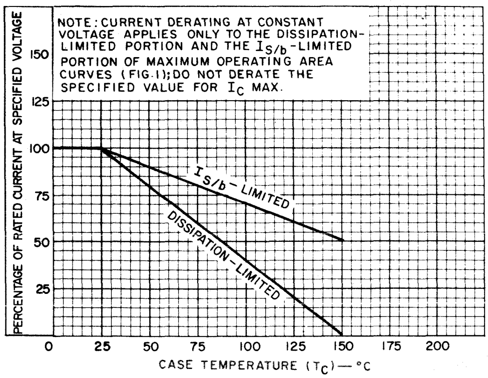


Fig.2 – Derating curves.

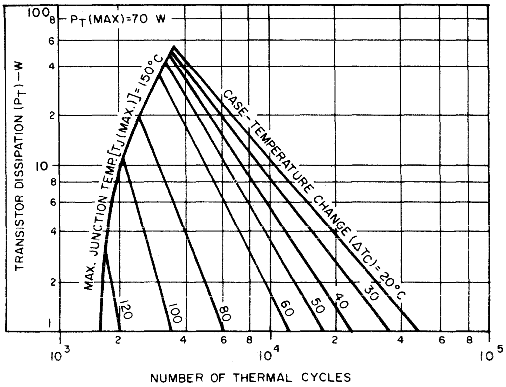


Fig.3 – Thermal-cycling ratings.

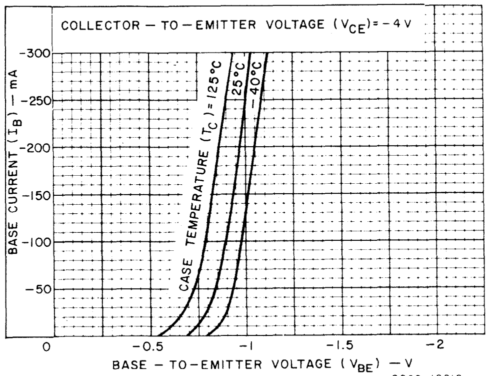


Fig.4 – Typical input characteristics.

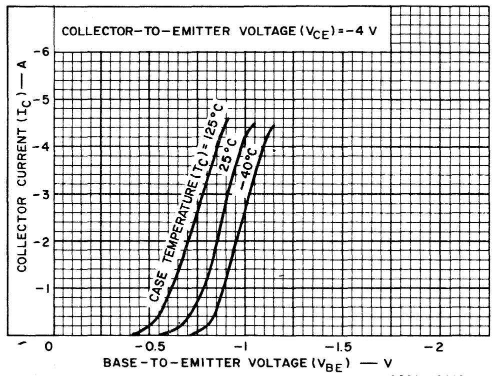


Fig.5 – Typical transfer characteristics.

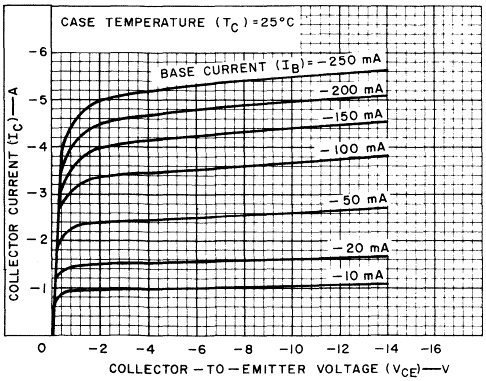


Fig.6 – Typical output characteristics.

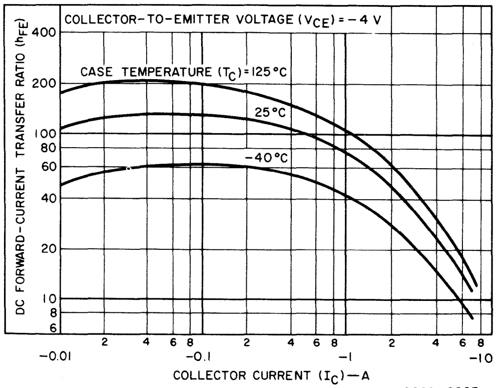


Fig.7 – Typical dc beta characteristics.

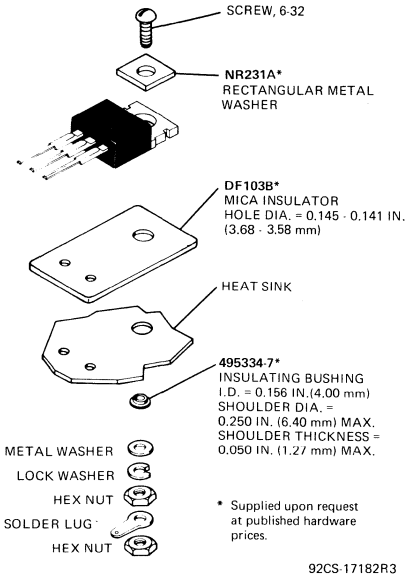
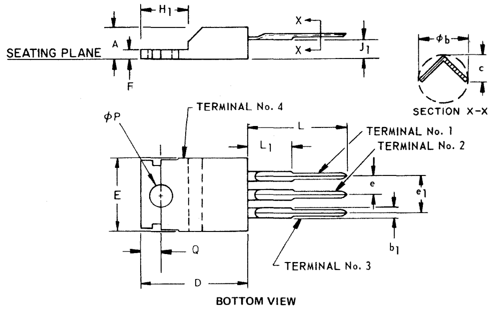


Fig.8 — Suggested mounting hardware for JEDEC TO-220AB.

For basic transistor theory, circuits, and application information, refer to "RCA Solid State Power Circuits Designer's Handbook", SP-52, or "RCA Transistor, Thyristor, & Diode Manual", SC-15.

DIMENSIONAL OUTLINE
JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991RI

NOTES:
1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 IN. (6.35 – 6.48 mm) from case.

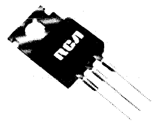
TERMINAL CONNECTIONS

Lead No.1 — Base
Lead No.2 — Collector
Lead No.3 — Emitter
Mounting Flange, Lead No.4 — Collector

RCA

Solid State
Division

Power Transistors
BD239 BD239B
BD239A BD239C



JEDEC TO-220 AB H-1535R1

Epitaxial-Base Silicon N-P-N VERSAWATT Transistors

For Power-Amplifier and
High-Speed-Switching Applications

Features:

- **30 W at 25°C case temperature**
- **4-A rated collector current**
- **Min. f_T of 3 MHz at 10 V, 200 mA**
- **Complements of p-n-p types BD240, BD240A, BD240B, and BD240C**

Types BD239, BD239A, BD239B, and BD239C are epitaxial-base silicon n-p-n transistors; they differ only in their voltage ratings. These devices are intended for a wide variety of switching and amplifier applications such as series and shunt regulators, and driver and output stages of high-fidelity amplifiers. The BD239-series power transistors are complements of the devices in the BD240 series. (The BD240-series devices are described in File No. 670.)

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		BD239	BD239A	BD239B	BD239C	
COLLECTOR-TO-EMITTER VOLTAGE:						
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}	55	70	90	115	V
With base open	V_{CEO}	45	60	80	100	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	5	5	5	V
CONTINUOUS COLLECTOR CURRENT	I_C	4	4	4	4	A
CONTINUOUS BASE CURRENT	I_B	1	1	1	1	A
TRANSISTOR DISSIPATION:	P_T					
At case temperatures up to 25°C		30	30	30	30	W
At ambient temperatures up to 25°C		2	2	2	2	W
At case temperatures above 25°C		← See Fig. 2 →				
TEMPERATURE RANGE:						
Storage & Operating (Junction)		← -65 to 150 →				°C
LEAD TEMPERATURE (During Soldering):						
At distance 1/8 in. (3.17 mm) from case for 10 s max.		← 235 →				°C

ELECTRICAL CHARACTERISTICS *at Case Temperature (T_C) = 25°C*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS								UNITS
		VOLTAGE V dc		CURRENT A dc		BD239		BD239A		BD239B		BD239C		
		V_{CE}	V_{BE}	I_C	I_B	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	30			0	–	0.3	–	0.3	–	–	–	–	mA
		60			0	–	–	–	–	–	0.3	–	0.3	mA
With base-to-emitter junction short-circuited	I_{CES}	45	0			–	0.2	–	–	–	–	–	–	mA
		60	0			–	–	–	0.2	–	–	–	–	mA
		80	0			–	–	–	–	–	0.2	–	–	mA
		100	0			–	–	–	–	–	–	–	0.2	mA
Emitter Cutoff Current	I_{EBO}		–5	0		–	1	–	1	–	1	–	1	mA
Collector-to-Emitter Breakdown Voltage: With base open	$V_{BR(CEO)}$			0.03[a]	0	45	–	60	–	80	–	100	–	V
DC Forward-Current Transfer Ratio	h_{FE}	4		0.2[a]		40	–	40	–	40	–	40	–	
		4		1[a]		15	–	15	–	15	–	15	–	
Base-to-Emitter Voltage	V_{BE}	4		1[a]		–	1.3	–	1.3	–	1.3	–	1.3	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$			1[a]	0.2	–	0.7	–	0.7	–	0.7	–	0.7	V
Common-Emitter Small-Signal Short-Circuit Forward-Current Transfer Ratio (f = 1 kHz)	h_{fe}	10		0.2		20	–	20	–	20	–	20	–	
Magnitude of Common Emitter Small-Signal Short-Circuit Forward-Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	10		0.2		3	–	3	–	3	–	3	–	
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$					–	4.17	–	4.17	–	4.17	–	4.17	°C/W
Junction-to-Ambient	$R_{\theta JA}$					–	62.5	–	62.5	–	62.5	–	62.5	°C/W

[a]Pulsed: Pulse duration = 300 μs, duty factor = 2%.

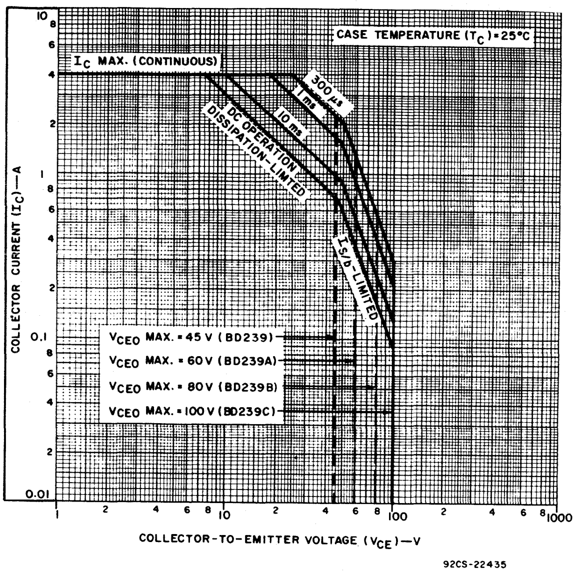


Fig. 1— Maximum safe operating areas for all types.

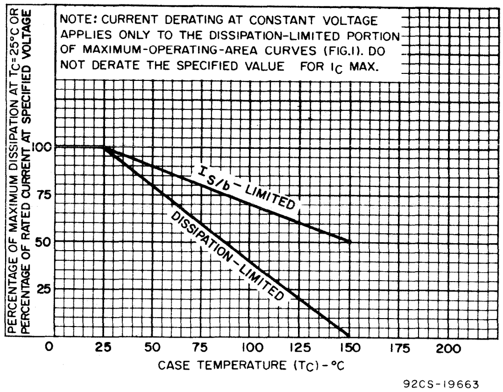


Fig. 2— Derating curves for all types.

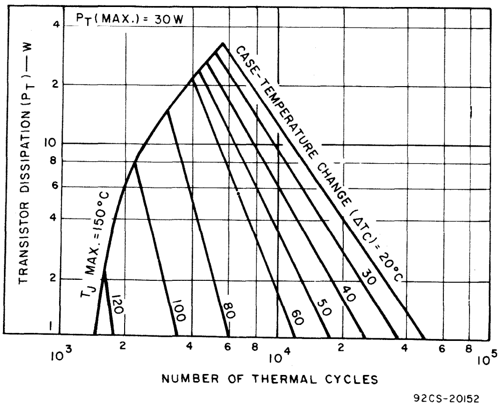


Fig. 3— Thermal-cycling ratings for all types.

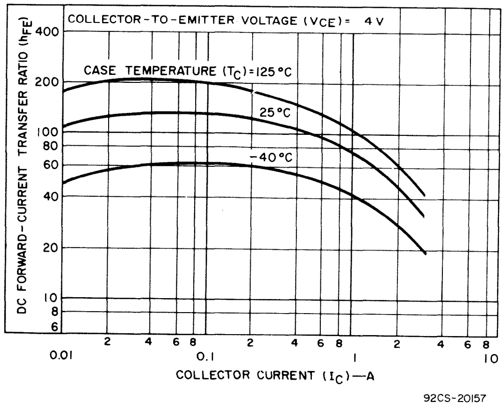


Fig. 4— Typical dc beta characteristics for all types.

DIMENSIONAL OUTLINE
JEDEC TO-220AB

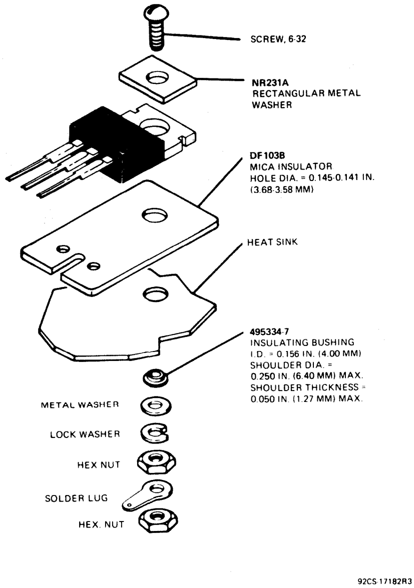
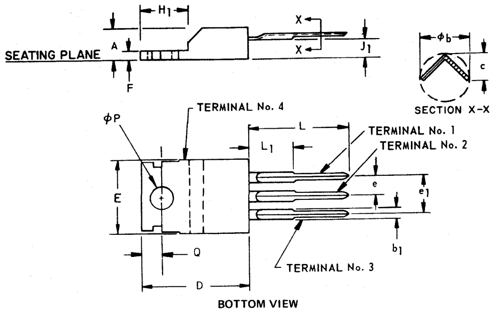


Fig. 5— Suggested mounting hardware for JEDEC TO-220AB.



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
ϕb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
ϕP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

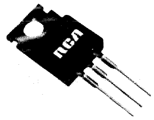
1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS

Terminal No. 1 – Base
Terminal No. 2 – Collector
Terminal No. 3 – Emitter
Terminal No. 4 – Collector

RCA Solid State Division

Power Transistors
BD240 BD240B
BD240A BD240C



JEDEC TO-220 AB H-1535R1

Epitaxial-Base Silicon P-N-P VERSAWATT Transistors

For Power-Amplifier and High-Speed-Switching Applications

Features:
- **30 W at 25°C case temperature**
- **4-A rated collector current**
- **Min. f_T of 3 MHz at 10 V, 200 mA**
- **Complements of n-p-n types BD239, BD239A, BD239B, and BD239C**

Types BD240, BD240A, BD240B, and BD240C are epitaxial-base silicon p-n-p transistors; they differ only in their voltage ratings. These devices are intended for a wide variety of switching and amplifier applications such as series and shunt regulators, and driver and output stages of high-fidelity amplifiers. The BD240-series power transistors are complements of the devices in the BD239 series. (The BD239-series devices are described in File No. 669.)

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		BD240	BD240A	BD240B	BD240C	
COLLECTOR-TO-EMITTER VOLTAGE:						
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}	−55	−70	−90	−115	V
With base open	V_{CEO}	−45	−60	−80	−100	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	−5	−5	−5	−5	V
CONTINUOUS COLLECTOR CURRENT	I_C	−4	−4	−4	−4	A
CONTINUOUS BASE CURRENT	I_B	−1	−1	−1	−1	A
TRANSISTOR DISSIPATION:	P_T					
At case temperatures up to 25°C		30	30	30	30	W
At ambient temperatures up to 25°C		2	2	2	2	W
At case temperatures above 25°C		← See Fig. 2 →				
TEMPERATURE RANGE:						
Storage & Operating (Junction)		← −65 to 150 →				°C
LEAD TEMPERATURE (During Soldering):						
At distance 1/8 in. (3.17 mm) from case for 10 s max.		← 235 →				°C

ELECTRICAL CHARACTERISTICS *at Case Temperature* $(T_C) = 25^oC$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS								UNITS
		VOLTAGE V dc		CURRENT A dc		BD240		BD240A		BD240B		BD240C		
		V_{CE}	V_{BE}	I_C	I_B	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	-30			0	–	-0.3	–	-0.3	–	–	–	–	mA
		-60			0	–	–	–	–	–	-0.3	–	-0.3	mA
With base-to-emitter junction short-circuited	I_{CES}	-45	0			–	-0.2	–	–	–	–	–	–	mA
		-60	0			–	–	–	0.2	–	–	–	–	mA
		-80	0			–	–	–	–	–	-0.2	–	–	mA
		-100	0			–	–	–	–	–	–	–	-0.2	mA
Emitter Cutoff Current	I_{EBO}		5	0		–	-1	–	-1	–	-1	–	-1	mA
Collector-to-Emitter Breakdown Voltage: With base open	$V_{BR(CEO)}$			-0.03[a]	0	-45	–	-60	–	-80	–	-100	–	V
DC Forward-Current Transfer Ratio	h_{FE}	-4		-0.2[a]		40	–	40	–	40	–	40	–	
		-4		-1[a]		15	–	15	–	15	–	15	–	
Base-to-Emitter Voltage	V_{BE}	-4		-1[a]		–	-1.3	–	-1.3	–	-1.3	–	-1.3	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$			-1[a]	-0.2	–	-0.7	–	-0.7	–	-0.7	–	-0.7	V
Common-Emitter Small-Signal Short-Circuit Forward-Current Transfer Ratio (f = 1 kHz)	h_{fe}	-10		-0.2		20	–	20	–	20	–	20	–	
Magnitude of Common Emitter Small-Signal Short-Circuit Forward-Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	-10		0.2		3	–	3	–	3	–	3	–	
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$					–	4.17	–	4.17	–	4.17	–	4.17	$^oC/W$
Junction-to-Ambient	$R_{\theta JA}$					–	62.5	–	62.5	–	62.5	–	62.5	$^oC/W$

[a]Pulsed: Pulse duration = 300 μs, duty factor = 2%.

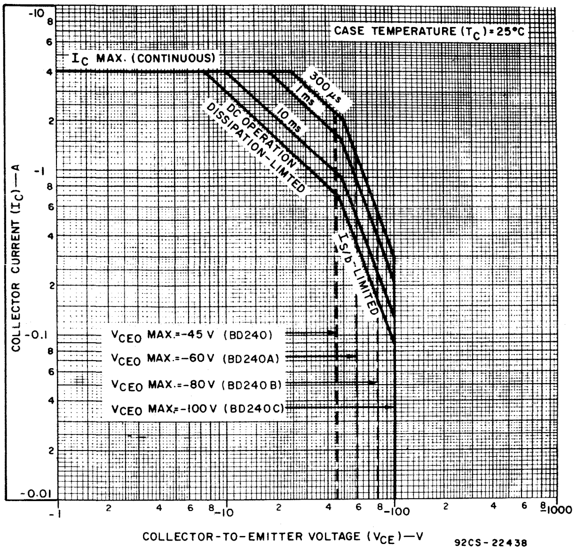


Fig. 1— Maximum safe operating areas for all types.

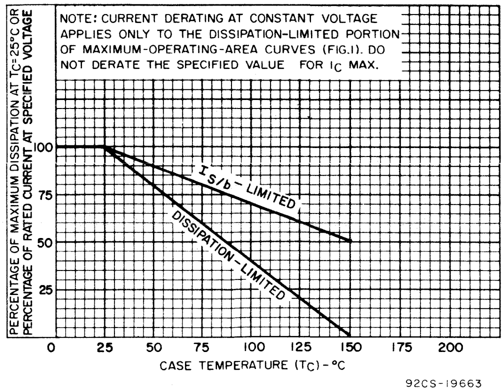


Fig. 2— Derating curves for all types.

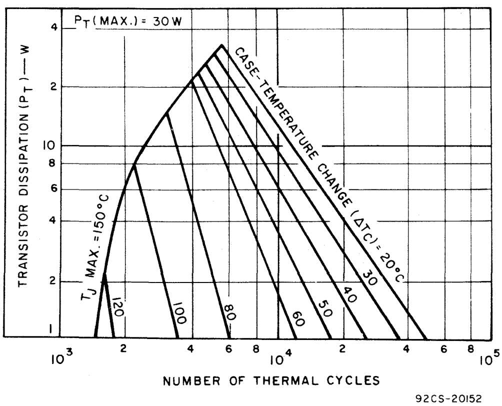


Fig. 3— Thermal-cycling ratings for all types.

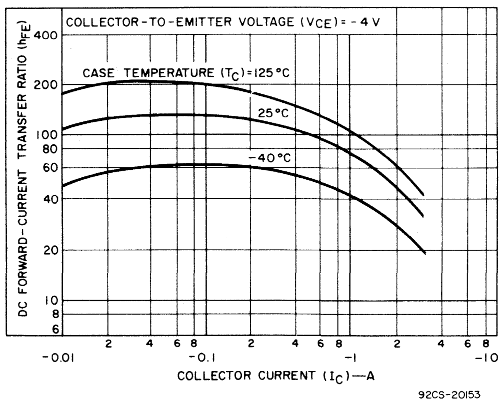
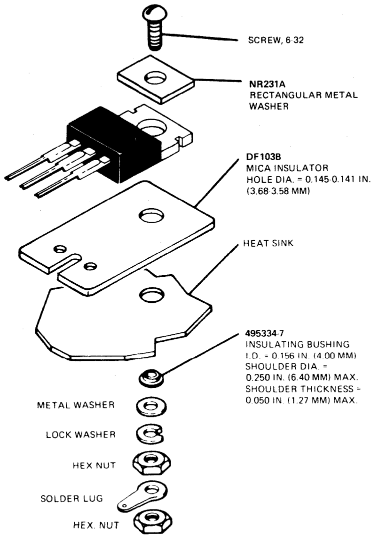


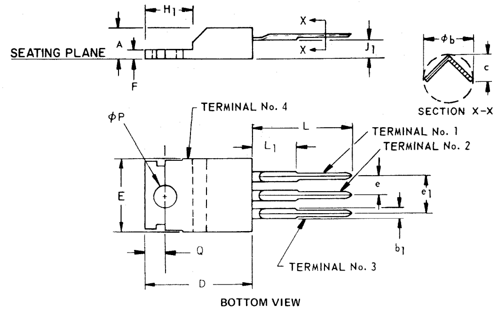
Fig. 4— Typical dc beta characteristics for all types.



92CS 17182R3

Fig. 5— Suggested mounting hardware for JEDEC TO-220AB.

DIMENSIONAL OUTLINE JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

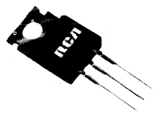
1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS

Terminal No. 1 — Base
Terminal No. 2 — Collector
Terminal No. 3 — Emitter
Terminal No. 4 — Collector

RCA Solid State Division

Power Transistors
BD241 BD241B BD241A BD241C



JEDEC TO-220 AB H-1535R1

Epitaxial-Base Silicon N-P-N VERSAWATT Transistors

For Power-Amplifier and High-Speed-Switching Applications

Features:

- **40 W at 25°C case temperature**
- **5-A rated collector current**
- **Min. f_T of 3 MHz at 10 V, 500 mA**
- **Complements of p-n-p types BD242, BD242A, BD242B, and BD242C**

Types BD241, BD241A, BD241B, and BD241C are epitaxial-base silicon n-p-n transistors; they differ only in their voltage ratings. These devices are intended for a wide variety of switching and amplifier applications such as series and shunt regulators, and driver and output stages of high-fidelity amplifiers. The BD241-series power transistors are complements of the devices in the BD242 series. (The BD242-series devices are described in File No. 672.)

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		BD241	BD241A	BD241B	BD241C	
COLLECTOR-TO-EMITTER VOLTAGE:						
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}	55	70	90	115	V
With base open	V_{CEO}	45	60	80	100	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	5	5	5	V
CONTINUOUS COLLECTOR CURRENT	I_C	5	5	5	5	A
CONTINUOUS BASE CURRENT	I_B	1	1	1	1	A
TRANSISTOR DISSIPATION:	P_T					
At case temperatures up to 25°C		40	40	40	40	W
At ambient temperatures up to 25°C .		2	2	2	2	W
At case temperatures above 25°C		← See Fig. 2 →				
TEMPERATURE RANGE:						
Storage & Operating (Junction)		← -65 to 150 →				°C
LEAD TEMPERATURE (During Soldering):						
At distance 1/8 in. (3.17 mm) from case for 10 s max.		← 235 →				°C

ELECTRICAL CHARACTERISTICS *at Case Temperature (T_C) = 25°C*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS								UNITS
		VOLTAGE V dc		CURRENT A dc		BD241		BD241A		BD241B		BD241C		
		V_{CE}	V_{BE}	I_C	I_B	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	30			0	–	0.3	–	0.3	–	–	–	–	mA
		60			0	–	–	–	–	–	0.3	–	0.3	mA
With base-to-emitter junction short-circuited	I_{CES}	45	0			–	0.2	–	–	–	–	–	–	mA
		60	0			–	–	–	0.2	–	–	–	–	mA
		80	0			–	–	–	–	–	0.2	–	–	mA
		100	0			–	–	–	–	–	–	–	0.2	mA
Emitter Cutoff Current	I_{EBO}		–5	0		–	1	–	1	–	1	–	1	mA
Collector-to-Emitter Breakdown Voltage: With base open	$V_{BR(CEO)}$			0.03^a	0	45	–	60	–	80	–	100	–	V
DC Forward-Current Transfer Ratio	h_{FE}	4		1^a		25	–	25	–	25	–	25	–	
		4		3^a		10	–	10	–	10	–	10	–	
Base-to-Emitter Voltage	V_{BE}	4		3^a		–	1.8	–	1.8	–	1.8	–	1.8	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$			3^a	0.6	–	1.2	–	1.2	–	1.2	–	1.2	V
Common-Emitter Small-Signal Short-Circuit Forward-Current Transfer Ratio (f = 1 kHz)	h_{fe}	10		0.5		20	–	20	–	20	–	20	–	
Magnitude of Common Emitter Small-Signal Short-Circuit Forward-Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	10		0.5		3	–	3	–	3	–	3	–	
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$					–	3.125	–	3.125	–	3.125	–	3.125	°C/W
Junction-to-Ambient	$R_{\theta JA}$					–	62.5	–	62.5	–	62.5	–	62.5	°C/W

[a]Pulsed: Pulse duration = 300 μs, duty factor = 2%.

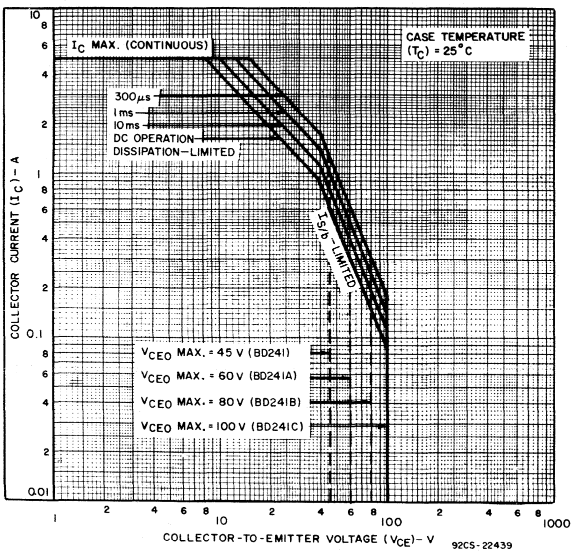


Fig. 1— Maximum safe operating areas for all types.

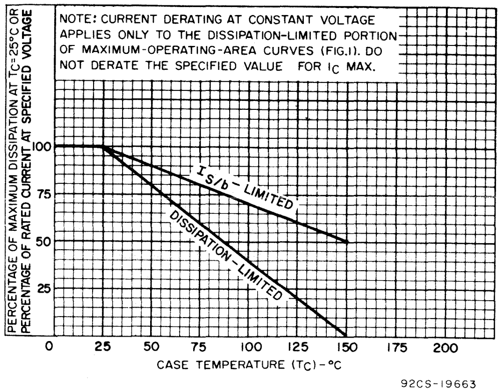


Fig. 2— Derating curves for all types.

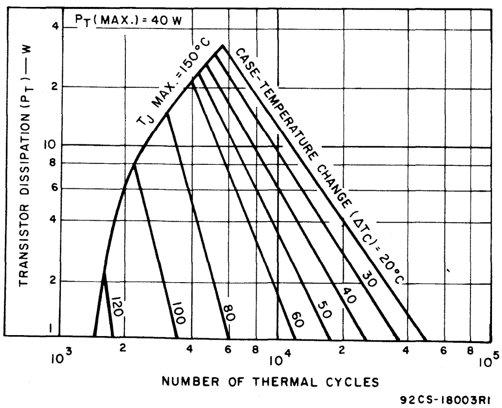


Fig. 3— Thermal-cycling ratings for all types.

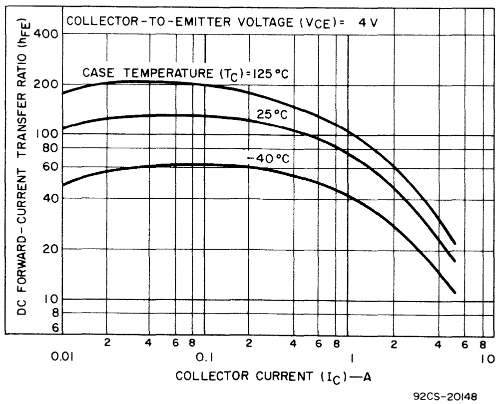


Fig. 4— Typical dc beta characteristics for all types.

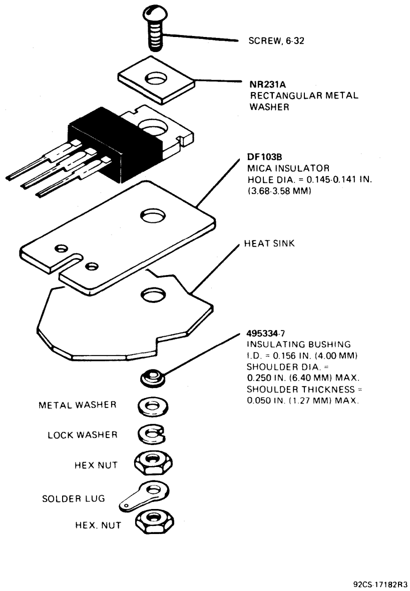
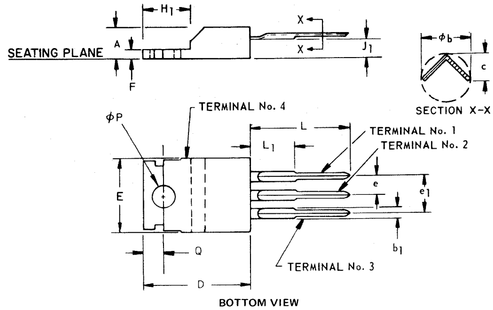


Fig. 5— Suggested mounting hardware for JEDEC TO-220AB.

DIMENSIONAL OUTLINE
JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

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NOTES:

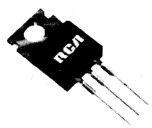
1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS

Terminal No. 1 — Base
Terminal No. 2 — Collector
Terminal No. 3 — Emitter
Terminal No. 4 — Collector

RCA
Solid State
Division

Power Transistors
BD242 BD242B
BD242A BD242C



JEDEC TO-220 AB H-1535R1

Epitaxial-Base Silicon P-N-P VERSAWATT Transistors

For Power-Amplifier and High-Speed-Switching Applications

Features:
- **40 W at 25°C case temperature**
- **5-A rated collector current**
- **Min. f_T of 3 MHz at 10 V, 500 mA**
- **Complements of n-p-n types BD241, BD241A, BD241B, and BD241C**

Types BD242, BD242A, BD242B, and BD242C are epitaxial-base silicon p-n-p transistors; they differ only in their voltage ratings. These devices are intended for a wide variety of switching and amplifier applications such as series and shunt regulators, and driver and output stages of high-fidelity amplifiers. The BD242-series power transistors are complements of the devices in the BD241 series. (The BD241-series devices are described in File No. 671.)

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		BD242	BD242A	BD242B	BD242C	
COLLECTOR-TO-EMITTER VOLTAGE:						
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}	−55	−70	−90	−115	V
With base open	V_{CEO}	−45	−60	−80	−100	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	−5	−5	−5	−5	V
CONTINUOUS COLLECTOR CURRENT	I_C	−5	−5	−5	−5	A
CONTINUOUS BASE CURRENT	I_B	−1	−1	−1	−1	A
TRANSISTOR DISSIPATION:	P_T					
At case temperatures up to 25°C		40	40	40	40	W
At ambient temperatures up to 25°C		2	2	2	2	W
At case temperatures above 25°C		← See Fig. 2 →				
TEMPERATURE RANGE:						
Storage & Operating (Junction)		← −65 to 150 →				°C
LEAD TEMPERATURE (During Soldering):						
At distance 1/8 in. (3.17 mm) from case for 10 s max.		← 235 →				°C

ELECTRICAL CHARACTERISTICS *at Case Temperature (T_C) = 25°C*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS								UNITS
		VOLTAGE V dc		CURRENT A dc		BD242		BD242A		BD242B		BD242C		
		V_{CE}	V_{BE}	I_C	I_B	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	-30			0	–	-0.3	–	-0.3	–	–	–	–	mA
		-60			0	–	–	–	–	–	-0.3	–	-0.3	
With base-to-emitter junction short-circuited	I_{CES}	-45	0			–	-0.2	–	–	–	–	–	–	
		-60	0			–	–	–	-0.2	–	–	–	–	
		-80	0			–	–	–	–	–	-0.2	–	–	
		-100	0			–	–	–	–	–	–	–	-0.2	
Emitter Cutoff Current	I_{EBO}		5	0		–	-1	–	-1	–	-1	–	-1	mA
Collector-to-Emitter Breakdown Voltage: With base open	$V_{BR(CEO)}$			-0.03[a]	0	-45	–	-60	–	-80	–	-100	–	V
DC Forward-Current Transfer Ratio	h_{FE}	-4		-1[a]		25	–	25	–	25	–	25	–	
		-4		-3[a]		10	–	10	–	10	–	10	–	
Base-to-Emitter Voltage	V_{BE}	-4		-3[a]		–	-1.8	–	-1.8	–	-1.8	–	-1.8	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$			-3[a]	-0.6	–	-1.2	–	-1.2	–	-1.2	–	-1.2	V
Common-Emitter Small-Signal Short-Circuit Forward-Current Transfer Ratio (f = 1 kHz)	h_{fe}	-10		-0.5		20	–	20	–	20	–	20	–	
Magnitude of Common Emitter Small-Signal Short-Circuit Forward-Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	-10		-0.5		3	–	3	–	3	–	3	–	
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$					–	3.125	–	3.125	–	3.125	–	3.125	°C/W
Junction-to-Ambient	$R_{\theta JA}$					–	62.5	–	62.5	–	62.5	–	62.5	

[a]Pulsed: Pulse duration = 300 μs, duty factor = 2%.

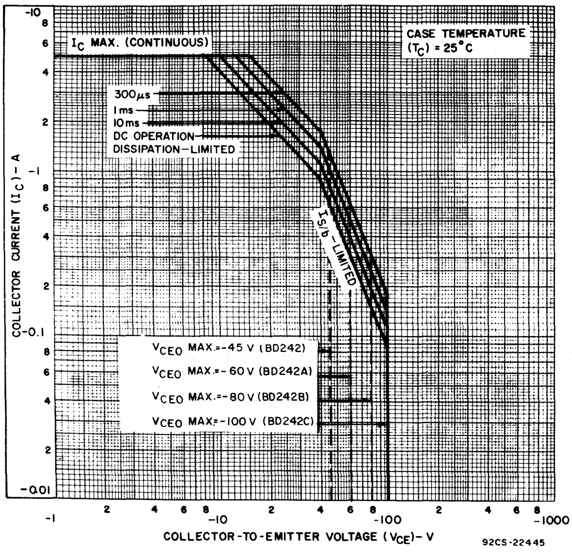


Fig. 1— Maximum safe operating areas for all types.

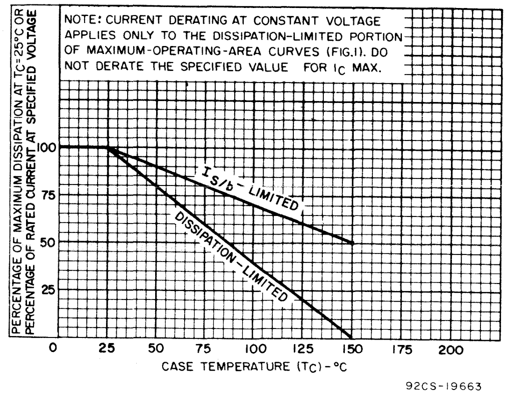


Fig. 2— Derating curves for all types.

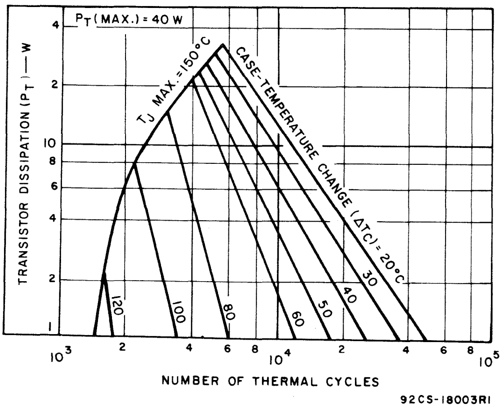


Fig. 3— Thermal-cycling ratings for all types.

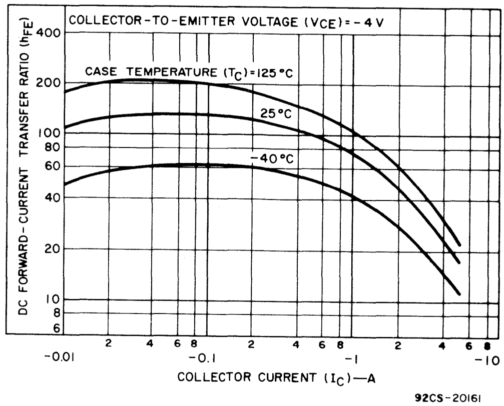


Fig. 4— Typical dc beta characteristics for all types.

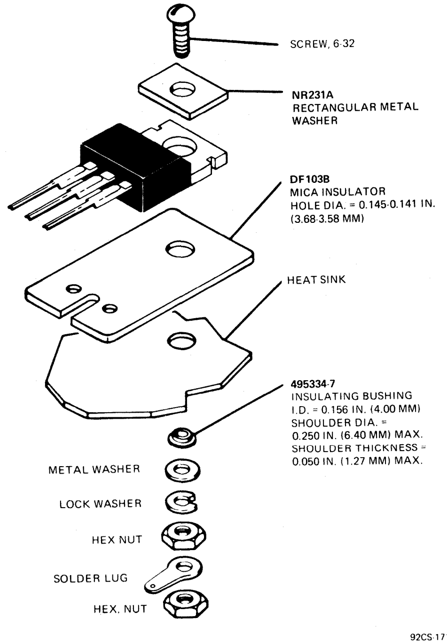
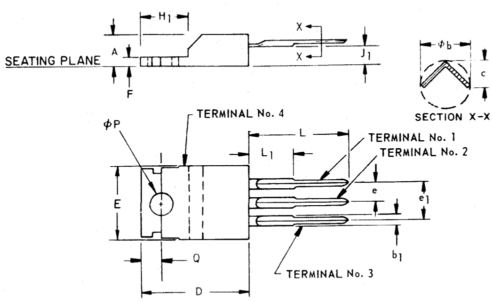


Fig. 5—Suggested mounting hardware for JEDEC TO-220AB.

DIMENSIONAL OUTLINE
JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

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NOTES:

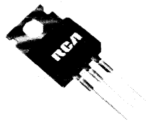
1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS

Terminal No. 1 — Base
Terminal No. 2 — Collector
Terminal No. 3 — Emitter
Terminal No. 4 — Collector

RCA
Solid State
Division

Power Transistors
BD243 BD243B
BD243A BD243C



JEDEC TO-220AB H-1535R1

Epitaxial-Base Silicon N-P-N VERSAWATT Transistors

For Power-Amplifier and High-Speed-Switching Applications

Features:

- **65 W at 25°C case temperature**
- **7-A rated collector current**
- **Min. f_T of 3 MHz at 10 V, 500 mA**
- **Complements of p-n-p types BD244, BD244A, BD244B, and BD244C**

Types BD243, BD243A, BD243B, and BD243C are epitaxial-base silicon n-p-n transistors; they differ only in their voltage ratings. These devices are intended for a wide variety of switching and amplifier applications such as series and shunt regulators, and driver and output stages of high-fidelity amplifiers. The BD243-series power transistors are complements of the devices in the BD244 series. (The BD244-series devices are described in File No. 674.)

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		BD243	BD243A	BD243B	BD243C	
COLLECTOR-TO-EMITTER VOLTAGE:						
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}	55	70	90	115	V
With base open	V_{CEO}	45	60	80	100	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	5	5	5	V
CONTINUOUS COLLECTOR CURRENT	I_C	7	7	7	7	A
PEAK COLLECTOR CURRENT	I_C (PEAK)	10	10	10	10	A
CONTINUOUS BASE CURRENT	I_B	3	3	3	3	A
TRANSISTOR DISSIPATION:	P_T					
At case temperatures up to 25°C		65	65	65	65	W
At ambient temperatures up to 25°C .		2	2	2	2	W
At case temperatures above 25°C		← See Fig. 2 →				
TEMPERATURE RANGE:						
Storage & Operating (Junction)		← -65 to 150 →				°C
LEAD TEMPERATURE (During Soldering):						
At distance 1/8 in. (3.17 mm) from case for 10 s max.		← 235 →				°C

ELECTRICAL CHARACTERISTICS *at Case Temperature (T_C) = 25°C*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS								UNITS
		VOLTAGE V dc		CURRENT A dc		BD243		BD243A		BD243B		BD243C		
		V_{CE}	V_{BE}	I_C	I_B	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	30			0	–	0.7	–	0.7	–	–	–	–	mA
		60			0	–	–	–	–	–	0.7	–	0.7	
With base-to-emitter junction short-circuited	I_{CES}	45	0			–	0.4	–	–	–	–	–	–	
		60	0			–	–	–	0.4	–	–	–	–	
		80	0			–	–	–	–	–	0.4	–	–	
		100	0			–	–	–	–	–	–	–	0.4	
Emitter Cutoff Current	I_{EBO}		–5	0		–	1	–	1	–	1	–	1	mA
Collector-to-Emitter Breakdown Voltage: With base open	$V_{BR(CEO)}$			0.03[a]	0	45	–	60	–	80	–	100	–	V
DC Forward-Current Transfer Ratio	h_{FE}	4		0.3[a]		30	–	30	–	30	–	30	–	
		4		3[a]		15	–	15	–	15	–	15	–	
Base-to-Emitter Voltage	V_{BE}	4		6[a]		–	2	–	2	–	2	–	2	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$			6[a]	1	–	1.5	–	1.5	–	1.5	–	1.5	V
Common-Emitter Small-Signal Short-Circuit Forward-Current Transfer Ratio (f = 1 kHz)	h_{fe}	10		0.5		20	–	20	–	20	–	20	–	
Magnitude of Common Emitter Small-Signal Short-Circuit Forward-Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	10		0.5		3	–	3	–	3	–	3	–	
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$					–	1.92	–	1.92	–	1.92	–	1.92	°C/W
Junction-to-Ambient	$R_{\theta JA}$					–	62.5	–	62.5	–	62.5	–	62.5	

[a]Pulsed: Pulse duration = 300 μs, duty factor = 2%.

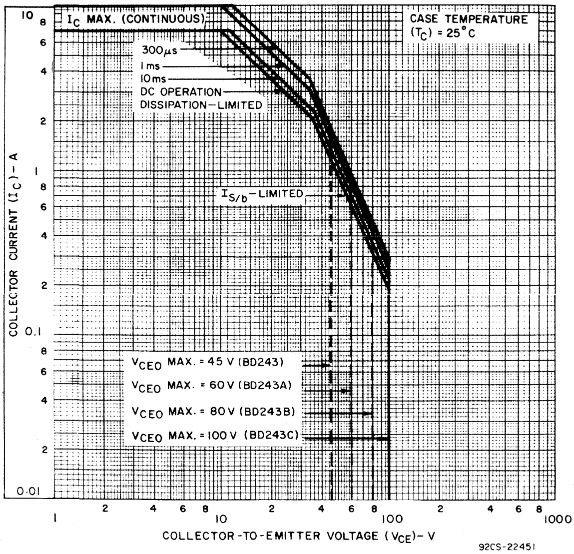


Fig. 1— Maximum safe operating areas for all types.

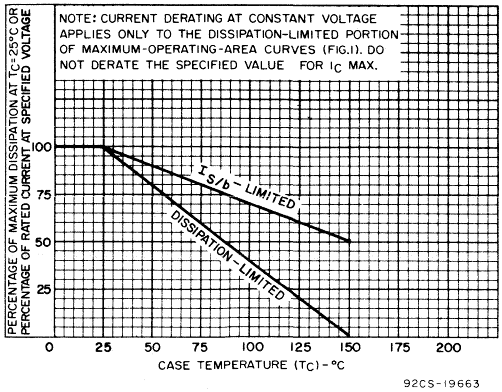


Fig. 2— Derating curves for all types.

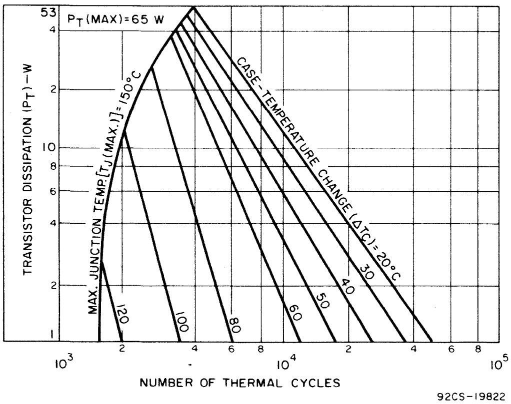


Fig. 3—Thermal-cycling ratings for all types.

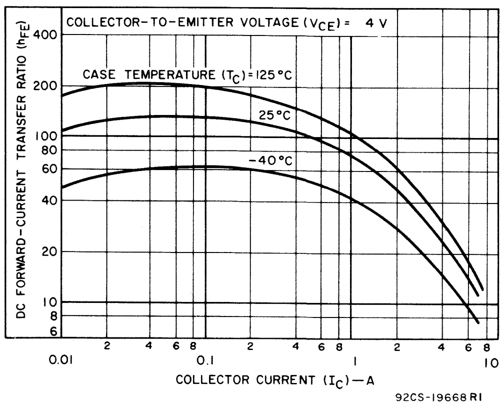


Fig. 4— Typical dc beta characteristics for all types.

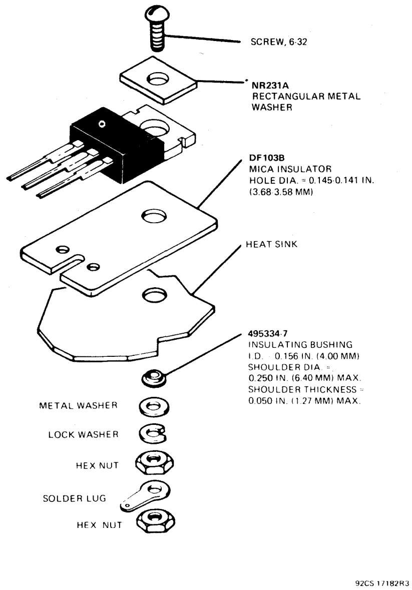
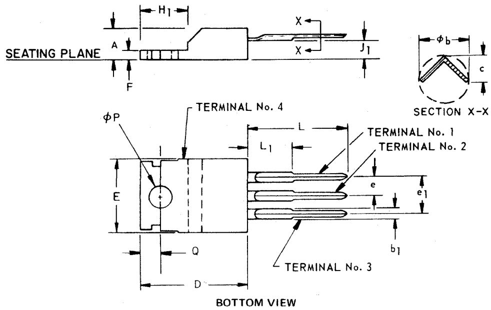


Fig. 5— Suggested mounting hardware for JEDEC TO-220AB.

DIMENSIONAL OUTLINE
JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

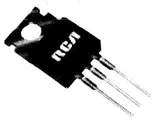
NOTES:
1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS

Terminal No. 1 — Base
Terminal No. 2 — Collector
Terminal No. 3 — Emitter
Terminal No. 4 — Collector

Solid State
Division

Power Transistors
BD244 BD244B
BD244A BD244C



JEDEC TO-220 AB H-1535R1

Epitaxial-Base Silicon P-N-P VERSAWATT Transistors

For Power-Amplifier and
High-Speed-Switching Applications

Features:
- **65 W at 25°C case temperature**
- **7-A rated collector current**
- **Min. f_T of 3 MHz at 10 V, 500 mA**
- **Complements of n-p-n types BD243, BD243A, BD243B, and BD243C**

Types BD244, BD244A, BD244B, and BD244C are epitaxial-base silicon p-n-p transistors; they differ only in their voltage ratings. These devices are intended for a wide variety of switching and amplifier applications such as series and shunt regulators, and driver and output stages of high-fidelity amplifiers. The BD244-series power transistors are complements of the devices in the BD243 series. (The BD243-series devices are described in File No. 673.)

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		BD244	BD244A	BD244B	BD244C	
COLLECTOR-TO-EMITTER VOLTAGE:						
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}	-55	-70	-90	-115	V
With base open	V_{CEO}	-45	-60	-80	-100	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	-5	-5	-5	-5	V
CONTINUOUS COLLECTOR CURRENT	I_C	-7	-7	-7	-7	A
PEAK COLLECTOR CURRENT	I_C (PEAK)	-10	-10	-10	-10	A
CONTINUOUS BASE CURRENT	I_B	-3	-3	-3	-3	A
TRANSISTOR DISSIPATION:	P_T					
At case temperatures up to 25°C		65	65	65	65	W
At ambient temperatures up to 25°C .		2	2	2	2	W
At case temperatures above 25°C		← See Fig. 2 →				
TEMPERATURE RANGE:						
Storage & Operating (Junction)		← -65 to 150 →				°C
LEAD TEMPERATURE (During Soldering):						
At distance 1/8 in. (3.17 mm) from case for 10 s max.		← 235 →				°C

ELECTRICAL CHARACTERISTICS *at Case Temperature (T_C) = 25°C*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS								UNITS
		VOLTAGE V dc		CURRENT A dc		BD244		BD244A		BD244B		BD244C		
		V_{CE}	V_{BE}	I_C	I_B	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	−30			0	–	−0.7	–	−0.7	–	–	–	–	mA
		−60			0	–	–	–	–	–	−0.7	–	−0.7	
With base-to-emitter junction short-circuited	I_{CES}	−45	0			–	−0.4	–	–	–	–	–	–	
		−60	0			–	–	–	−0.4	–	–	–	–	
		−80	0			–	–	–	–	–	−0.4	–	–	
		−100	0			–	–	–	–	–	–	–	−0.4	
Emitter Cutoff Current	I_{EBO}		5	0		–	−1	–	−1	–	−1	–	−1	mA
Collector-to-Emitter Breakdown Voltage: With base open	$V_{BR(CEO)}$			−0.03[a]	0	−45	–	−60	–	−80	–	−100	–	V
DC Forward-Current Transfer Ratio	h_{FE}	−4		−0.3[a]		30	–	30	–	30	–	30	–	
		−4		−3[a]		15	–	15	–	15	–	15	–	
Base-to-Emitter Voltage	V_{BE}	−4		−6[a]		–	−2	–	−2	–	−2	–	−2	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$			−6[a]	−1	–	−1.5	–	−1.5	–	−1.5	–	−1.5	V
Common-Emitter Small-Signal Short-Circuit Forward-Current Transfer Ratio (f = 1 kHz)	h_{fe}	−10		−0.5		20	–	20	–	20	–	20	–	
Magnitude of Common Emitter Small-Signal Short-Circuit Forward-Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	−10		−0.5		3	–	3	–	3	–	3	–	
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$					–	1.92	–	1.92	–	1.92	–	1.92	°C/W
Junction-to-Ambient	$R_{\theta JA}$					–	62.5	–	62.5	–	62.5	–	62.5	

[a]Pulsed: Pulse duration = 300 μs, duty factor = 2%.

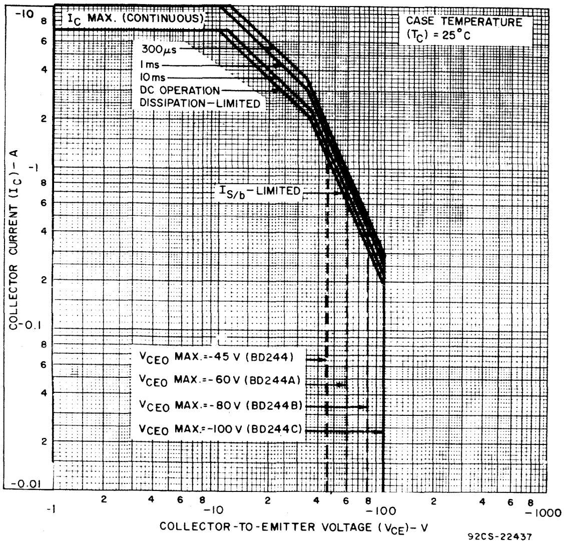


Fig. 1— Maximum safe operating areas for all types.

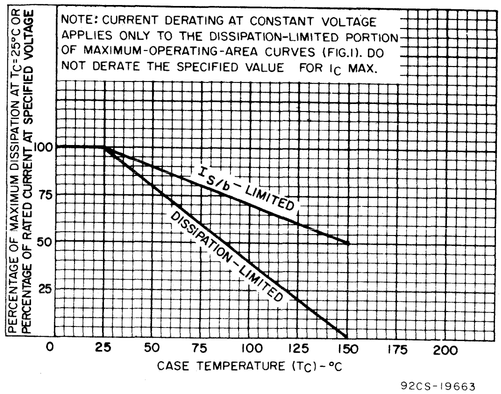


Fig. 2— Derating curves for all types.

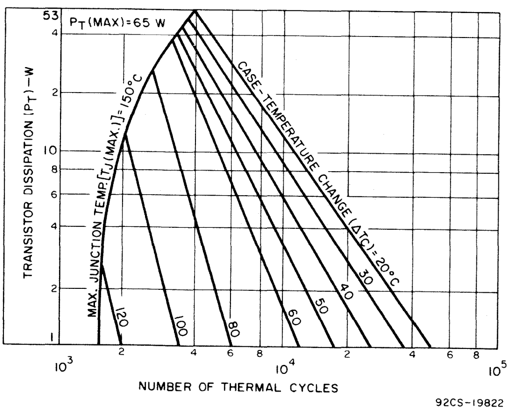


Fig. 3— Thermal-cycling ratings for all types.

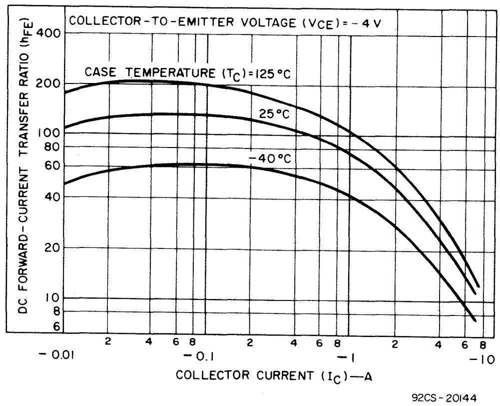


Fig. 4— Typical dc beta characteristics for all types.

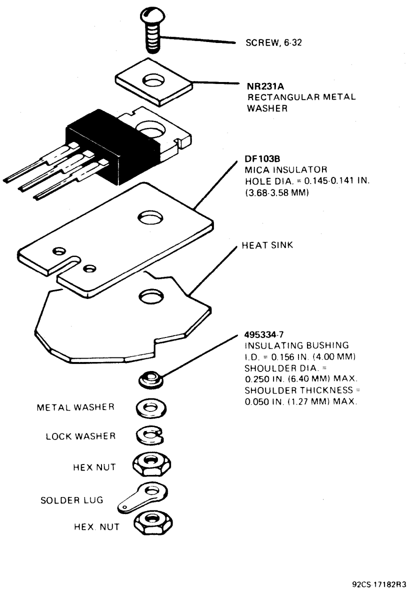
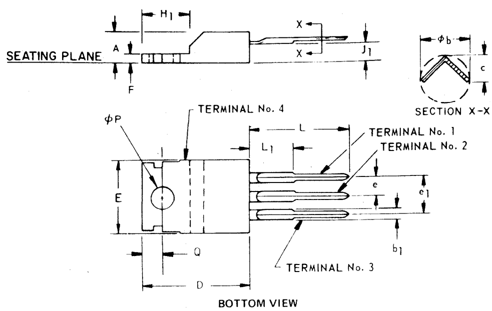


Fig. 5— Suggested mounting hardware for JEDEC TO-220AB.

DIMENSIONAL OUTLINE
JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
ϕb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
ϕP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

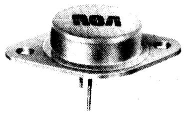
1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS

Terminal No. 1 — Base
Terminal No. 2 — Collector
Terminal No. 3 — Emitter
Terminal No. 4 — Collector

RCA Solid State Division

Power Transistors
2N6470 2N6471 2N6472
2N6246 2N6247 2N6248 2N6469



JEDEC TO-3

H-1570

Silicon N-P-N and P-N-P Epitaxial-Base High-Power Transistors

General-Purpose Types for Switching and Linear-Amplifier Applications

Features:

- **High dissipation capability: 125 W at 25°C**
- **Low saturation voltages**
- **Maximum safe-area-of-operation curves**
- **Hermetically sealed JEDEC TO-3 package**
- **High gain at high current**
- **Thermal-cycling rating curve**

RCA-2N6246, 2N6247, 2N6248, and 2N6469▲ are epitaxial-base silicon p-n-p transistors featuring high gain at high current. RCA-2N6470, 2N6471, and 2N6472● are epitaxial-base silicon n-p-n transistors. They may be used as complements to the 2N6469, 2N6246, and 2N6247, respectively. All of these devices have a dissipation capability of 125 watts at case temperatures up to 25°C. They differ in voltage ratings and in the currents at which the parameters are controlled. All are supplied in the JEDEC TO-3 package.

▲ Formerly RCA Dev. Nos. TA7281, TA7280, TA7279, and TA8724, respectively.

● Formerly RCA Dev. Nos. TA8726, TA8443, and TA8442, respectively.

Maximum Ratings, *Absolute-Maximum Values:*

		N-P-N	2N6470	2N6471	2N6472		
		P-N-P	2N6469◆	2N6246◆	2N6247◆	2N6248◆	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}		50	70	90	110	V
COLLECTOR-TO-EMITTER VOLTAGE:							
* With 1.5 volts (V_{BE}) of reverse bias, and external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CEX}		50	70	90	110	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}		45	65	85	105	V
With base open	V_{CEO}		40	60	80	100	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}		5	5	5	5	V
*CONTINUOUS COLLECTOR CURRENT	I_C		15	15	15	10	A
*CONTINUOUS BASE CURRENT	I_B		5	5	5	5	A
*TRANSISTOR DISSIPATION:	P_T						
At case temperatures up to 25°C			125	125	125	125	W
At case temperatures above 25°C			← See Fig. 3 →				
*TEMPERATURE RANGE:							
Storage & Operating (Junction)			← -65 to +200 →				°C
*PIN TEMPERATURE (During Soldering):							
At distances ⩾ 1/32" (0.8 mm) from seating plane for 10 s max.			← +235 →				°C

* In accordance with JEDEC registration data format (JS-6 RDF-2).

◆ **For p-n-p devices, voltage and current values are negative.**

ELECTRICAL CHARACTERISTICS FOR N-P-N TYPES, *At case temperature (T_C) = 25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: VOLTAGE V dc V_{CE}	V_{EB}	V_{BE}	CURRENT A dc I_C	I_B	LIMITS: 2N6470 Min.	2N6470 Max.	2N6471 Min.	2N6471 Max.	2N6472 Min.	2N6472 Max.	UNITS
Collector-Cutoff Current: With external base-emitter resistance (R_{BE}) = 100Ω	I_{CER}	35 55 75					– – –	500 – –	– – –	– 500 –	– – –	– – 500	µA
* With base-emitter junction reverse biased and external base-to-emitter resistance (R_{BE}) = 100Ω	I_{CEX}	45 65 85		−1.5 −1.5 −1.5			– – –	500 – –	– – –	– 500 –	– – –	– – 500	µA
* At T_C = 150°C	I_{CEX}	40 60 80		−1.5 −1.5 −1.5			– – –	5 – –	– – –	– 5 –	– – –	– – 5	mA
* With base open	I_{CEO}	20 30 40				0 0 0	– – –	1 – –	– – –	– 1 –	– – –	– – 1	mA
* Emitter-Cutoff Current	I_{EBO}		5				–	1	–	1	–	1	mA
* DC Forward-Current Transfer Ratio	h_{FE}	4 4			5[a] 15[a]		20 5	150 –	20 5	150 –	20 5	150 –	
* Collector-to-Emitter Sustaining Voltage With base open	$V_{CEO}(sus)$				0.2	0	40[b]	–	60[b]	–	80[b]	–	V
With external base-emitter resistance (R_{BE}) = 100Ω	$V_{CER}(sus)$				0.2		45[b]	–	65[b]	–	85[b]	–	V
With base-emitter junction reverse-biased and external base-to-emitter resistance (R_{BE}) = 100Ω	$V_{CEX}(sus)$			−1.5	0.2		50[b]	–	70[b]	–	90[b]	–	V
* Base-to-Emitter Voltage	V_{BE}	4 4			5[a] 15[a]		– –	1.3 3.5	– –	1.3 3.5	– –	1.3 3.5	V
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				5[a] 15[a]	0.5 5	– –	1.3 3.5	– –	1.3 3.5	– –	1.3 3.5	V
* Magnitude of Common-Emitter Small-Signal Short-Circuit Forward-Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	4			1		5	–	5	–	5	–	
* Common-Emitter, Small-Signal, Short-Circuit, Forward-Current Transfer Ratio (f = 1 kHz)	h_{fe}	4			1		25	–	25	–	25	–	
Thermal Resistance (Junction-to-case)	$R_{\theta JC}$						–	1.4	–	1.4	–	1.4	°C/W

* In accordance with JEDEC registration data format (JS-6 RDF-2).

[a] Pulsed; pulse duration = 300 µs, duty factor = 1.8%.

[b] *CAUTION: Sustaining voltages $V_{CEO}(sus)$, $V_{CER}(sus)$, and $V_{CEX}(sus)$ MUST NOT be measured on a curve tracer. (See Fig. 24.)*

ELECTRICAL CHARACTERISTICS FOR P-N-P TYPES, *At case temperature (T_C) = 25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS								UNITS
		VOLTAGE V dc			CURRENT A dc		2N6469		2N6246		2N6247		2N6248		
		V_{CE}	V_{EB}	V_{BE}	I_C	I_B	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Collector-Cutoff Current: With external base-emitter resistance (R_{BE}) = 100Ω	I_{CER}	−35					–	−200	–	–	–	–	–	–	μA
		−55					–	–	–	−200	–	–	–	–	
		−75					–	–	–	–	–	−200	–	–	
		−95					–	–	–	–	–	–	–	−200	
* With base-emitter junction reverse biased and external base-to-emitter resistance (R_{BE}) 100Ω	I_{CEX}	−45		1.5			–	−200	–	–	–	–	–	–	μA
		−65		1.5			–	–	–	−200	–	–	–	–	
		−85		1.5			–	–	–	–	–	−200	–	–	
		−100		1.5			–	–	–	–	–	–	–	−200	
* At T_C = 150°C		−45		1.5			–	−5	–	–	–	–	–	–	mA
		55		1.5			–	–	–	−5	–	–	–	–	
		−70		1.5			–	–	–	–	–	−5	–	–	
		−90		1.5			–	–	–	–	–	–	–	−5	
* With base open	I_{CEO}	−20				0	–	−1	–	–	–	–	–	–	mA
		−30				0	–	–	–	−1	–	–	–	–	
		−40				0	–	–	–	–	–	−1	–	–	
		−50				0	–		–	–	–	–	–	−1	
* Emitter-Cutoff Current	I_{EBO}		−5				–	−5	–	−5	–	−1	–	−1	mA
* DC Forward-Current Transfer Ratio	h_{FE}	−4			−5[a]		20	150	–	–	–	–	20	100	
		−4			−7[a]		–	–	20	100	–	–	–	–	
		−4			−6[a]		–	–	–	–	20	100	–	–	
		−4			−10[a]		–	–	–	–	–	–	5	–	
		−4			−15[a]		5	–	5	–	5	–	–	–	
* Collector-to-Emitter Sustaining Voltage With base open	$V_{CEO}(sus)$				−0.2	0	−40[b]	–	−60[b]	–	−80[b]	–	−100[b]	–	V
With external base-emitter resistance (R_{BE}) = 100Ω	$V_{CER}(sus)$				−0.2		−45[b]	–	−65[b]	–	−85[b]	–	−105[b]	–	
With base-emitter junction reverse-biased and external base-to-emitter resistance (R_{BE}) = 100Ω	$V_{CEX}(sus)$			1.5	−0.2		−50[b]	–	−70[b]	–	−90[b]	–	−110[b]	–	
* Base-to-Emitter Voltage	V_{BE}	−4			−15[a]		–	−3.5	–	–	–	–	–	–	V
		−4			−7[a]		–	–	–	−2	–	–	–	–	
		−4			−6[a]		–	–	–	–	–	−1.8	–	–	
		−4			−5[a]		–	–	–	–	–	–	–	−1.8	
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				−5[a]	−0.5	–	−1.3	–	–	–	–	–	−1.3	V
					−7[a]	−0.7	–	–	–	−1.3	–	–	–	–	
					−6[a]	−0.6	–	–	–	–	–	−1.3	–	–	
					−15[a]	−5	–	−3.5	–	–	–	–	–	–	
					−15[a]	−3	–	–	–	−2.5	–	–	–	–	
					−15[a]	−4	–	–	–	–	–	−3.5	–	–	
					−10[a]	−2	–	–	–	–	–	–	–	−3.5	
* Magnitude of Common-Emitter Small-Signal Short-Circuit Forward-Current Transfer Ratio (f = 2 MHz)	$\|h_{fe}\|$	−4			−1		5	–	5	–	5	–	5	–	
* Common-Emitter, Small-Signal, Short-Circuit, Forward-Current Transfer Ratio (f = 1 kHz)	h_{fe}	−4			−1		25	–	25	–	25	–	25	–	
Thermal Resistance (Junction-to-case)	$R_{\theta JC}$						–	1.4	–	1.4	–	1.4	–	1.4	°C/W

* In accordance with JEDEC registration data format (JS-6 RDF-2).

[a] Pulsed; pulse duration = 300 μs, duty factor = 1.8%.

[b] *CAUTION: Sustaining voltages $V_{CEO}(sus)$, $V_{CER}(sus)$, and $V_{CEX}(sus)$ MUST NOT be measured on a curve tracer, (See Fig. 24.)*

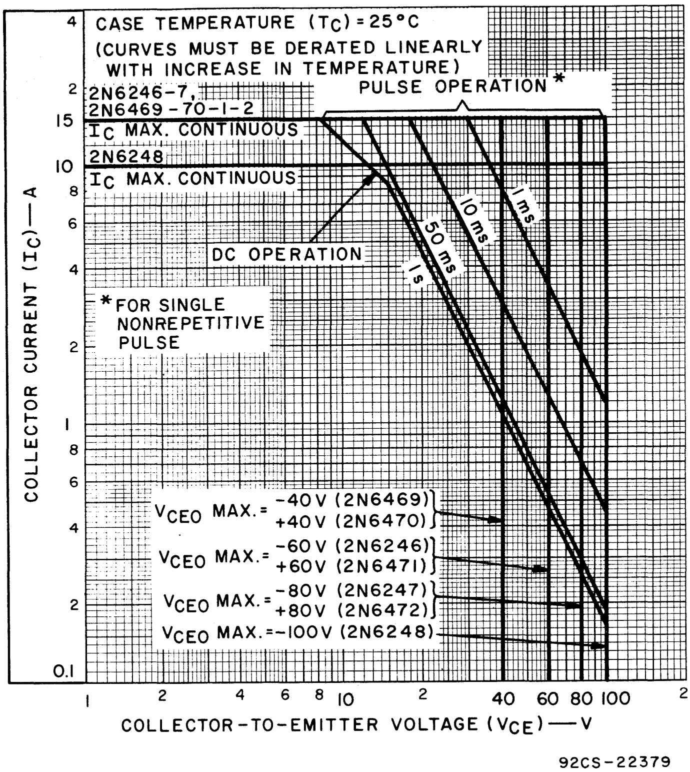


Fig.1 — Maximum operating areas for all types.

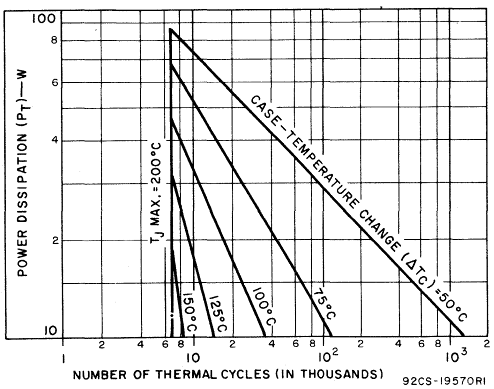


Fig.2 — Thermal-cycling rating chart for all types.

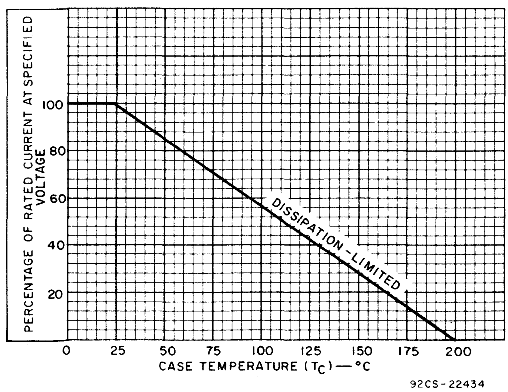


Fig.3 — Current derating for all types.

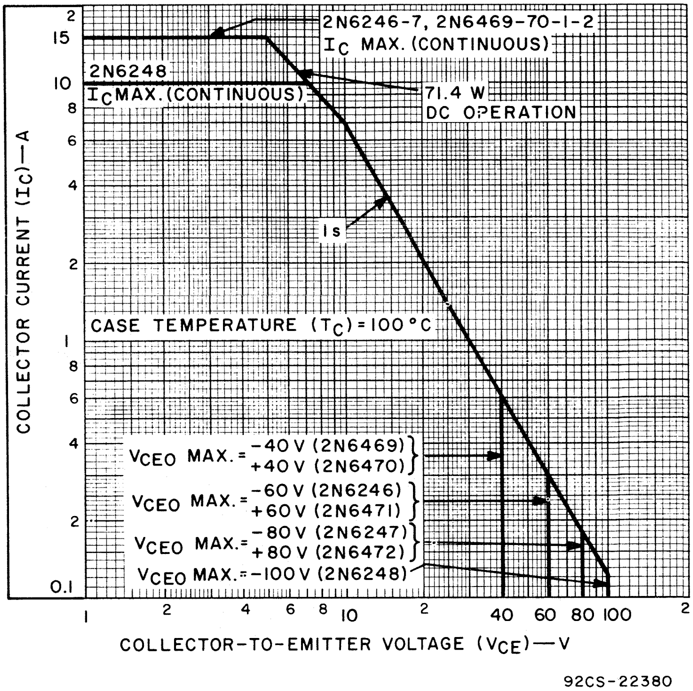


Fig.4 — Maximum operating areas for all types.

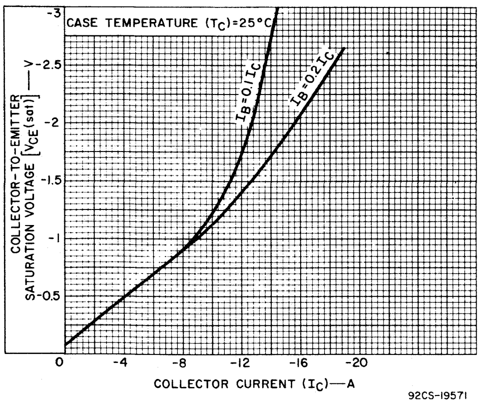


Fig.5 — Typical collector-to-emitter saturation-voltage characteristics for 2N6246, 2N6247, 2N6248, and 2N6469.

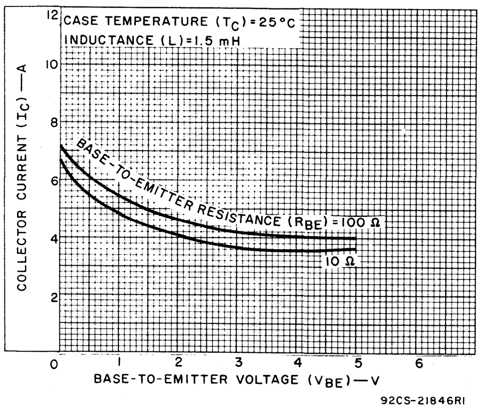


Fig.6 — Minimum reverse-bias second-breakdown characteristics for all types. (Values for p-n-p types are negative).

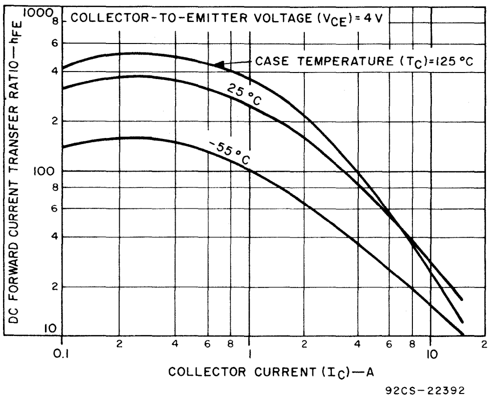


Fig.7 – Typical dc beta characteristics for 2N6470, 2N6471, and 2N6472.

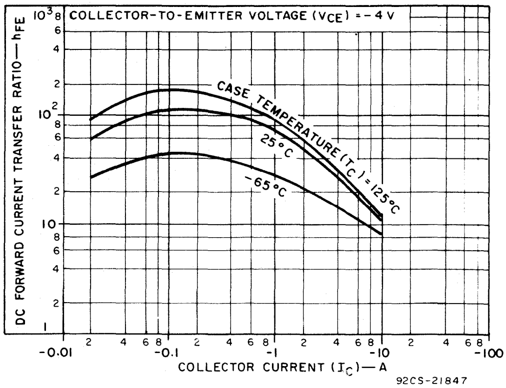


Fig.8 – Typical dc beta characteristics for 2N6248.

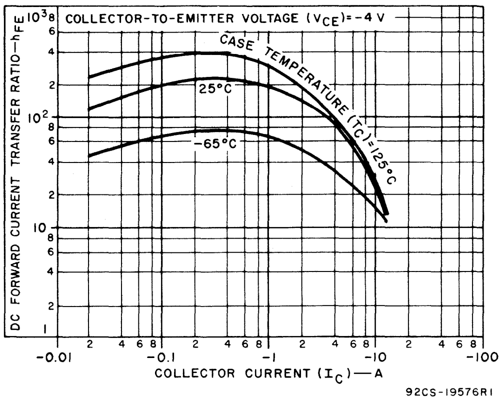


Fig.9 – Typical dc beta characteristics for 2N6246, 2N6247, and 2N6469.

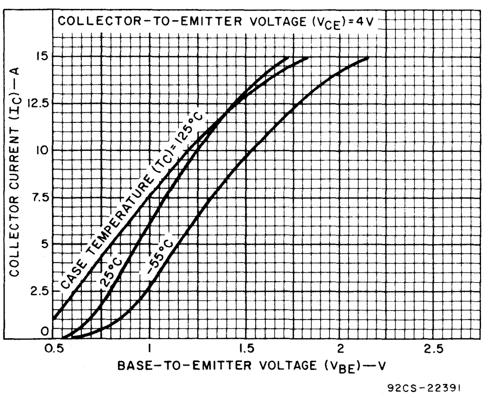


Fig.10 – Typical transfer characteristics for 2N6470, 2N6471, and 2N6472.

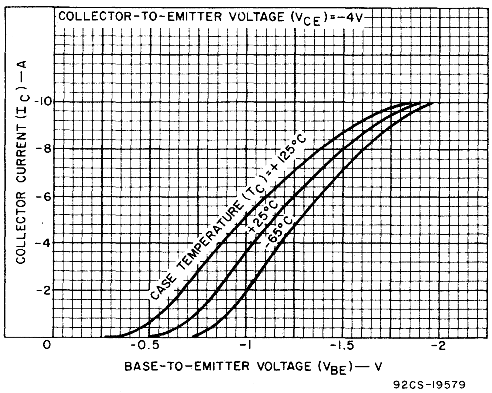


Fig.11 – Typical transfer characteristics for 2N6246, 2N6247, 2N6248, and 2N6469.

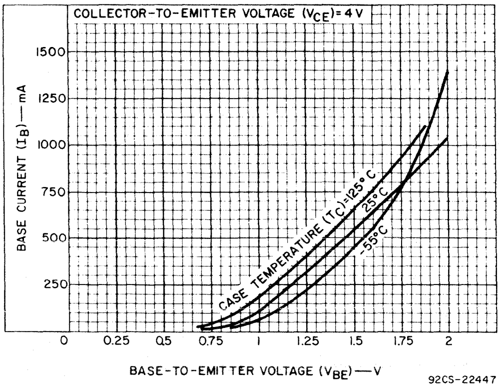


Fig.12 – Typical input characteristics for 2N6470, 2N6471, and 2N6472.

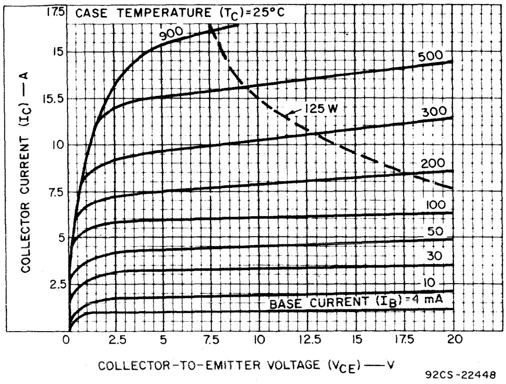


Fig.13 – Typical output characteristics for 2N6470, 2N6471, and 2N6472.

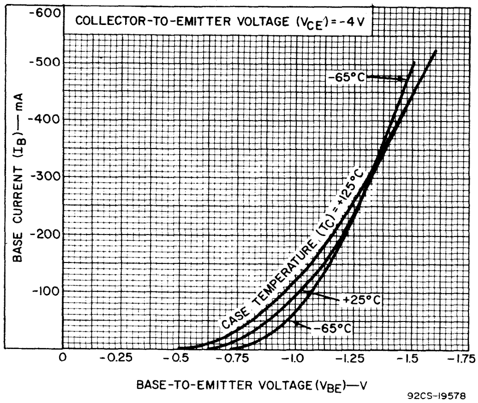


Fig.14 – Typical input characteristics for 2N6248.

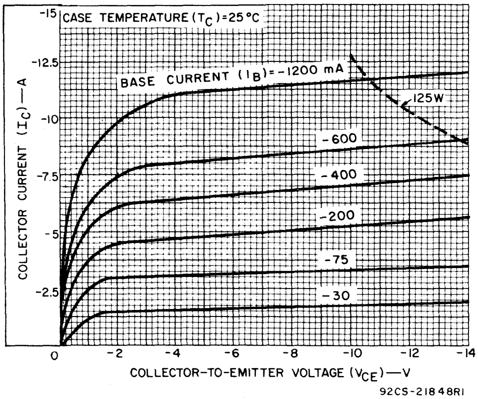


Fig.15 – Typical output characteristics for 2N6248.

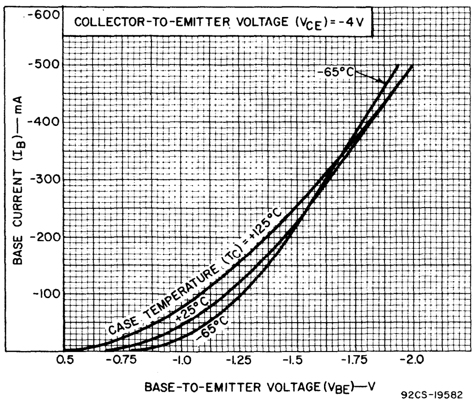


Fig.16 – Typical input characteristics for 2N6246, 2N6247, and 2N6469.

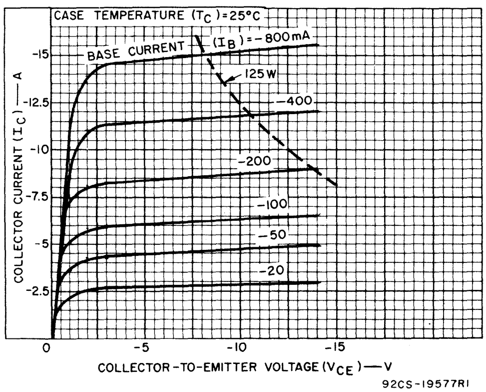


Fig.17 – Typical output characteristics for 2N6246, 2N6247, and 2N6469.

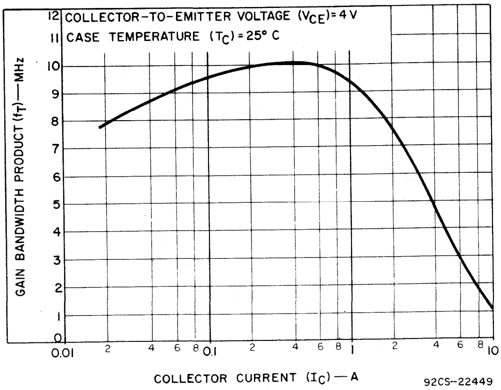


Fig.18 — Typical gain-bandwidth product vs. collector current for 2N6470, 2N6471, and 2N6472.

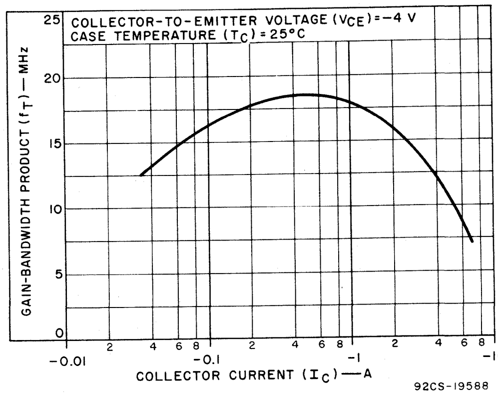


Fig.19 — Typical gain-bandwidth product vs. collector current for 2N6246, 2N6247, 2N6248, and 2N6469.

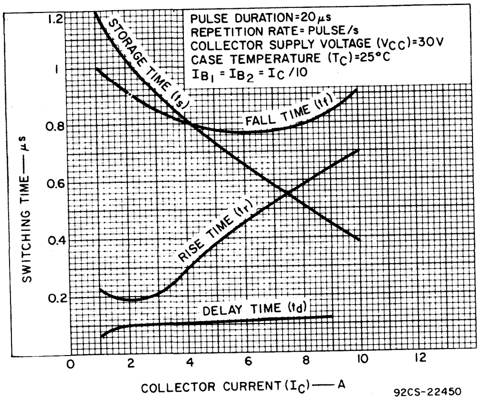


Fig.20 — Typical saturated switching characteristics for 2N6470, 2N6471, and 2N6472.

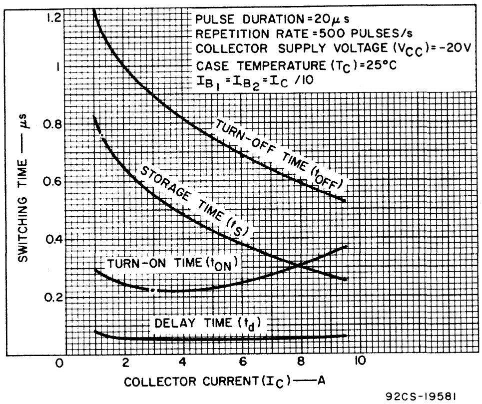
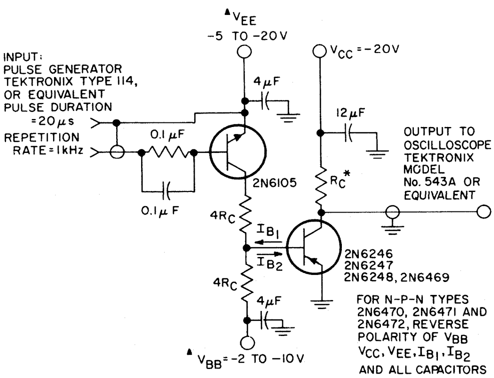


Fig.21 — Typical saturated switching characteristics for 2N6246, 2N6247, 2N6248, and 2N6469.



* R_C IS CHOSEN FOR I_C
▲ V_{EE} AND V_{BB} ARE MEASURED FOR I_{B1} AND I_{B2}
I_{B1} AND I_{B2} ARE MEASURED WITH TEKTRONIX CURRENT PROBE P-6019 AND TYPE 134 AMPLIFIER, OR EQUIVALENT 92CS-19586R1

Fig.22 — Circuit used to measure saturated switching times.

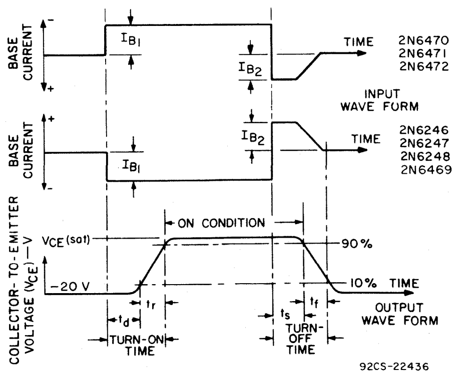


Fig.23 — Oscilloscope display for measurement of switching times.

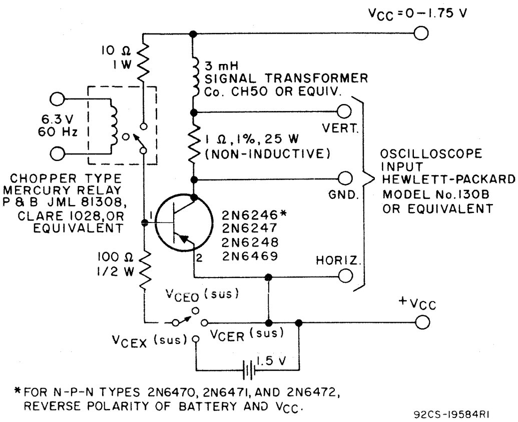
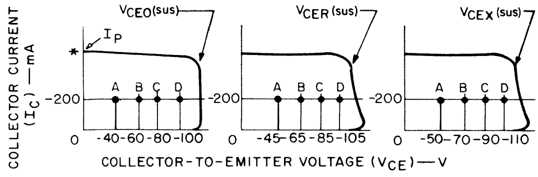


Fig.24 — Circuit used to measure sustaining voltages $V_{CEO}(sus)$, $V_{CER}(sus)$, and $V_{CEX}(sus)$ for all types.

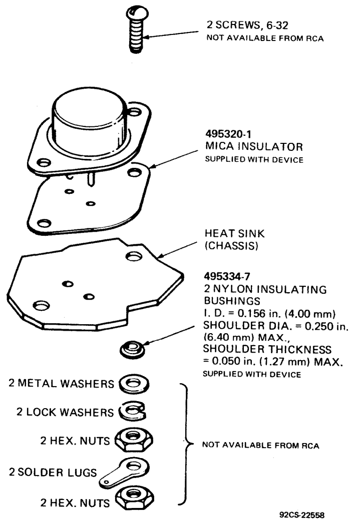


* PULSE CURRENT (I_P) RANGE = 0.6 – 0.8 A

THE SUSTAINING VOLTAGES $V_{CEO}(sus)$, $V_{CER}(sus)$, AND $V_{CEX}(sus)$ ARE ACCEPTABLE WHEN THE TRACES FALL TO THE RIGHT AND ABOVE POINT "A" FOR TYPES 2N6469 AND 2N6470; POINT "B" FOR 2N6246 and 2N6471; POINT "C" FOR 2N6247 AND 2N6472; AND POINT "D" FOR 2N6248. VALUES FOR N-P-N TYPES ARE POSITIVE.

92CS-22452

Fig.25 — Oscilloscope display for measurement of sustaining voltages (test circuit shown in Fig.24).

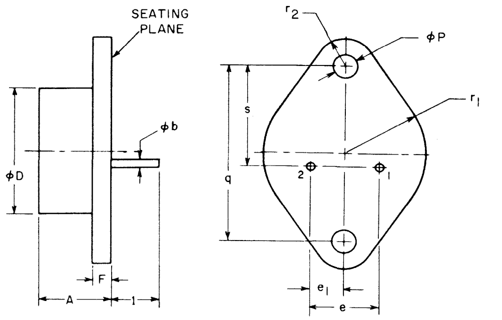


In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.26 — Suggested mounting hardware.

For basic transistor theory, circuits, and application information, refer to "RCA Solid State Power Circuits Designer's Handbook", SP-52, or "RCA Transistor, Thyristor, & Diode Manual", SC-15.

DIMENSIONAL OUTLINE JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
ϕb	0.038	0.043	0.97	1.09	2
ϕD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e_1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
l	0.312		7.92		2
ϕP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r_1		0.525		13.34	
r_2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:
1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS–15222

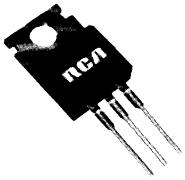
TERMINAL CONNECTIONS

Pin 1 — Base
Pin 2 — Emitter
Case — Collector
Mounting Flange — Collector

RCA

Solid State
Division

Power Transistors
2N6486 2N6489
2N6487 2N6490
2N6488 2N6491



JEDEC TO-220AB H-1535

15-A, 75-W, Silicon N-P-N and P-N-P Epitaxial-Base VERSAWATT Transistors

Complementary Pairs for General-Purpose Switching and Amplifier Applications

Features:

- **Thermal-cycling ratings**
- **Maximum safe-area-of-operation curves**
- **Color-coded packages of molded-silicone plastic:**
  Green – p-n-p (2N6489, 2N6490, 2N6491)
  Gray – n-p-n (2N6486, 2N6487, 2N6488)

RCA-2N6486–2N6491●, inclusive, are epitaxial-base silicon transistors. The 2N6486, 2N6487, and 2N6488 are n-p-n complements of p-n-p types 2N6489, 2N6490, and 2N6491, respectively. All these devices are intended for a wide variety of medium-power switching and amplifier applications, and are particularly useful in high-fidelity amplifiers utilizing complementary-symmetry circuits.

● Formerly RCA Dev. Nos. TA8325, TA8324, TA8323, TA8328, TA8327, and TA8326, respectively.

These devices are supplied in the RCA VERSAWATT package in color-coded molded-silicone plastic; the 2N6489–2N6491 (p-n-p) devices are green, and the 2N6486–2N6488 (n-p-n) devices are gray. All are regularly supplied in the JEDEC TO-220AB straight-lead version of the package. They are also available on special order in a variety of lead-form configurations. Detailed information on these and other VERSAWATT outlines is contained in "RCA's Lineup of Power Transistors" (PSP-704).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		N-P-N	2N6486	2N6487	2N6488	
		P-N-P	2N6489♦	2N6490♦	2N6491♦	
* COLLECTOR-TO-BASE VOLTAGE	V_{CBO}		50	70	90	V
COLLECTOR-TO-EMITTER VOLTAGE:						
* With 1.5 volts (V_{BE}) of reverse bias, and external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CEX}		50	70	90	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}		45	65	85	V
With base open	V_{CEO}		40	60	80	V
* EMITTER-TO-BASE VOLTAGE	V_{EBO}		5	5	5	V
* CONTINUOUS COLLECTOR CURRENT	I_C		15	15	15	A
* CONTINUOUS BASE CURRENT	I_B		5	5	5	A
* TRANSISTOR DISSIPATION:	P_T					
At case temperatures up to 25°C			75	75	75	W
At ambient temperatures up to 25°C			1.8	1.8	1.8	W
At case temperatures above 25°C				Derate linearly 0.6		W/°C
At ambient temperatures above 25°C				Derate linearly 0.0144		W/°C
* TEMPERATURE RANGE:						
Storage and operating (Junction)				–65 to +150		°C
* LEAD TEMPERATURE (During soldering): At distance ≥ 1/8 in. (3.17 mm) from seating plane for 10 s max.				235		°C

* In accordance with JEDEC registration data format JS-6 RDF-2.

♦ For p-n-p devices, voltage and current values are negative.

11-73

ELECTRICAL CHARACTERISTICS, *At case temperature (T_C) = 25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: VOLTAGE V dc V_{CE}	V_{EB}	V_{BE}	CURRENT A dc I_C	I_B	LIMITS: 2N6486 2N6489◆ Min.	Max.	2N6487 2N6490◆ Min.	Max.	2N6488 2N6491◆ Min.	Max.	UNITS
Collector-Cutoff Current: With external base-emitter resistance (R_{BE}) = 100Ω	I_{CER}	35 55 75					– – –	500 – –	– – –	– 500 –	– – –	– – 500	μA
* With base-emitter junction reverse biased and external base-to-emitter resistance (R_{BE}) = 100Ω	I_{CEX}	45 65 85		–1.5 –1.5 –1.5			– – –	500 – –	– – –	– 500 –	– – –	– – 500	μA
* At T_C = 150°C	I_{CEX}	40 60 80		–1.5 –1.5 –1.5			– – –	5 – –	– – –	– 5 –	– – –	– – 5	mA
* With base open	I_{CEO}	20 30 40				0 0 0	– – –	1 – –	– – –	– 1 –	– – –	– – 1	mA
* Emitter-Cutoff Current	I_{EBO}		5				–	1	–	1	–	1	mA
* DC Forward-Current Transfer Ratio	h_{FE}	4 4			5[a] 15[a]		20 5	150 –	20 5	150 –	20 5	150 –	
* Collector-to-Emitter Sustaining Voltage With base open	$V_{CEO}(sus)$				0.2	0	40[b]	–	60[b]	–	80[b]	–	V
With external base-emitter resistance (R_{BE}) = 100Ω	$V_{CER}(sus)$				0.2		45[b]	–	65[b]	–	85[b]	–	V
With base-emitter junction reverse-biased and external base-to-emitter resistance (R_{BE}) = 100Ω	$V_{CEX}(sus)$			–1.5	0.2		50[b]	–	70[b]	–	90[b]	–	V
* Base-to-Emitter Voltage	V_{BE}	4 4			5[a] 15[a]		– –	1.3 3.5	– –	1.3 3.5	– –	1.3 3.5	V
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				5[a] 15[a]	0.5 5	– –	1.3 3.5	– –	1.3 3.5	– –	1.3 3.5	V
* Magnitude of Common-Emitter Small-Signal Short-Circuit Forward-Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	4			1		5	–	5	–	5	–	
* Common-Emitter, Small-Signal, Short-Circuit, Forward-Current Transfer Ratio (f = 1 kHz)	h_{fe}	4			1		25	–	25	–	25	–	
Thermal Resistance (Junction-to-case)	$R_{\theta JC}$						–	1.67	–	1.67	–	1.67	°C/W
(Junction-to-ambient)	$R_{\theta JA}$						–		–	70	–	70	°C/W

* In accordance with JEDEC registration data format (JS-6 RDF-2).

[a] Pulsed; pulse duration = 300 μs, duty factor = 1.8%.

[b] *CAUTION: Sustaining voltages $V_{CEO}(sus)$, $V_{CER}(sus)$, and $V_{CEX}(sus)$ MUST NOT be measured on a curve tracer. (See Fig. 15)*

◆ For p-n-p devices, voltage and current values are negative.

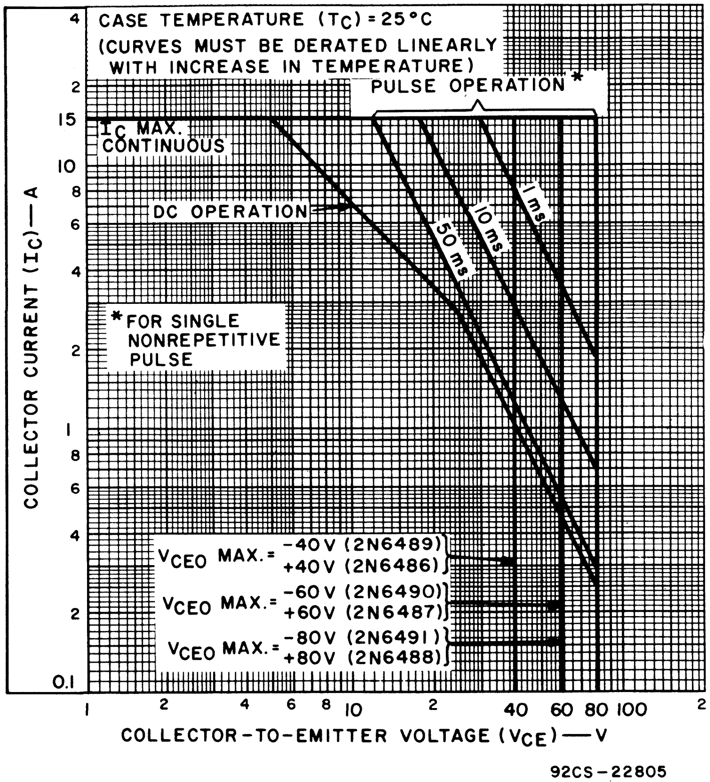


Fig.1 — Maximum operating areas for all types♦.

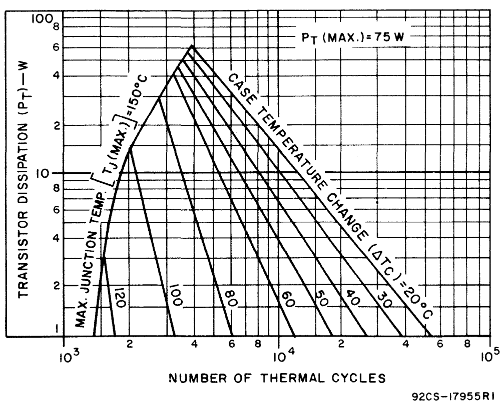


Fig.2 — Thermal-cycling rating chart for all types.

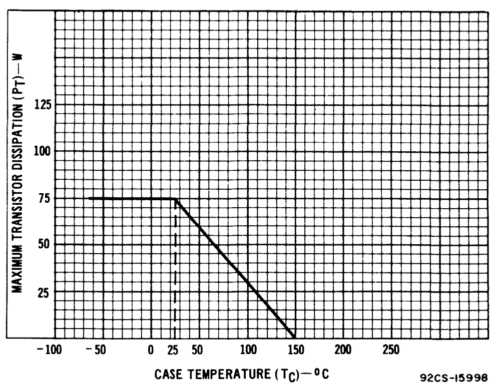


Fig.3 — Current derating for all types.

♦ For p-n-p devices, voltage and current values are negative.

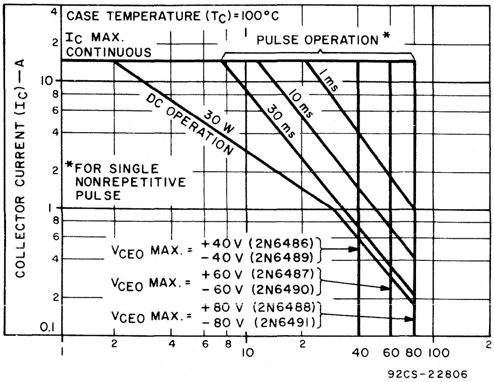


Fig.4 — Maximum operating areas for all types◆.

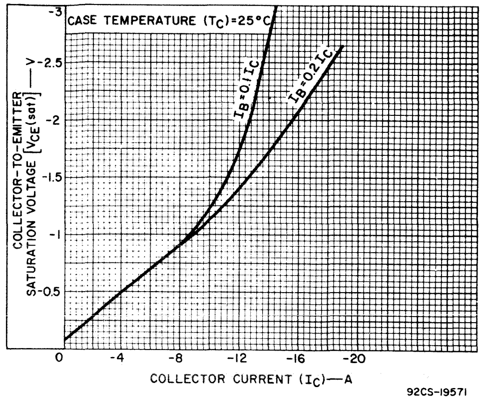


Fig.5 — Typical collector-to-emitter saturation-voltage characteristics for all types.

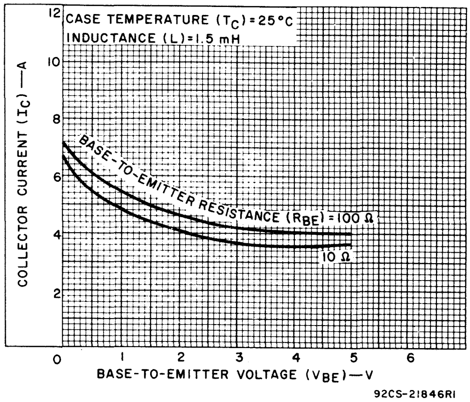


Fig.6 — Minimum reverse-bias second-breakdown characteristics for all types◆.

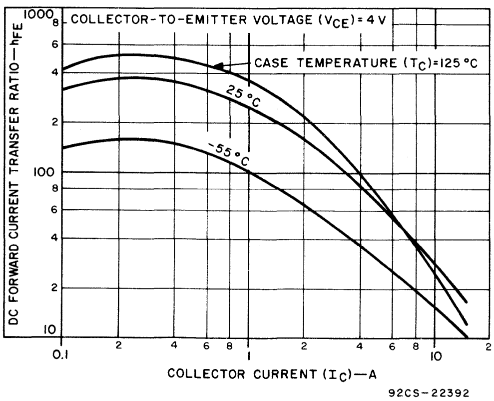


Fig.7 — Typical dc beta characteristics for all types◆.

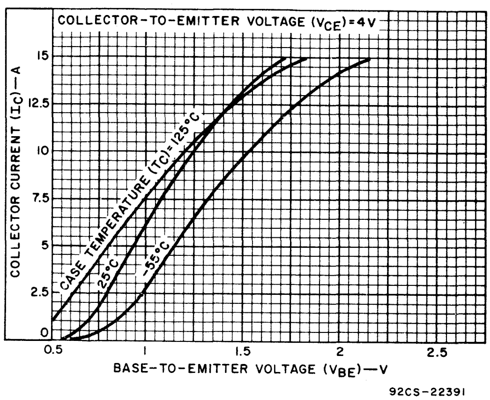


Fig.8 — Typical transfer characteristics for all types◆.

◆ For p-n-p devices, voltage and current values are negative.

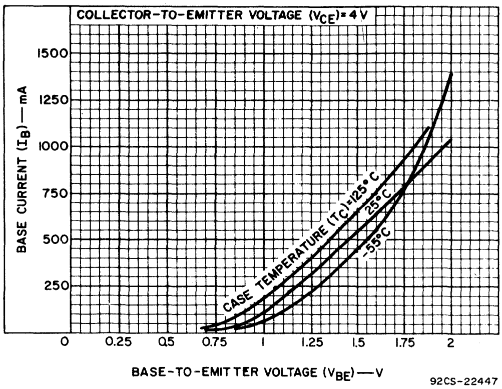


Fig.9 — Typical input characteristics for all types♦

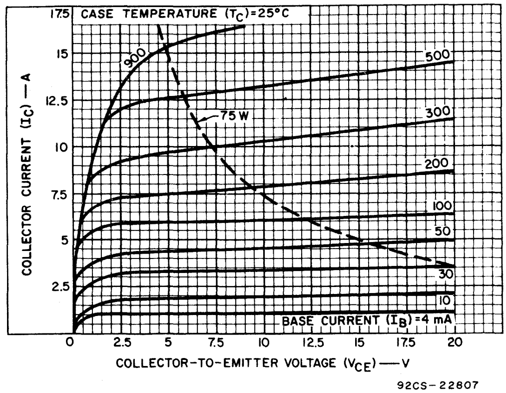


Fig.10 — Typical output characteristics for all types♦.

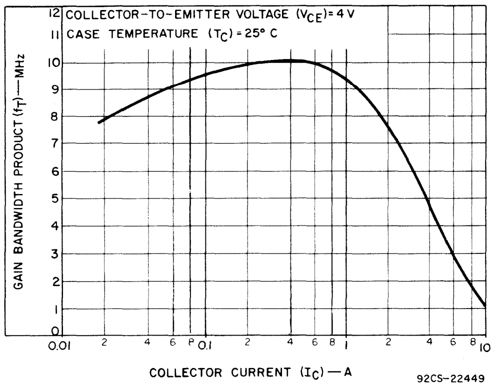


Fig.11 — Typical gain-bandwidth product vs. collector current for all types♦.

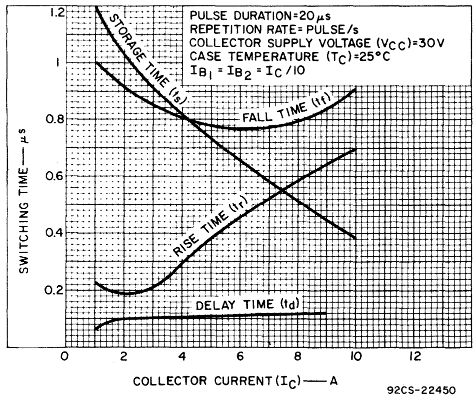


Fig.12 — Typical saturated switching characteristics for all types♦.

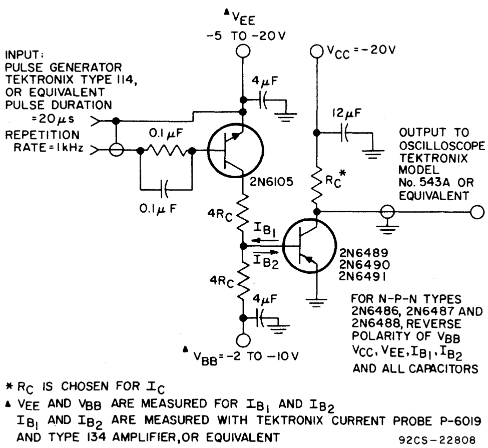


Fig.13 — Circuit used to measure saturated switching times.

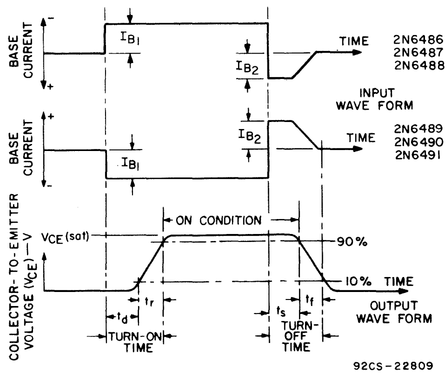
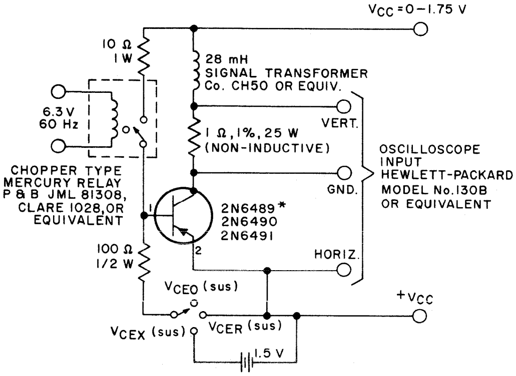


Fig.14 — Oscilloscope display for measurement of switching times.

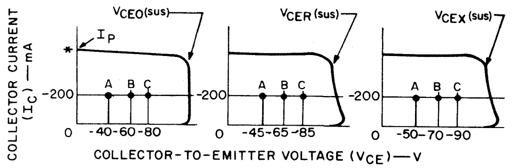
♦ For p-n-p devices, voltage and current values are negative.



*FOR N-P-N TYPES 2N6486, 2N6487, AND 2N6488, REVERSE POLARITY OF BATTERY AND V_{CC}.

92CS-22810

Fig. 15 – Circuit used to measure sustaining voltages V_{CEO}(sus), V_{CER}(sus), and V_{CEX}(sus) for all types.

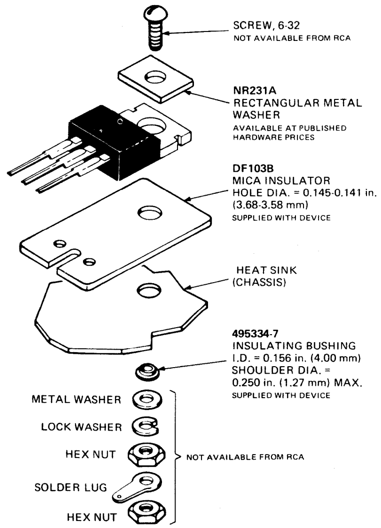


*PULSE CURRENT (I_P) RANGE = 0.6–0.8 A

THE SUSTAINING VOLTAGES V_{CEO}(sus), V_{CER}(sus), AND V_{CEX}(sus) ARE ACCEPTABLE WHEN THE TRACES FALL TO THE RIGHT AND ABOVE POINT "A" FOR TYPES 2N6486 AND 2N6489; POINT "B" FOR 2N6487 AND 2N6490; AND POINT "C" FOR 2N6488 AND 2N6491.

92CS-22811

Fig. 16 – Oscilloscope display for measurement of sustaining voltages (test circuit shown in Fig. 15).

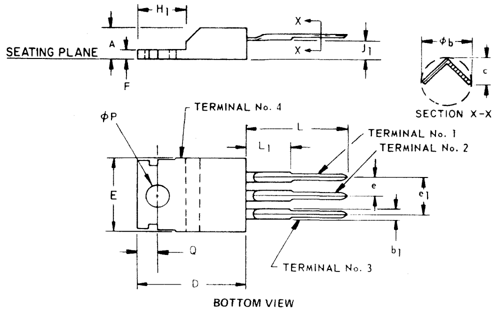


92CS-22563

In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 17 – Suggested mounting hardware for JEDEC TO-220AB.

DIMENSIONAL OUTLINE JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 (6.35 – 6.48 mm) from case.

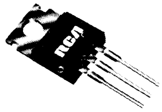
TERMINAL CONNECTIONS JEDEC TO-220AB

Terminal No.1 – Base
Terminal No.2 – Collector
Terminal No.3 – Emitter
Terminal No.4 – Collector

Solid State
Division

Power Transistors

RCA29 RCA29B
RCA29A RCA29C



JEDEC TO-220 AB H-1535

Epitaxial-Base, Silicon N-P-N VERSAWATT Transistors

For Power-Amplifier and
High-Speed-Switching Applications

Features:

- **30 W at 25°C case temperature**
- **3 A rated collector current**
- **Min. f_T of 3 MHz at 10 V, 200 mA**
- **Designed for complementary use with RCA30, RCA30A, RCA30B, and RCA30C p-n-p types**

RCA29, RCA29A, RCA29B, and RCA29C are epitaxial-base, silicon n-p-n transistors. They are intended for a wide variety of switching and amplifier applications, such as series and shunt regulators and driver and output stages of high-fidelity amplifiers. These new plastic power transistors are designed for complementary use with devices in the RCA30 series. They differ from each other in voltage ratings and in the currents at which the parameters are controlled.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		RCA29	RCA29A	RCA29B	RCA29C	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	40	60	80	100	V
COLLECTOR-TO-EMITTER VOLTAGE:						
With base open	V_{CEO}	40	60	80	100	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	5	5	5	V
*CONTINUOUS COLLECTOR CURRENT	I_C	3	3	3	3	A
*CONTINUOUS BASE CURRENT	I_B	1	1	1	1	A
TRANSISTOR DISSIPATION:	P_T					
At case temperatures up to 25°C		30	30	30	30	W
At ambient temperatures up to 25°C		2	2	2	2	W
TEMPERATURE RANGE:						
Storage & Operating (Junction)		← -65 to 150 →				°C
*LEAD TEMPERATURE (During Soldering):						
At distance 1/8 in. (3.17 mm) from case for 10 s max.		← 235 →				°C

*Differs from TIP series

11-73

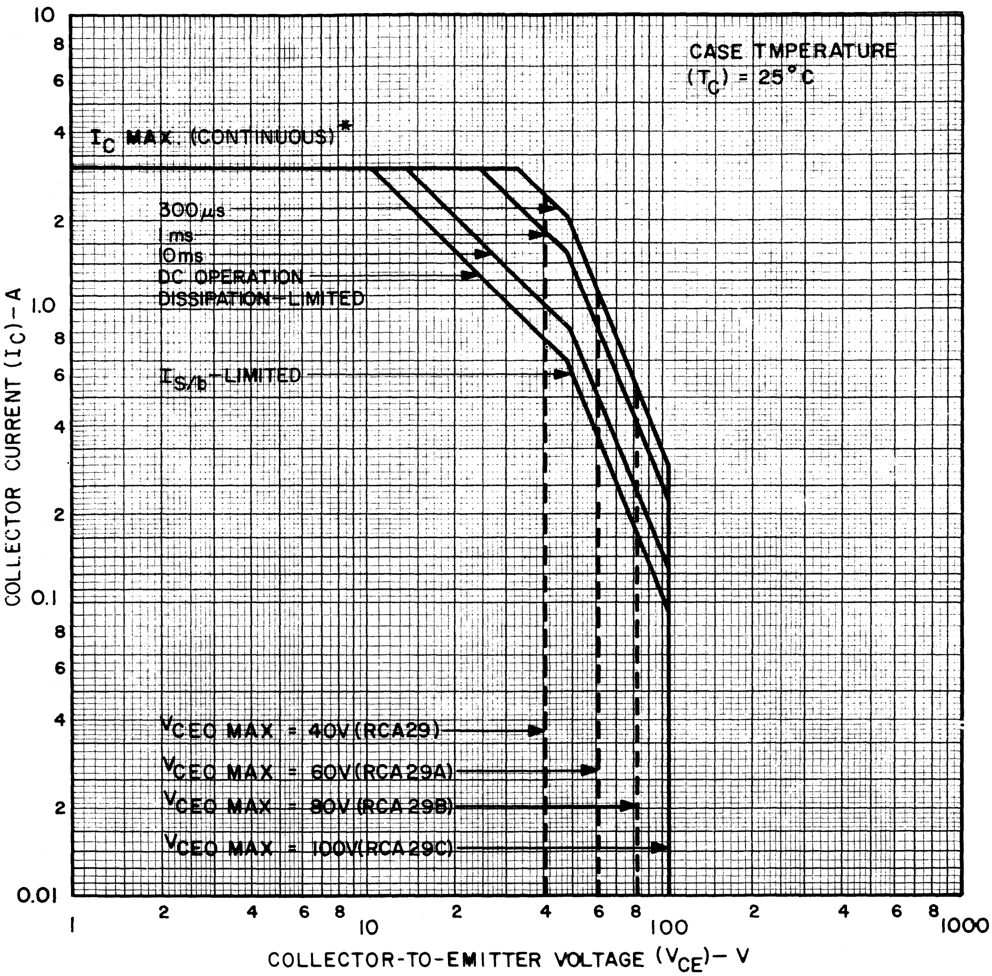
ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS								UNITS
		DC VOLTAGE (V)			DC CURRENT (A)		RCA29		RCA29A		RCA29B		RCA29C		
		V_{CE}	V_{EB}	V_{BE}	I_C	I_B	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Collector-Cutoff Current: With base open	I_{CEO}	30 60				0 0	– –	0.3 –	– –	0.3 –	– –	– 0.3	– –	– 0.3	mA
With base-emitter junction short-circuited	I_{CES}	40 60 80 100		0 0 0 0			– – – –	0.2 – – –	– – – –	– 0.2 – –	– – – –	– – 0.2 –	– – – –	– – – 0.2	
Emitter-Cutoff Current	I_{EBO}		5		0		–	1	–	1	–	1	–	1	mA
Collector-to-Emitter Breakdown Voltage: With base open	$V_{BR(CEO)}$				0.03[a]	0	40	–	60	–	80	–	100	–	V
DC Forward-Current Transfer Ratio	h_{FE}	4 4			0.2[a] 1[a]		40 15	– 75	40 15	– 75	40 15	– 75	40 15	– 75	
Base-to-Emitter Voltage	V_{BE}	4			1[a]		–	1.3	–	1.3	–	1.3	–	1.3	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				1[a]	0.125	–	0.7	–	0.7	–	0.7	–	0.7	V
Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 1 kHz)	h_{fe}	10			0.2		20	–	20	–	20	–	20	–	
Magnitude of Common Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	10			0.2		3	–	3	–	3	–	3	–	
Saturated Switching Time: (R_L = 30 Ω) See Figs. 2 & 3 Turn-on time $t_d + t_r$	t_{ON}	(V_{CC}) 30			1	0.1[c]	0.5 (typ.)		0.5 (typ.)		(0.5 (typ.)		0.5 (typ.)		µs
Turn-off time $t_s + t_f$	t_{OFF}	(V_{CC}) 30			1	0.1[c]	2 (typ.)		2 (typ.)		2 (typ.)		2 (typ.)		
Unclamped Inductive Load Energy[b] (L = 20 mH) See Fig. 4		(V_{CC}) 10					–	32	–	32	–	32	–	32	mJ
Thermal Resistance Junction-to-Case	$R_{\theta JC}$						–	4.17	–	4.17	–	4.17	–	4.17	°C/W
Junction-to-Ambient	$R_{\theta JA}$						–	62.5	–	62.5	–	62.5	–	62.5	

[a]Pulsed: Pulse duration = 300 µs, duty factor = 2%

[b]Based upon ability of device to perform in circuit shown in Fig. 4.

[c]I_{B_1} = I_{B_2} = value shown.



* DIFFERS FROM TIP SERIES

Fig. 1—Maximum safe operating areas for all types

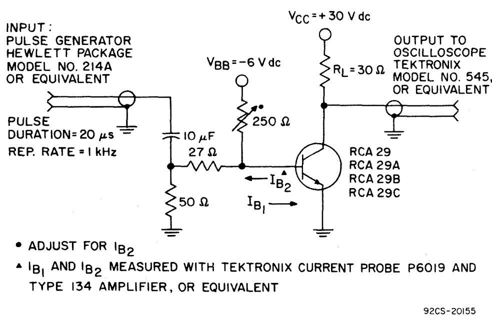


Fig. 2—Circuit used to measure switching times for all types

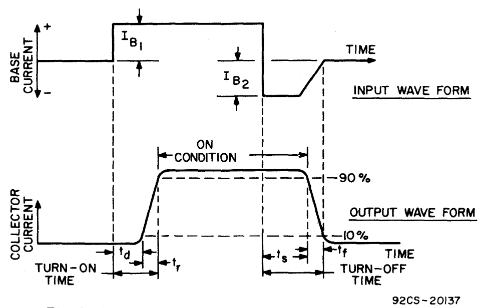


Fig. 3—Phase relationship between input current and output voltage showing reference points for specification of switching times (test circuit shown in Fig. 2)

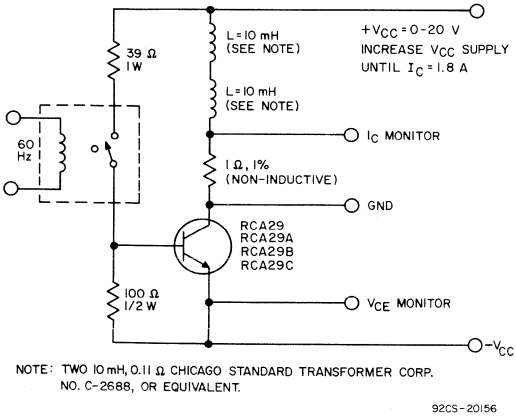


Fig. 4—Circuit for measuring inductive-load switching for all types

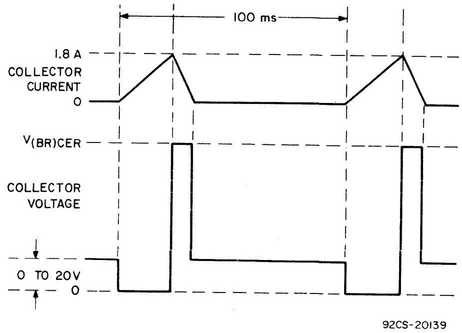


Fig. 5—Inductive-load switching voltage and current waveforms (test circuit shown in Fig. 4)

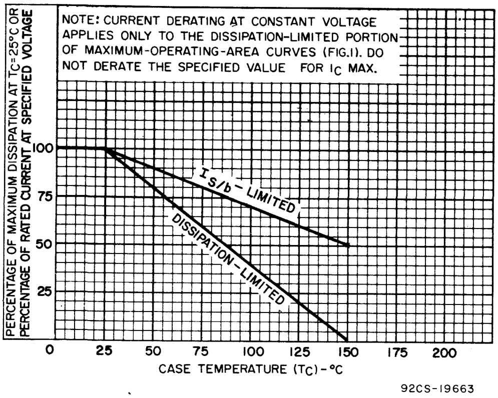


Fig. 6—Derating curves for all types

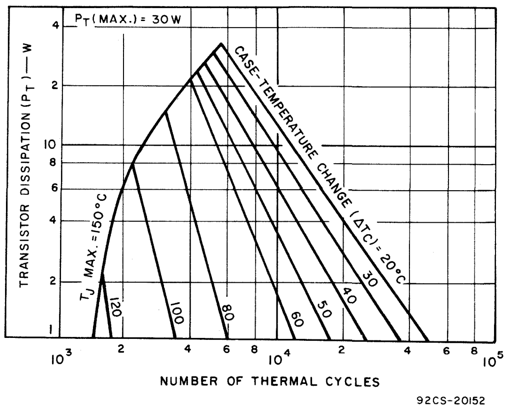


*Fig. 7—Thermal-cycling ratings for all types**

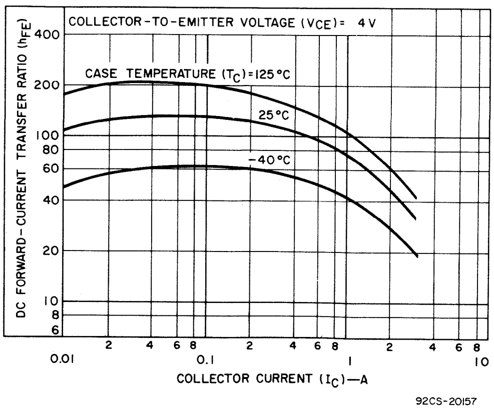
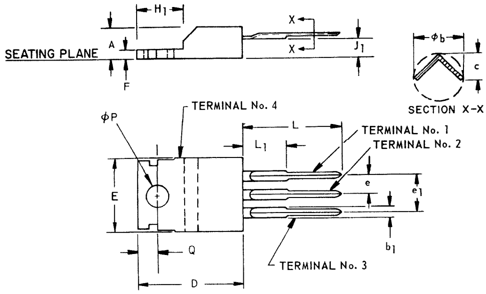


*Fig. 8—Typical dc beta characteristics for all types**

*Differs from TIP series

DIMENSIONAL OUTLINE

JEDEC TO-220AB



BOTTOM VIEW

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
ϕb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
ϕP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

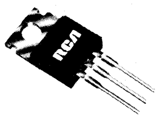
TERMINAL CONNECTIONS

Lead No. 1 – Base
Lead No. 2 – Collector
Lead No. 3 – Emitter
Mounting Flange, Lead No. 4 – Collector

Solid State
Division

Power Transistors

RCA30 RCA30B
RCA30A RCA30C



JEDEC TO-220 AB H-1535

Epitaxial-Base, Silicon P-N-P VERSAWATT Transistors

For Power-Amplifier and
High-Speed-Switching Applications

Features:

- **30 W at 25°C case temperature**
- **3 A rated collector current**
- **Min. f_T of 3 MHz at 10 V, 200 mA**
- **Designed for complementary use with RCA29, RCA29A, RCA29B, and RCA29C n-p-n types**

RCA30, RCA30A, RCA30B, and RCA30C are epitaxial-base, silicon p-n-p transistors. They are intended for a wide variety of switching and amplifier applications, such as series and shunt regulators and driver and output stages of high-fidelity amplifiers.

These new plastic power transistors are designed for complementary use with devices in the RCA29 series. They differ from each other in voltage ratings and in the currents at which the parameters are controlled.

MAXIMUM RATINGS, *Absolute-Maximum Values:*		RCA30	RCA30A	RCA30B	RCA30C	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	-40	-60	-80	-100	V
COLLECTOR-TO-EMITTER VOLTAGE:						
With base open	V_{CEO}	-40	-60	-80	-100	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	-5	-5	-5	-5	V
*CONTINUOUS COLLECTOR CURRENT	I_C	-3	-3	-3	-3	A
*CONTINUOUS BASE CURRENT	I_B	-1	-1	-1	-1	A
TRANSISTOR DISSIPATION:	P_T					
At case temperatures up to 25°C		30	30	30	30	W
At ambient temperatures up to 25°C		2	2	2	2	W
TEMPERATURE RANGE:						
Storage and Operating (Junction)		← -65 to 150 →				°C
*LEAD TEMPERATURE (During Soldering):						
At distance 1/8 in. (3.17 mm) from case for 10 s max.		← 235 →				°C

*Differs from TIP series

11-73

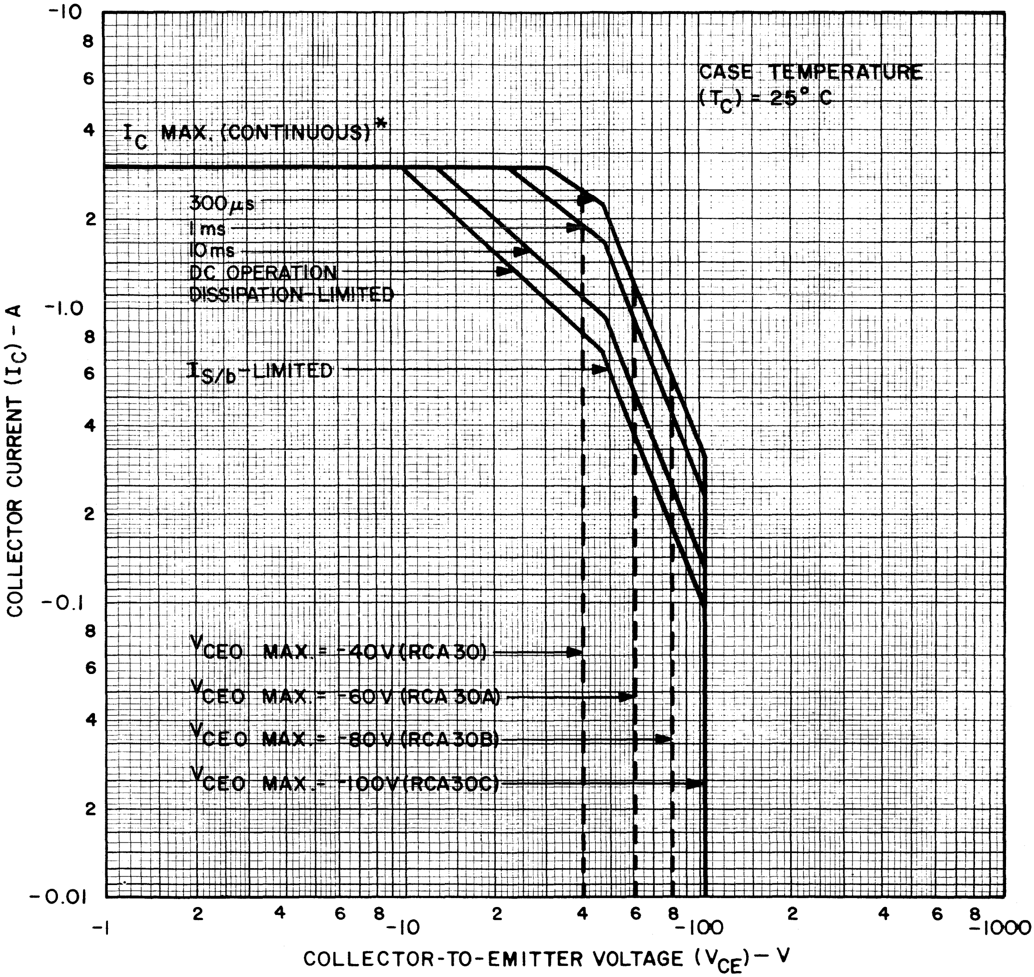
ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS								UNITS
		DC VOLTAGE (V)			DC CURRENT (A)		RCA30		RCA30A		RCA30B		RCA30C		
		V_{CE}	V_{EB}	V_{BE}	I_C	I_B	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Collector-Cutoff Current: With base open	I_{CEO}	-30				0	—	-0.3	—	-0.3	—	—	—	—	mA
		-60				0	—	—	—	—	—	-0.3	—	-0.3	mA
With base emitter junction short-circuited	I_{CES}	-40		0			—	-0.2	—	—	—	—	—	—	mA
		-60		0			—	—	—	-0.2	—	—	—	—	mA
		-80		0			—	—	—	—	—	-0.2	—	—	mA
		-100		0			—	—	—	—	—	—	—	-0.2	mA
Emitter-Cutoff Current	I_{EBO}		-5		0		—	-1	—	-1	—	-1	—	-1	mA
Collector-to-Emitter Breakdown Voltage: With base open	$V_{BR(CEO)}$				-0.03[a]	0	-40	—	-60	—	-80	—	-100	—	V
DC Forward-Current Transfer Ratio	h_{FE}	-4			-0.2[a]		40	—	40	—	40	—	40	—	
		-4			-1[a]		15	75	15	75	15	75	15	75	
Base-to-Emitter Voltage	V_{BE}	-4			-1[a]		—	-1.3	—	-1.3	—	-1.3	—	-1.3	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				-1[a]	-0.125	—	-0.7	—	-0.7	—	-0.7	—	-0.7	V
Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 1 kHz)	h_{fe}	-10			-0.2		20	—	20	—	20	—	20	—	
Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Radio (f = 1 MHz)	$\lvert h_{fe} \rvert$	-10			-0.2		3	—	3	—	3	—	3	—	
Saturated Switching Time: (R_L = 30 Ω) See Figs. 2 & 3 — Turn-on time $t_d + t_r$	t_{ON}	(V_{CC}) -30			-1	-0.1[c]	0.3 (typ.)		0.3 (typ.)		0.3 (typ.)		0.3 (typ.)		μs
Turn-off time $t_s + t_f$	t_{OFF}	(V_{CC}) -30			-1	-0.1[c]	1 (typ.)		1 (typ.)		1 (typ.)		1 (typ.)		μs
Unclamped Inductive Load Energy[b] (L = 20 mH) See Fig. 4		(V_{CC}) -10					—	32	—	32	—	32	—	32	mJ
Thermal Resistance Junction-to-Case	$R_{\theta JC}$						—	4.17	—	4.17	—	4.17	—	4.17	°C/W
Junction-to-Ambient	$R_{\theta JA}$						—	62.5	—	62.5	—	62.5	—	62.5	°C/W

[a]Pulsed: Pulse duration = 300 μs, duty factor = 2%

[b]Based upon ability of device to perform in circuit shown in Fig. 4.

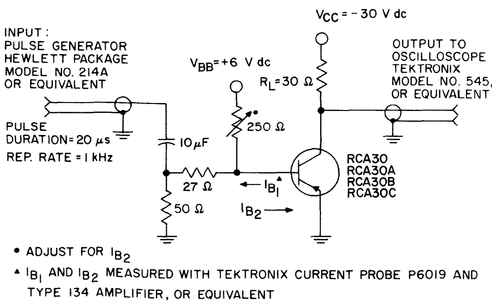
[c]$I_{B_1} = I_{B_2}$ = value shown.



*DIFFERS FROM TIP SERIES

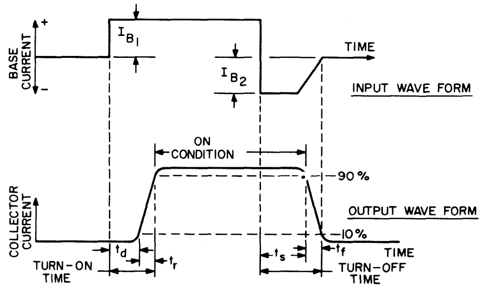
92CS-20149

Fig. 1—Maximum safe operating areas for all types.



92CS-20150

Fig. 2—Circuit used to measure switching times for all types.



92CS-20137

Fig. 3—Phase relationship between input current and output voltage showing reference points for specification of switching times (test circuit shown in Fig. 2).

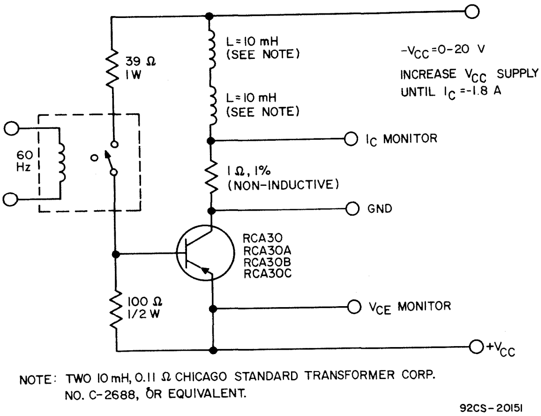


Fig. 4—Circuit for measuring inductive-load switching for all types.

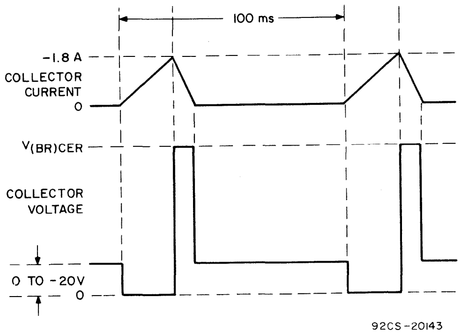


Fig. 5—Inductive-load switching voltage and current waveforms (test circuit shown in Fig. 4).

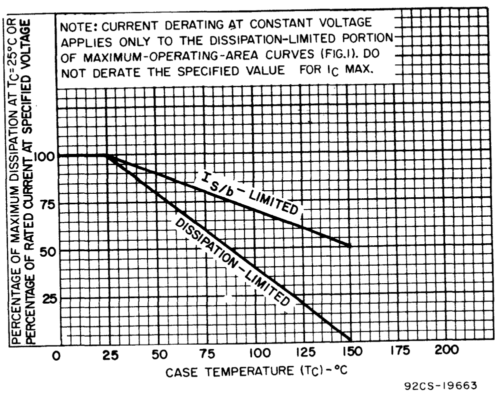


Fig. 6—Derating curves for all types.

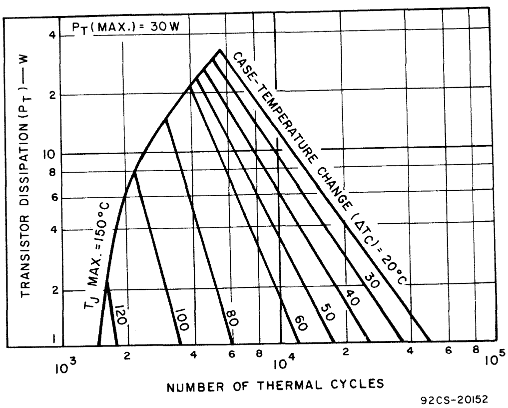


Fig. 7—Thermal cycling ratings for all types.*

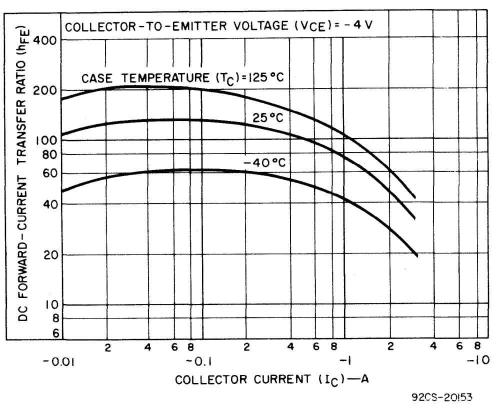
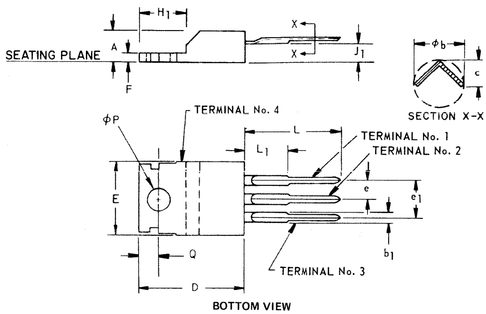


Fig. 8—Typical dc beta characteristics for all types.*

*Differs from TIP series

DIMENSIONAL OUTLINE

JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS

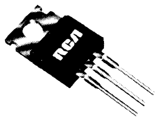
Lead No. 1 – Base
Lead No. 2 – Collector
Lead No. 3 – Emitter
Mounting Flange, Lead No. 4 – Collector

Solid State Division

Power Transistors

RCA31 RCA31B RCA31A RCA31C

Epitaxial-Base, Silicon N-P-N VERSAWATT Transistors



JEDEC TO-220 AB H-1535

For Power-Amplifier and High-Speed-Switching Applications

Features:

- **40 W at 25°C case temperature**
- **5 A rated collector current**
- **Min. f_T of 3 MHz at 10 V, 500 mA**
- **Designed for complementary use with RCA32, RCA32A, RCA32B, and RCA32C p-n-p types**

RCA31, RCA31A, RCA31B, and RCA31C are epitaxial-base, silicon n-p-n transistors. They are intended for a wide variety of switching and amplifier applications, such as series and shunt regulators and driver and output stages of high-fidelity amplifiers. These new plastic power transistors are designed for complementary use with devices in the RCA32 series. They differ from each other in voltage ratings and in the currents at which the parameters are controlled.

MAXIMUM RATINGS, *Absolute-Maximum Values:*		RCA31	RCA31A	RCA31B	RCA31C	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	40	60	80	100	V
COLLECTOR-TO-EMITTER VOLTAGE:						
With base open	V_{CEO}	40	60	80	100	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	5	5	5	V
*CONTINUOUS COLLECTOR CURRENT	I_C	5	5	5	5	A
*CONTINUOUS BASE CURRENT	I_B	1	1	1	1	A
TRANSISTOR DISSIPATION:	P_T					
At case temperatures up to 25°C		40	40	40	40	W
At ambient temperatures up to 25°C		2	2	2	2	W
TEMPERATURE RANGE:						
Storage and Operating (Junction)		← -65 to 150 →				°C
*LEAD TEMPERATURE (During Soldering):						
At distance 1/8 in. (3.17 mm) from case for 10 s max.		← 235 →				°C

*Differs from TIP series

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS								UNITS
		DC VOLTAGE (V)			DC CURRENT (A)		RCA31		RCA31A		RCA31B		RCA31C		
		V_{CE}	V_{EB}	V_{BE}	I_C	I_B	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Collector-Cutoff Current: With base open	I_{CEO}	30				0	–	0.3	–	0.3	–	–	–	–	mA
		60				0	–	–	–	–	–	0.3	–	0.3	
With base-emitter junction short-circuited	I_{CES}	40		0			–	0.2	–	–	–	–	–	–	
		60		0			–	–	–	0.2	–	–	–	–	
		80		0			–	–	–	–	–	0.2	–	–	
		100		0			–	–	–	–	–	–	–	0.2	
Emitter-Cutoff Current	I_{EBO}		5		0		–	1	–	1	–	1	–	1	mA
Collector-to-Emitter Breakdown Voltage: With base open	$V_{BR(CEO)}$				0.03^a	0	40	–	60	–	80	–	100	–	V
DC Forward-Current Transfer Ratio	h_{FE}	4			1^a		25	–	25	–	25	–	25	–	
		4			3^a		10	50	10	50	10	50	10	50	
Base-to-Emitter Voltage	V_{BE}	4			3^a		–	1.8	–	1.8	–	1.8	–	1.8	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				3^a	0.375	–	1.2	–	1.2	–	1.2	–	1.2	V
Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 1 kHz)	h_{fe}	10			0.5		20	–	20	–	20	–	20	–	
Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	10			0.5		3	–	3	–	3	–	3	–	
Saturated Switching Time: (R_L = 30 Ω) See Figs. 2 & 3															
Turn-on-time $t_d + t_r$	t_{ON}	(V_{CC}) 30			1	0.1^c	0.5 (typ.)		0.5 (typ.)		0.5 (typ.)		0.5 (typ.)		μs
Turn-off time $t_s + t_f$	t_{OFF}	(V_{CC}) 30			1	0.1^c	2 (typ.)		2 (typ.)		2 (typ.)		2 (typ.)		
Unclamped Inductive Load Energy[b] (L = 20 mH) See Fig. 4		(V_{CC}) 10					–	32	–	32	–	32	–	32	mJ
Thermal Resistance Junction-to-Case	$R_{\theta JC}$						–	3.125	–	3.125	–	3.125	–	3.125	°C/W
Junction-to-Ambient	$R_{\theta JA}$						–	62.5	–	62.5	–	62.5	–	62.5	

[a]Pulsed: Pulse duration = 300 μs, duty factor = 2%
[b]Based upon ability of device to perform in circuit shown in Fig. 4.
[c]$I_{B_1} = I_{B_2}$ = value shown

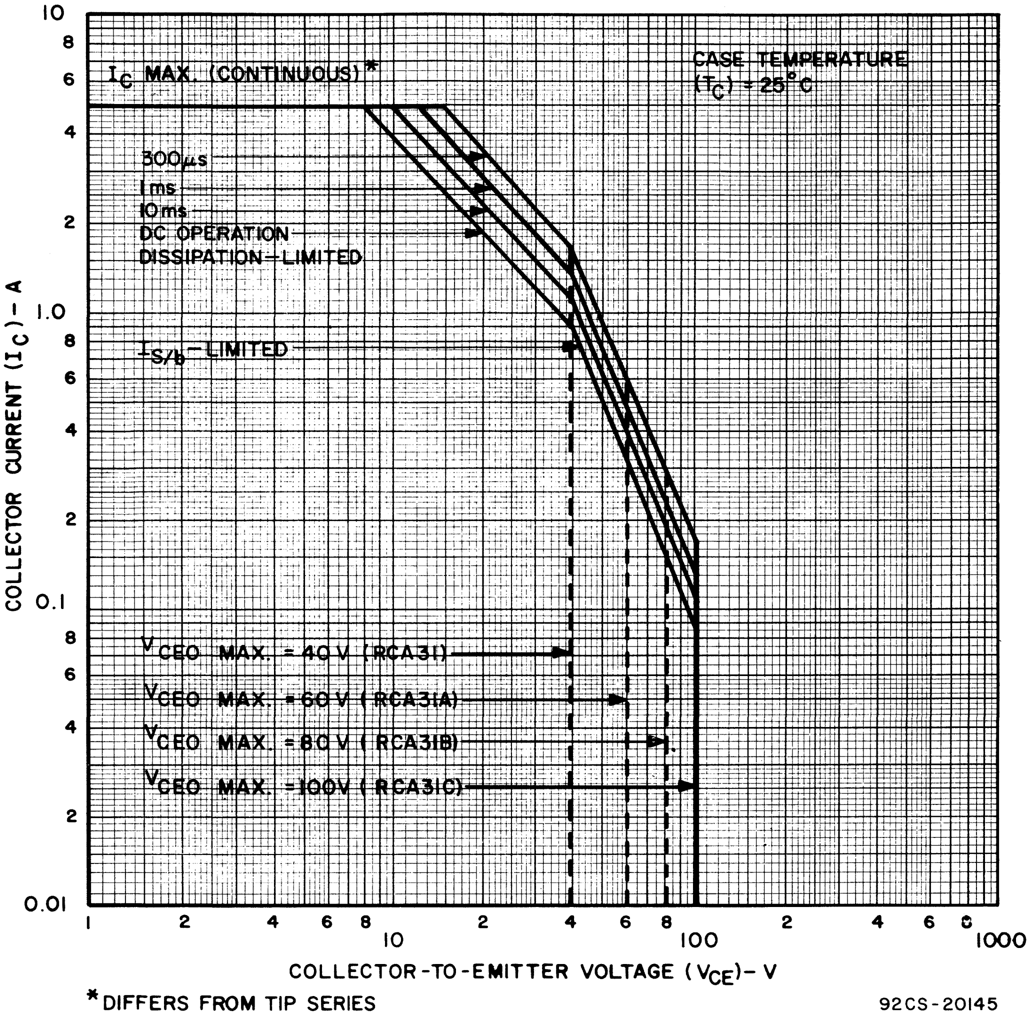


Fig. 1—Maximum safe operating areas for all types.

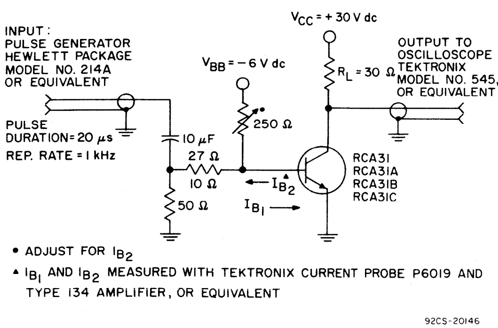


Fig. 2—Circuit used to measure switching times for all types.

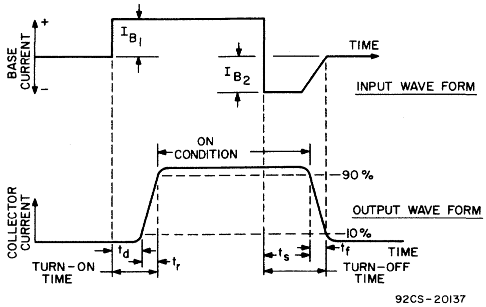


Fig. 3—Phase relationship between input current and output voltage showing reference points for specification of switching times (test circuit shown in Fig. 2).

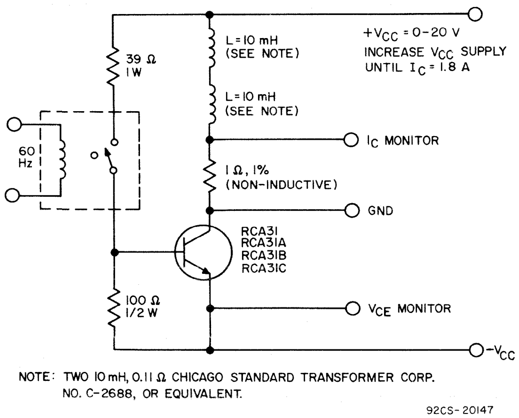


Fig. 4—Circuit for measuring inductive-load switching for all types.

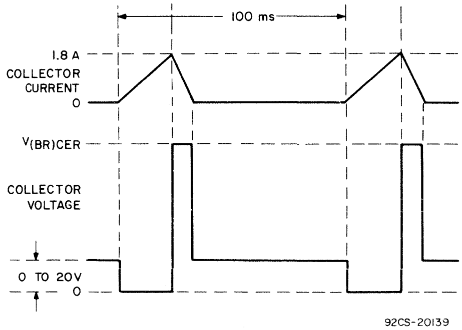


Fig. 5—Inductive-load switching voltage and current waveforms (test circuit shown in Fig. 4).

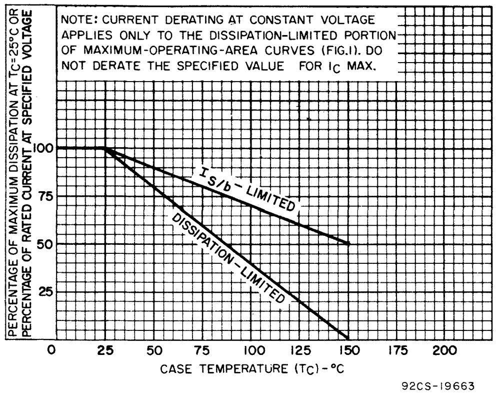


Fig. 6—Derating curves for all types.

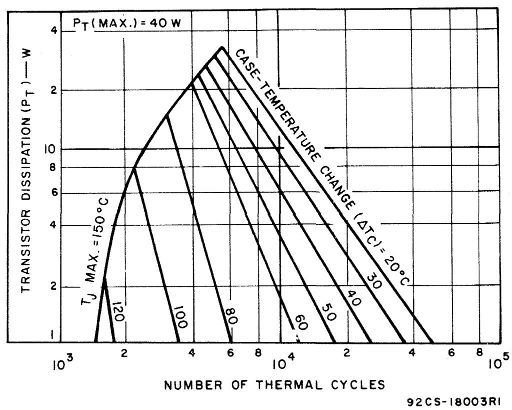


Fig. 7—Thermal-cycling ratings for all types.*

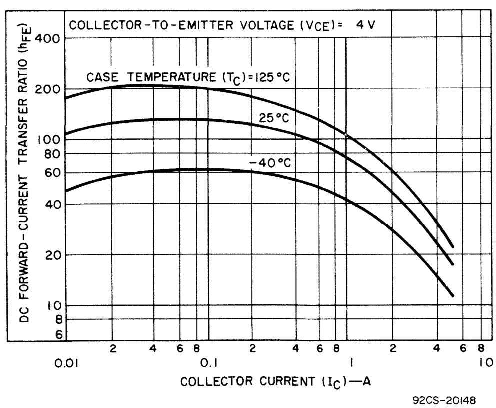
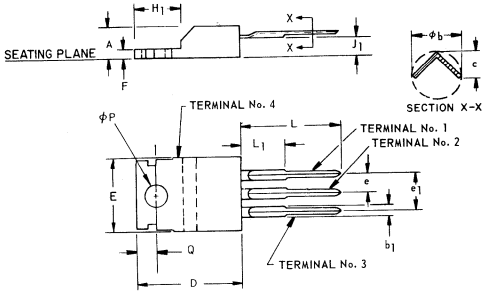


Fig. 8—Typical dc beta characteristics for all types.*

*Differs from TIP series

DIMENSIONAL OUTLINE

JEDEC TO-220AB



BOTTOM VIEW

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

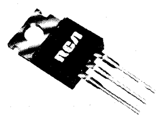
TERMINAL CONNECTIONS

Lead No. 1 – Base
Lead No. 2 – Collector
Lead No. 3 – Emitter
Mounting Flange, Lead No. 4 – Collector

Solid State
Division

Power Transistors

RCA32 RCA32B
RCA32A RCA32C



JEDEC TO-220 AB H-1535

Epitaxial-Base, Silicon P-N-P VERSAWATT Transistors

For Power-Amplifier and
High-Speed-Switching Applications

Features:

- **40 W at 25°C case temperature**
- **5 A rated collector current**
- **Min. f_T of 3 MHz at 10 V, 500 mA**
- **Designed for complementary use with RCA31, RCA31A, RCA31B, and RCA31C n-p-n types**

RCA32, RCA32A, RCA32B, and RCA32C are epitaxial-base, silicon p-n-p transistors. They are intended for a wide variety of switching and amplifier applications, such as series and shunt regulators and driver and output stages of high-fidelity amplifiers. These new plastic power transistors are designed for complementary use with devices in the RCA31 series. They differ from each other in voltage ratings and in the currents at which the parameters are controlled.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		RCA32	RCA32A	RCA32B	RCA32C	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	-40	-60	-80	-100	V
COLLECTOR-TO-EMITTER VOLTAGE:						
With base open	V_{CEO}	-40	-60	-80	-100	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	-5	-5	-5	-5	V
*CONTINUOUS COLLECTOR CURRENT	I_C	-5	-5	-5	-5	A
*CONTINUOUS BASE CURRENT	I_B	-1	-1	-1	-1	A
TRANSISTOR DISSIPATION:	P_T					
At case temperatures up to 25°C		40	40	40	40	W
At ambient temperatures up to 25°C		2	2	2	2	W
TEMPERATURE RANGE:						
Storage & Operating (Junction)		←—-65 to 150—→				°C
*LEAD TEMPERATURE (During Soldering):						
At distance 1/8 in. (3.17 mm) from case for 10 s max.		←—235—→				°C

*Differs from TIP series

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ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS								UNITS
		DC VOLTAGE (V)			DC CURRENT (A)		RCA32		RCA32A		RCA32B		RCA32C		
		V_{CE}	V_{EB}	V_{BE}	I_C	I_B	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Collector-Cutoff Current: With base open	I_{CEO}	-30				0	–	-0.3	–	-0.3	–	–	–	–	mA
		-60				0	–	–	–	–	–	-0.3	–	-0.3	mA
With base-emitter junction short-circuited	I_{CES}	-40		0			–	-0.2	–	–	–	–	–	–	mA
		-60		0			–	–	–	-0.2	–	–	–	–	mA
		-80		0			–	–	–	–	–	-0.2	–	–	mA
		-100		0			–	–	–	–	–	–	–	-0.2	mA
Emitter-Cutoff Current	I_{EBO}		-5		0		–	-1	–	-1	–	-1	–	-1	mA
Collector to Emitter Breakdown Voltage With base open	$V_{BR(CEO)}$				-0.03[a]	0	-40	–	-60	–	-80	–	-100	–	V
DC Forward Current Transfer Ratio	h_{FE}	-4			-1[a]		25	–	25	–	25	–	25	–	
		-4			-3[a]		10	50	10	50	10	50	10	50	
Base-to-Emitter Voltage	V_{BE}	-4			-3[a]		–	-1.8	–	-1.8	–	-1.8	–	-1.8	V
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$				-3[a]	-0.375	–	-1.2	–	-1.2	–	-1.2	–	-1.2	V
Common-Emitter Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 1 kHz)	h_{fe}	-10			-0.5		20	–	20	–	20	–	20	–	
Magnitude of Common Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	-10			-0.5		3	–	3	–	3	–	3	–	
Saturated Switching Time: (R_L = 30Ω) See Figs. 2 & 3 Turn-on time $t_d + t_r$	t_{ON}	(V_{CC}) -30			-1	-0.1[c]	0.3 (typ.)		0.3 (typ.)		0.3 (typ.)		0.3 (typ.)		μs
Turn-off time $t_s + t_f$	t_{OFF}	(V_{CC}) -30			-1	-0.1[c]	1 (typ.)		1 (typ.)		1 (typ.)		1 (typ.)		μs
Unclamped Inductive Load Energy[b] (L = 20 mH) See Fig. 4		(V_{CC}) -10					–	32	–	32	–	32	–	32	mJ
Thermal Resistance Junction-to-Case	$R_{\theta JC}$						–	3.125	–	3.125	–	3.125	–	3.125	°C/W
Junction-to-Ambient	$R_{\theta JA}$						–	62.5	–	62.5	–	62.5	–	62.5	°C/W

[a]Pulsed Pulse duration = 300 μs, duty factor = 2%

[b]Based upon ability of device to perform in circuit shown in Fig. 4.

[c]$I_{B_1} = I_{B_2}$ = value shown

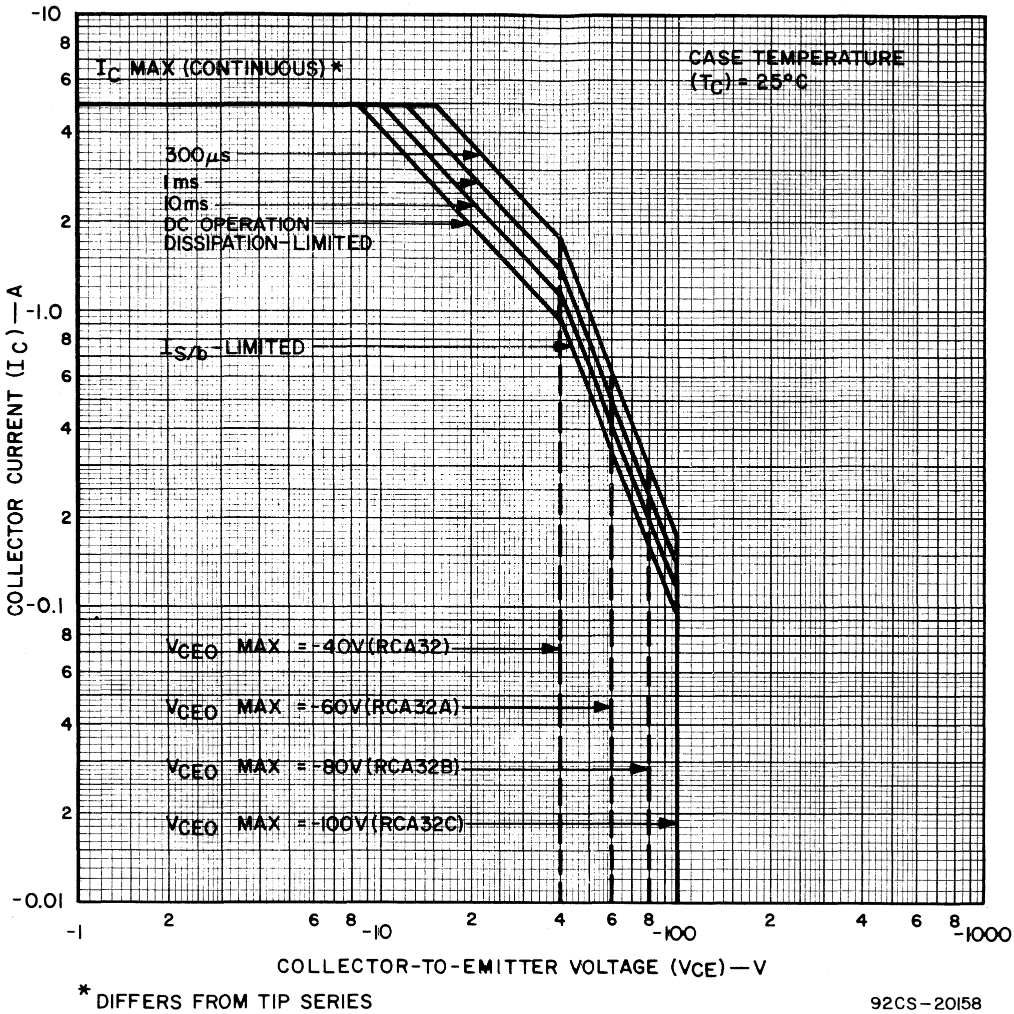


Fig. 1—Maximum safe operating areas for all types

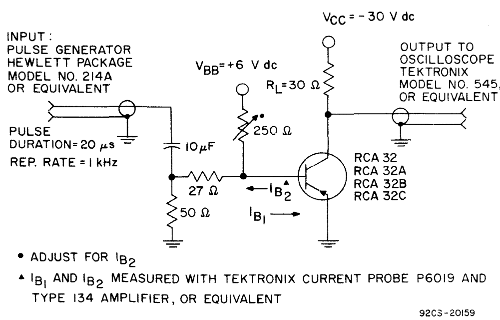


Fig. 2—Circuit used to measure switching times for all types

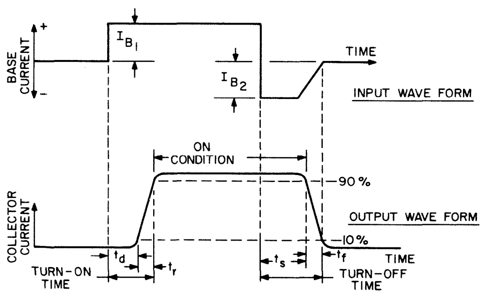


Fig. 3—Phase relationship between input current and output voltage showing reference points for specification of switching times (test circuit shown in Fig. 2)

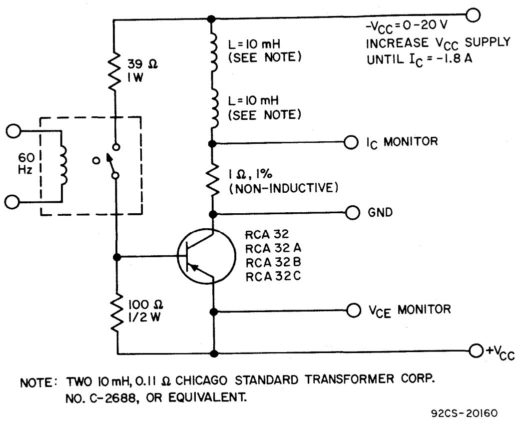


Fig. 4—Circuit for measuring inductive-load switching for all types

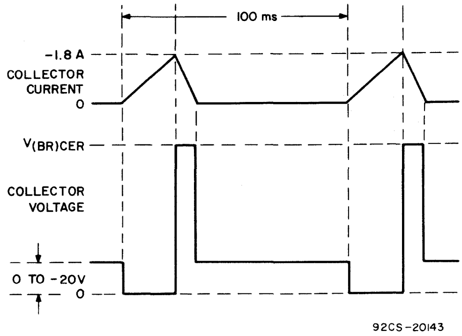


Fig. 5—Inductive-load switching voltage and current waveforms (test circuit shown in Fig. 4)

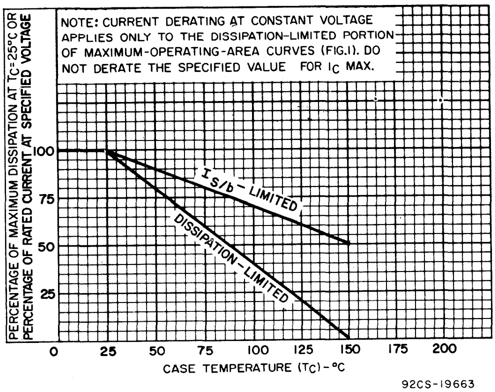


Fig. 6—Derating curves for all types

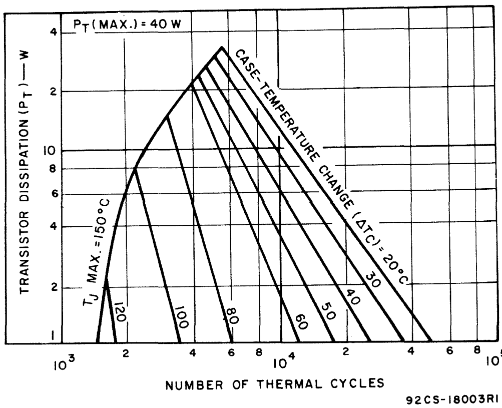


*Fig. 7—Thermal-cycling ratings for all types**

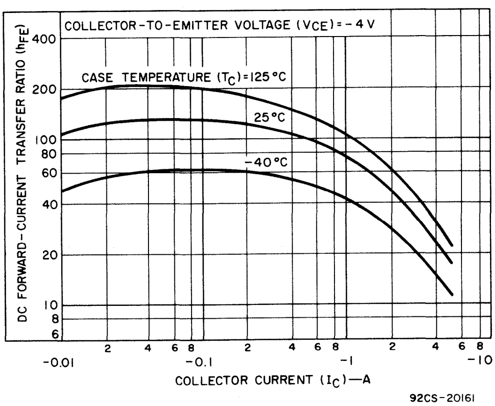
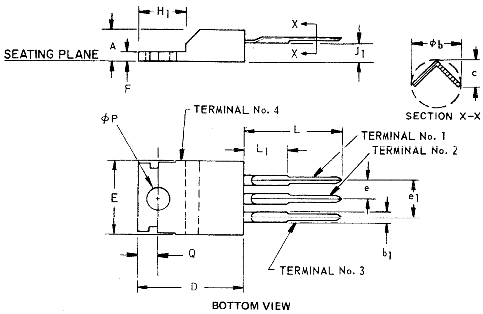


*Fig. 8—Typical dc beta characteristics for all types**

*Differs from TIP series

DIMENSIONAL OUTLINE

JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
ϕb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
ϕP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS

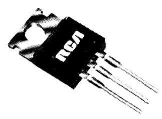
Lead No. 1 — Base
Lead No. 2 — Collector
Lead No. 3 — Emitter
Mounting Flange, Lead No. 4 — Collector

RCA

Solid State
Division

Power Transistors

RCA41 RCA41B
RCA41A RCA41C



JEDEC TO-220 AB H-1535

Epitaxial-Base, Silicon N-P-N VERSAWATT Transistors

For Power-Amplifier and
High-Speed-Switching Applications

Features:

- **65 W at 25°C case temperature**
- **7 A rated collector current**
- **Min. f_T of 3 MHz at 10 V, 500 mA**
- **Designed for complementary use with RCA42, RCA42A, RCA42B, and RCA42C p-n-p types**

RCA41, RCA41A, RCA41B, and RCA41C are epitaxial-base, silicon n-p-n transistors. They are intended for a wide variety of switching and amplifier applications, such as series and shunt regulators and driver and output stages of high-fidelity amplifiers. These new plastic power transistors are designed for complementary use with devices in the RCA42 series. They differ from each other in voltage ratings and in the currents at which the parameters are controlled.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		RCA41	RCA41A	RCA41B	RCA41C	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	40	60	80	100	V
COLLECTOR-TO-EMITTER VOLTAGE:						
With base open	V_{CEO}	40	60	80	100	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	5	5	5	V
*CONTINUOUS COLLECTOR CURRENT	I_C	7	7	7	7	A
*CONTINUOUS BASE CURRENT	I_B	3	3	3	3	A
TRANSISTOR DISSIPATION:	P_T					
At case temperatures up to 25°C		65	65	65	65	W
At ambient temperatures up to 25°C		2	2	2	2	W
TEMPERATURE RANGE:						
Storage & Operating (Junction)		←— -65 to 150 —→				°C
*LEAD TEMPERATURE (During Soldering):						
At distance 1/8 in. (3.17 mm) from case for 10 s max.		←— 235 —→				°C

*Differs from TIP series

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS								UNITS
		DC VOLTAGE (V)			DC CURRENT (A)		RCA41		RCA41A		RCA41B		RCA41C		
		V_{CE}	V_{EB}	V_{BE}	I_C	I_B	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Collector-Cutoff Current: With base open	I_{CEO}	30				0	–	0.7	–	0.7	–	–	–	–	mA
		60				0	–	–	–	–	–	0.7	–	0.7	mA
With base-emitter junction short-circuited	I_{CES}	40		0			–	0.4	–	–	–	–	–	–	mA
		60		0			–	–	–	0.4	–	–	–	–	mA
		80		0			–	–	–	–	–	0.4	–	–	mA
		100		0			–	–	–	–	–	–	–	0.4	mA
Emitter-Cutoff Current	I_{EBO}		5		0		–	1	–	1	–	1	–	1	mA
Collector-to-Emitter Breakdown Voltage: With base open	$V_{(BR)CEO}$				0.03[a]	0	40	–	60	–	80	–	100	–	V
DC Forward Current Transfer Ratio	h_{FE}	4			0.3[a]		30	–	30	–	30	–	30	–	
		4			3[a]		15	75	15	75	15	75	15	75	
* Base-to-Emitter Voltage	V_{BE}	4			6[a]		–	2.2	–	2.2	–	2.2	–	2.2	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				6[a]	0.6	–	2	–	2	–	2	–	2	V
Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 1 kHz)	h_{fe}	10			0.5		20	–	20	–	20	–	20	–	
Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	10			0.5		3	–	3	–	3	–	3	–	
Saturated Switching Time: (R_L = 5 Ω) See Figs. 2 & 3 Turn-on time $t_d + t_r$	t_{ON}	(V_{CC}) 30			6	0.6[c]	0.6 (typ.)		0.6 (typ.)		0.6 (typ.)		0.6 (typ.)		μs
* Turn-off Time $t_s + t_f$	t_{OFF}	(V_{CC}) 30			6	0.6[c]	1.2 (typ.)		1.2 (typ.)		1.2 (typ.)		1.2 (typ.)		μs
Unclamped Inductive Load Energy[b] (L = 20 mH) (See Fig. 4)		(V_{CC}) 10					–	62.5	–	62.5	–	62.5	–	62.5	mJ
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$						–	1.92	–	1.92	–	1.92	–	1.92	°C/W
Junction-to-Ambient	$R_{\theta JA}$						–	62.5	–	62.5	–	62.5	–	62.5	°C/W

[a]Pulsed: Pulse duration = 300 μs, duty factor = 2%

[b]Based upon ability of device to perform in circuit shown in Fig. 4.

[c]$I_{B_1} = I_{B_2}$ = value shown

*Differs from TIP series

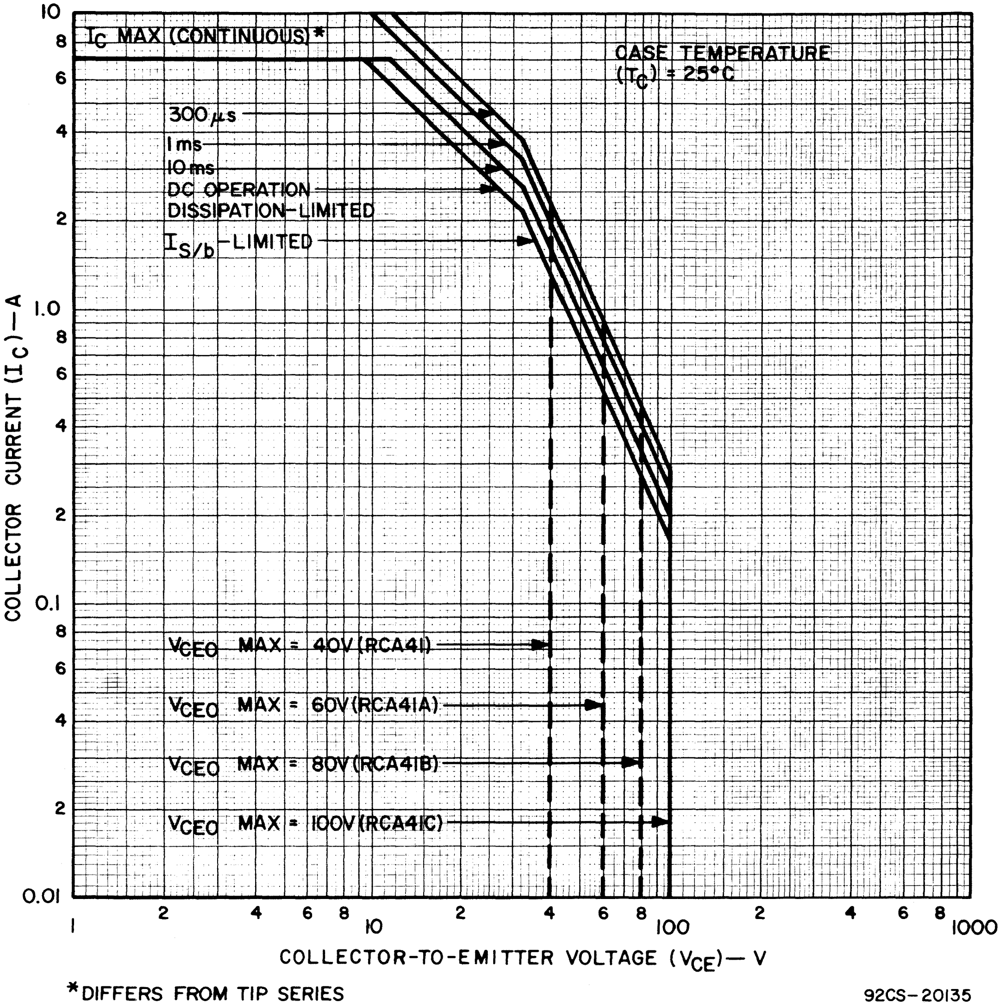


Fig. 1—Maximum safe operating areas for all types

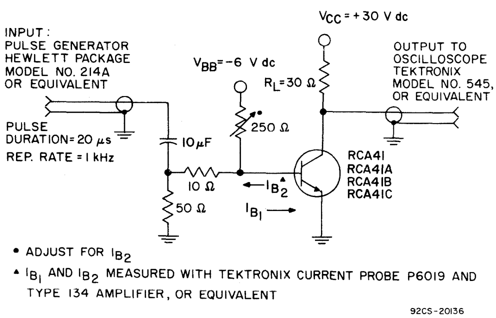


Fig. 2—Circuit used to measure switching times for all types

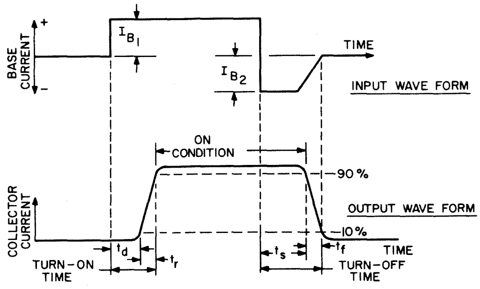


Fig. 3—Phase relationship between input current and output voltage showing reference points for specification of switching times (test circuit shown in Fig. 2)

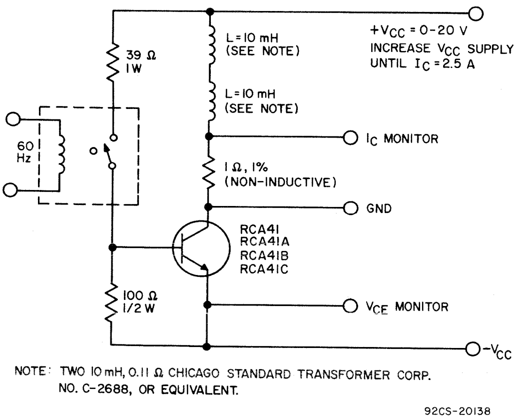


Fig. 4—Circuit for measuring inductive-load switching for all types

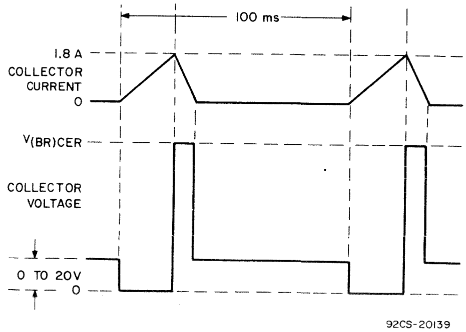


Fig. 5—Inductive-load switching voltage and current waveforms (test circuit shown in Fig. 4)

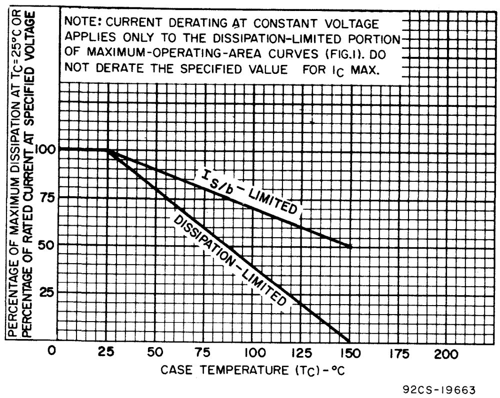


Fig. 6—Derating curves for all types

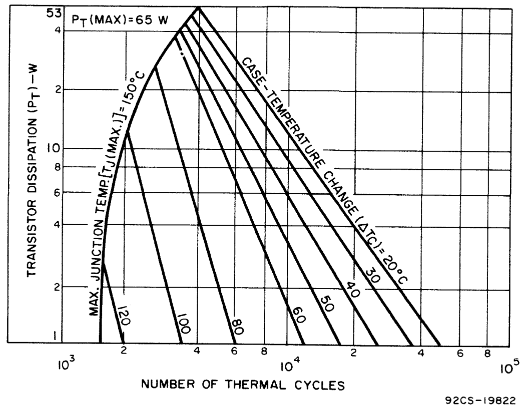


*Fig. 7—Thermal-cycling ratings for all types**

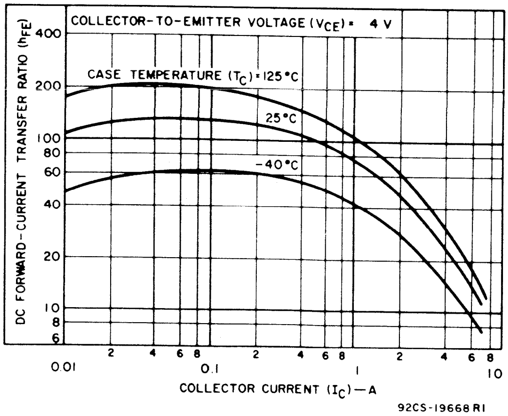
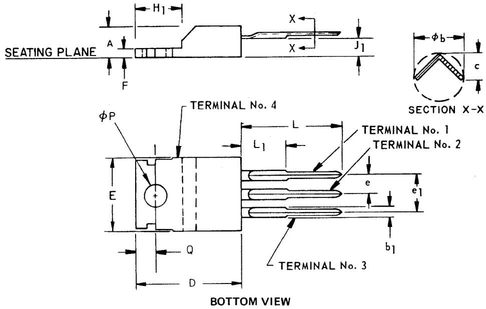


*Fig. 8—Typical dc beta characteristics for all types**

*Differs from TIP series

DIMENSIONAL OUTLINE

JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:
1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

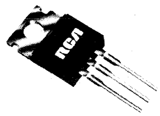
TERMINAL CONNECTIONS

Lead No. 1—Base
Lead No. 2—Collector
Lead No. 3—Emitter
Mounting Flange, Lead No. 4—Collector

Solid State
Division

Power Transistors

RCA42 RCA42B
RCA42A RCA42C



JEDEC TO-220 AB H-1535

Epitaxial-Base, Silicon P-N-P VERSAWATT Transistors

For Power-Amplifier and High-Speed-Switching Applications

Features:

- **65 W at 25°C case temperature**
- **7 A rated collector current**
- **Min. f_T of 3 MHz at 10 V, 500 mA**
- **Designed for complementary use with RCA41, RCA41A, RCA41B, and RCA41C n-p-n types.**

RCA42, RCA42A, RCA42B, and RCA42C are epitaxial-base, silicon p-n-p transistors. They are intended for a wide variety of switching and amplifier applications, such as series and shunt regulators and driver and output stages of high-fidelity amplifiers.

These new plastic power transistors are designed for complementary use with devices in the RCA41 series. They differ from each other in voltage ratings and in the currents at which the parameters are controlled.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		RCA42	RCA42A	RCA42B	RCA42C	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	-40	-60	-80	-100	V
COLLECTOR-TO-EMITTER VOLTAGE:						
With base open	V_{CBO}	-40	-60	-80	-100	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	-5	-5	-5	-5	V
*CONTINUOUS COLLECTOR CURRENT	I_C	-7	-7	-7	-7	A
*CONTINUOUS BASE CURRENT	I_B	-3	-3	-3	-3	A
TRANSISTOR DISSIPATION:	P_Y					
At case temperatures up to 25°C		65	65	65	65	W
At ambient temperatures up to 25°C		2	2	2	2	W
TEMPERATURE RANGE:						
Storage & Operating (Junction)		← 65 to 150 →				°C
*LEAD TEMPERATURE (During Soldering):						
At distance 1/8 in. (3.17 mm) from case for 10 s max.		← 235 →				°C

*Differs from TIP series

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ELECTRICAL CHARACTERISTICS, *At Case Temperature* (T_C) = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: DC VOLTAGE (V) V_{CE}	V_{EB}	V_{BE}	DC CURRENT (A) I_C	I_B	LIMITS: RCA42 MIN.	RCA42 MAX.	RCA42A MIN.	RCA42A MAX.	RCA42B MIN.	RCA42B MAX.	RCA42C MIN.	RCA42C MAX.	UNITS
Collector-Cutoff Current: With base open	I_{CEO}	-30				0	–	-0.7	–	-0.7	–	–	–	–	mA
		-60				0						-0.7		-0.7	
With base-emitter junction short-circuited	I_{CES}	-40		0			–	-0.4	–	–	–	–	–	–	
		-60		0			–	–	–	-0.4	–	–	–	–	
		-80		0			–	–	–	–	–	-0.4	–	–	
		-100		0			–	–	–	–	–	–	–	-0.4	
Emitter-Cutoff Current	I_{EBO}		-5		0		–	-1	–	-1	–	-1	–	-1	mA
Collector-to-Emitter Breakdown Voltage: With base open	$V_{(BR)CEO}$				-0.03[a]	0	-40	–	-60	–	-80	–	-100	–	V
DC Forward-Current Transfer Ratio	h_{FE}	-4			-0.3[a]		30	–	30	–	30	–	30	–	
		-4			-3[a]		15	75	15	75	15	75	15	75	
* Base-to-Emitter Voltage	V_{BE}	-4			-6[a]		–	-2.2	–	-2.2	–	-2.2	–	-2.2	V
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				-6[a]	-0.6	–	-2	–	-2	–	-2	–	-2	V
Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 1 kHz)	h_{fe}	-10			-0.5		20	–	20	–	20	–	20	–	
Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	-10			-0.5		3	–	3	–	3	–	3	–	
Saturated Switching Time: (R_L = 5 Ω) See Figs. 2 & 3 — Turn-on time $t_d + t_r$	t_{ON}	(V_{CC}) -30			-6	-0.6[c]	0.4 (typ.)		0.4 (typ.)		0.4 (typ.)		0.4 (typ.)		µs
* Turn-off time $t_s + t_f$	t_{OFF}	(V_{CC}) -30			-6	-0.6[c]	0.9 (typ.)		0.9 (typ.)		0.9 (typ.)		0.9 (typ.)		µs
Unclamped Inductive Load Energy[b] (L = 20 mH) See Fig. 4		(V_{CC}) -10					–	62.5	–	62.5	–	62.5	–	62.5	mJ
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$						–	1.92	–	1.92	–	1.92	–	1.92	°C/W
Junction-to-Ambient	$R_{\theta JA}$						–	62.5	–	62.5	–	62.5	–	62.5	°C/W

[a]Pulsed: Pulse duration = 300 µs, duty factor = 2%

[b]Based upon ability of device to perform in circuit shown in Fig. 4.

[c]$I_{B1} = I_{B2}$ = value shown

*Differs from TIP series

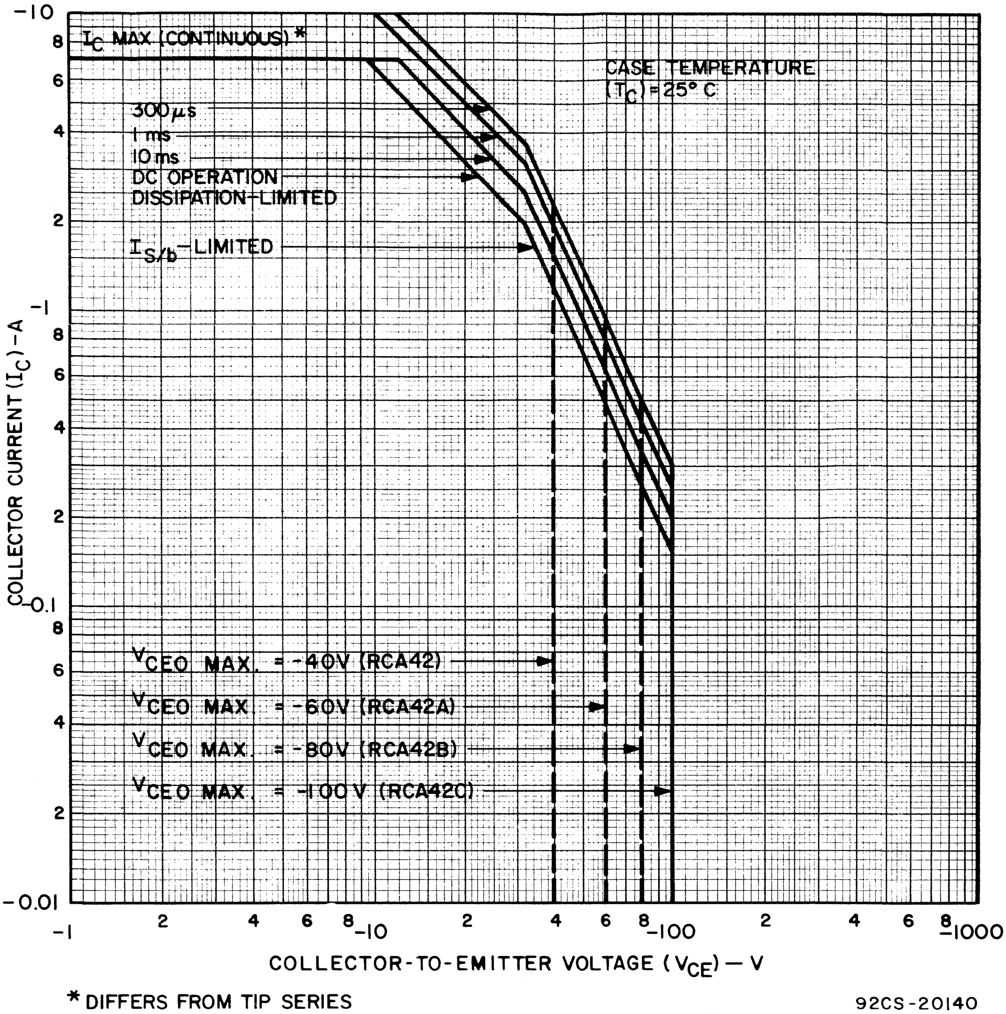


Fig. 1—Maximum safe operating areas for all types.

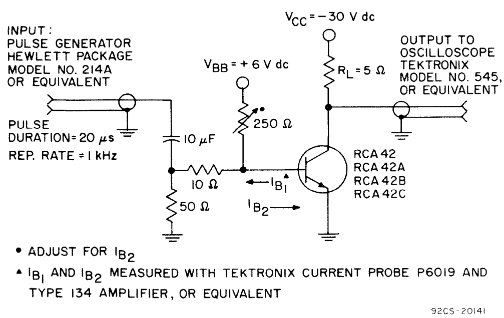


Fig. 2—Circuit used to measure switching times for all types.

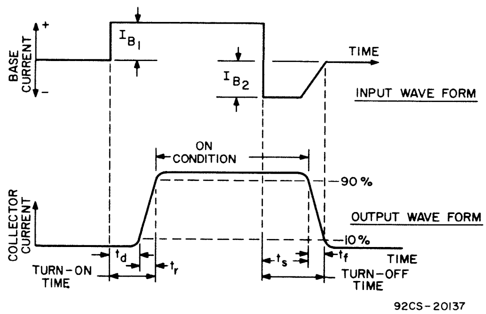


Fig. 3—Phase relationship between input current and output voltage showing reference points for specification of switching times (test circuit shown in Fig. 2).

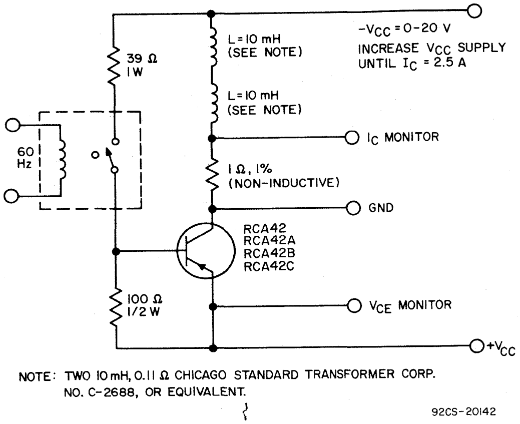


Fig. 4—Circuit for measuring inductive-load switching for all types.

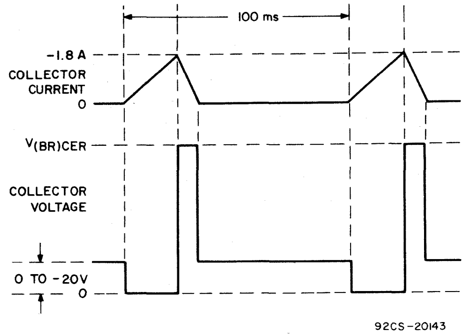


Fig. 5—Inductive-load switching voltage and current waveforms (test circuit shown in Fig. 4).

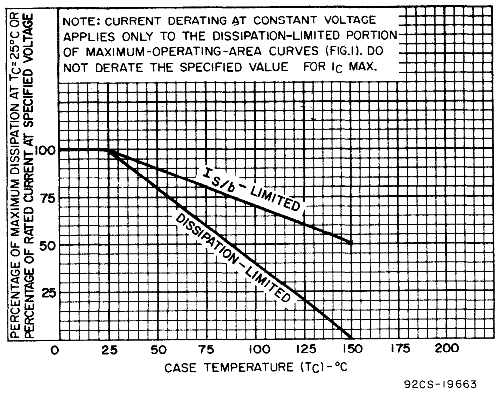


Fig. 6—Derating curves for all types.

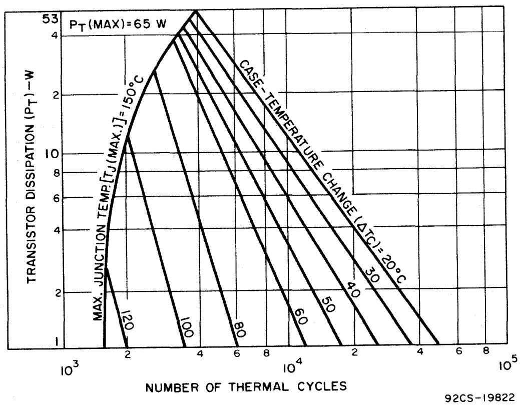


*Fig. 7—Thermal-cycling ratings for all types.**

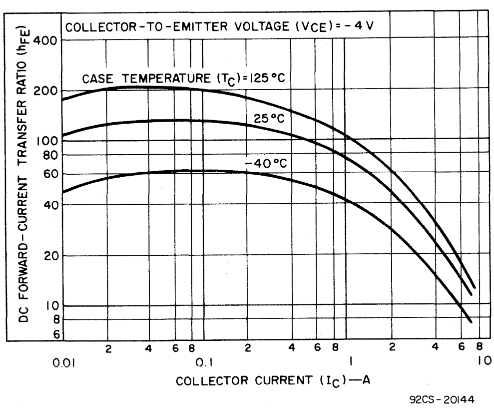
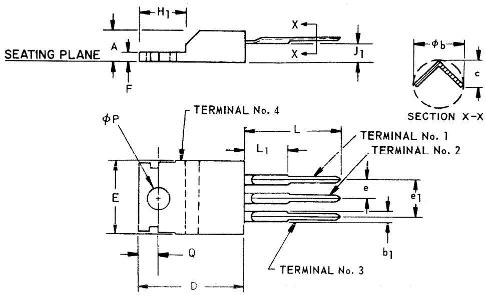


*Fig. 8—Typical dc beta characteristics for all types.**

*Differs from TIP series.

DIMENSIONAL OUTLINE

JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

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NOTES:

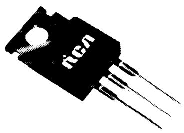
1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS

Lead No. 1 – Base
Lead No. 2 – Collector
Lead No. 3 – Emitter
Mounting Flange, Lead No. 4 – Collector

RCA Solid State Division

Power Transistors
RCA101, 201 RCA103, 203
RCA102, 202 RCA104, 204



JEDEC TO-220AB H-1535

7-A, 75-W, Silicon N-P-N and P-N-P Epitaxial-Base REVERSAWATT Transistors

Complementary Pairs for Audio Amplifiers
—Up to 20 W Music Power per Channel

Features:

- **Thermal-cycling ratings**
- **Maximum safe-area-of-operation curves**
- **Color-coded packages of molded silicone plastic:**
  Green – p-n-p (RCA-101 – RCA-104)
  Gray – n-p-n (RCA-201 – RCA-204)

RCA-101 – 104 and 201 – 204 are epitaxial-base silicon p-n-p and n-p-n transistors. They are intended for use in output stages of high-fidelity amplifiers.

These devices are RCA REVERSAWATT transistors in color-coded molded silicone plastic packages; the 101 – 104 (p-n-p) units are green and the 201 – 204 (n-p-n) units are gray for ease of identification.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		101 201	102 103 202 203	104 204	
COLLECTOR-TO-BASE VOLTAGE: With emitter open	V_{CBO}	40	60	80	V
COLLECTOR-TO-EMITTER VOLTAGE: With base open	V_{CEO}	40	60	80	V
EMITTER-TO-BASE VOLTAGE: With collector open	V_{EBO}	← 4.0 →			V
COLLECTOR CURRENT (Continuous)	I_C	← 7.0 →			A
BASE CURRENT (Continuous)	I_B	← 3.0 →			A
TRANSISTOR DISSIPATION: At case temperatures up to 25°C	P_T	← 75 →			W
At case temperatures above 25°C		Derate linearly at 0.600 W/°C or see Fig. 2.			
TEMPERATURE RANGE: Storage & Operating (Junction)		← -65 to +150° →			°C
LEAD TEMPERATURE (During Soldering): At distance ≥ 1/8 in. (3.17 mm) from case for 10 s max.		← +235 →			°C

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ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	DC COLLECTOR VOLTAGE (V)		DC EMITTER OR BASE VOLTAGE (V)		DC CURRENT (A)			LIMITS P-N-P TYPES 101 / N-P-N TYPES 201		102 / 202		103 / 203		104 / 204		UNITS
		V_{CE}	V_{CB}	V_{EB}	V_{BE}	I_C	I_B	I_E	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Collector-Cutoff Current: With emitter open	I_{CBO}		40					0	–	0.1	–	–	–	–	–	–	mA
			60					0	–	–	–	0.1	–	0.1	–	–	
			80					0	–	–	–	–	–	–	–	0.1	
At T_C = 150°C			40					0	–	2.0	–	–	–	–	–	–	
			60					0	–	–	–	2.0	–	2.0	–	–	
			80					0	–	–	–	–	–	–	–	2.0	
Emitter-Cutoff Current: With collector open	I_{EBO}			4.0		0			–	1.0	–	1.0	–	1.0	–	1.0	mA
Collector-to Emitter Breakdown Voltage: With base open	$V_{(BR)CEO}$					0.1*	0		40	–	60	–	60	–	80	–	V
Base-Emitter Voltage	V_{BE}	2.0				2.0*			–	1.2	–	1.2	–	–	–	–	V
		2.0				1.0			–	–	–	–	–	1.2	–	1.2	
DC Forward-Current Transfer Ratio	h_{FE}	2.0				1.0			–	–	–	–	30	150	30	150	–
		2.0				2.0			25	150	25	150	–	–	–	–	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$								–	1.66	–	1.66	–	1.66	–	1.66	°C/W

*Pulsed: Pulse duration = 300 μs, duty factor ≤ 2%.

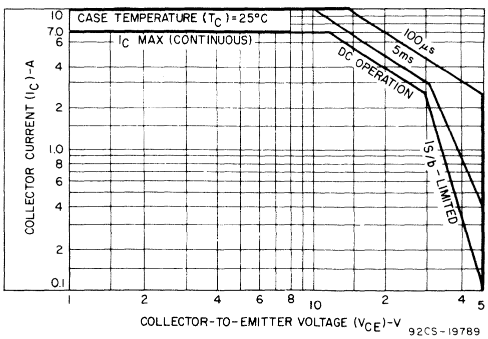


Fig. 1–Maximum operating areas for types 101–104 and 201–204.

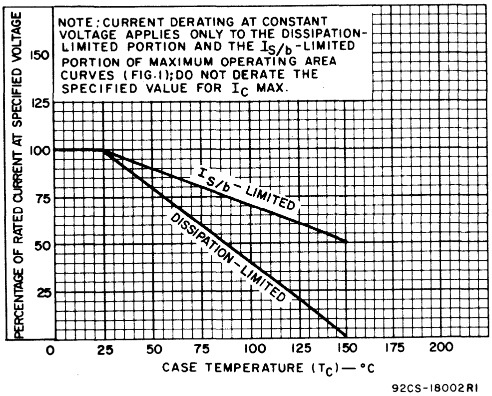


Fig. 2—Derating curves for all types.

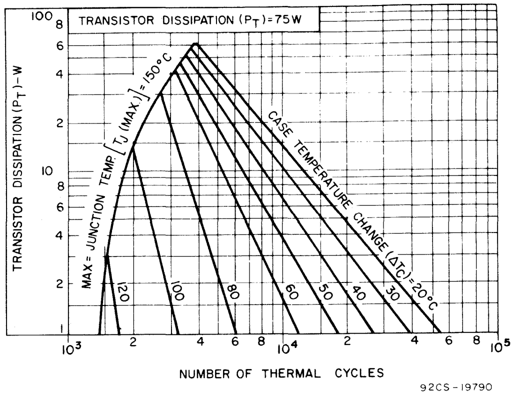


Fig. 3—Thermal-cycling ratings for all types.

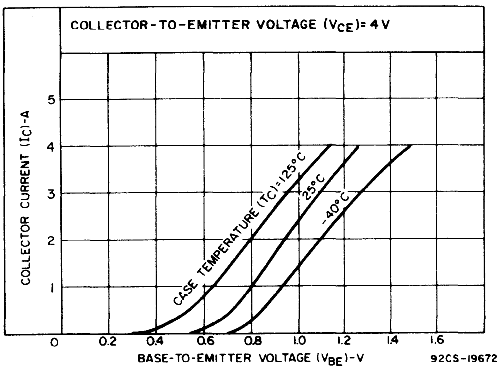


Fig. 4—Typical transfer characteristics for types 201—204.

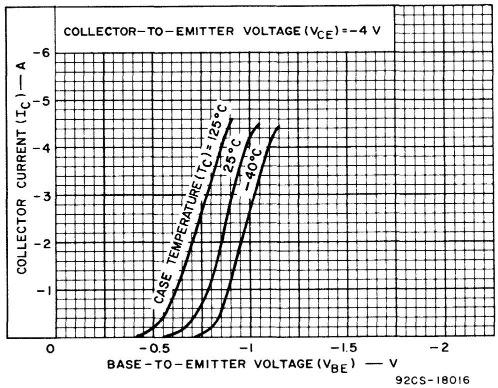


Fig. 5—Typical transfer characteristics for types 101—104.

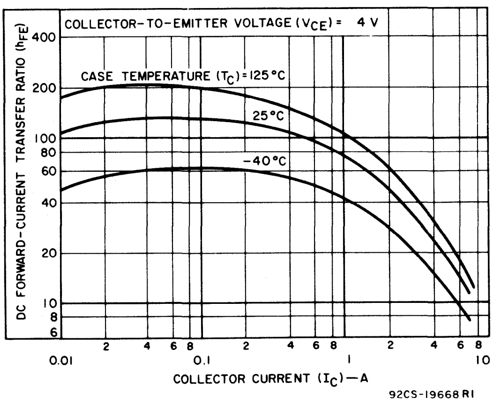
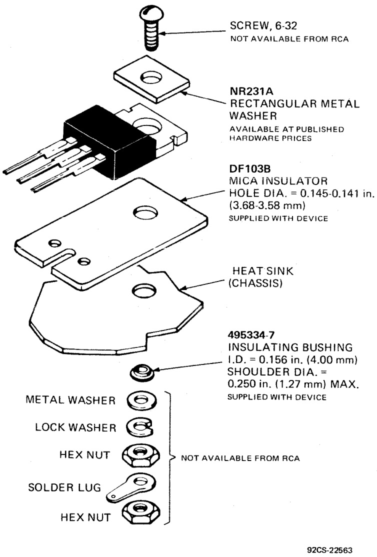


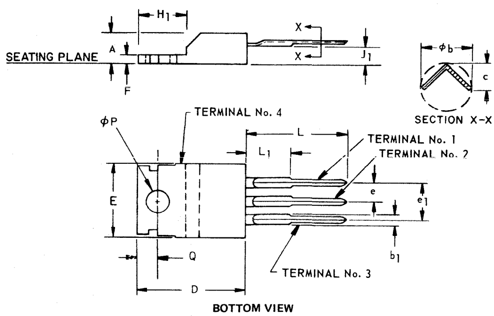
Fig. 6—Typical dc beta characteristics for types 101—104 and 201—204.



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 7–Suggested mounting hardware for all types.

DIMENSIONAL OUTLINE JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
ϕb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
ϕP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:
1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

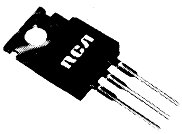
TERMINAL CONNECTIONS

Lead No. 1 – Emitter
Lead No. 2 – Collector
Lead No. 3 – Base
Mounting Flange – Collector

Solid State
Division

Power Transistors

RCA105
RCA205



JEDEC TO-220 AB H-1535

7-A, 65-W, Silicon N-P-N and P-N-P Epitaxial-Base REVERSAWATT Transistors

Complementary Pairs for Audio Amplifiers
—Up to 20 W Music Power Per Channel

Features:
- **Thermal-cycling ratings**
- **Maximum safe-area-of-operation curves**
- **Color-coded packages of molded silicone plastic:**
  Green — p-n-p (RCA-105)
  Gray — n-p-n (RCA 205)

RCA-105 and RCA-205 are epitaxial-base silicon p-n-p and n-p-n, respectively, transistors. They are intended for use in output stages of high-fidelity amplifiers.

These devices are RCA REVERSAWATT transistors in color-coded molded silicone plastic packages; the 105 (p-n-p) unit is green, and the 205 (n-p-n) unit is gray for ease of identification.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		105 205	
COLLECTOR-TO-BASE VOLTAGE: With emitter open	V_{CBO}	50	V
COLLECTOR-TO-EMITTER VOLTAGE: With base open	V_{CEO}	50	V
EMITTER-TO-BASE VOLTAGE: With collector open	V_{EBO}	4.0	V
COLLECTOR CURRENT (Continuous)	I_C	7.0	A
BASE CURRENT (Continuous)	I_B	2.5	A
TRANSISTOR DISSIPATION: At case temperatures up to 25°C	P_T	65	W
At case temperatures above 25°C		Derate linearly at 0.522 W/°C or see Fig. 2.	
TEMPERATURE RANGE: Storage & Operating (Junction)		−65 to + 150°	°C
LEAD TEMPERATURE (During Soldering): At distance ≥ 1/8 in. (3.17 mm) from case for 10 s max.		+235	°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless otherwise specified*

CHARACTERISTIC	SYMBOL	DC COLLECTOR VOLTAGE (V)		DC EMITTER OR BASE VOLTAGE (V)		DC CURRENT (A)			LIMITS 105 205		UNITS
		V_{CE}	V_{CB}	V_{EB}	V_{BE}	I_C	I_B	I_E	MIN.	MAX.	
Collector-Cutoff Current: With emitter open	I_{CBO}		50					0	–	0.1	mA
At T_C = 150°C	I_{CBO}		50					0	–	2.0	mA
Emitter-Cutoff Current: With collector open	I_{EBO}			4.0		0		–	–	1.0	mA
Collector-to-Emitter Breakdown Voltage: With base open	$V_{(BR)CEO}$					0.1*	0		50	–	V
Base-Emitter Voltage	V_{BE}	2.0				2.0*			–	1.2	V
DC Forward-Current Transfer Ratio	h_{FE}	2.0				2.0*			25	100	–
Thermal Resistance Junction to Case	$R_{\theta JC}$								–	1.92	°C/W

*Pulsed: Pulse duration = 300 μs, duty factor ≤ 2%.

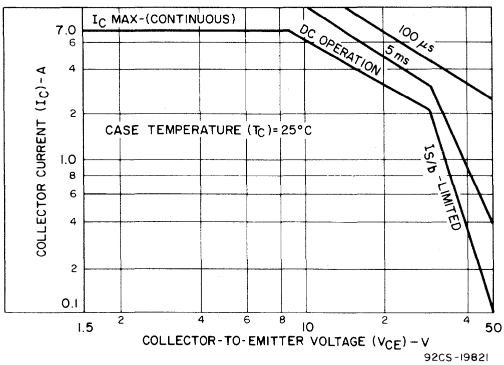


Fig. 1—Maximum operating areas for types 105 and 205.

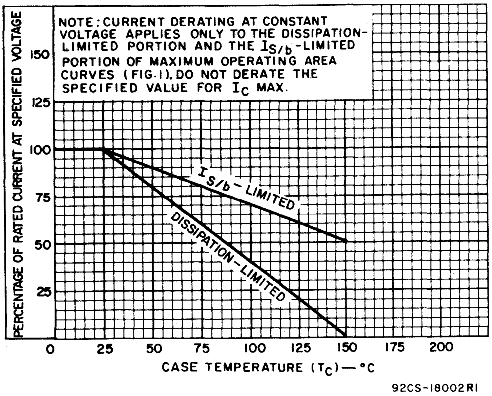


Fig. 2—Derating curves for types 105 and 205.

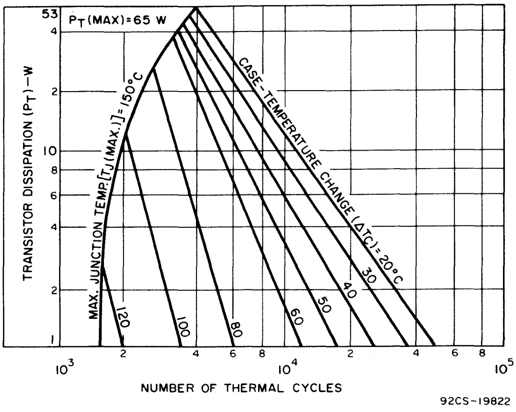


Fig. 3—Thermal-cycling ratings for types 105 and 205.

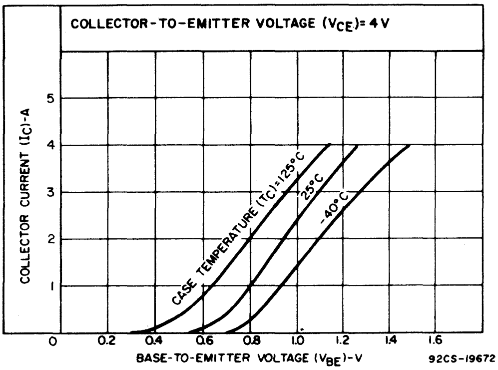


Fig. 4—Typical transfer characteristics for type 205.

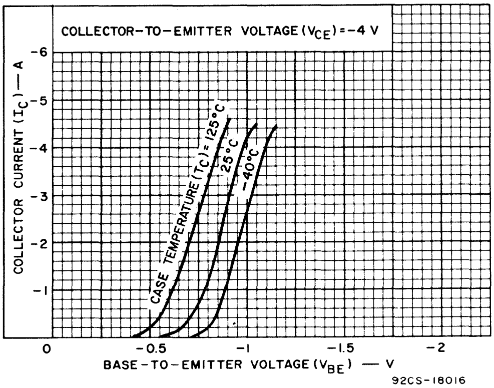


Fig. 5—Typical transfer characteristics for type 105.

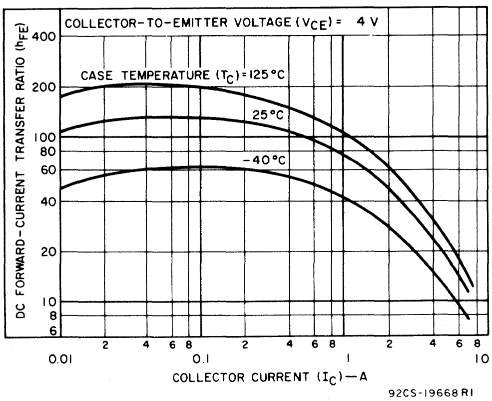
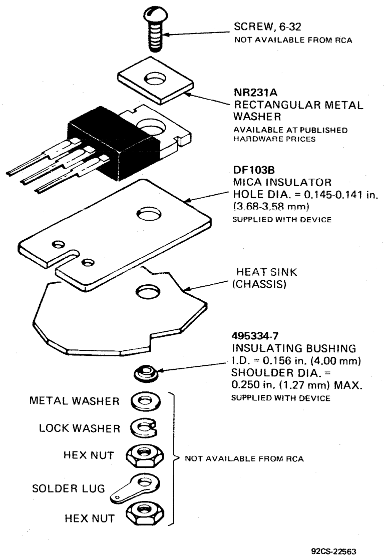


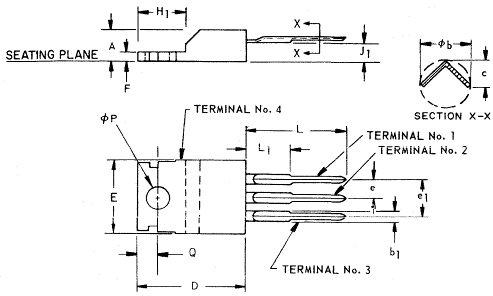
Fig. 6—Typical dc beta characteristics for types 105 and 205.



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 7—Suggested mounting hardware for types 105 and 205.

DIMENSIONAL OUTLINE JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
ϕb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
ϕP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

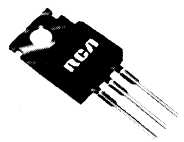
TERMINAL CONNECTIONS

Lead No. 1 – Emitter
Lead No. 2 – Collector
Lead No. 3 – Base
Mounting Flange – Collector

Solid State
Division

Power Transistors

RCA370 RCA520
RCA371 RCA521



JEDEC TO-220AB H1535R1

5-A, 40-W, Silicon N-P-N and P-N-P Epitaxial-Base REVERSAWATT Transistors

For Use in 5- to 10-Watt Audio Amplifiers Utilizing Complementary-Symmetry Circuits

Features:

- **Thermal-cycling ratings**
- **Maximum-safe-area-of-operation curves**
- **Color-coded packages of molded silicone plastic:**
  - **Green — p-n-p RCA-370-1**
  - **Gray — n-p-n RCA-520-1**

RCA—370, 371, 520, and 521 are epitaxial-base silicon p-n-p and n-p-n transistors. They are intended for medium-power amplifier applications, and are especially designed for use in 5- to 10-watt audio amplifiers utilizing complementary-symmetry circuits.

These devices are packaged in RCA REVERSAWATT molded silicone plastic packages; the 370 and 371 (p-n-p) devices are green, and the 520 and 521 (n-p-n) units gray for ease in identification.

MAXIMUM RATINGS, *Absolute-Maximum Values:*		**370 (p-n-p) 520 (n-p-n)**	**371 (p-n-p) 521 (n-p-n)**	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	30	40	V
COLLECTOR-TO-EMITTER VOLTAGE:				
With base open	V_{CEO}	30	40	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4	4	V
CONTINUOUS COLLECTOR CURRENT	I_C	5	5	A
CONTINUOUS BASE CURRENT	I_B	2	2	A
TRANSISTOR DISSIPATION:	P_T			
At case temperatures up to 25°C		40	40	W
At case temperatures above 25°C		Derate linearly at 0.32 W/°C or See Fig. 3		
TEMPERATURE RANGE:				
Storage & Operating (Junction)		−65 to 150		°C
TERMINAL TEMPERATURE (During Soldering):				
At distance ≥ 1/8 in. (3.17 mm) from case for 10 s max.		235		°C

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ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C*

CHARACTERISTIC	SYMBOL	DC COLLECTOR VOLTAGE (V)		DC EMITTER OR BASE VOLTAGE (V)		DC CURRENT (A)			LIMITS				UNITS
									370 (p-n-p) 520 (n-p-n)		371 (p-n-p) 521 (n-p-n)		
		V_{CB}	V_{CE}	V_{EB}	V_{BE}	I_C	I_B	I_E	MIN.	MAX.	MIN.	MAX.	
Collector-Base Cutoff Current: With emitter open	I_{CBO}	30						0	–	100	–	–	µA
		40						0	–	–	–	100	
Emitter-Cutoff Current	I_{EBO}			4		0			–	100	–	100	µA
Collector-to-Emitter Sustaining Voltage: With base open	$V_{CEO}(sus)^a$					0.1	0		30	–	40	–	V
DC Forward Current Transfer Ratio	h_{FE}^a		1			1			25	–	40	–	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$								–	3.12	–	3.12	°C/W

[a]Pulsed: Pulse duration ≤ 300 µs, duty factor ≤ 2%.

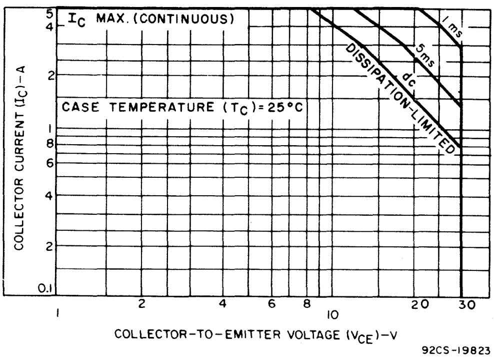


Fig. 1—Maximum operating areas for types 370 and 520.

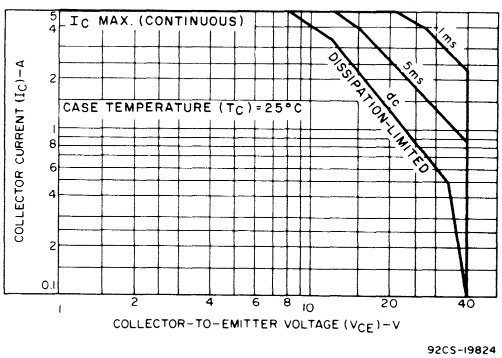


Fig. 2—Maximum operating areas for types 371 and 521.

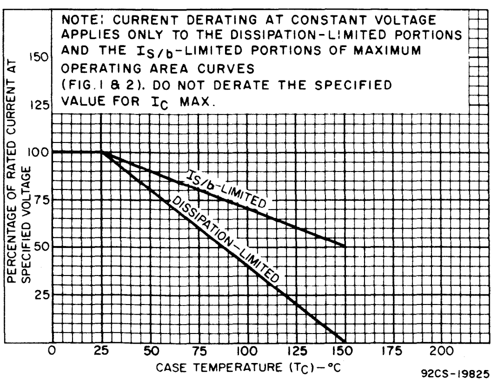


Fig. 3—Derating curves for all types.

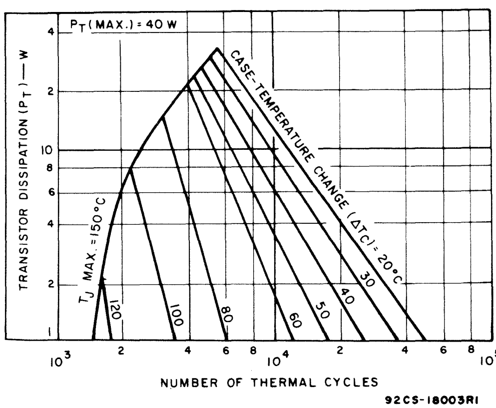


Fig. 4—Thermal-cycling ratings for all types.

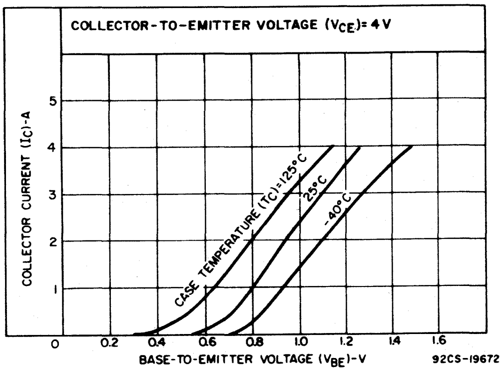


Fig. 5—Typical transfer characteristics for types 520 and 521.

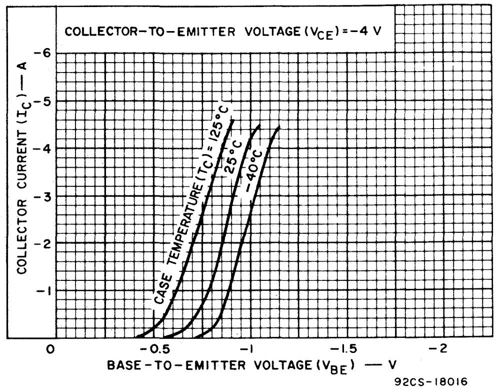


Fig. 6—Typical transfer characteristics for types 370 and 371.

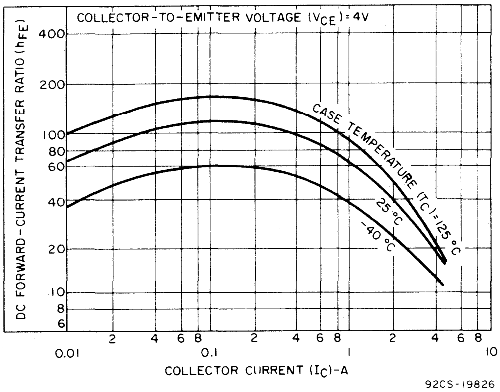
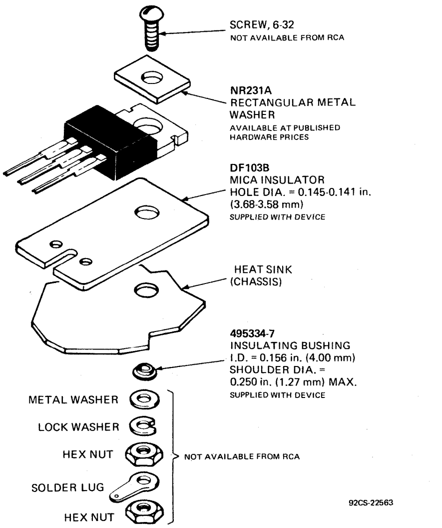


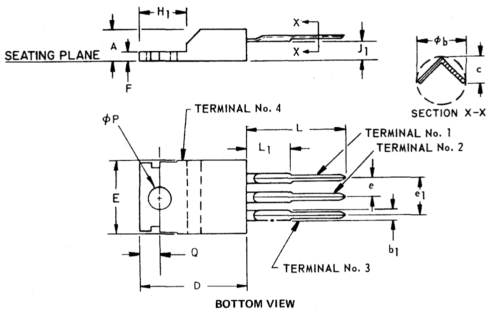
Fig. 7—Typical dc beta characteristics for all types.



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 8—Suggested mounting hardware for all types.

DIMENSIONAL OUTLINE JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

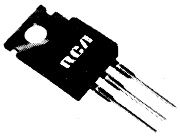
1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS

Terminal No. 1 – Emitter
Terminal No. 2 – Collector
Terminal No. 3 – Base
Mounting Flange, Terminal No. 4 – Collector

Solid State
Division

Power Transistors
45190 45191 45192 45193 45194 45195



JEDEC TO-220AB H-1535

7-A,40-W, Silicon N-P-N and P-N-P Epitaxial-Base REVERSAWATT Transistors

Complementary Pairs for Power Amplifiers and Switching Circuits

- **Thermal-cycling ratings**
- **Maximum safe-area-of-operation curves**
- **Color-coded packages of molded silicone plastic:**
  Green—p-n-p (RCA-45193-5)
  Gray —n-p-n (RCA 45190-2)

RCA-45190-45192 and RCA-45193-45195 are epitaxial-base silicon n-p-n and p-n-p transistors. They are intended for use in high-fidelity power amplifiers and in switching circuits.

These devices are packaged in RCA REVERSAWATT molded silicone plastic packages; the 45190-45192 (n-p-n) units are gray, and the 45193-45195 (p-n-p) units are green for ease in identification.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		45190 (n-p-n) 45193 (p-n-p)	45191 (n-p-n) 45194 (p-n-p)	45192 (n-p-n) 45195 (p-n-p)	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	40	60	80	V
COLLECTOR-TO-EMITTER VOLTAGE					
With base open	V_{CEO}	40	60	80	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	←	5	→	V
COLLECTOR CURRENT (Continuous)	I_C	←	7	→	A
BASE CURRENT (Continuous)	I_B	←	2	→	A
TRANSISTOR DISSIPATION	P_T				
At case temperatures up to 25°C		←	40	→	W
At case temperatures above 25°C			Derate linearly at 0.32 W/°C or see Fig. 2		
TEMPERATURE RANGE:					
Storage & Operating (Junction)		←	-65 to 150	→	°C
TERMINAL TEMPERATURE (During Soldering):					
At distance ≥ 1/8 in. (3.17 mm) from case for 10 s max.		←	235	→	°C

11-73

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25°C unless otherwise specified.

CHARACTERISTIC	SYMBOL	DC COLLECTOR VOLTAGE V		DC EMITTER VOLTAGE V	DC CURRENT A			LIMITS						UNITS
								45190 (n-p-n) 45193 (p-n-p)		45191 (n-p-n) 45194 (p-n-p)		45192 (n-p-n) 45195 (p-n-p)		
		V_{CB}	V_{CE}	V_{EB}	I_C	I_B	I_E	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Collector-Cutoff Current: With emitter open	I_{CBO}	40 60 80					0 0 0	– – –	100 – –	– – –	– 100 –	– – –	– – 100	µA
Collector-Cutoff Current: With base open	I_{CEO}	40 60 80				0 0 0		– – –	1 – –	– – –	– 1 –	– – –	– – 1	mA
Collector-Cutoff Current: With base-emitter junction reverse-biased	I_{CEX}		40 60 80	1.5 1.5 1.5				– – –	0.1 – –	– – –	– 0.1 –	– – –	– – 0.1	mA
T_C = 125°C	I_{CEX} (T_C = 125°C)		40 60 80	1.5 1.5 1.5				– – –	2 – –	– – –	– 2 –	– – –	– – 2	
Emitter-Cutoff Current	I_{EBO}			5	0			–	1	–	1	–	1	mA
Collector-to-Emitter Sustaining Voltage: With base open	$V_{CEO}(sus)^a$				0.1	0		40	–	60	–	80	–	V
Base-to-Emitter Voltage	V_{BE}^a		2		1.5			–	1.2	–	1.2	–	1.2	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)^a$				1.5 4	0.15 1		– –	0.6 1.4	– –	0.6 1.4	– –	0.6 1.4	V
Gain-Bandwidth Product (At f = 1 MHz)	f_T		10		1			2	–	2	–	2	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}^a		2 2		1.5 4			25 10	100 –	25 10	100 –	20 7	80 –	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$							–	3.12	–	3.12	–	3.12	°C/W

[a]Pulsed: Pulse duration ≤300 µs, duty factor ≤2%.

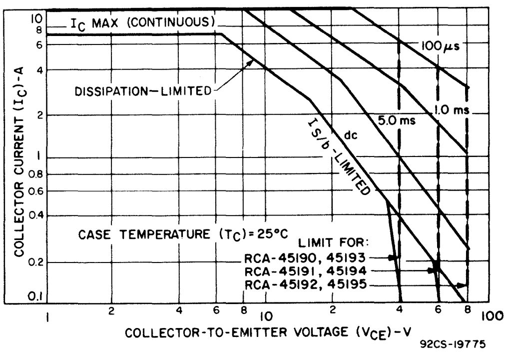


Fig. 1–Maximum operating areas for types 45190-5.

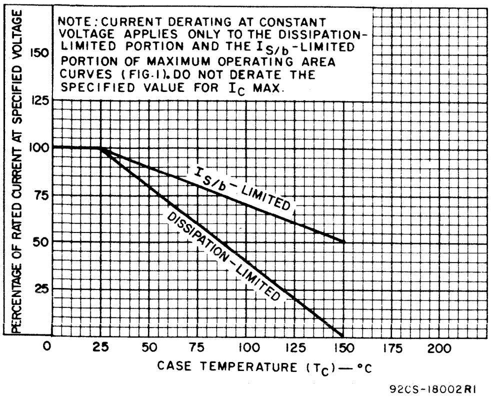


Fig. 2–Derating curves for types 45190-5.

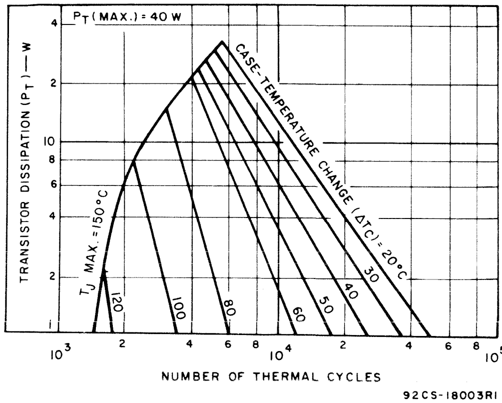


Fig. 3–Thermal-cycling ratings for types 45190-5.

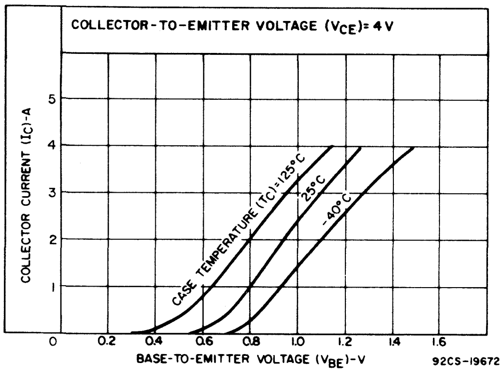


Fig. 4–Typical transfer characteristics for types 45190-2.

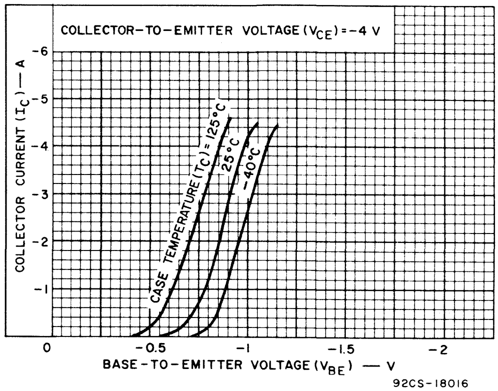


Fig. 5–Typical transfer characteristics for types 45193-5.

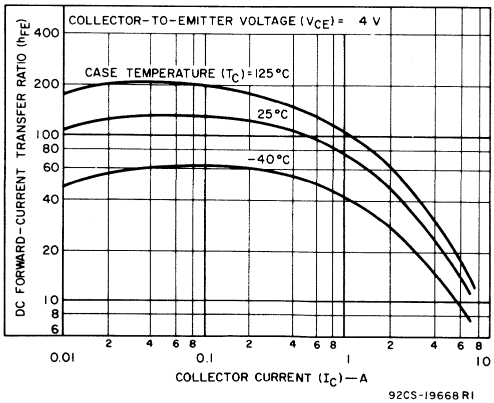
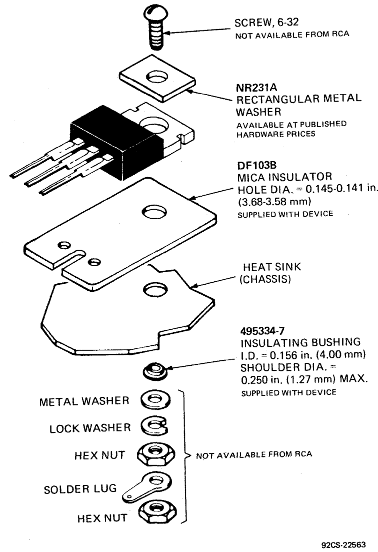


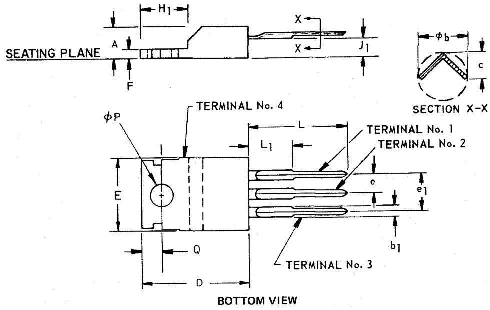
Fig. 6–Typical dc beta characteristics for types 45190-5.



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 7—Suggested mounting hardware for JEDEC TO-220 AB.

DIMENSIONAL OUTLINE JEDEC TO-220 AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS

Terminal No. 1 – Emitter
Terminal No. 2 – Collector
Terminal No. 3 – Base
Mounting Flange, Terminal No. 4 – Collector

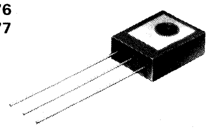
High-Voltage Power Transistors

RCA
Solid State
Division

Power Transistors

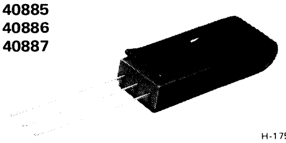
2N6175 40885
2N6176 40886
2N6177 40887

2N6175
2N6176
2N6177



H-1642

40885
40886
40887



H-1756

High-Voltage, Medium-Power Silicon N-P-N Transistors

For High-Speed Switching and Linear-Amplifier Applications

Features

- **Thermal fatigue ratings**
- **High frequency response: f_T = 20 MHz**
- **Maximum area-of-operation curves for DC and pulse operation**
- **Designed to assure freedom from second breakdown in class A, B, and C operation at maximum ratings**
- **High voltage ratings:**
  V_{CEO}(sus) = 350 V max. (2N6177, 40887)
  = 300 V max. (2N6176, 40886)
  = 250 V max. (2N6175, 40885)
- **Low saturation voltage:**
  V_{CE}(sat) = 0.5 V max.

RCA types 2N6175, 2N6176, and 2N6177* are silicon n-p-n transistors with high breakdown voltages, high frequency response, and fast switching speeds. Types 40885, 40886, and 40887 are electrically identical to the 2N6175–2N6177, respectively, but are supplied with factory-attached heat clips.

Typical applications for these devices include TV video output, RGB output, chroma output, TV blanking, solenoid drivers, off-line inverters, regulators, audio output, and electrostatic deflection in display circuits.

*Formerly Dev. Nos. TA7739, TA7740 and TA7134, respectively.

MAXIMUM RATINGS, Absolute-Maximum Values:

		2N6175 40885	2N6176 40886	2N6177 40887	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	300	350	450	V
*COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE	V_{CEO}(sus)	250	300	350	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	6	6	6	V
*COLLECTOR CURRENT	I_C	1.0	1.0	1.0	A
*BASE CURRENT	I_B	0.5	0.5	0.5	A
*TRANSISTOR DISSIPATION	P_T				
At case temperatures up to 25°C		20	20	20	W
		(2N6175, 2N6176, 2N6177)			
At case temperatures above 25°C		See Fig. 15			
At ambient temperatures up to 25°C		0.8	0.8	0.8	W
		(2N6175, 2N6176, 2N6177)			
		1.4	1.4	1.4	W
		(40885, 40886, 40887)			
At ambient temperatures above 25°C		See Fig. 16			
For pulse operation		See Figs. 6, 7, & 8			
*TEMPERATURE RANGE:					
Storage & Operating (Junction)		← -65 to 135 →			°C
*LEAD TEMPERATURE (During soldering):					
At distance ≥ 1/16 in. (1.59 mm) from case for 10 s max.		← 230 →			°C

*Types 2N6175, 2N6176, and 2N6177 in accordance with JEDEC registration data format JS-9 RDF-8.

ELECTRICAL CHARACTERISTICS, at case temperature (T_C) = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: DC COLLECTOR VOLTAGE (V) V_{CB}	V_{CE}	DC EMITTER OR BASE VOLTAGE (V) V_{EB}	V_{BE}	DC CURRENT (mA) I_C	I_E	I_B	LIMITS 2N6175 40885 MIN.	MAX.	2N6176 40886 MIN.	MAX.	2N6177 40887 MIN.	MAX.	UNITS
Collector-Cutoff Current: With base open	I_{CEO}		300					0	–	–	–	–	–	20	μA
			200					0	–	50	–	50	–	–	
* With emitter open	I_{CBO}	360							–	–	–	–	–	20	
		280							–	–	–	50	–	–	
		240							–	50	–	–	–	–	
With base-emitter junction reverse-biased	I_{CEV}		450		-1.5				–	–	–	–	–	500	
			300		-1.5				–	500	–	500	–	–	
* Emitter-Cutoff Current	I_{EBO}			6					–	20	–	20	–	20	μA
DC Forward-Current Transfer Ratio	h_{FE}		10			50			–	–	–	–	30*	150	
			10			20			30*	190	30*	150	–	–	
			10			5			–	–	15	–	15	–	
			10			1			15	–	–	–	–	–	
Collector-to-Emitter Sustaining Voltage: With base open (See Figs. 9 & 10)	$V_{CEO}(sus)$					50		0	250[a]	–	300[a]	–	350[a]	–	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$					50		4	–	1.3	–	1.3	–	1.3	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					50		4	–	0.5	–	0.5	–	0.5	V
* Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$					1	0		300		350		450		V
* Low-Frequency, Common-Emitter, Small-Signal, Short-Circuit, Forward-Current Transfer Ratio (f = 1 kHz)	h_{fe}		10			5			25	–	25	–	25	–	
* Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward-Current Transfer Ratio (f = 3 MHz)	$\|h_{fe}\|$		20			20			7	–	7	–	7	–	
* Real Part of Common-Emitter, Small-Signal, Short-Circuit Input Impedance (f = 1 MHz)	$Re(h_{ie})$		20			20			–	300	–	–	–	–	Ω
			10			5			–	–	–	300	–	300	
* Output Capacitance (at 1 MHz)	C_{cb}	20					0		–	8	–	8	–	8	pF
Second-Breakdown Collector Current: With base forward biased[c] tp = 0.4 s	$I_{S/b}$[b]		150						133	–	133	–	133	–	mA
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$								– (2N6175)	5.5 (2N6175)	– (2N6176)	5.5 (2N6176)	– (2N6177)	5.5 (2N6177)	°C/W
Junction-to-Ambient	$R_{\theta JA}$								– (2N6175)	138 (2N6175)	– (2N6176)	138 (2N6176)	– (2N6177)	138 (2N6177)	
									– (40885)	78.6 (40885)	– (40886)	78.6 (40886)	– (40887)	78.6 (40887)	

* Types 2N6175, 2N6176, and 2N6177 in accordance with JEDEC registration data format JS-9 RDF-8.

[a] CAUTION: The sustaining votlage V_{CEO}(sus) MUST NOT be measured on a curve tracer. The sustaining voltage should be measured by means of the test circuit shown in Fig. 9.

[b] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage.

[c] Specified value of $I_{S/b}$ for given value of V_{CE} as base voltage is increased from zero in a positive direction.

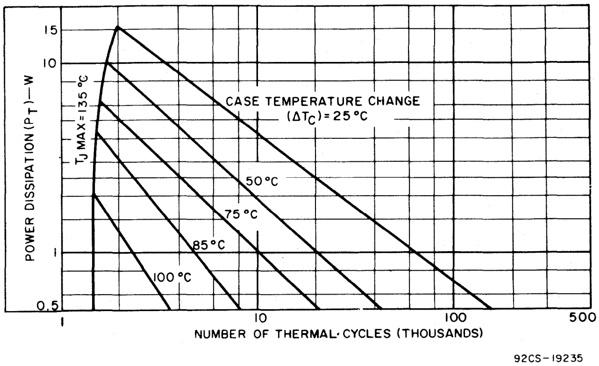


Fig. 1—Thermal-cycling rating chart.

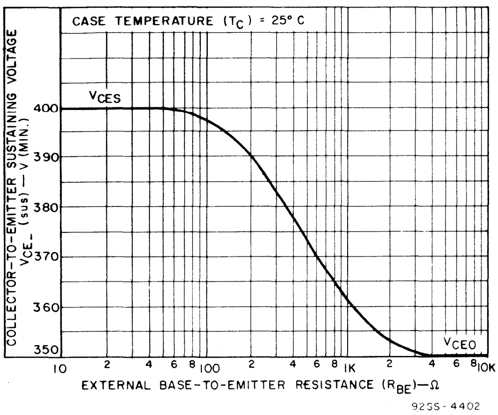


Fig.2—Sustaining voltage vs. base-to-emitter resistance for types 2N6177 and 40877.

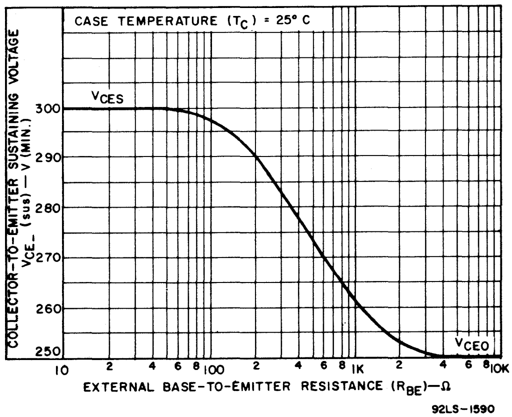


Fig.3—Sustaining voltage vs. base-to-emitter resistance for types 2N6175 and 40885.

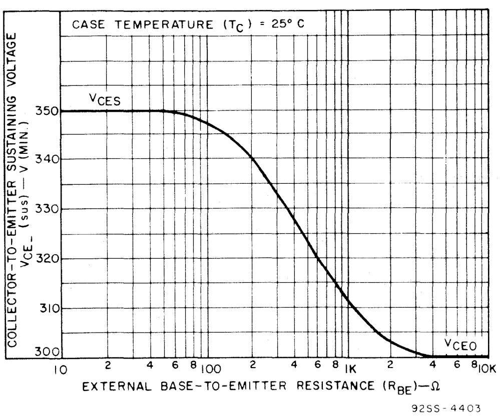


Fig.4—Sustaining voltage vs. base-to-emitter resistance for types 2N6176 and 40886.

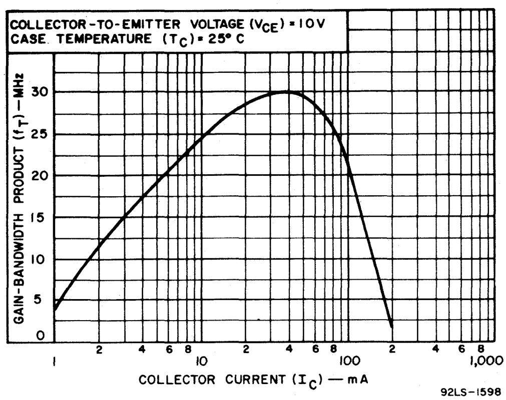


Fig.5—Typical gain-bandwidth product for all types.

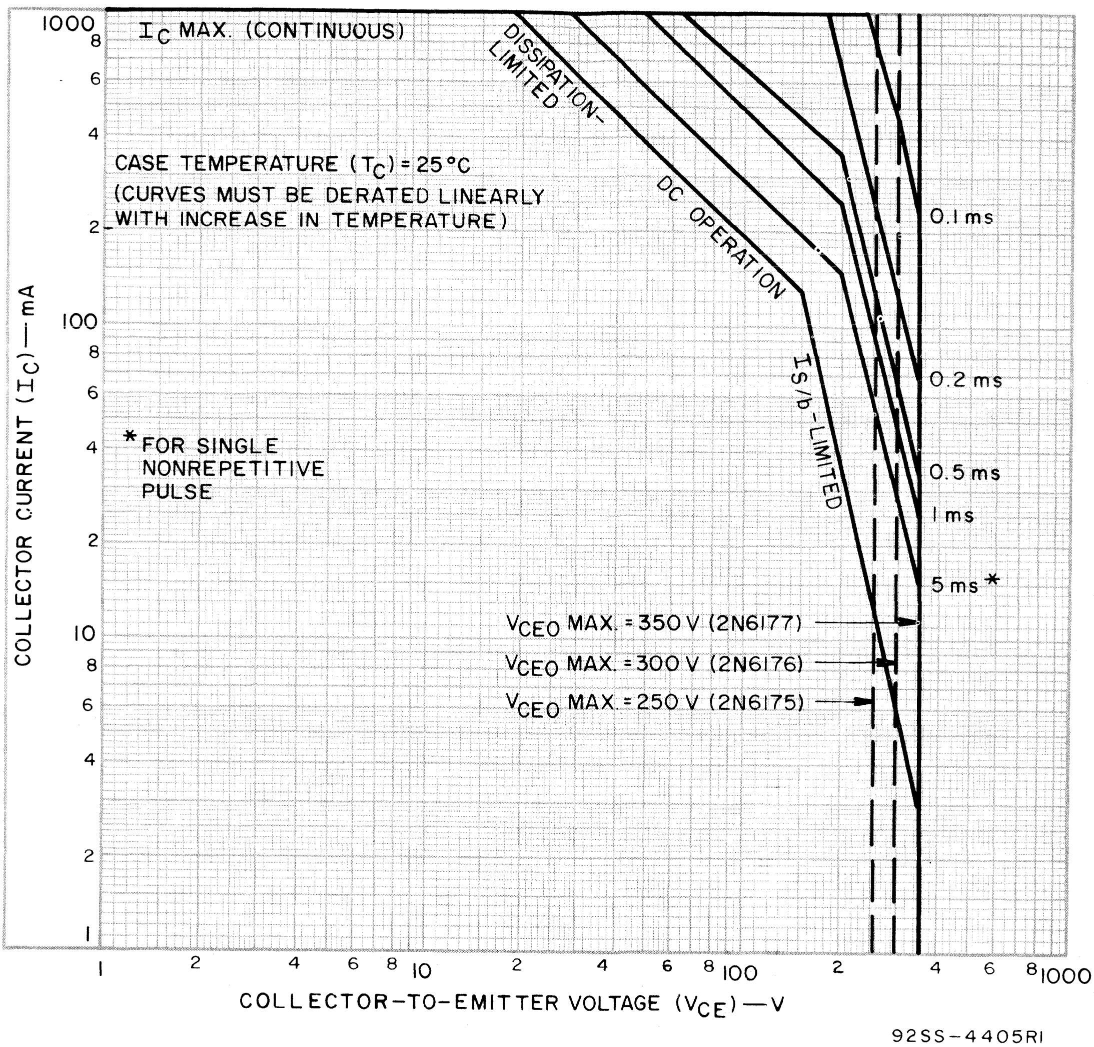


Fig.6—Maximum safe-operating-areas for types 2N6175, 2N6176, and 2N6177.

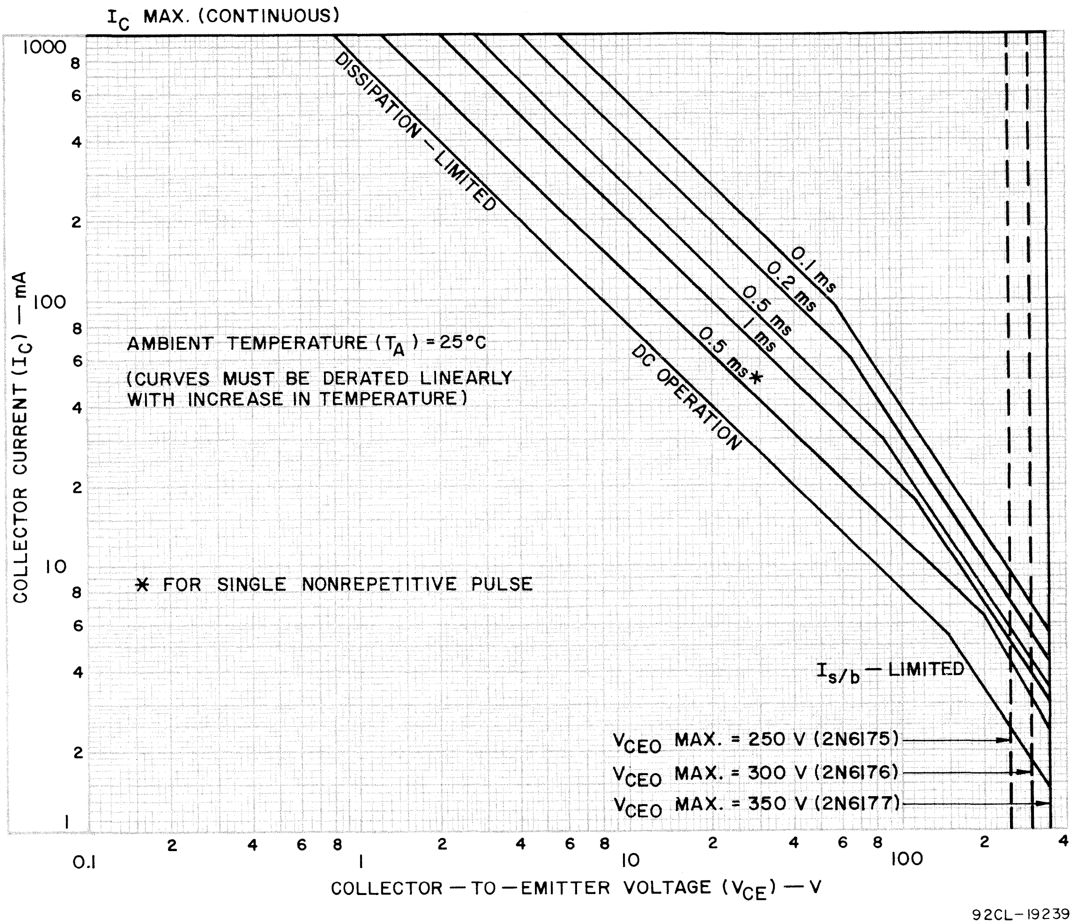


Fig.7–Maximum safe area-of-operation at ambient temperature for types 2N6175, 2N6176, and 2N6177.

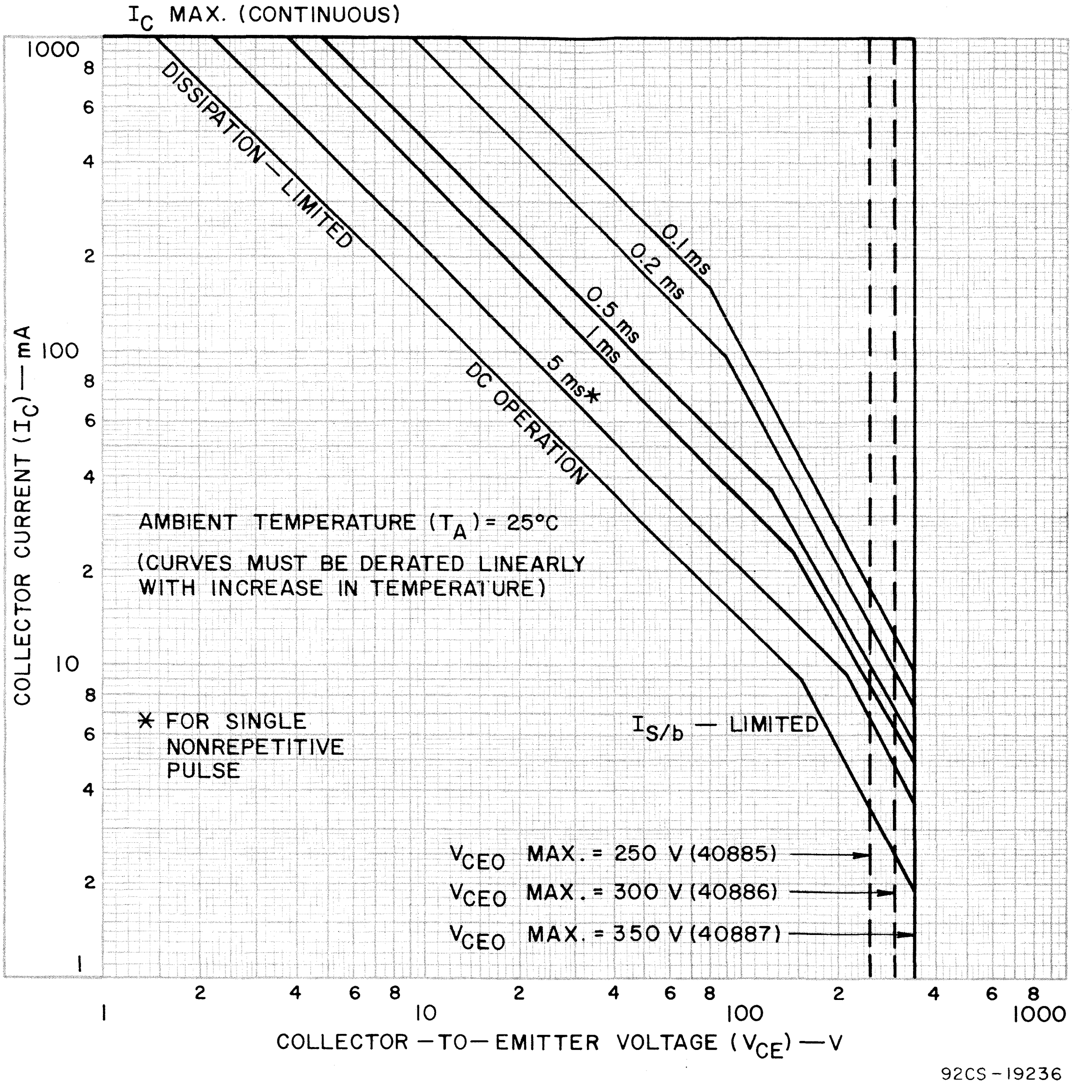


Fig.8—Maximum safe area-of-operation for types 40885, 40886, and 40887.

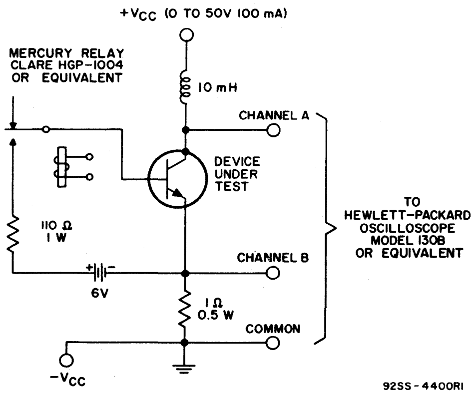
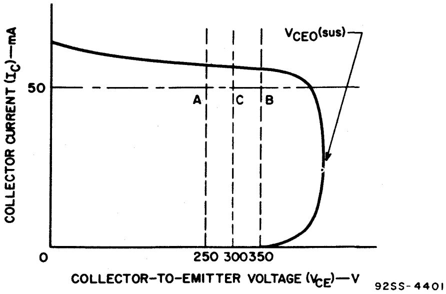


Fig.9—Circuit used to measure sustaining voltage, $V_{CEO}(sus)$.



The sustaining voltage $V_{CEO}(sus)$ is acceptable when the trace falls to the right and above point "A" for type 2N6175 or 40885. The trace must fall to the right and above point "B" for type 2N6177 or 40887 and above and to the right of point "C" for type 2N6176 or 40886.

Fig.10—Oscilloscope display for measurement of sustaining voltages (test circuit shown in Fig. 9).

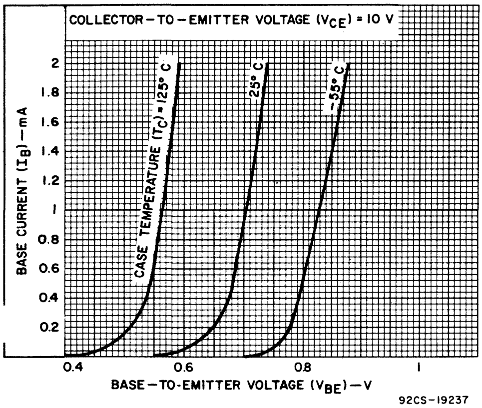


Fig.11—Typical input characteristics for all types.

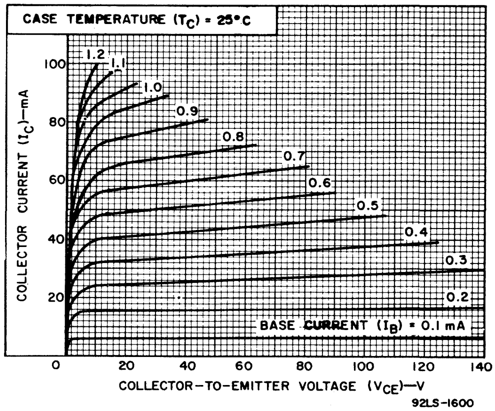


Fig.12—Typical output characteristics for all types.

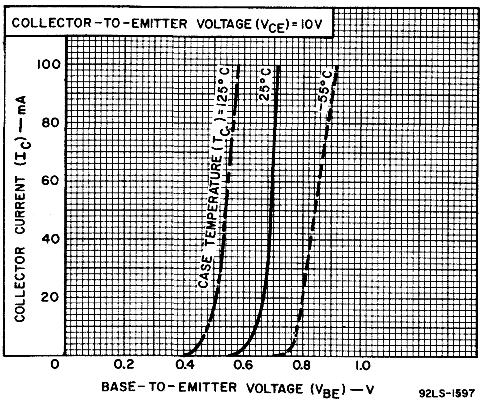


Fig.13—Typical transfer characteristics for all types.

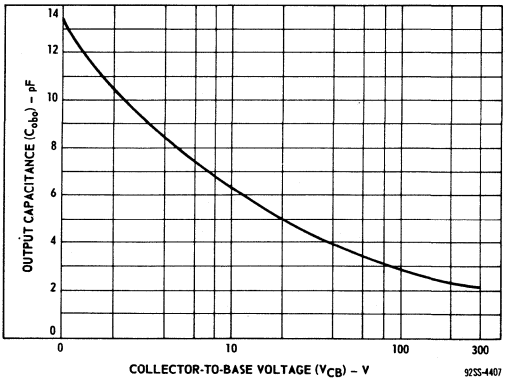


Fig.14—Typical output capacitance vs collector-to-base voltage for all types.

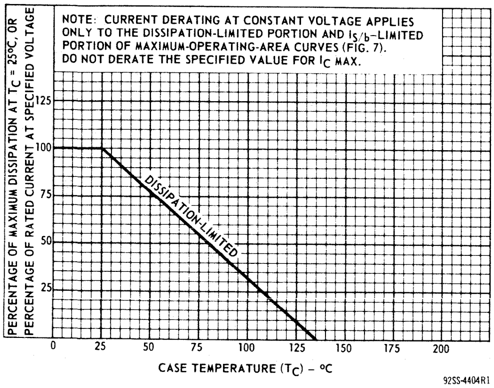


Fig.15—Dissipation derating curve for all types.

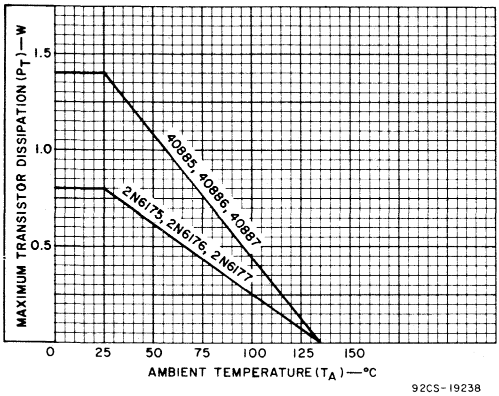


Fig.16—Dissipation derating curves for all types.

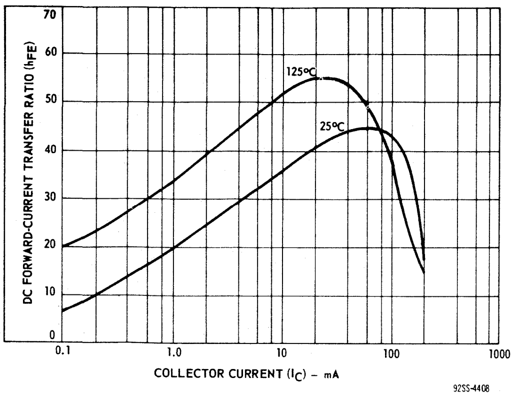
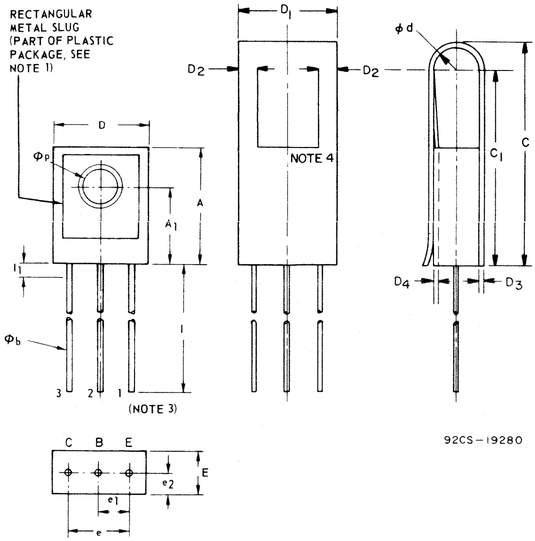


Fig.17—Typical DC-beta characteristics for all types.

DIMENSIONAL OUTLINE

"Plastic TO-5"



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.385	0.395	9.78	10.03	
A_1	0.251	0.261	6.37	6.63	
ϕb	0.016	0.019	0.41	0.48	2
C	0.858		21.79		
C_1	0.750		19.05		
D	0.305	0.315	7.75	8.00	
D_1	0.300		7.62		
D_2	0.070		1.77		
D_3	0.0329		0.813		
D_4	0.021	0.041	0.533	1.04	
ϕd	0.073	0.077	1.85	1.95	
E	0.145	0.155	3.68	3.94	
e	0.195	0.205	4.95	5.21	
e_1	0.095	0.105	2.41	2.67	
e_2	0.070	0.080	1.78	2.03	
ℓ	0.725	0.745	18.41	18.91	
ℓ_1	0.125	0.250	3.17	6.35	
ϕp	0.112	0.118	2.84	2.99	

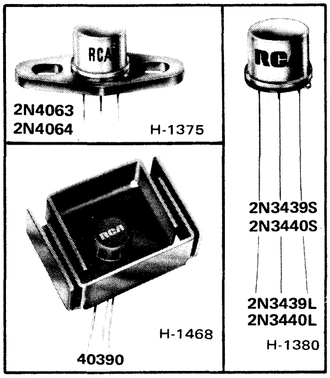
NOTE 1: To attach to heat-sink, use a 4-40 binding-head screw and a No. 4 flat washer. The recommended screw torque (for even distribution of mounting pressure and optimum thermal contact) is 6 in.-lb.
NOTE 2: Three leads. Leads are pretinned to the ℓ_1 dimension.
NOTE 3: Lead numbering from right to left with rectangular metal slug facing observer.
NOTE 4: Tab to be sheared through and set inward as shown.

TERMINAL CONNECTIONS

Lead 1 – Emitter
Lead 2 – Base
Lead 3 – Collector

Solid State
Division

Power Transistors
2N3439 2N3440 2N4063 2N4064 40390



High-Voltage Silicon N-P-N Transistors

For High-Speed Switching and Linear-Amplifier Applications

Features

- **High voltage ratings:**
  V_{CBO} = 450 V max. (2N3439, 2N4063)
  = 300 V max. (2N3440, 2N4064)
  V_{CEO}(sus) = 350 V max. (2N3439, 2N4063)
  = 250 V max. (2N3440, 2N4064)
- **Maximum-area-of-operation curves**
- **Low saturation voltages**

These devices are generally available with ½-inch leads (TO-39 package). They are also available in the U.S.A., Canada, Latin America, and Far East with 1½-inch leads (TO-5 package); the shorter-lead versions are specified by a suffix letter "S" after the type number, and the longer-lead versions by a suffix letter "L".

RCA-2N3439*, 2N3440**, 2N4063, 2N4064, and 40390 are epitaxial-base silicon n-p-n transistors with high breakdown voltages, high-frequency response, and fast switching speeds. These transistors are intended for industrial, commercial, and military equipment. Typical applications include high-voltage differential and operational amplifiers, high-voltage inverters, and high-voltage, low-current switching and series regulators.

The 2N3439 and the 2N3440 differ primarily in their voltage ratings; the 2N4063 and 2N4064 have the same voltage ratings as the 2N3439 and 2N3440 respectively, but employ a flange package. Type 40390 is a 2N3440 with a factory-attached heat radiator; it is intended for printed-circuit-board-applications.

* Formerly RCA Dev. No. TA2458.
** Formerly RCA Dev. No. TA2470.

Absolute-Maximum Values:		2N3439 2N4063	2N3440 2N4064 40390	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	450	300	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE	V_{CEO}(sus)	350	250	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	7	7	V
COLLECTOR CURRENT	I_C	1	1	A
BASE CURRENT	I_B	0.5	0.5	A
TRANSISTOR DISSIPATION	P_T			
At case temperatures up to 25° C		10	10(2N3440)	W
		–	10(2N4064)	W
At free-air temperatures up to 25° C		–	3.5(40390)	W
At free-air temperatures up to 50° C		1(2N3439)	1(2N3440)	W
At free-air temperatures above 25° C or 50° C		See Fig. 2.		
For pulse operation		See Fig. 9.		
TEMPERATURE RANGE:				
Storage & Operating (Junction)		← −65 to 200 →		°C
LEAD TEMPERATURE (During soldering):				
At distance ≥ 1/32 in. from seating plane for 10 s max.		← 255 →		°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C*

Characteristic	Symbol	TEST CONDITIONS: DC Collector Volts V_{CB}	V_{CE}	DC Emitter or Base Volts V_{EB}	V_{BE}	DC Current (milliamperes) I_C	I_E	I_B	LIMITS: Types 2N3439 2N4063 Min.	Max.	Types 2N3440 2N4064 40390 Min.	Max.	Units
Collector-Cutoff Current	I_{CEO}		300					0	-	20	-	-	µA
			200					0	-	-	-	50	µA
	I_{CEV}		450		-1.5				-	500	-	-	µA
			300		-1.5				-	-	-	500	µA
Emitter-Cutoff Current	I_{EBO}			6		0			-	20	-	20	µA
DC Forward-Current Transfer Ratio	h_{FE}		10			20			40	160	40	160	
			10			2			30	-	-	-	
Collector-to-Emitter Sustaining Voltage: *(See Figs. 3 & 4.)* With base open	$V_{CEO}(sus)$					50		0	350[a]	-	250[a]	-	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$					50		4	-	1.3	-	1.3	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					50		4	-	0.5	-	0.5	V
Small-Signal, Forward-Current Transfer Ratio (at 5 MHz)	h_{fe}		10			10			3	-	3	-	
Output Capacitance (at 1 MHz)	C_{ob}	10					0		-	10	-	10	pF
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$		200						50	-	50	-	mA
Thermal Resistance: Junction-to-Case	θ_{J-C}								-	17.5	-	17.5	°C/W

[a]**CAUTION:** The sustaining voltage $V_{CEO}(sus)$ **MUST NOT** be measured on a curve tracer. The sustaining voltage should be measured by means of the test circuit shown in Fig. 3.

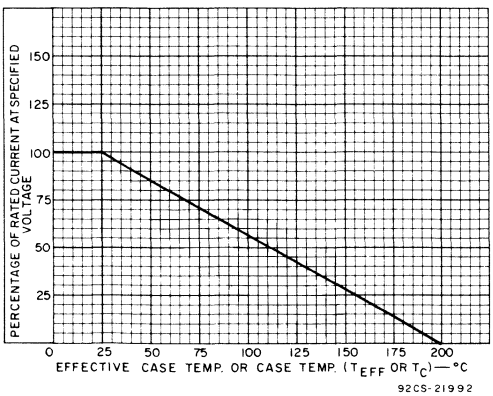


Fig. 1 – Current derating curve for all types.

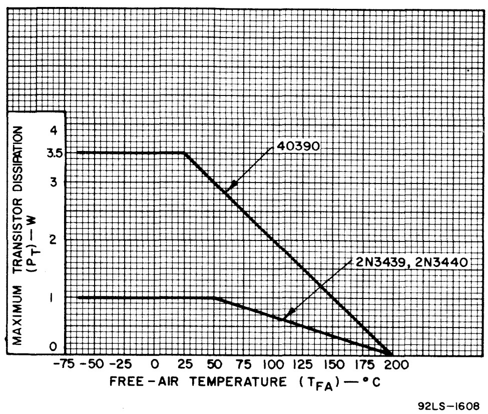


Fig. 2 – Dissipation derating curve for 2N3439, 2N3440, and 40390.

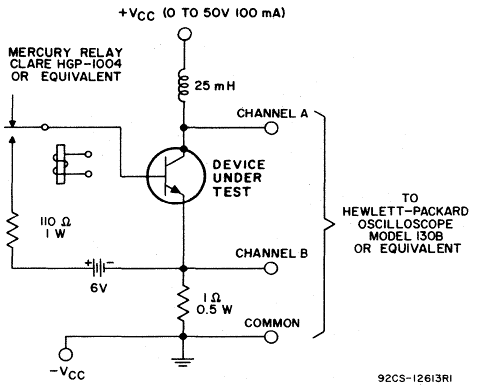
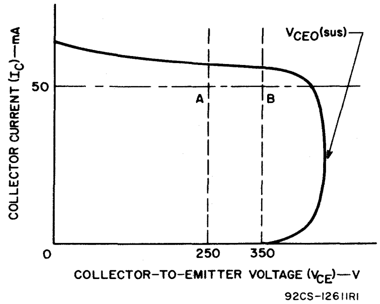


Fig. 3 – Circuit used to measure sustaining voltage, V_{CEO}(sus), for all types.



The sustaining voltage V_{CEO}(sus) is acceptable when the trace falls to the right and above point "A" for types 2N3440. 2N4064 and 40390. The trace must fall to the right and above point "B" for types 2N3439 and 2N4063.

Fig. 4 – Oscilloscope display for measurement of sustaining voltages (test circuit shown in Fig. 3).

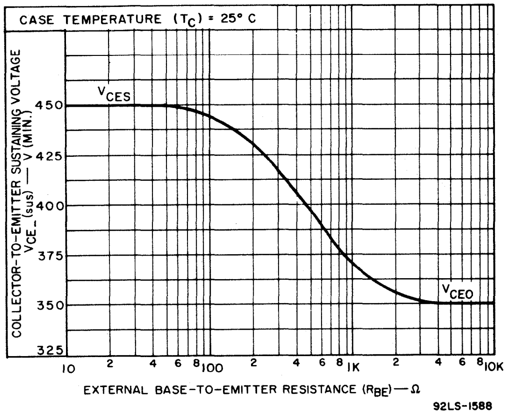


Fig. 5 – Sustaining voltage vs. base-to-emitter resistance for 2N3439 and 2N4063.

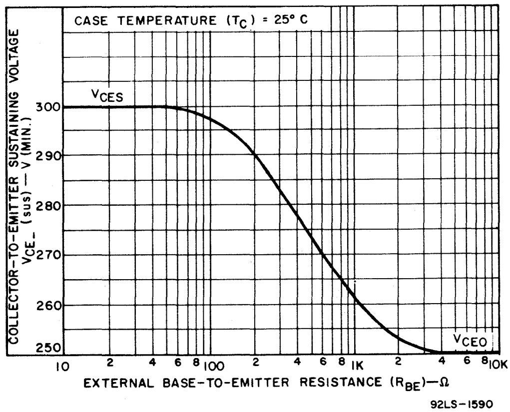


Fig. 6 – Sustaining voltage vs. base-to-emitter resistance for 2N3440, 2N4064, and 40390.

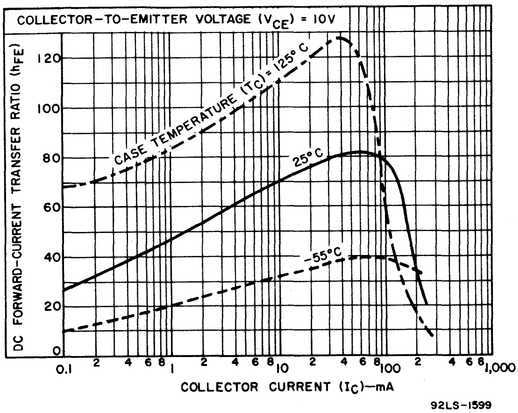


Fig. 7 – Typical dc-beta characteristics for all types.

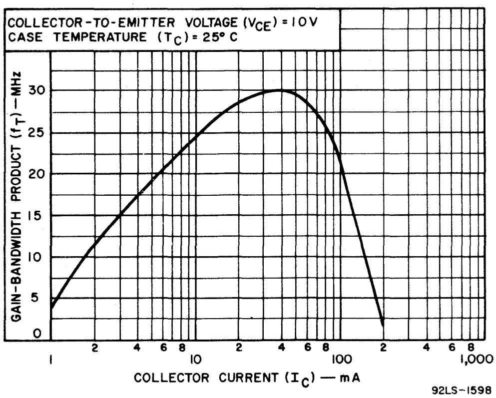


Fig. 8 – Typical gain-bandwidth product for all types.

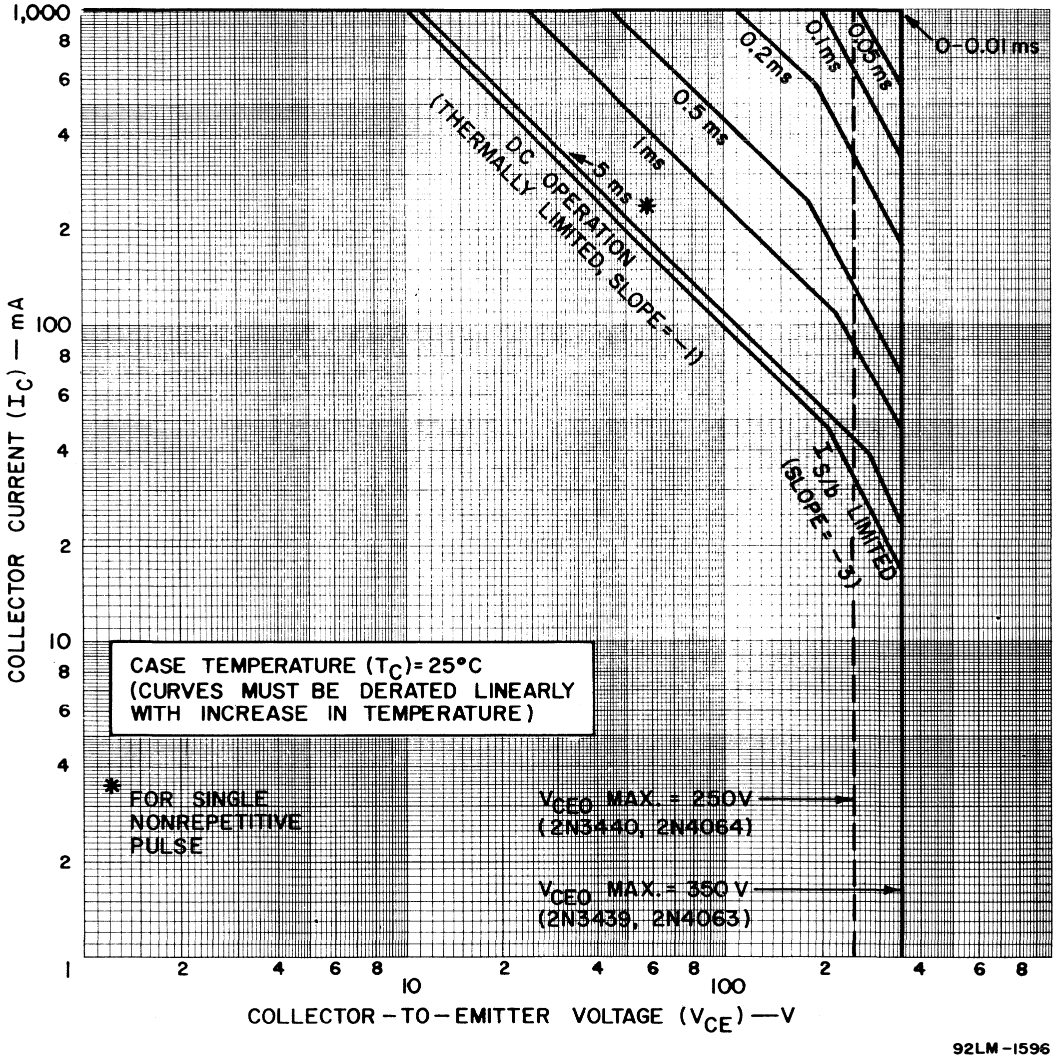


Fig. 9 – Maximum operating areas for 2N3439, 2N3440, 2N4063 and 2N4064.

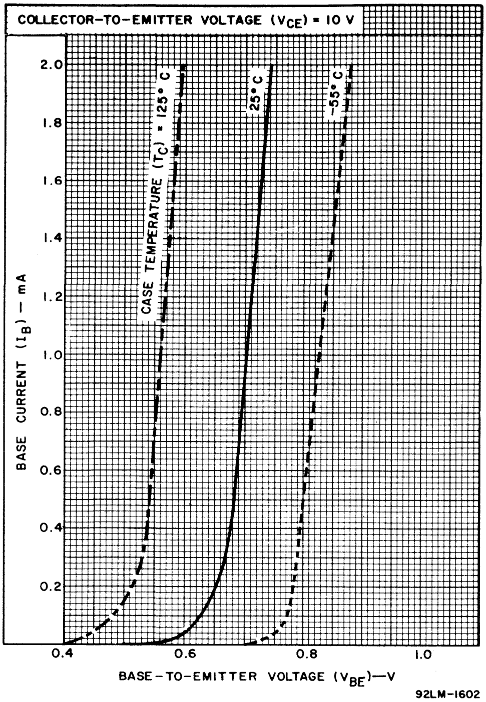


Fig. 10 — Typical input characteristics for all types.

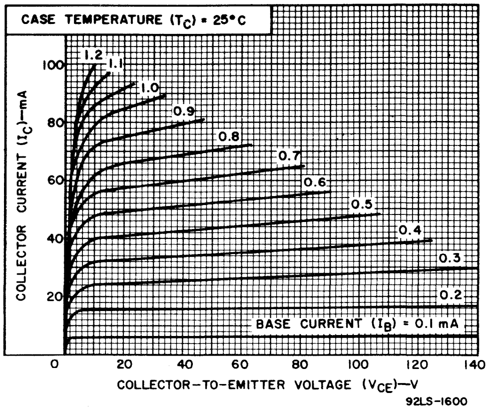


Fig. 11 — Typical output characteristics for all types.

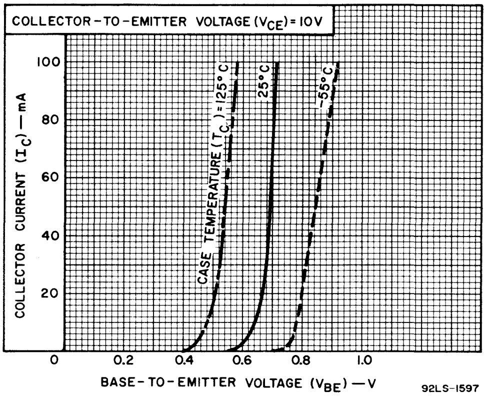
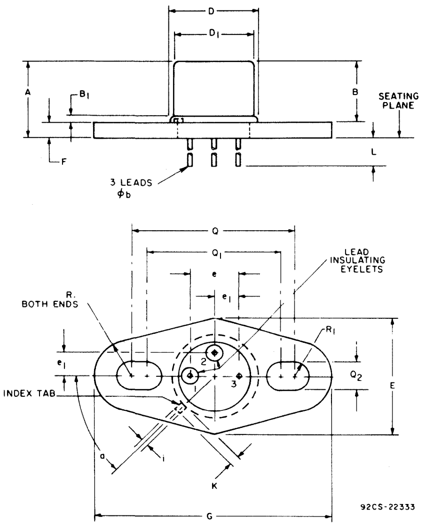


Fig. 12 — Typical transfer characteristics for all types.

DIMENSIONAL OUTLINE FOR 2N4063 AND 2N4064



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	0.328	–	8.33	
B	0.240	0.260	6.10	6.60	
B_1	0.009	0.125	0.229	3.18	
ϕ_b	0.016	0.019	0.406	0.483	
D	0.335	0.370	8.51	9.40	
D_1	0.305	0.335	7.75	8.51	
E	0.495	0.505	12.57	12.83	
e	0.200 T.P.		5.08 T.P.		1
e_1	0.100 T.P.		2.54 T.P.		1
F	0.062	0.068	1.57	1.74	
G	0.995	1.005	25.27	25.53	
i	0.028	0.034	0.711	0.864	
k	0.029	0.045	0.737	1.14	
L (long lead)	1.430	–	36.32	–	
L (short lead)	0.430	–	10.92	–	
Q	0.685	0.691	17.40	17.55	
Q_1	0.559	0.565	14.20	14.35	
Q_2	0.128	0.132	3.25	3.35	
R	0.156 T.P.		3.96 T.P.		1
R_1	0.064	0.066	1.63	1.67	
α	45° T.P.				1, 2

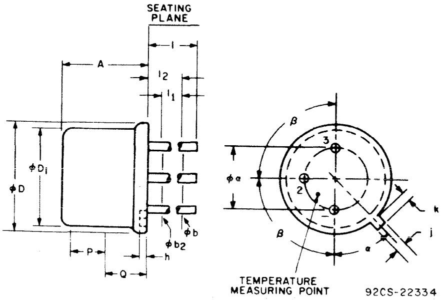
NOTES:

1. True position. 2. Tab centerline.

TERMINAL CONNECTIONS

Lead 1 — Emitter
Lead 2 — Base
Flange, Lead 3 — Collector

DIMENSIONAL OUTLINE FOR 2N3439 AND 2N3440



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
ϕa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
ϕb	0.016	0.021	0.406	0.533	2
ϕb_2	0.016	0.019	0.406	0.483	2
ϕD	0.350	0.370	8.89	9.40	
ϕD_1	0.305	0.335	8.00	8.51	
h	0.009	0.041	0.229	1.04	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
l {long lead	1.500		38.10		2
l {short lead	0.500		12.70		2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and l. Diameter is uncontrolled in l_1.

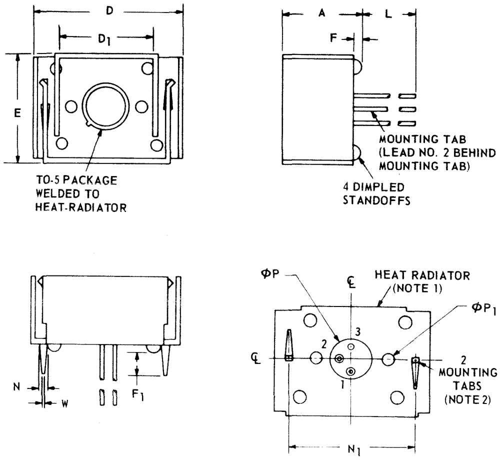
Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

TERMINAL CONNECTIONS

Lead 1 — Emitter
Lead 2 — Base
Case, Lead 3 — Collector

DIMENSIONAL OUTLINE FOR 40390



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	0.630	–	16.00	
D	1.205	1.235	30.61	31.37	
D_1	0.775	0.785	19.69	19.93	
E	0.875	0.905	22.22	22.99	
F	0.040	0.055	1.02	1.40	
F_1	0.160	0.195	4.06	4.95	
L {long lead	1.410	–	35.81	–	
L {short lead	0.410	–	10.41	–	
ϕP	0.295	0.305	7.493	7.747	
ϕP_1	0.093	0.095	2.362	2.413	
N	0.048	0.062	1.21	1.57	
N_1	0.998	1.002	25.349	25.450	3
W	0.048	0.052	1.219	1.320	

NOTES:

1. **0.035 C.R.S., finish—electroless nickel plate.**
2. **Recommended hole size for printed-circuit board is** 0.070 in. (1.78 mm) dia.
3. **Measured at bottom of heat-radiator.**

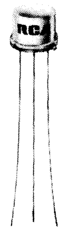
92CS-22335

TERMINAL CONNECTIONS

Lead 1 — Emitter
Lead 2 — Base
Heat-Radiator, Lead 3 — Collector

RCA Solid State Division

Power Transistors
2N5415
2N5416



JEDEC TO–5

H-1380

Silicon P-N-P High-Voltage Transistors

For High-Speed Switching and Linear-Amplifier Applications in Military, Industrial and Commercial Equipment

Features:

- **2N5415, 2N5416 — P–N–P Complements of: 2N3440, 2N3439**
- **Maximum safe-area-of-operation curves**
- **High voltage ratings:**
  V_{CBO} = −350 V max. (2N5416)
  V_{CEO}(sus) = −300 V max. (2N5416); −200 V max. (2N5415)

RCA-2N5415 and 2N5416* are silicon p-n-p transistors with high breakdown voltages, high frequency response, and fast switching speeds.

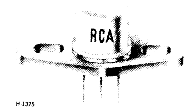
These transistors differ primarily in their voltage ratings.

In Europe, these devices are supplied in TO-39 packages, i.e., with 0.5-inch leads.

Typical applications include high-voltage differential and operational amplifiers; high-voltage inverters; and high-voltage, low-current switching and series regulators.

* Formerly RCA Dev. Types TA2819 and TA2819A, respectively.

ALSO AVAILABLE . . .



H-1375

Types 2N5415 and 2N5416 are also available with a factory-attached mounting flange.

Please submit requirements to your RCA Technical Sales Representative, or write to RCA Low-Frequency Transistor Marketing, Somerville, N.J. 08876.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	2N5415	2N5416	
*COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	−200	−350	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:			
* With base open, V_{CEO}(sus)	−200	−300	V
With external base-to-emitter resistance (R_{BE}) = 50Ω, V_{CER}(sus)	−	−350	V
*EMITTER-TO-BASE VOLTAGE, V_{EBO}	−4	−6	V
*COLLECTOR CURRENT, I_C	−1	−1	A
*BASE CURRENT, I_B	−0.5	−0.5	A
*TRANSISTOR DISSIPATION, P_T			
At case temperatures up to 25°C	10	10	W
At case temperatures above 25°C	*See Figs. 1 & 2.*		
At ambient temperatures up to 50°C	1	1	W
At ambient temperatures above 50°C	Derate linearly at 6.7		mW/°C
*TEMPERATURE RANGE:			
Storage & Operating (Junction)	−65 to +200		°C
*LEAD TEMPERATURE (During Soldering):			
At distance ≥1/32 in. (0.8 mm) from seating plane for 10s max.	255		°C

*In accordance with JEDEC registration data format (JS–9 RDF–8)

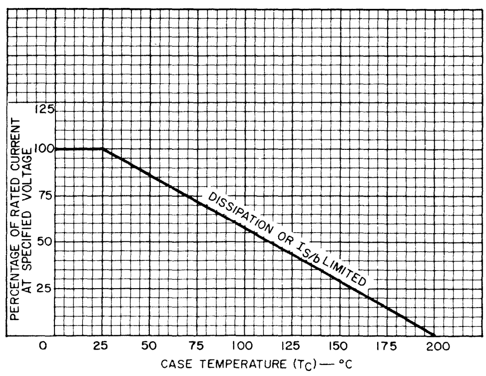


Fig. 1 - Dissipation derating curve

92LS-1469R1

ELECTRICAL CHARACTERISTICS, *Case Temperature* $(T_C) = 25^oC$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS							LIMITS				UNITS
		DC Collector Voltage (V)		DC Emitter or Base Voltage (V)		DC Current (mA)			Type 2N5415		Type 2N5416		
		V_{CB}	V_{CE}	V_{EB}	V_{BE}	I_C	I_E	I_B	Min.	Max.	Min.	Max.	
Collector-Cutoff Current: With base open	I_{CEO}		−250					0	–	–	–	−50	µA
			−150					0	–	−50	–	–	
* With emitter open	I_{CBO}	−280						0	–	–	–	−50	µA
		−175						0	–	−50	–	–	
* With base-emitter junction reverse-biased	I_{CEV}		−300		1.5				–	–	–	−50	µA
			−200		1.5				–	−50	–	–	
* Emitter-Cutoff Current	I_{EBO}			−6		0			–	–	–	−20	µA
				−4		0			–	−20	–	–	
* DC Forward-Current Transfer Ratio	h_{FE}		−10			−50			–	–	30	120	
			−10			−50			30	150	–	–	
Collector-to-Emitter Sustaining Voltage: With base open *(See Fig. 3 & 4)*	$V_{CEO}(sus)$					−50		0	−200[a]	–	−300[a]	–	V
With external base-to-emitter resistance (R_{BE}) = 50 Ω	$V_{CER}(sus)$					−50			–	–	−350[a]	–	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$		−10			−50			–	−1.5	–	−1.5	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					−50		5	–	−2.5	–	−2	V
* Common-Emitter, Small-Signal, Short-Circuit, Forward-Current Transfer Ratio (at 1 kHz)	h_{fe}		−10			−5			25	–	25	–	
* Magnitude of Common-Emitter, Small-Signal, Short-Circuit Forward-Current Transfer Ratio (at 5 MHz)	$\|h_{fe}\|$		−10			−10			3	–	3	–	
* Real Part of Common-Emitter Small-Signal, Short-Circuit Impedance (at 1 MHz)	$Re(h_{ie})$		-10			−5			–	300	–	300	Ω
* Common-Base, Short-Circuit, Input Capacitance (at 1 MHz)	C_{ib}			−5		0			–	75	–	75	pF
Output Capacitance (at 1 MHz)	C_{ob}	−10					0		–	15	–	15	pF
Second-Breakdown[b] Collector Current: With base forward biased[c]	$I_{S/b}$[d]		−100						−100	–	−100	–	mA
Thermal Resistance: (Junction-to-Case)	θ_{J-C}								–	17.5	–	17.5	°C/W

[a] CAUTION: The sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$ MUST NOT be measured on a curve tracer. The sustaining voltage should be measured by means of the test circuit shown in Fig. 3.

[b] Regions for safe-operation with forward bias are shown in Fig. 2.

[c] Specified value of $I_{S/b}$ for given value of V_{CE} as base voltage is increased from zero in a positive direction.

[d] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage.

* In accordance with JEDEC registration data format (JS-9 RDF-3)

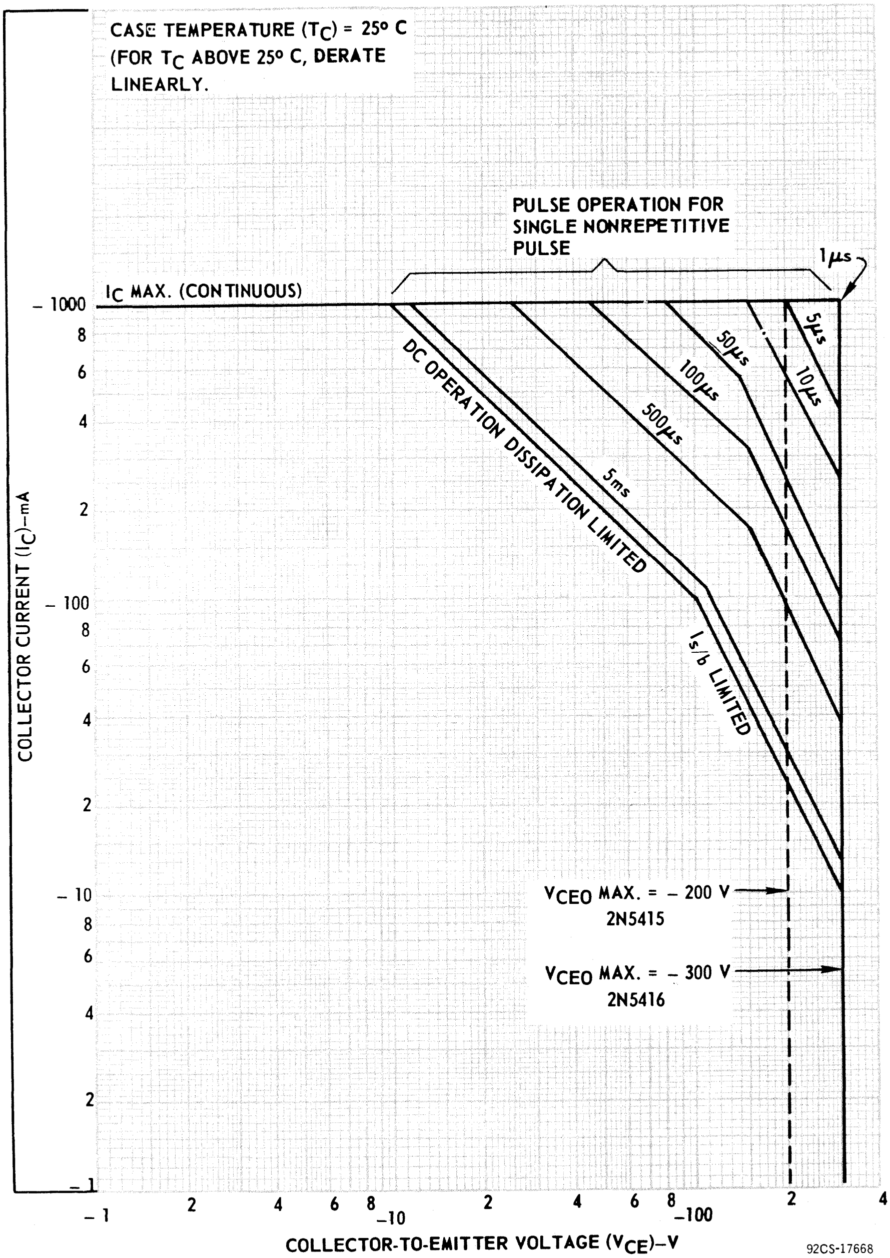


Fig. 2 - Maximum safe operating areas

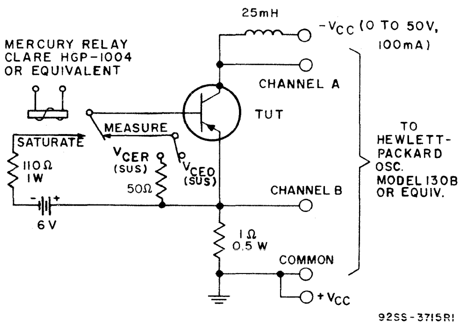
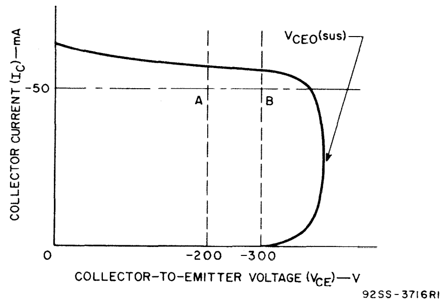


Fig. 3 - Circuit used to measure sustaining voltages, V_{CEO}(sus) and V_{CER}(sus) for both types



The sustaining voltage V_{CEO} (sus) is acceptable when the trace falls to the right and above point "A" for type 2N5415. The trace must fall to the right and above point "B" for type 2N5416.

Fig. 4 - Oscilloscope display for measurement of sustaining voltages (test circuit shown in Fig. 3)

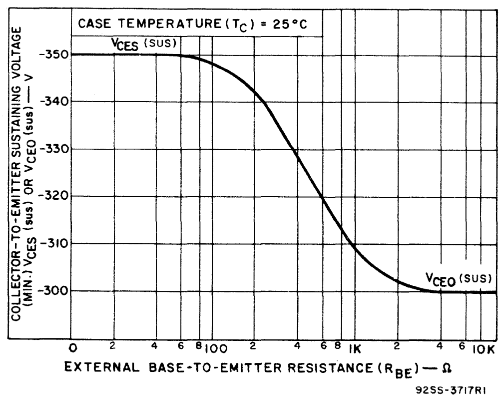


Fig. 5 - Sustaining voltage vs. base-to-emitter resistance for type 2N5416

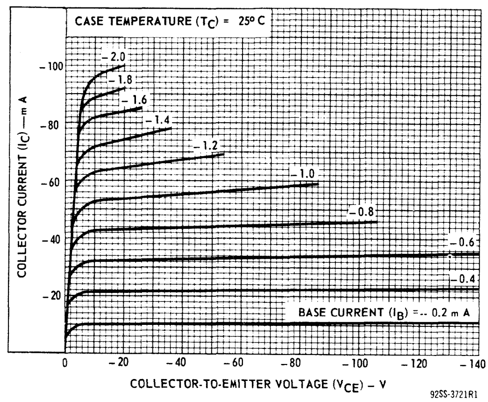


Fig. 6 - Typical output characteristics for both types

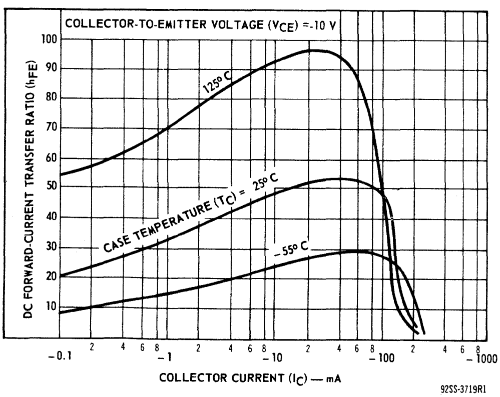


Fig. 7 - Typical dc beta for both types

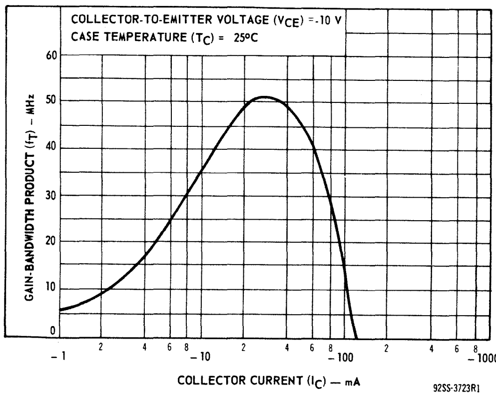


Fig. 8 - Typical gain-bandwidth product for both types

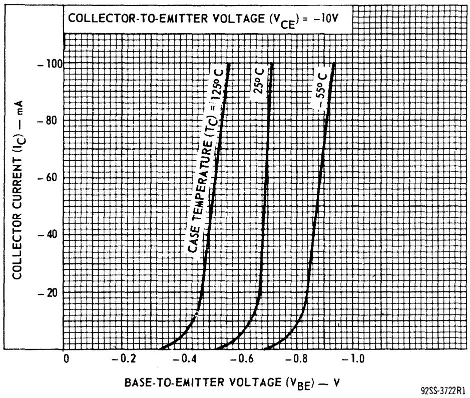


Fig. 9 - Typical transfer characteristics for both types

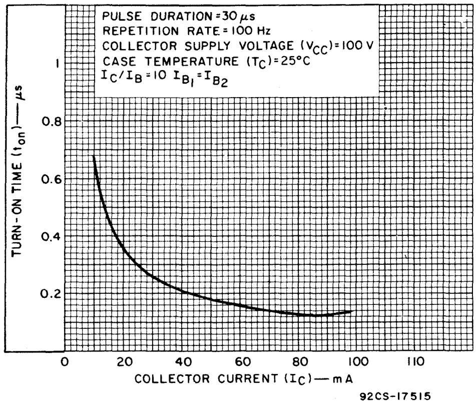


Fig. 11 - Typical turn-on time characteristic for both types

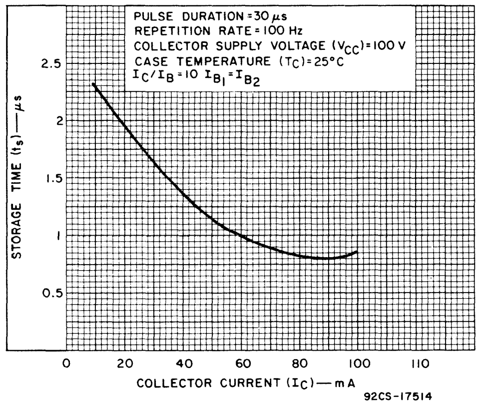


Fig. 12 - Typical storage-time characteristic for both types

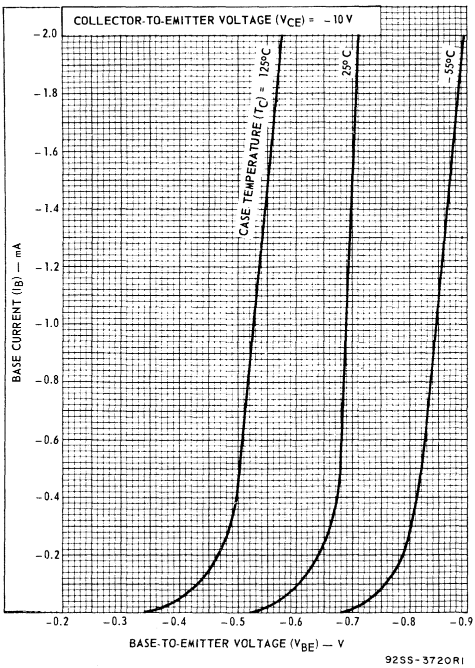


Fig. 10 - Typical input characteristics for both types

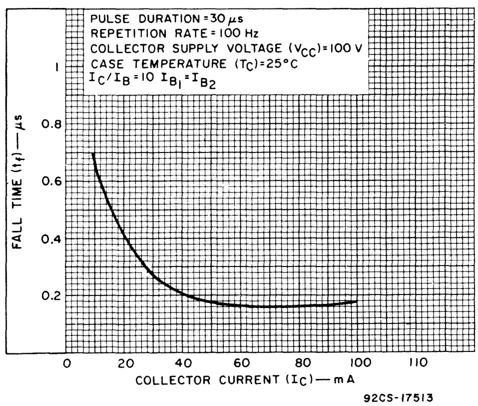


Fig. 13 - Typical fall-time characteristic for both types

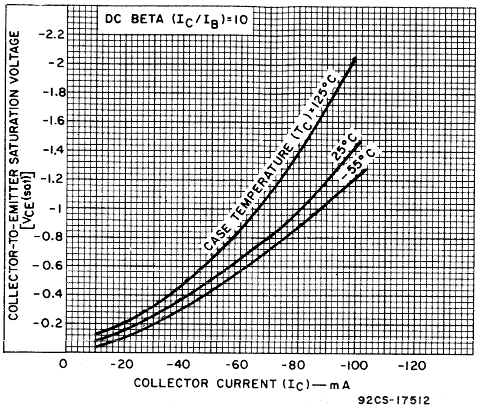
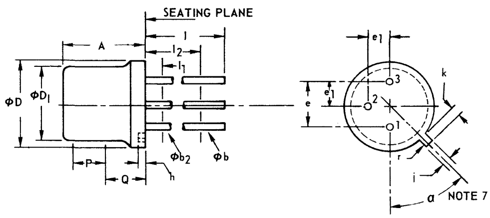


Fig. 14 - Typical collector-to-emitter saturation voltage for both types

DIMENSIONAL OUTLINE
JEDEC TO–5



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.240	0.260	6.10	6.60	
φb	0.016	0.021	0.406	0.533	2
$φb_2$	0.016	0.019	0.406	0.483	2
φD	0.335	0.370	8.51	9.40	
$φD_1$	0.305	0.335	7.75	8.51	
e	0.200 T.P.		5.08 T.P.		4, 5
e_1	0.100 T.P.		2.54 T.P.		5
h	0.009	0.125	0.229	3.18	
i	0.028	0.034	0.711	0.864	5
k	0.029	0.045	0.737	1.14	3, 5
l	1.500	–	38.10	—	2
l_1	–	0.050	–	1.27	2
l_2	0.250	–	6.35	–	2
P	0.100	–	2.54	–	1
Q	–	–	–	–	6
r	–	0.007	–	0.179	
α	45° T. P.		–		5, 7

NOTES:

1. This zone is controlled for automatic handling. The variation in actual diameter within the zone shall not exceed 0.010 in. (0.254 mm).
2. (Three leads) $φb_2$ applies between l_1 and l_2. φb applies between l_2 and 1.5 in. (38.20 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond 1.5 in. (38.10 mm) from seating plane.
3. Measured from maximum diameter of the actual device.
4. Leads having maximum diameter 0.019 in. (0.483 mm) measured in gaging plane 0.054 in. (1.37 mm) + 0.001 in. (0.25 mm) – 0.000 in. (0.000 mm) below the seating plane of the device shall be within 0.007 in. (0.178 mm) of their true positions relative to the maximum-width tab.
5. The device may be measured by direct methods or by the gage and gaging procedure described on gage drawing GS-1.
6. Details of outline in this zone optional.
7. Tab centerline.

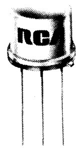
92SS-3821

TERMINAL CONNECTIONS

Lead 1 – Emitter
Lead 2 – Base
Case, Lead 3 – Collector

Solid State
Division

Power Transistors
Preliminary Data
BFT19 BFT19A BFT19B



JEDEC TO-39 H-1381

Silicon P-N-P High-Voltage Transistors

For High-Speed Switching and Linear-Amplifier Applications in Military, Industrial and Commercial Equipment

Features:

- **Maximum safe-area-of-operation curves**
- **High voltage ratings:**
  V_{CBO} = −400 V max. (BFT19B); −300 V max. (BFT19A); −200 V max. (BFT19)
  V_{CEO}(sus) = −350 V max. (BFT19B); −250 V max. (BFT19A); −150 V max. (BFT19)

RCA-BFT19, BFT19A, and BFT19B are silicon p-n-p transistors with high breakdown voltages, high frequency response, and fast switching speeds. These transistors differ in their voltage ratings.

Typical applications include high-voltage differential and operational amplifiers; high-voltage inverters, and high-voltage, low-current switching and series regulators.

MAXIMUM RATINGS, *Absolute-Maximum Values:*		BFT19	BFT19A	BFT19B	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	−200	−300	−400	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:					
With base open	V_{CEO}(sus)	−150	−250	−350	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}(sus)	−200	−300	−400	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	−5	−5	−5	V
COLLECTOR CURRENT (Continuous)	I_C	−1	−1	−1	A
BASE CURRENT (Continuous)	I_B	−0.5	−0.5	−0.5	A
TRANSISTOR DISSIPATION:	P_T				
At case temperatures up to 25°C		5	5	5	W
At case temperatures above 25°C		See Figs. 1 & 4.			
At ambient temperatures up to 25°C		1	1	1	W
At ambient temperatures above 25°C		Derate linearly at 5.7 mW/°C			
TEMPERATURE RANGE:					
Storage and Operating (Junction)		←— −65 to 200 —→			°C
PIN TEMPERATURE (During Soldering):					
At distance ⩾ 1/32 in. (0.8 mm) from case for 10 s max.		←— 255 —→			°C

10-73

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS						LIMITS						UNITS
		VOLTAGE V dc			CURRENT mA			BFT19		BFT19A		BFT19B		
		V_{CB}	V_{CE}	V_{EB}	I_C	I_E	I_B	Min.	Max.	Min.	Max.	Min.	Max.	
Collector-Cutoff Current: With emitter open	I_{CBO}	−100 −200 −300					0 0 0	— — —	−100 — —	— — —	— −100 —	— — —	— — −100	μA
Emitter-Cutoff Current	I_{EBO}			−5	0			—	−100	—	−100	—	−100	μA
DC Forward-Current Transfer Ratio	h_{FE}		−10 −10 −10		−10 −30 −50			20 25 20	— — —	20 25 20	— — —	20 25 20	— — —	
Collector-to-Emitter Sustaining Voltage (*See Figs. 2 and 3*): With base open	$V_{CEO}(sus)$				−10		0	−150[a]	—	−250[a]	—	−350[a]	—	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$				−10			−200[a]	—	−300[a]	—	−400[a]	—	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$				−30		−3	—	−1.8	—	−1.8	—	−1.8	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				−10 −30		−1 −3	— —	−1 −2.5	— —	−1 −2.5	— —	−1 −2.5	V
Common-Emitter, Small-Signal, Short-Circuit, Forward-Current Transfer Ratio (at 1 kHz)	h_{fe}		−10		−5			25	—	25	—	25	—	
Magnitude of Common-Emitter, Small-Signal, Short-Circuit Forward-Current Transfer Ratio (at 5 MHz)	$\|h_{fe}\|$		−10		−30			5	—	5	—	5	—	
Common-Base, Short-Circuit, Input Capacitance (at 1 MHz)	C_{ib}			−5	0			—	75	—	75	—	75	pF
Output Capacitance (at 1 MHz)	C_{ob}	−10				0		—	15	—	15	—	15	pF
Second-Breakdown[b] Collector Current: With base forward biased[c]	$I_{S/b}$[d]	−100						−50	—	−50	—	−50	—	mA
Thermal Resistance: (Junction-to-Case)	$R_{\theta JC}$							—	35	—	35	—	35	°C/W

[a] CAUTION: The sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$ MUST NOT be measured on a curve tracer. The sustaining voltage should be measured by means of the test circuit shown in Fig. 2.

[b] Regions for safe-operation with forward bias are shown in Fig. 1.

[c] Specified value of $I_{S/b}$ for given value of V_{CE} as base voltage is increased from zero in a positive direction.

[d] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage.

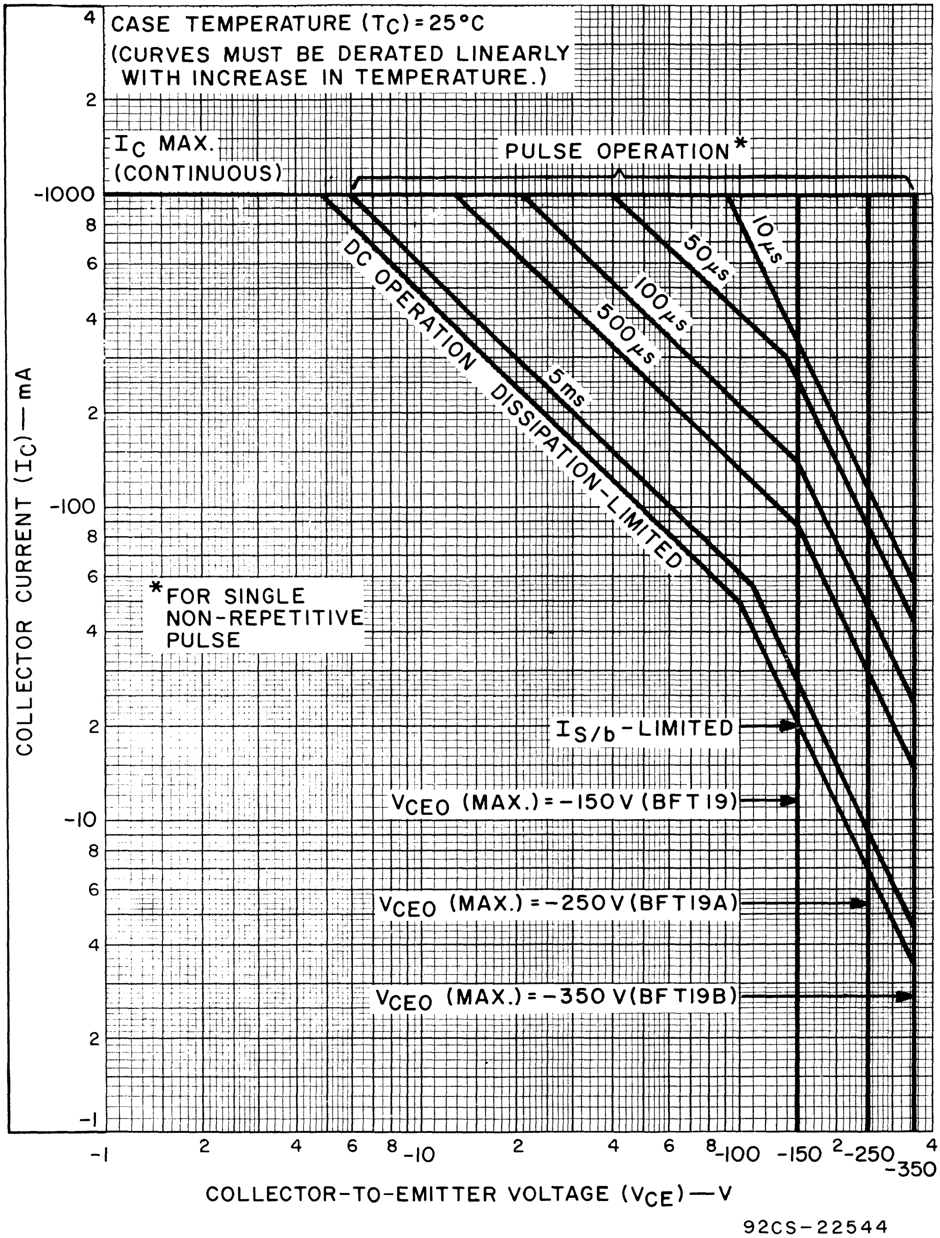


Fig. 1 — Maximum operating areas for all types.

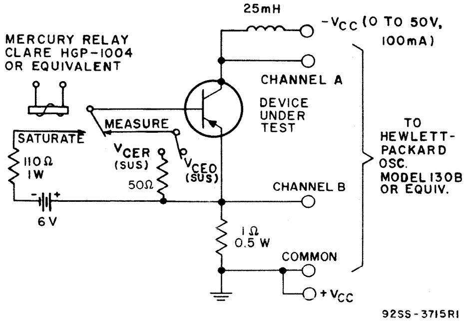
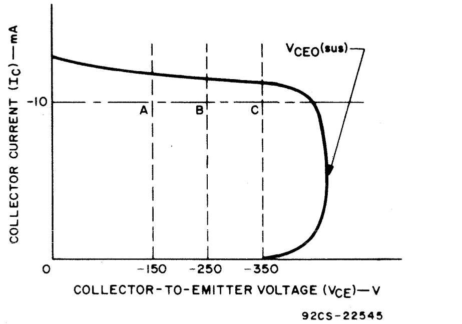


Fig. 2 – Circuit used to measure sustaining voltages, $V_{CEO}(sus)$ and $V_{CER}(sus)$.



The sustaining voltage V_{CEO}(sus) is acceptable when the trace falls to the right and above point "A" for type BFT19. The trace must fall to the right and above point "B" for type BFT19A, and point "C" for BFT19B.

Fig. 3 – Oscilloscope display for measurement of sustaining voltages (test circuit shown in Fig. 2).

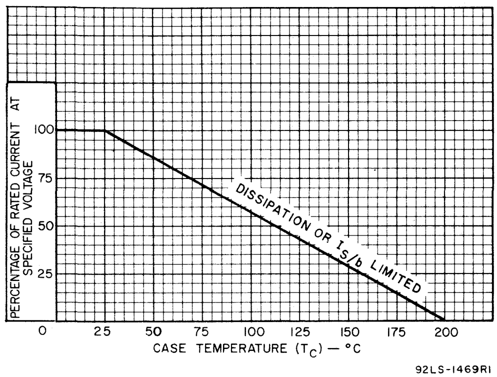


Fig. 4 – Dissipation derating curve.

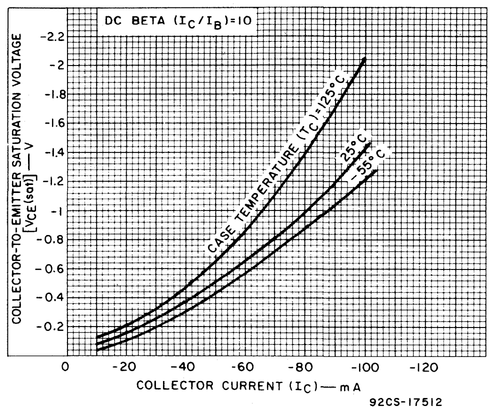


Fig. 5 – Typical collector-to-emitter saturation voltage.

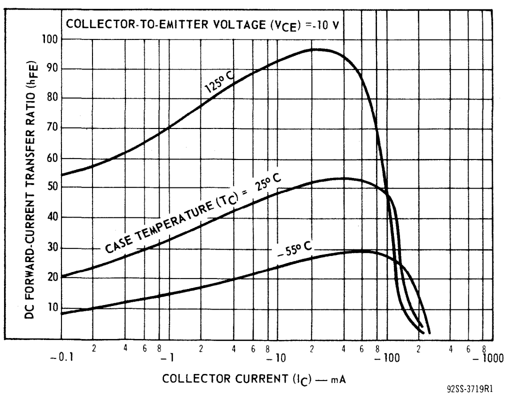


Fig. 6 – Typical dc beta characteristics.

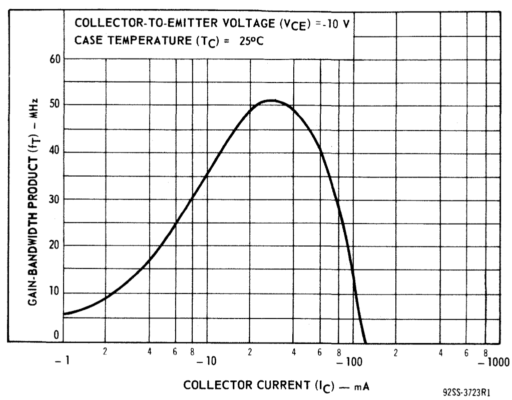


Fig. 7 – Typical gain-bandwidth product.

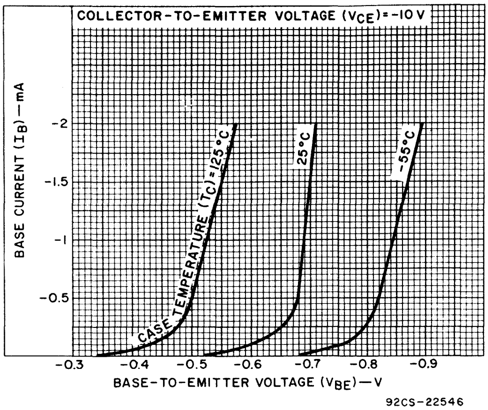


Fig. 8 — Typical input characteristics.

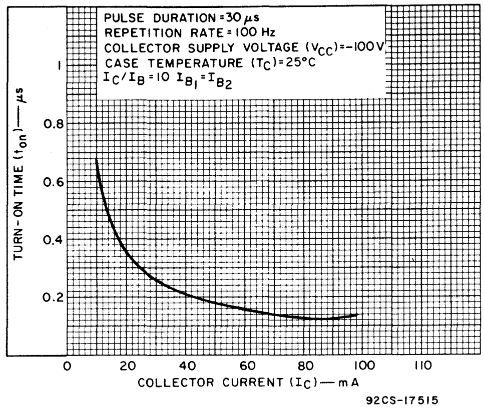


Fig. 9 — Typical turn-on time characteristic.

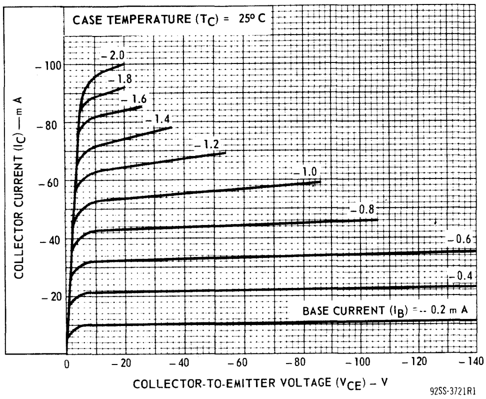


Fig. 10 — Typical output characteristics.

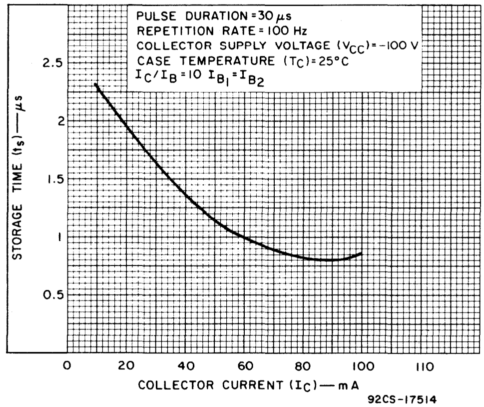


Fig. 11 — Typical storage-time characteristic.

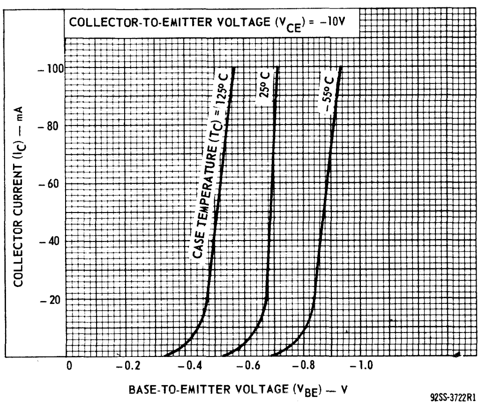


Fig. 12 — typical transfer characteristics.

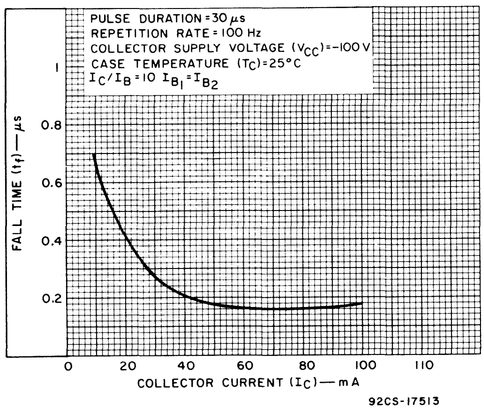
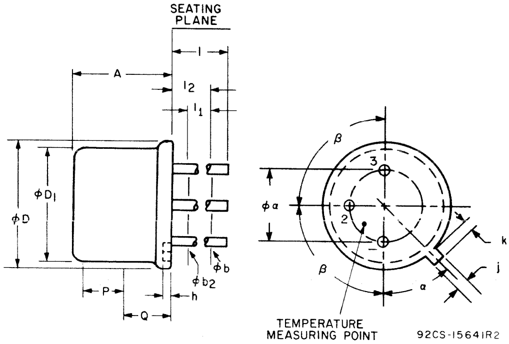


Fig. 13 — Typical fall-time characteristic.

DIMENSIONAL OUTLINE FOR ALL TYPES
JEDEC TO-39



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
φa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
φb	0.016	0.021	0.406	0.533	2
φb2	0.016	0.019	0.406	0.483	2
φD	0.350	0.370	8.89	9.40	
φD1	0.315	0.335	8.00	8.51	
h	0.009	0.125	0.229	3.18	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
l	0.500		12.70		2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads) ϕ b_2 applies between l_1 and l_2. ϕb applies between l_2 and 0.5 in. (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond 0.5 in. (12.70 mm) from seating plane.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

TERMINAL CONNECTIONS

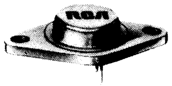
Lead 1 — Emitter

Lead 2 — Base

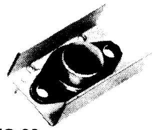
Lead 3 — Collector, Case

RCA Solid State Division

Power Transistors
2N3583-2N3585 40374, 2N4240



JEDEC TO-66 H-1340



JEDEC TO-66 With Integral Heat Radiator H-1470A

High-Voltage Silicon N-P-N Transistors

For High-Speed Switching and Linear-Amplifier Applications

Features

- **100-percent tested to assure freedom from second breakdown in both forward- and reverse-bias conditions when operated within specified limits**
- **JEDEC TO-66 package for 2N3583, 2N3584, 2N3585, and 2N4240**
- **JEDEC TO-66 package with heat radiator for 40374**
- **Economy types for ac/dc circuits**
- **Fast turn-on time at high collector current**

RCA-2N3583,• 2N3584,• 2N3585,• 2N4240,• and 40374 are silicon n-p-n transistors with high breakdown voltages and fast switching speeds.

Type 40374 is a 2N3583 with a factory-attached heat radiator to increase the free-air dissipation rating. This device is intended for those applications which require a power transistor for mounting on a printed-circuit board. Tabs are provided on the underside of the radiator for mounting purposes and making electrical connection to the collector.

Typical applications for these transistors include high-voltage operational amplifiers, high-voltage switches, switching regulators, converters, inverters, deflection- and hi-fi amplifiers.

These transistors are also intended for a wide variety of applications in ac/dc commercial equipment.

Heat-radiator versions of types 2N3584, 2N3585, and 2N4240 can also be supplied on special order.

•Formerly Dev. Nos. TA2510, TA2511, TA2512, and TA2871, respectively.

MAXIMUM RATINGS, *Absolute-maximum values:*

		2N3583	2N3584	2N3585 2N4240	40374	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	250	375	500	250	V
*COLLECTOR-TO-EMITTER VOLTAGE, sustaining	$V_{CEO}(sus)$	175	250	300	175	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	6	6	6	6	V
*CONTINUOUS COLLECTOR CURRENT	I_C	1	2	2	2	A
*PEAK COLLECTOR CURRENT		5	5	5	5	A
*CONTINUOUS BASE CURRENT	I_B	1	1	1	1	A
*TRANSISTOR DISSIPATION	P_T					
At case temperature (T_C) = 25°C		35	35	35	35	W
At case temperatures above 25°C		Derate linearly at 0.2 W/°C				
For other conditions		See Figs. 7, 8, 9, 21, 22, & 23				
*TEMPERATURE RANGE:						
Storage & Operating (Junction)		←—— -65 to 200 ——→				°C
*PIN TEMPERATURE:						
1/16 in. (1.58 mm) from seating plane for 10 s max.		235	235	235	235	°C

*In accordance with JEDEC registration data format JS-6 RDF-2 (2N3583), JS-6 RDF-1 (2N3584, 2N3585, 2N4240)

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ELECTRICAL CHARACTERISTICS *at Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: DC COLLECTOR VOLTAGE–V		DC EMITTER OR BASE VOLTAGE–V		DC CURRENT mA			LIMITS: TYPES 2N3583 & 40374		TYPE 2N3584		TYPE 2N3585		TYPE 2N4240		UNITS
		V_{CB}	V_{CE}	V_{EB}	V_{BE}	I_C	I_E	I_B	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
* Collector-Cutoff Current	I_{CEO}		150					0	–	10	–	5	–	5	–	5	mA
* Collector-Cutoff Current	I_{CEX}		225		–1.5				–	1.0	–	–	–	–	–	–	mA
			340		–1.5				–	–	–	1.0	–	–	–	–	
			450		–1.5				–	–	–	–	–	1.0	–	2.0	
At T_C = 150°C	I_{CEX}		225		–1.5				–	3	–	–	–	–	–	–	mA
			300		–1.5				–	–	–	3	–	3	–	5.0	
* Emitter-Cutoff Current	I_{EBO}			6		0			–	5.0	–	0.5	–	0.5	–	0.5	mA
* DC Forward-Current Transfer Ratio	h_{FE}		2			750			–	–	–	–	–	–	10	100	
			2			1 A			–	–	8	80	8	80	–	–	
			10			100			40	–	40	–	40	–	40	–	
			10			500			40	200	–	–	–	–	–	–	
			10			750			–	–	–	–	–	–	30	150	
			10			1 A			10	–	25	100	25	100	–	–	
Collector-to-Emitter Sustaining Voltage: (See Figs. 1, 2, & 12) * With base open	$V_{CEO}(sus)$					200		0	175●	–	250●	–	300●	–	300●	–	V
With external base-to-emitter resistance (R_{BE}) = 50Ω	$V_{CER}(sus)$					200			250●	–	300●	–	400●	–	400●	–	V
* Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$					750		75	–	–	–	–	–	–	–	1.8	V
						1 A		100	–	1.4	–	1.4	–	1.4	–	–	
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					750		75	–	–	–	–	–	–	–	1.0	V
						1 A		125	–	5	–	0.75	–	0.75	–	–	
Small-Signal Forward Current Transfer Ratio f = 5 MHz	h_{fe}		10			200			3	–	3	–	3	–	3	–	
* f = 1 kHz			30			100			25	350	–	–	–	–	–	–	
* Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio f = 5 MHz	$\|h_{fe}\|$		10			200			2	–	2	–	2	–	3	–	
Output Capacitance (f = 1 MHz)	C_{obo}	10					0		–	120	–	120	–	120	–	120	pF
Second-Breakdown Collector Current with base forward-biased** (See Figs. 22 & 23)	$I_{S/b}$▲		100						350	–	350	–	350	–	350	–	mA
Second-Breakdown Energy with base reverse-biased R_{BE} = 20Ω, L = 100 μH	$E_{S/b}$†				–4				50	–	200	–	200	–	50	–	μJ
* Saturated Switching Time: Rise Time (See Figs. 13, 16, 17, & 18)	t_r	(V_{CC}) 200				1 A		100	–	–	–	3	–	3	–	–	μs
						750		75	–	–	–	–	–	–	–	0.5	
Storage Time (See Figs. 14, 16, 17, & 18)	t_s	(V_{CC}) 200				1 A		100	–	–	–	4	–	4	–	–	μs
						750		75	–	–	–	–	–	–	–	6	
Fall Time (See Figs. 15, 16, 17, & 18)	t_f	(V_{CC}) 200				750		75	–	–	–	–	–	–	–	3	μs
						1 A		100	–	–	–	3	–	3	–	–	
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$								5(Max.) 2N3583		–	5	–	5	–	5	°C/W
Junction-to-Ambient	$R_{\theta JA}$								70 (Max.) 2N3583		–	70	–	70	–	70	°C/W
									30 (Max.) 40374		–	–	–	–	–	–	

*In accordance with JEDEC registration data format JS-6 RDF-2 (2N3583), JS-6 RDF-1 (2N3584, 2N3585, 2N4240)

● **CAUTION**: The sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$ **MUST NOT** be measured on a curve tracer. These sustaining voltages should be measured by means of the test circuit shown in Fig. 1.

▲ $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage.

** Specified value of $I_{S/b}$ for given value of V_{CE} as base voltage is increased from zero in a positive direction.

† $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse bias conditions. $E_{S/b} = 1/2\ LI^2$, where L is a series load or leakage inductance and I is the peak collector current from Figs. 3, 4, and 5.

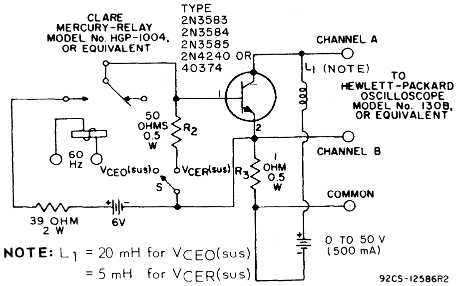


Fig. 1—Circuit used to measure sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$ for all types.

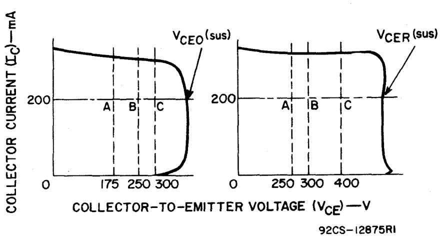


Fig. 2—Oscilloscope display for measurement of sustaining voltages (test circuit shown in Fig. 1).

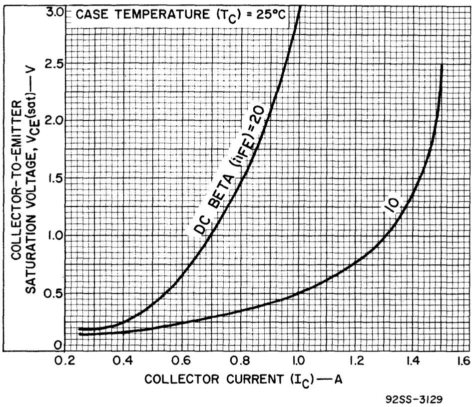


Fig. 3—Typical collector-to-emitter saturation voltage vs. current for types 2N3584 and 2N3585.

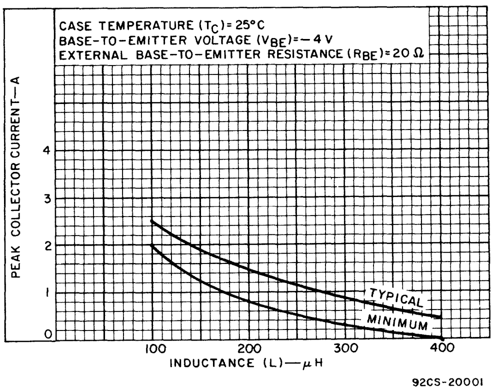


Fig. 4—Reverse-bias second breakdown characteristics for types 2N3584 and 2N3585.

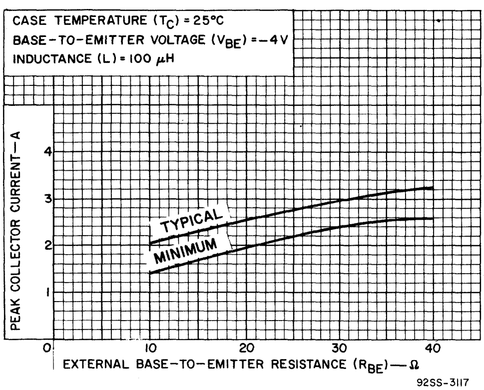


Fig. 5—Reverse-bias second breakdown characteristics for types 2N3584 and 2N3585.

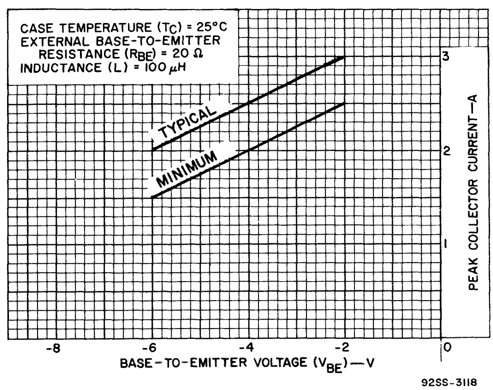


Fig. 6—Reverse-bias second breakdown characteristics for types 2N3584 and 2N3585.

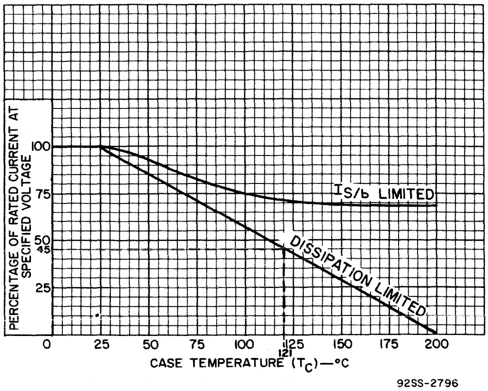


Fig.7—Dissipation derating curves for all types.

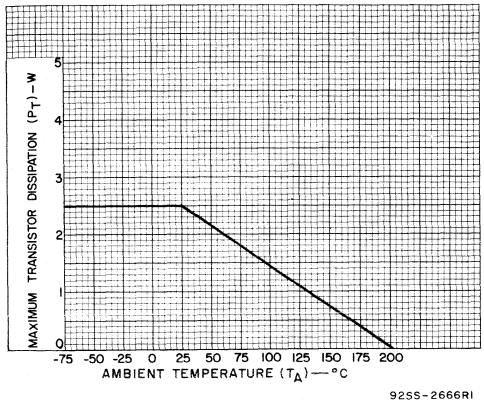


Fig. 8—Dissipation derating curve for types 2N3583, 2N3584, 2N3585, and 2N4240.

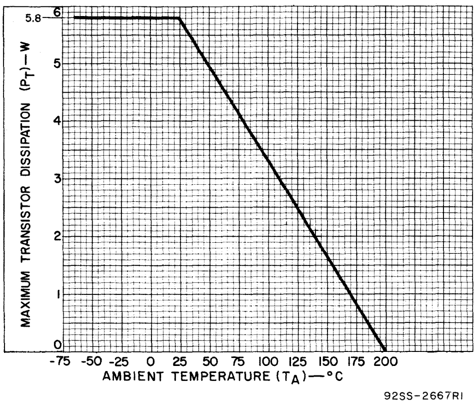


Fig. 9—Dissipation derating curve for type 40374.

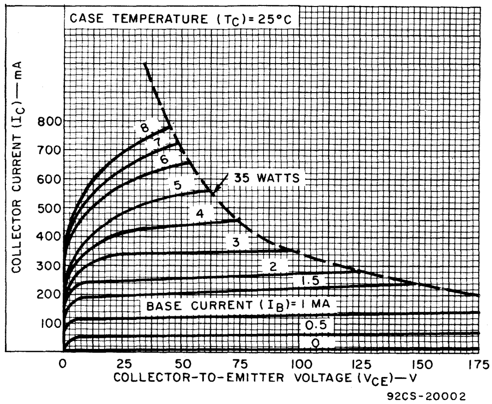


Fig. 10—Typical output characteristics for types 2N3583 and 40374.

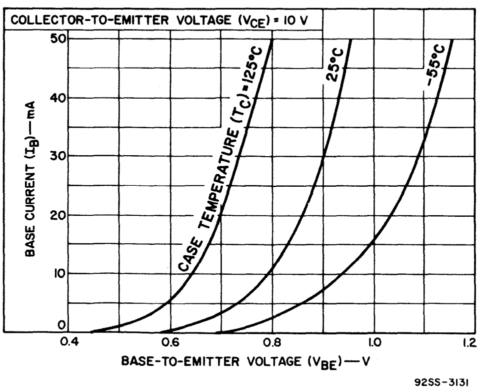


Fig. 11—Typical input characteristics for all types.

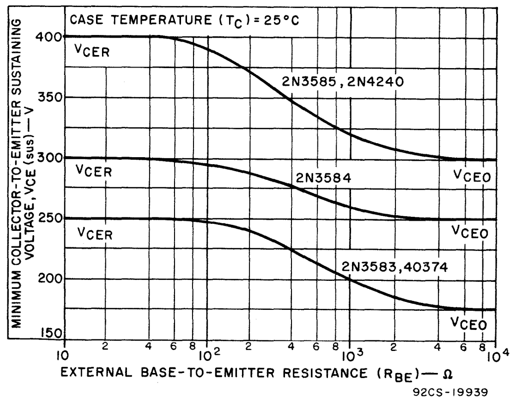


Fig. 12—Sustaining voltage vs. base-to-emitter resistance for all types.

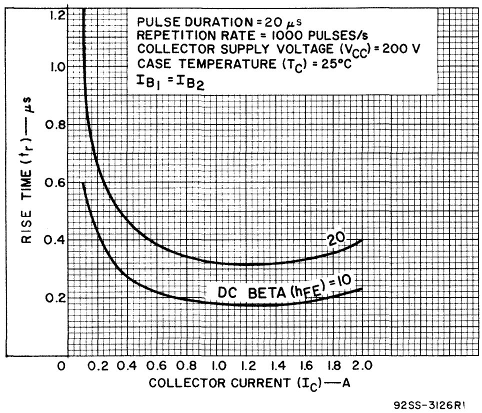


Fig. 13—Typical rise time vs. collector current for types 2N3584 and 2N3585.

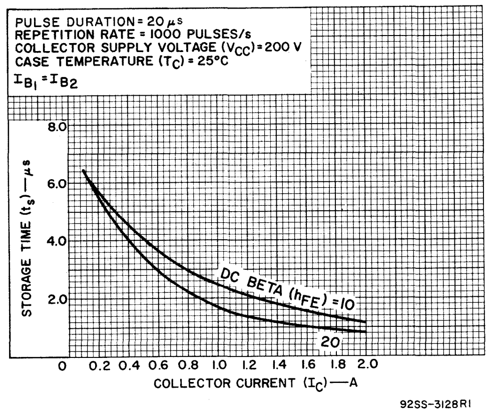


Fig. 14—Typical storage time vs. collector current for types 2N3584 and 2N3585.

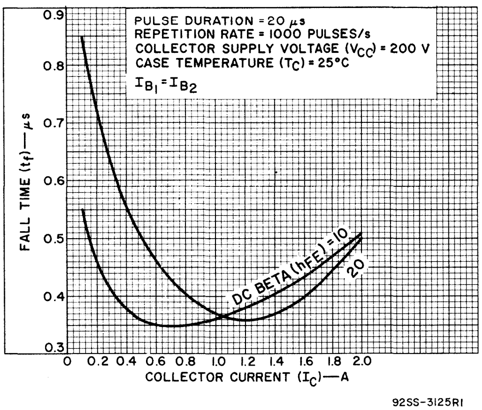


Fig. 15—Typical fall time vs. collector current for types 2N3584 and 2N3585.

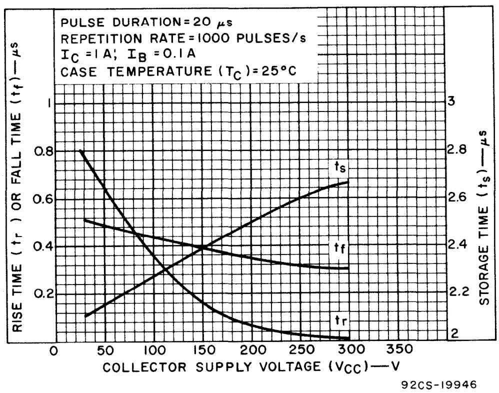


Fig. 16—Typical rise time, fall time, and storage time vs, collector supply voltage for types 2N3584 and 2N3585.

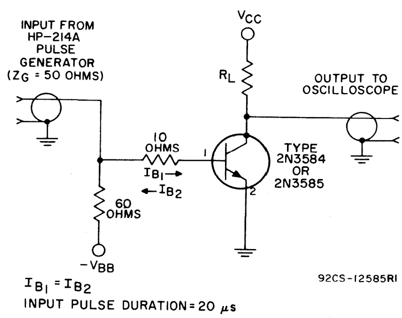


Fig. 17—Circuit used to measure switching times for types 2N3584 and 2N3585.

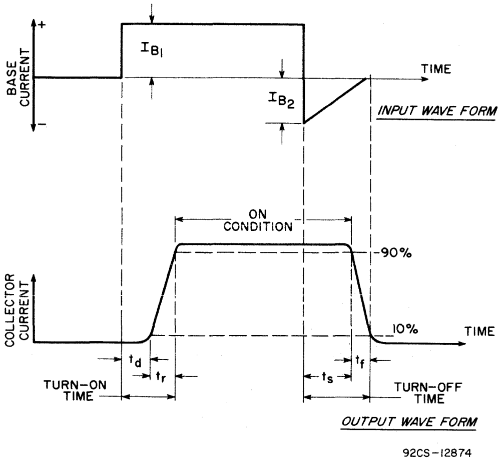


Fig. 18—Phase relationship between input and output currents, showing reference points for specification of switching times (test circuit shown in Fig. 17).

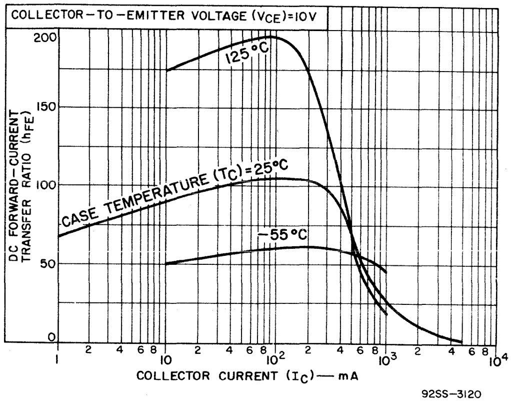


Fig. 19—Typical dc beta vs. collector current for types 2N3583, 2N4240, and 40374.

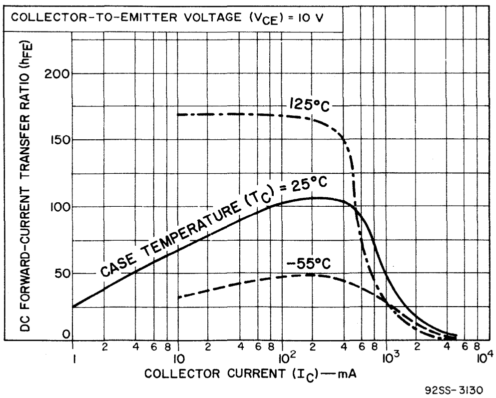


Fig. 20—Typical dc beta vs. collector current for types 2N3584 and 2N3585.

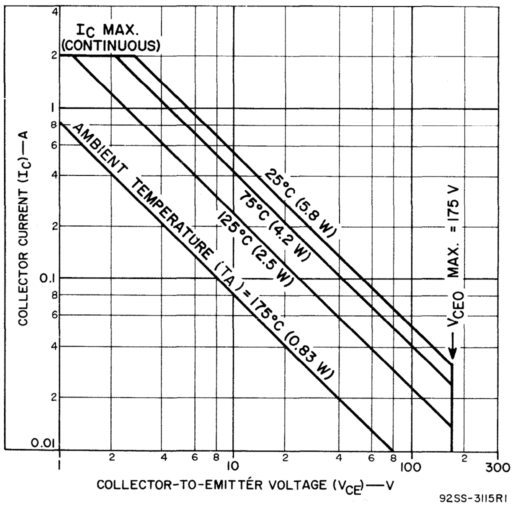


Fig. 21—Maximum operating areas for type 40374.

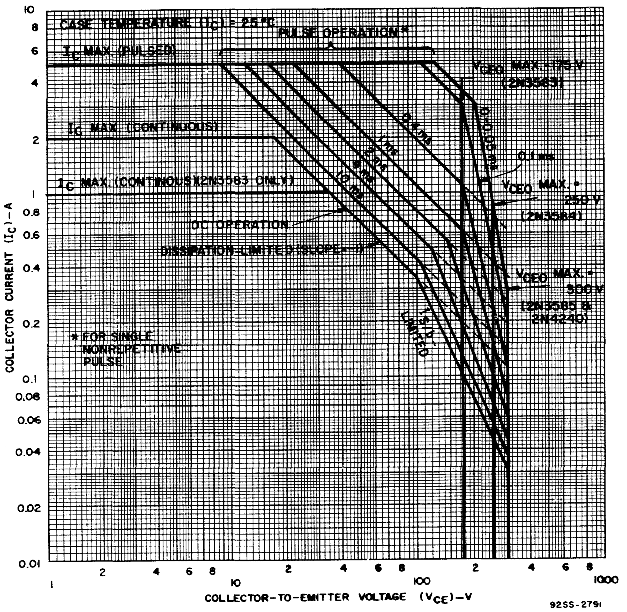


Fig. 22—Maximum operating areas for types 2N3583, 2N3584, 2N3585, and 2N4240 (dc conditions).

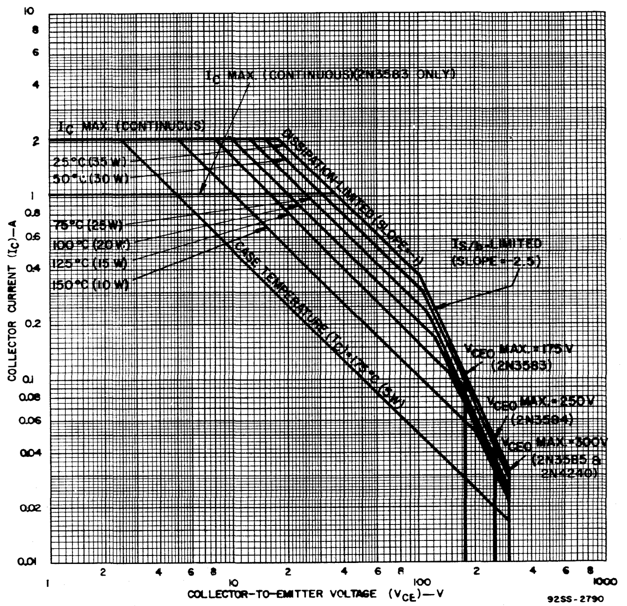
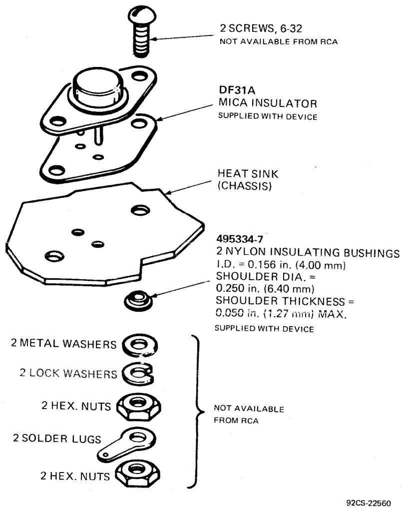


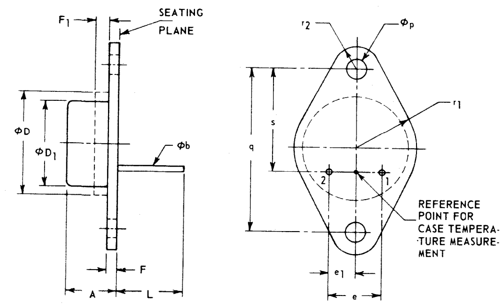
Fig. 23—Maximum operating areas for types 2N3583, 2N3584, 2N3585, and 2N4240 (pulse conditions).



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 24—Suggested mounting hardware for types 2N3583, 2N3584, 2N3585, and 2N4240.

DIMENSIONAL OUTLINE FOR TYPES 2N3583, 2N3584, 2N3585, AND 2N4240
JEDEC TO-66



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	0.250	0.340	6.35	8.64	
ϕb	0.028	0.034	0.711	0.863	
ϕD	—	0.620	—	15.75	
ϕD1	0.470	0.500	11.94	12.70	
e	0.190	0.210	4.83	5.33	
e1	0.093	0.107	2.36	2.72	
F	0.050	0.075	1.27	1.91	2
F1	—	0.050	—	1.27	1
L	0.360	—	9.14	—	
ϕp	0.142	0.152	3.61	3.86	
q	0.958	0.962	24.33	24.43	
r1	—	0.350	—	8.89	
r2	—	0.145	—	3.68	
s	0.570	0.590	14.48	14.99	

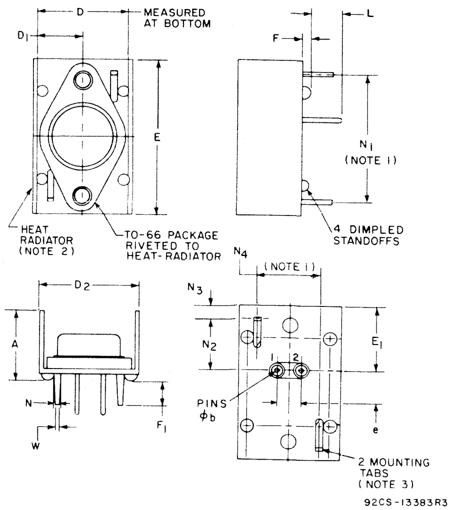
NOTES:
1. The outline contour is optional within zone defined by ϕD and F1.
2. Dimension does not include sealing flange.

92SS 3738

TERMINAL CONNECTIONS FOR TYPES 2N3583, 2N3584, 2N3585, AND 2N4240

Pin 1 - Base
Pin 2 - Emitter
Case, Mounting Flange - Collector

DIMENSIONAL OUTLINE FOR TYPE 40374 JEDEC TO-66 WITH HEAT RADIATOR



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A		0.616		15.64	
ϕb	0.028	0.034	0.711	0.864	
D	0.750	0.760	19.05	19.30	
D1	0.375	0.380	9.52	9.65	
D2	0.820	0.920	20.83	23.37	
E	1.297	1.327	32.94	33.70	
E1	0.551	0.561	13.99	14.25	
e	0.190	0.210	4.83	5.33	
F	0.30	0.55	7.62	13.97	
F1	0.175	0.210	4.44	5.33	
L	0.170		4.31		
N	0.052	0.065	1.32	1.65	
N1	1.098	1.102	27.89	27.99	1
N2	0.448	0.452	11.38	11.47	
N3	0.099	0.113	0.25	0.29	
N4	0.498	0.502	12.65	12.75	
W	0.048	0.060	1.22	1.52	

NOTES:
1. Measured at bottom of heat radiator.
2. 0.035 in. (0.889 mm) C.R.S., tin plated.
3. Recommended hole size for printed-circuit board is 0.070 in. (1.778 mm) dia.

TERMINAL CONNECTIONS FOR TYPE 40374

Pin 1 - Base
Pin 2 - Emitter
Heat-Radiator - Collector

RCA

Solid State Division

Power Transistors

2N6211, 2N6212
2N6213, 2N6214

JEDEC TO-66

H-1340

High-Voltage Medium-Power Silicon P-N-P Transistors

For Switching and Amplifier Applications
In Military, Industrial, and Commercial Equipment

Features:

- **High voltage ratings:**
  - $V_{CEO}(sus)$ = **−400 V max. (2N6214)**
  - = **−350 V max. (2N6213)**
  - = **−300 V max. (2N6212)**
  - = **−225 V max. (2N6211)**
- **Large safe-operating area**
- **Complements to 2N3585 transistor family**
- **Thermal-cycling rating**

RCA types 2N6211, 2N6212, 2N6213, and 2N6214● are epitaxial silicon p-n-p transistors with high breakdown-voltage ratings and fast switching speeds. They are supplied in the popular JEDEC TO-66 package; they differ in breakdown-voltage ratings and leakage-current values.

● Formerly RCA Dev. Nos. TA7719, TA7410, TA8330, and TA8331, respectively.

Applications:

- **Power-Switching Circuits**
- **Switching Regulators**
- **Converters**
- **Inverters**
- **High-Fidelity Amplifiers**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N6211	2N6212	2N6213	2N6214	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	−275	−350	−400	−450	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:						
With base open	$V_{CEO}(sus)$	−225	−300	−350	−400	V
With external base-to-emitter resistance (R_{BE}) = 50 Ω	$V_{CER}(sus)$	−250	−325	−375	−425	V
* With base-emitter junction reverse-biased (V_{BE} = 1.5 V)	$V_{CEX}(sus)$	−275	−350	−400	−450	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	−6	−6	−6	−6	V
*COLLECTOR CURRENT (Continuous)	I_C	−2	−2	−2	−2	A
*BASE CURRENT (Continuous)	I_B	−1	−1	−1	−1	A
TRANSISTOR DISSIPATION:	P_T					
* At case temperatures up to 100°C and V_{CE} up to 50 V		20	20	20	20	W
At case temperatures up to 25°C and V_{CE} up to 40 V		35	35	35	35	W
At case temperatures up to 25°C and V_{CE} above 40 V		See Fig. 1				
At case temperatures above 25°C and V_{CE} above 40 V		See Figs. 1 & 6.				
*TEMPERATURE RANGE:						
Storage & Operating (Junction)		← 65 to 200 →				°C
*LEAD TEMPERATURE (During Soldering):						
At distance ≥ 1/32 in. (0.8 mm) from case for 10s max.		← 230 →				°C

*In accordance with JEDEC registration data format (JS-6 RDF-1)

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ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C) = 25°C Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Voltage V dc V_{CE}	V_{BE}	Current A dc I_C	I_E	I_B	LIMITS 2N6211 Min.	2N6211 Max.	2N6212 Min.	2N6212 Max.	2N6213 Min.	2N6213 Max.	2N6214 Min.	2N6214 Max.	UNITS
Collector-Cutoff Current: With base open	I_{CEO}	−150				0	–	−5	–	−5	–	−5	–	−5	mA
* With base-emitter junction reverse-biased	I_{CEV}	−250	1.5				–	−0.5	–	–	–	–	–	–	mA
		−315	1.5				–	–	–	−0.5	–	–	–	–	
		−360	1.5				–	–	–	–	–	−0.5	–	–	
		−410	1.5				–	–	–	–	–	–	–	−1	
* With base-emitter junction reverse biased and T_C = 100°C	I_{CEV}	−250	1.5				–	−5	–	–	–	–	–	–	mA
		−315	1.5				–	–	–	−5	–	–	–	–	
		−360	1.5				–	–	–	–	–	−5	–	–	
		−410	1.5				–	–	–	–	–	–	–	−10	
* Emitter-Cutoff Current	I_{EBO}		6	0			–	−1	–	−0.5	–	−0.5	–	−0.5	mA
* DC Forward-Current Transfer Ratio	h_{FE}	−2.8		−1			10	100	–	–	–	–	–	–	
		−3.2		−1			–	–	10	100	–	–	–	–	
		−4		−1			–	–	–	–	10	100	–	–	
		−5		−1			–	–	–	–	–	–	10	100	
* Collector-to-Emitter Sustaining Voltage: With base open	$V_{CEO}(sus)$			−0.2		0	−225	–	−300	–	−350	–	−400	–	V
With external base-to-emitter resistance (R_{BE}) = 50 Ω	$V_{CER}(sus)$			−0.2			−250	–	−325	–	−375	–	−425	–	V
With base-emitter junction reverse-biased and external base-to-emitter resistance (R_{BE}) = 50 Ω	$V_{CEX}(sus)$		1.5	−0.2			−275	–	−350	–	−400	–	−450	–	V
* Emitter-to-Base Voltage	V_{EBO}					0.5 mA	–	–	−6	–	−6	–	−6	–	V
						1 mA	−6				–	–	–	–	
* Emitter-to-Base Saturation Voltage	$V_{BE}(sat)$			−1		−0.125	–	−1.4	–	−1.4	–	−1.4	–	−1.4	V
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$			−1		−0.125	–	−1.4	–	−1.6	–	−2	–	−2.5	V
Output Capacitance (f = 1 MHz)	C_{obo}	−10 (V_{CB})			0		–	220	–	220	–	220	–	220	pF
Second-Breakdown Collector Current (Base forward-biased)	$I_{S/b}$	−40					−0.875	–	−0.875	–	−0.875	–	−0.875	–	A
* Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward-Current Transfer Ratio (f = 5 MHz)	$\|h_{fe}\|$	−10		−0.2			4	–	4	–	4	–	4	–	
* Saturated Switching Times: Rise time	t_r	V_{CC} = −200 V		−1		I_{B1} & I_{B2} −0.125	–	0.6	–	0.6	–	0.6	–	0.6	μs
Storage time	t_s	V_{CC} = −200 V		−1		I_{B1} & I_{B2} −0.125	–	2.5	–	2.5	–	2.5	–	2.5	μs
Fall time	t_f	V_{CC} = −200 V		−1		I_{B1} & I_{B2} −0.125	–	0.6	–	0.6	–	0.6	–	0.6	μs
Thermal Resistance (Junction-to-case)	$R_{\theta JC}$	−10		−1			–	5	–	5	–	5	–	5	°C/W

*In accordance with JEDEC registration data format JS-6 RDF-1.

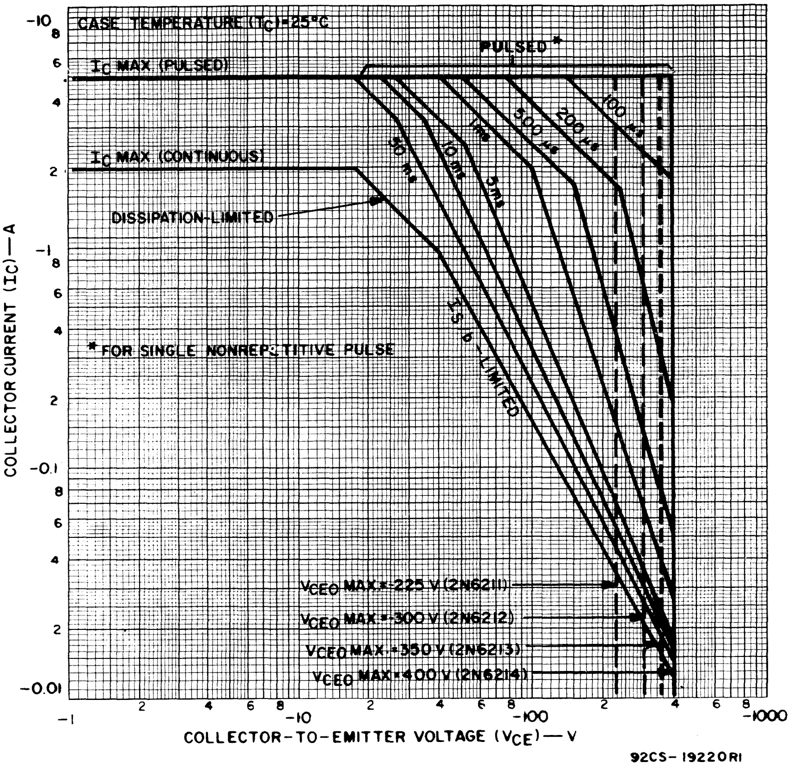


Fig. 1—Maximum operating areas for all types.

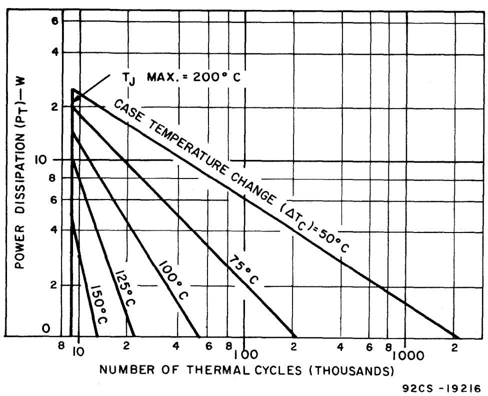


Fig. 2—Maximum operating areas for all types.

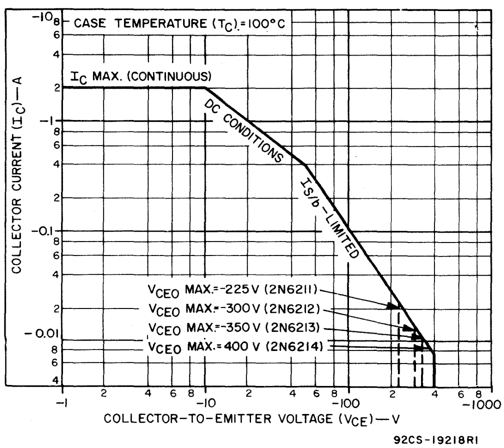


Fig. 3—Thermal-cycling rating chart for all types.

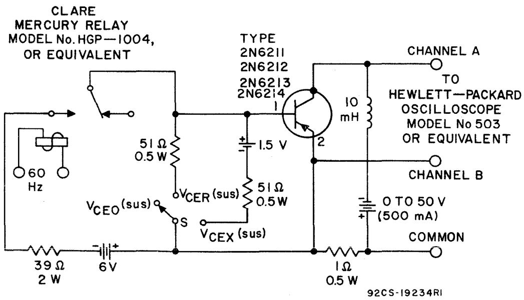


Fig. 4—Circuit used to measure sustaining voltages $V_{CEO}(sus)$, $V_{CER}(sus)$ and $V_{CEX}(sus)$ for all types.

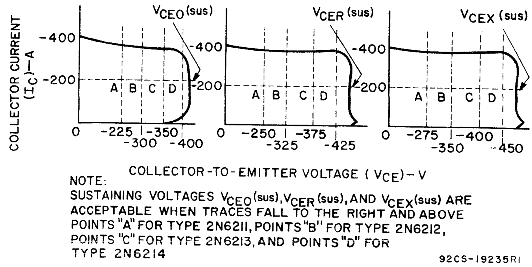


Fig. 5—Oscilloscope display for measurement of sustaining voltages (test circuit shown in Fig 4).

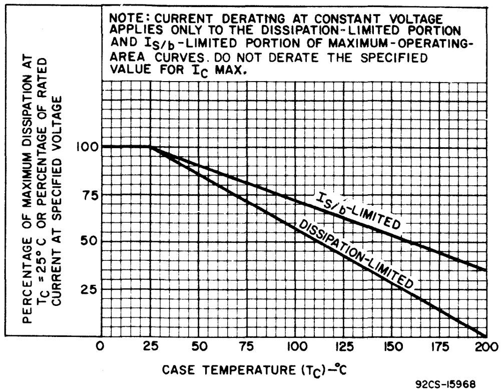


Fig. 6—Derating curves for all types.

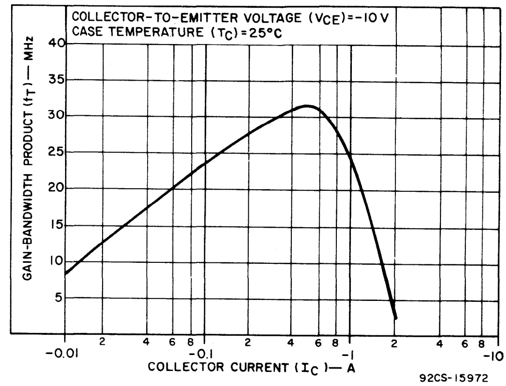


Fig. 7—Typical gain-bandwidth product for all types.

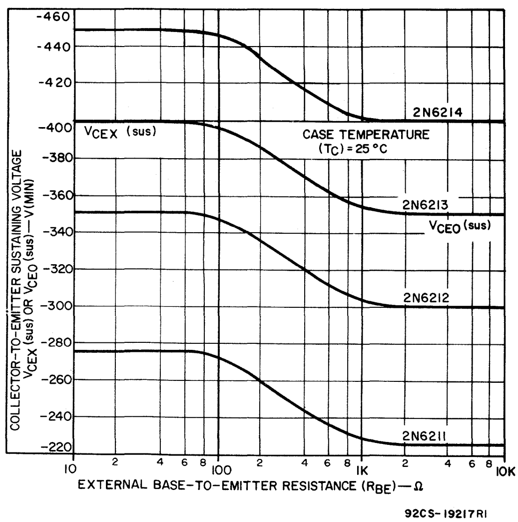


Fig. 8—Collector-to-emitter sustaining-voltage characteristics for all types.

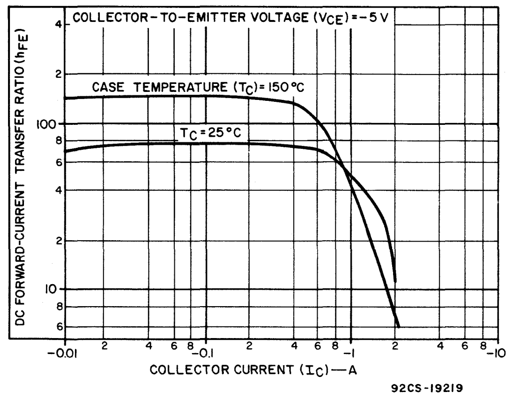


Fig. 9—Typical dc beta characteristic for all types.

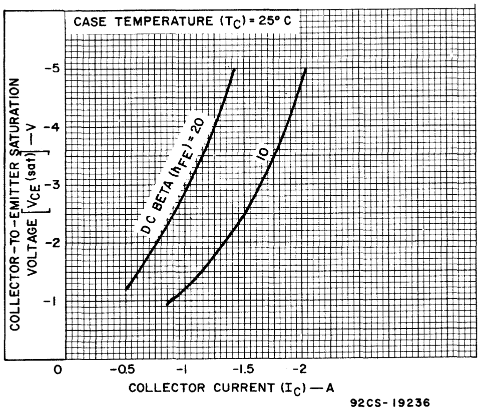


Fig. 10—Typical saturation-voltage characteristics for all types.

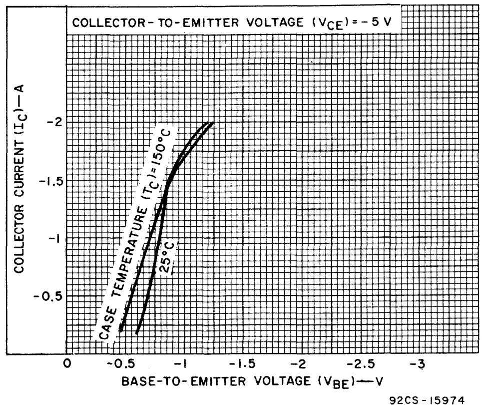


Fig. 11—Typical transfer characteristics for all types.

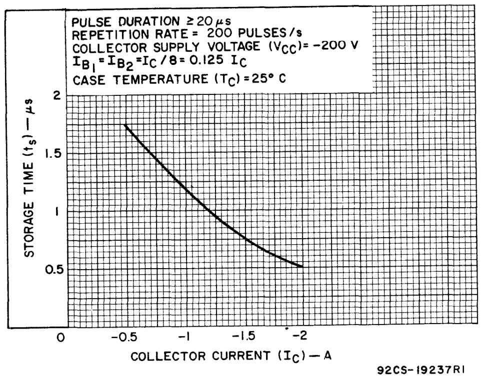


Fig. 12—Typical storage-time characteristic for all types.

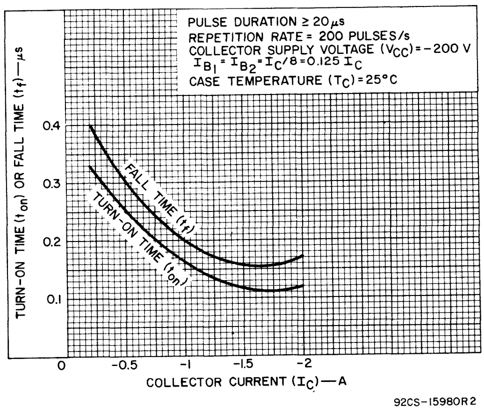


Fig. 13—Typical turn-on time and fall-time characteristics for all types.

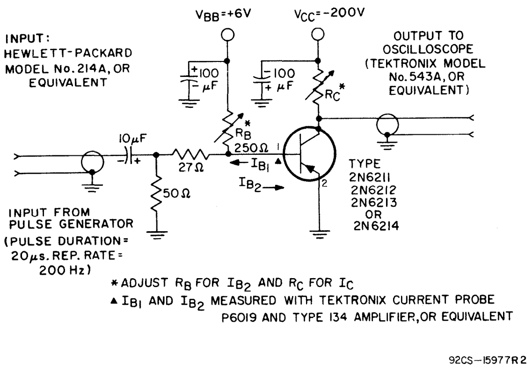


Fig. 14—Circuit used to measure saturated switching times for all types.

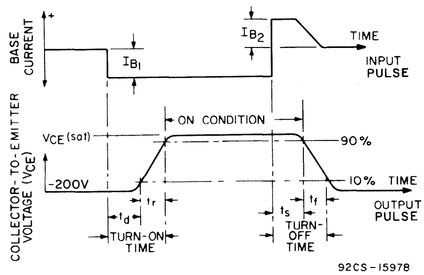
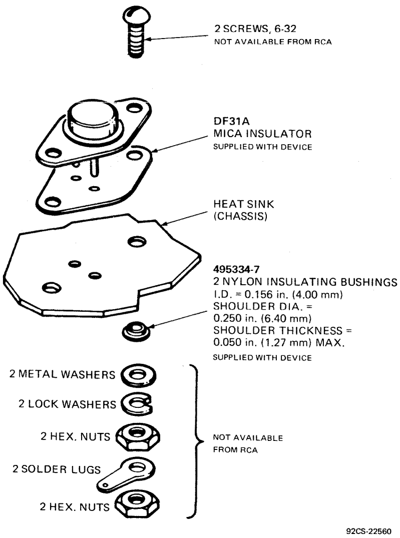


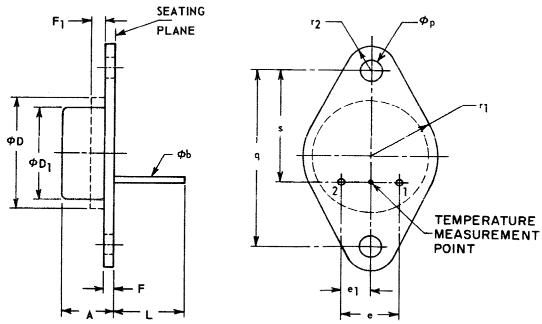
Fig. 15—Phase relationship between input current and output voltage showing reference points for specification of switching times. (Test circuit shown in Fig. 14).



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 16—Suggested mounting hardware for all types.

DIMENSIONAL OUTLINE
JEDEC TO-66



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	0.250	0.340	6.35	8.64	
φb	0.028	0.034	0.711	0.863	
φD	–	0.620	–	15.75	
φD1	0.470	0.500	11.94	12.70	
e	0.190	0.210	4.83	5.33	
e1	0.093	0.107	2.36	2.72	
F	0.050	0.075	1.27	1.91	2
F1	–	0.050	–	1.27	1
L	0.360	–	9.14	–	
φp	0.142	0.152	3.61	3.86	
q	0.958	0.962	24.33	24.43	
r1	–	0.350	–	8.89	
r2	–	0.145	–	3.68	
s	0.570	0.590	14.48	14.99	

NOTES:
1. The outline contour is optional within zone defined by φD and F_1.
2. Dimension does not include sealing flange.

92SS-3738

TERMINAL CONNECTIONS

Pin 1 — Base
Pin 2 — Emitter
Case — Collector
Mounting Flange — Collector

RCA
Solid State
Division

Power Transistors
2N6077
2N6078
2N6079

JEDEC TO-66

H-1340

High-Voltage, High-Power Silicon N-P-N Transistors

For Switching and Linear Applications

Features

- **Maximum safe-area-of-operation curves**
- **Low saturation voltages**
- **High voltage ratings :**
  V_{CER}(sus) = 300 V (2N6077)
  275 V (2N6078)
  375 V (2N6079)
- **High dissipation rating : P_T = 45 W**

RCA-2N6077, 2N6078, and 2N6079 are multiple epitaxial silicon n-p-n power transistors utilizing a multiple-emitter-site structure. Multiple-epitaxial construction maximizes the volt-ampere characteristic of the device and provides fast switching speeds. Multiple-emitter-site design ensures uniform current flow throughout the structure, which produces a high $I_{S/b}$ and a large safe-operation area.

These devices use the popular JEDEC TO-66 package; they differ mainly in voltage ratings, leakage-current limits, and V_{CE}(sat) ratings.

The 2N6077 is characterized for switching applications with load lines in the active region. These applications include sweep circuits and all circuits using the transistor as an active voltage clamp.

Type 2N6078 is characterized for switching applications with the load line extending into the reverse-bias region. Its voltage ratings make this device useful for switching regulators operating directly from a rectified 110-V or 220-V power line. The unit is rated to take surge currents up to 5 A and maintain saturation.

The 2N6079 is characterized for use in inverters operating directly from a rectified 110-V power line. The leakage current is specified at 450 volts; therefore the device can also be used in a series bridge configuration on a 220-V line. The V_{EBO} rating of 9 volts eases requirements on the drive transformer in inverter applications. Storage time, an important factor in the frequency stability of an inverter, is specified in Fig. 12 , which shows variation in storage time with variation in load current from zero to maximum (4 A).

MAXIMUM RATINGS, *Absolute-Maximum Values:*		2N6077	2N6078	2N6079	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	300	275	375	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:					
With base open	V_{CEO}(sus)	275	250	350	V
* With reverse bias (V_{BE}) of −1.5 V	V_{CEX}(sus)	300	275	375	V
With external base-to-emitter resistance (R_{BE}) $\leq 50\ \Omega$	V_{CER}(sus)	300	275	375	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	6	6	9	V
*COLLECTOR CURRENT:	I_C				
Continuous		7	7	7	A
Peak		10	10	10	A
*CONTINUOUS BASE CURRENT	I_B	4	4	4	A
*TRANSISTOR DISSIPATION:	P_T				
At case temperatures up to 25°C and V_{CE} up to 40 V		45	45	45	W
At case temperatures up to 25°C and V_{CE} above 40 V			See Fig. 1		
At case temperatures above 25°C and V_{CE} above 40 V			See Figs. 1, 2, & 3		
*TEMPERATURE RANGE:					
Storage & Operating (Junction)			−65 to +200		°C
*PIN TEMPERATURE (During Soldering):					
At distances $\geq$ 1/32 in. (0.8 mm) from case for 10 s max.			230		°C

* In accordance with JEDEC registration data format (JS-6, RDF-1).

ELECTRICAL CHARACTERISTICS, *Case Temperature (T_C) = 25°C*

Characteristic	Symbol	Test Conditions						Limits									Units
		DC Collector Voltage (V)	DC Emitter Voltage (V)		DC Current (A)			Type 2N6077			Type 2N6078			Type 2N6079			
		V_{CE}	V_{CB}	V_{BE}	I_C	I_B	I_E	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Collector-Cutoff Current: With base open	I_{CEO}	250				0		–	–	2	–	–	–	–	–	–	mA
* With base-emitter junction reverse biased	I_{CEV}	250 450		−1.5 −1.5				– –	– –	5 –	– –	– –	0.05 –	– –	– –	– 0.5	mA
* With base-emitter junction reverse biased	I_{CEV} T_C = 125°C	250 450		−1.5 −1.5				– –	– –	8 –	– –	– –	0.2 –	– –	– –	– 5	mA
* Emitter-Cutoff Current	I_{EBO}			−6 −9	0 0			– –	– –	1 –	– –	– –	1 –	– –	– –	– 1	mA
* Collector-to-Emitter Sustaining Voltage *(see Figs. 15 & 16)* With base open	$V_{CEO}(sus)$[b]				0.2			275[b]	–	–	250[b]	–	–	350[b]	–	–	V
With external base-to-emitter resistance (R_{BE}) = 50 Ω	$V_{CER}(sus)$[b]				0.2			300[b]	–	–	275[b]	–	–	375[b]	–	–	V
* Emitter-to-Base Voltage	V_{EBO}						0.001	6	–	–	6	–	–	9	–	–	V
* DC Forward-Current Transfer Ratio	h_{FE}	1			1.2			12	28	70	12	28	70	12	28	50	
* Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$[a]				1.2 3 4 5	0.2 0.6 0.8 1		– – – –	1.0 1.2 – –	1.6 1.9 – –	– – – –	1.0 – – 1.5	1.6 – – 2	– – – –	1.0 – 1.3 –	1.6 – 2 –	V
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$[a]				1.2 3 4 5	0.2 0.6 0.8 1		– – – –	0.15 0.25 – –	0.5 1 – –	– – – –	0.15 – – 0.8	0.5 – – 3	– – – –	0.15 – 0.5 –	0.5 – 3 –	V
Output Capacitance (At 1 MHz)	C_{obo}		10				0	–	–	150	–	–	150	–		150	pF
* Magnitude of Common Emitter, Small-Signal, Short-Circuit, Forward-Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	10			0.2			1	7	–	1	7	–	1	7	–	
Second Breakdown Collector Current (With base forward biased) Pulse duration (non-repetitive) = 1 s	$I_{S/b}$[c]	50						0.9	–	–	0.9	–	–	0.9	–	–	A
Second Breakdown[c] Energy (With base reverse biased) R_B = 50 Ω, L = 100 μH	$E_{S/b}$[d]			−4	3			0.45	–	–	0.45	–	–	0.45	–	–	mJ
Switching Times: Delay *(See Figs. 10, 17, & 18)*	t_d	V_{CC} = 250 V			1.2	0.2[e]		–	0.02	–	–	0.02	–	–	0.02	–	μs
* Rise *(See Figs. 13, 17, & 18)*	t_r	V_{CC} = 250 V			1.2	0.2[e]		–	0.3	0.75	–	0.3	0.75	–	0.3	0.75	μs
* Storage *(See Figs. 11, 12, 17 & 18)*	t_s	V_{CC} = 250 V			1.2	0.2[e]		–	2.8	5	–	2.8	5	–	2.8	5	μs
* *(See Figs. 14, 17, & 18)*	t_f	V_{CC} = 250 V			1.2	0.2[e]		–	0.3	0.75	–	0.3	0.75	–	0.3	0.75	μs
Thermal Resistance (Junction-to-Case)	$\theta_{J\text{-}C}$	20			2.5			–	–	3.9	–	–	3.9	–	–	3.9	°C/W

[a] Pulsed; pulse duration ≤350 μs, Duty factor = 2%.

[b] CAUTION: The sustaining voltages $V_{CEO}(sus)$, and $V_{CER}(sus)$, MUST NOT be measured on a curve tracer. These sustaining voltages should be measured by means of the test circuit shown in Fig. 15.

[c] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward biased for transistor operation in the active region.

[d] $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse bias conditions. $E_{S/b} = 1/2\ LI^2$ where L is a series load or leakage inductance, and I is the peak collector current.

[e] $I_{B1} = I_{B2}$ = value shown.

* In accordance with JEDEC registration data format (JS-6 RDF-1).

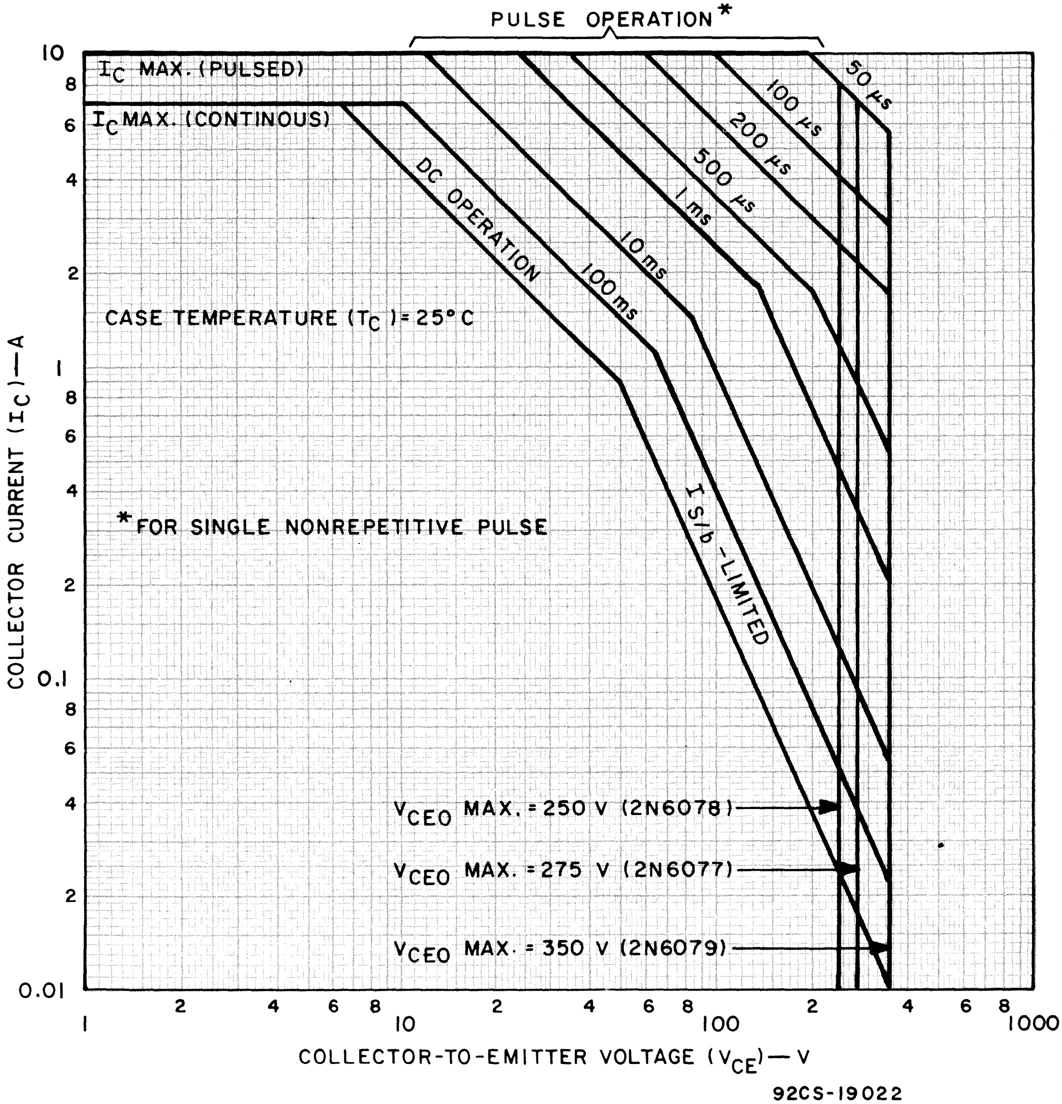


Fig.1—Maximum operating areas for all types.

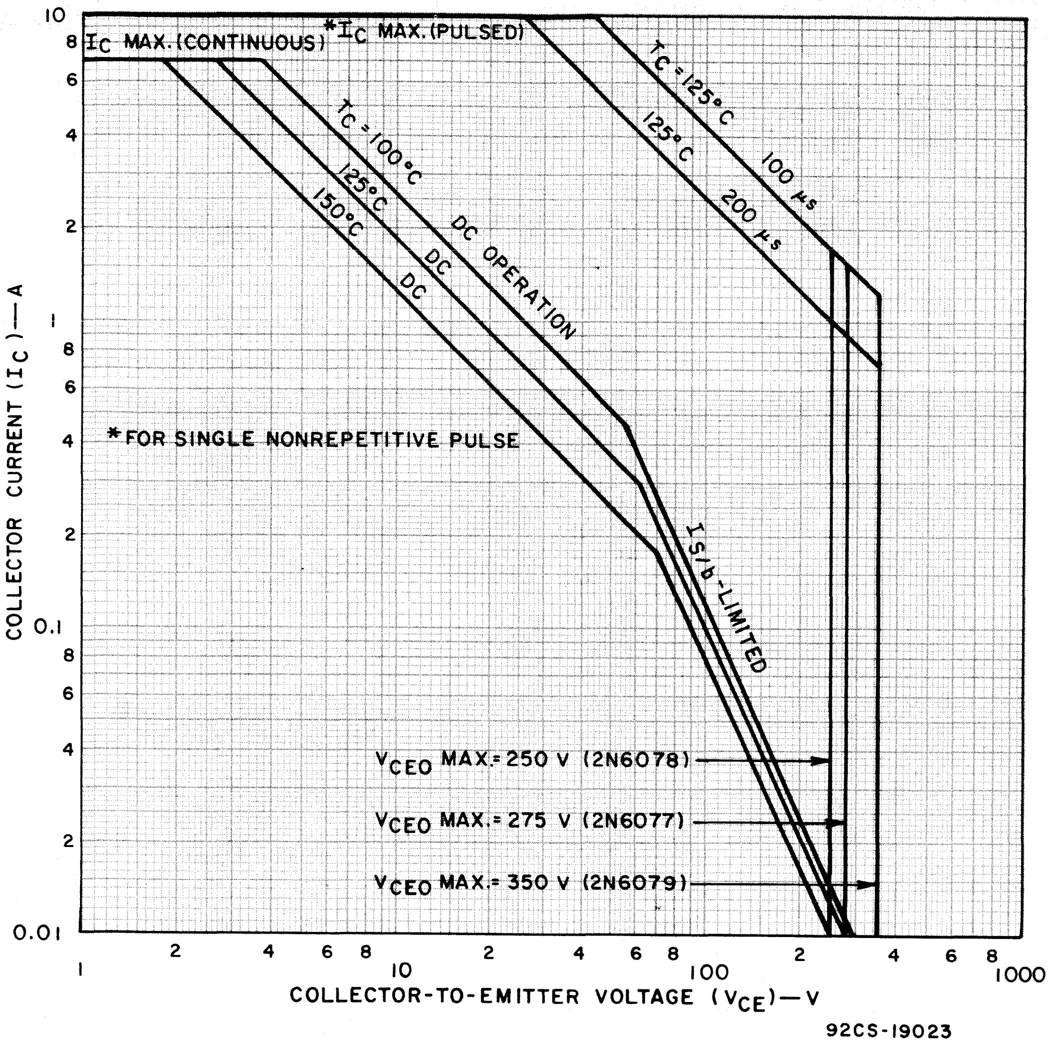


Fig.2—Maximum operating areas for all types.

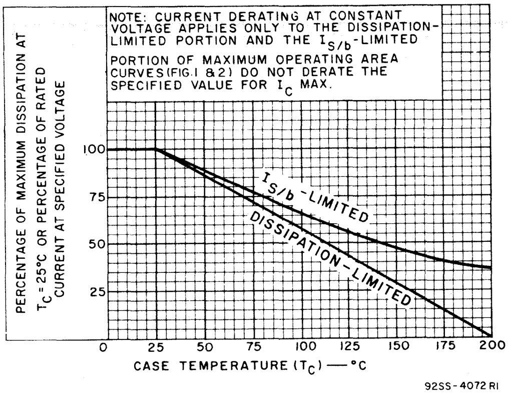


Fig.3—Derating curve for all types.

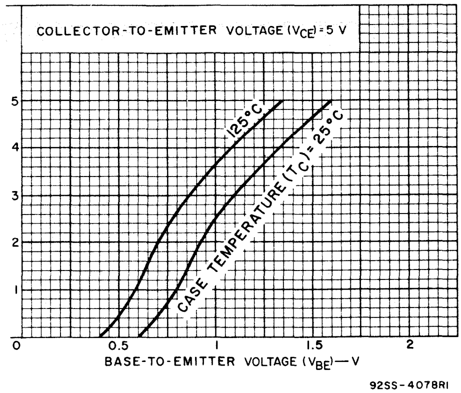


Fig.4—Typical transfer characteristics for all types.

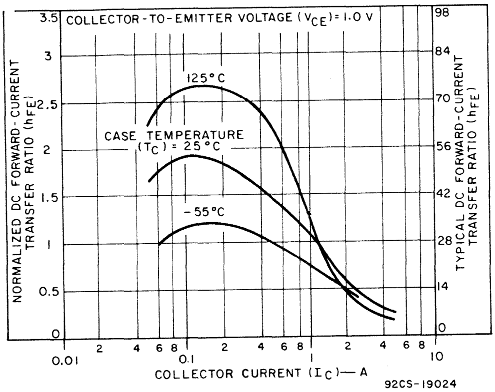


Fig.5—Typical normalized dc beta characteristics for all types.

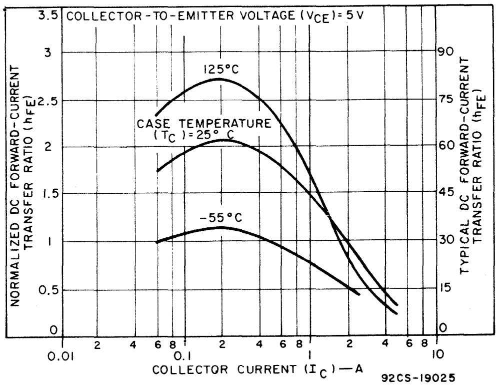


Fig.6—Typical normalized dc beta characteristics for all types.

Note (Figs. 5 & 6): To estimate min., max. h_{FE} at any current and temperature, read normalized dc forward-current transfer ratio and multiply by min., max. specifications given in Electrical Characteristics Chart (p. 2).

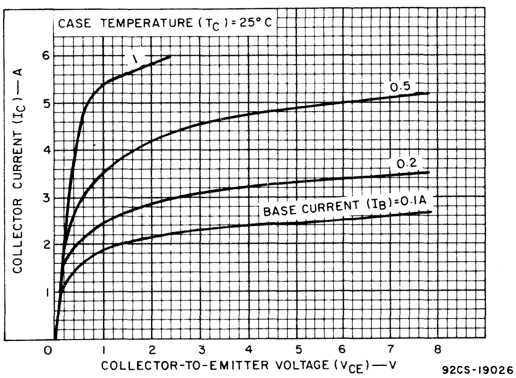


Fig.7—Typical output characteristics for all types.

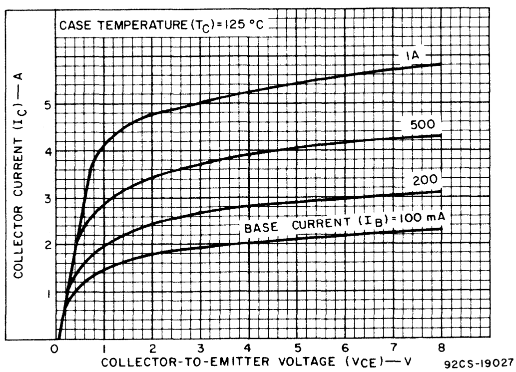


Fig.8—Typical output characteristics for all types.

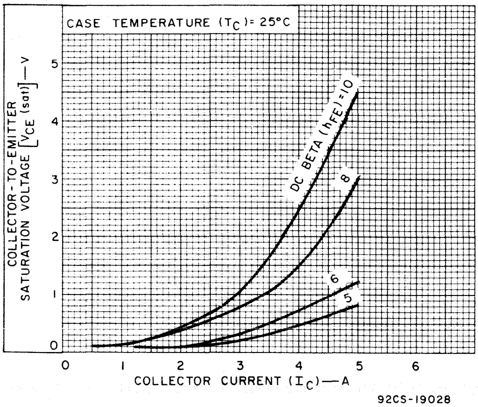


Fig.9—Typical saturation voltage characteristics for all types.

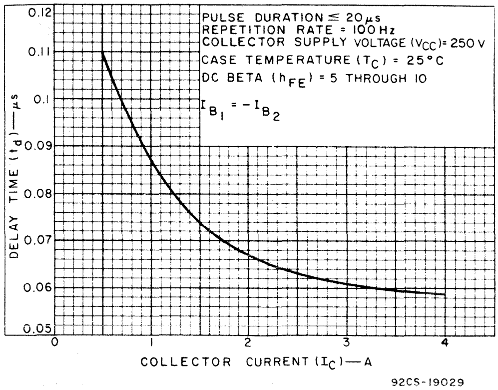


Fig.10—Typical delay-time characteristic for all types.

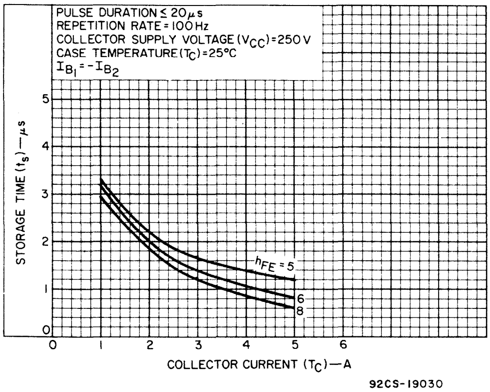


Fig.11—Typical storage-time characteristic for all types (with constant forced gain).

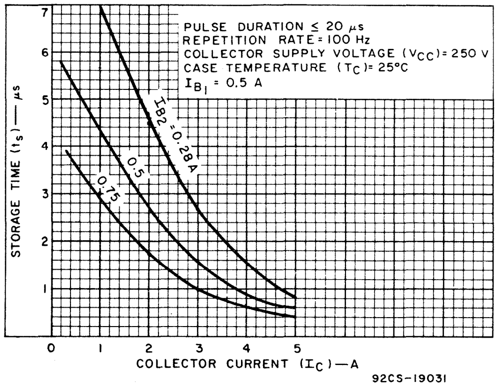


Fig.12—Typical storage-time characteristic for all types (with constant-base drives).

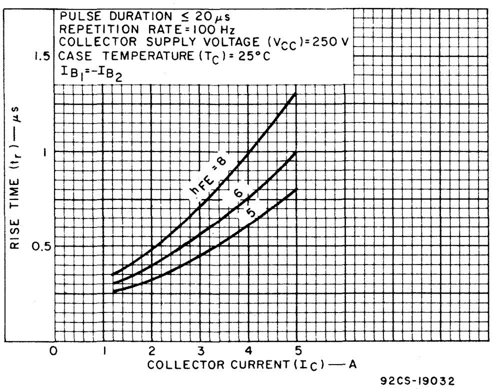


Fig.13—Typical rise-time characteristic for all types.

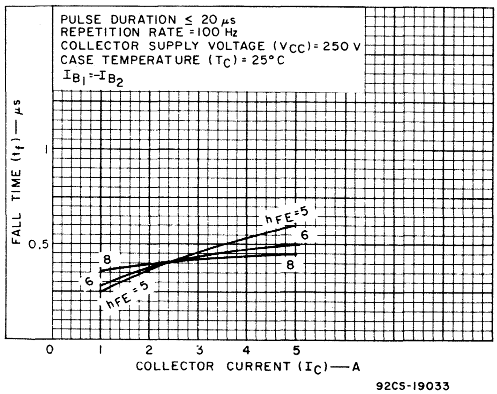


Fig.14—Typical fall-time characteristic for all types.

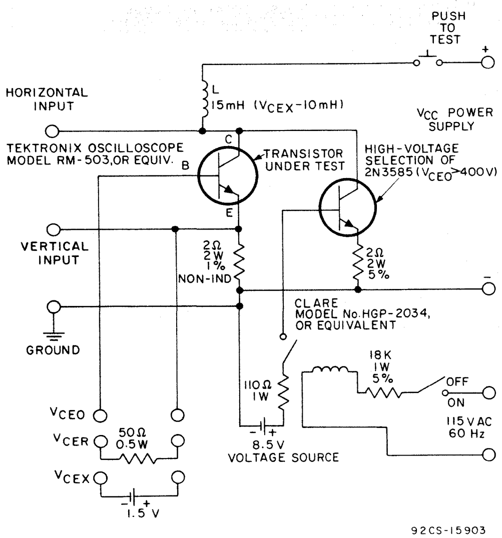
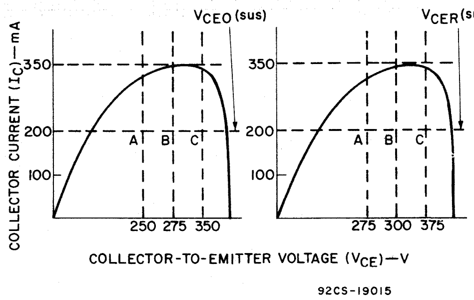


Fig.15—Circuit used to measure sustaining voltages V_{CEO}(sus), V_{CER}(sus) for all types.



The sustaining voltages V_{CEO}(sus) and V_{CER}(sus) are acceptable when the traces fall to the right and above point "A" for type 2N6078 point "B" for type 2N6077 and point "C" for type 2N6079.

Fig.16—Oscilloscope display for measurement of sustaining voltages (test circuit shown in Fig. 15).

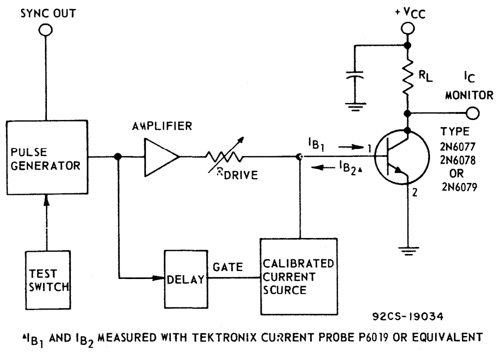


Fig.17—Circuit used to measure switching times for all types.

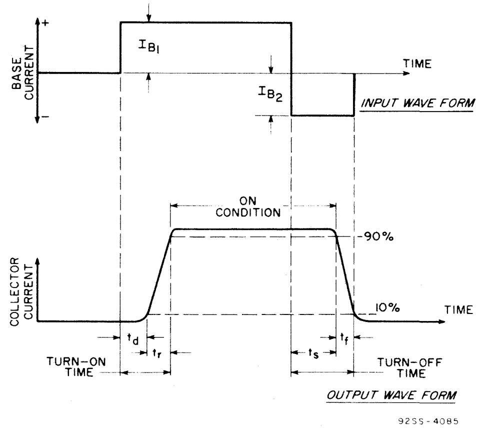
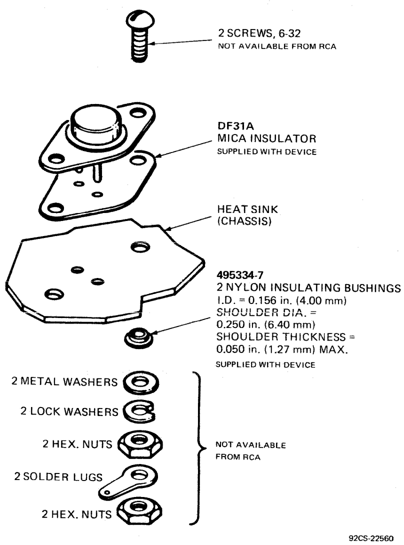


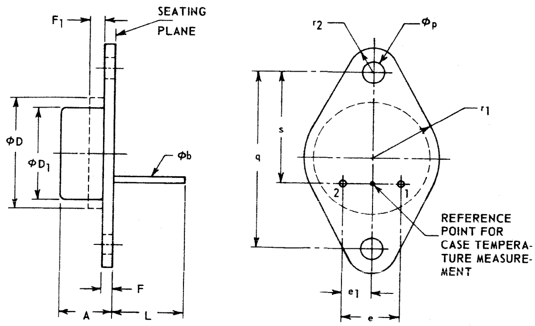
Fig.18—Phase relationship between input and output currents showing reference points for specification of switching times. (Test circuit shown in Fig. 17).



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.19— Suggested hardware for all types.

DIMENSIONAL OUTLINE (JEDEC TO-66)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.340	6.35	8.64	
φb	0.028	0.034	0.711	0.863	
φD		0.620		15.75	
φD1	0.470	0.500	11.94	12.70	
e	0.190	0.210	4.83	5.33	
e1	0.093	0.107	2.36	2.72	
F	0.050	0.075	1.27	1.91	2
F1		0.050		1.27	1
L	0.360		9.14		
φp	0.142	0.152	3.61	3.86	
q	0.958	0.962	24.33	24.43	
r1		0.350		8.89	
r2		0.145		3.68	
s	0.570	0.590	14.48	14.99	

NOTES:
1. The outline contour is optional within zone defined by φD and F_1.
2. Dimension does not include sealing flanges.

92SS-3738

TERMINAL CONNECTIONS

Pin 1 — Base

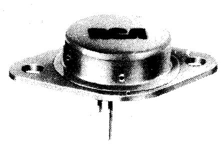
Pin 2 — Emitter

Mounting Flange, Case-Collector

Solid State
Division

Power Transistors

RCA410



JEDEC
TO-3

H-1570

High-Voltage, High-Power Silicon N-P-N Power Transistor

For Switching and Linear Applications in Military, Industrial, and Commercial Equipment

Features:

- **Maximum safe-area-of-operation curves**
- **Low saturation voltage: $V_{CE}(sat)$ = 0.8 V (max.)**
- **High voltage rating: $V_{CEO}(sus)$ = 200 V**
- **High dissipation rating: P_T = 125 W**

RCA-410 is an epitaxial silicon n-p-n power transistor utilizing a multiple-emitter-site structure. This device employs the popular JEDEC TO-3 package.

Featuring high breakdown-voltage ratings and low saturation-voltage values, the RCA-410 is especially suitable for use in inverters, deflection circuits, switching regulators, high-voltage bridge amplifiers, ignition circuits, and other high-voltage switching applications.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	200	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE		
With base open, $V_{CEO}(sus)$	200	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}	5	V
COLLECTOR CURRENT:		
Continuous, I_C	7	A
Peak	10	A
BASE CURRENT (Continuous), I_B	2	A
TRANSISTOR DISSIPATION, P_T:		
At case temperatures up to 25°C and V_{CE} up to 75 V	125	W
At case temperatures up to 25°C and V_{CE} above 75 V	See Fig. 2.	
At case temperatures above 25°C and V_{CE} above 75 V	See Figs. 1 & 2.	
TEMPERATURE RANGE:		
Storage & Operating (Junction)	-65 to +200	°C
PIN TEMPERATURE (During Soldering):		
At distances ≥ 1/32 in. (0.8 mm) from case for 10 s max.	230	°C

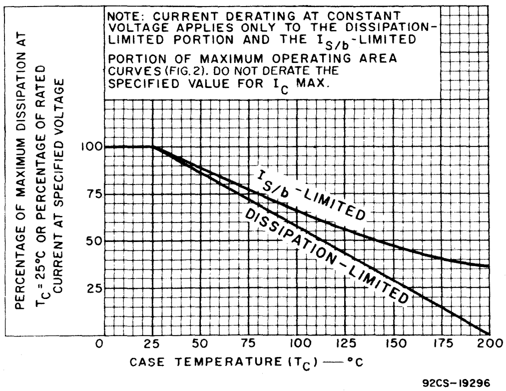


Fig. 1—Dissipation and current derating curves.

ELECTRICAL CHARACTERISTICS, Case Temperature (T_C) = 25°C Unless Otherwise Specified

Characteristic	Symbol	Test Conditions: DC Collector Voltage (V)	Test Conditions: DC Emitter or Base Voltage (V)		Test Conditions: DC Current (A)		Limits			Units
		V_{CE}	V_{EB}	V_{BE}	I_C	I_B	Min.	Typ.	Max.	
Collector-Cutoff Current: With base open	I_{CEO}	200					–	–	0.25	mA
With base-emitter junction reverse-biased & T_C = 125°C	I_{CEV}	200		−1.5			–	–	0.5	mA
Emitter-Cutoff Current	I_{EBO}		5				–	–	5.0	mA
DC Forward-Current Transfer Ratio	h_{FE}	5 5			1.0[a] 2.5[a]		30 10	– –	90 –	
Collector-to-Emitter Sustaining Voltage: With base open (See Figs. 3 & 4.)	$V_{CEO}(sus)$[b]				0.1		200[b]	–	–	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$				1.0[a]	0.1	–	0.9	1.5	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				1.0[a]	0.1	–	0.2	0.8	V
Second-Breakdown Collector Current: (With base forward-biased) Pulse duration (non-repetitive) = 1 s	$I_{S/b}$[c]	150					0.3	–	–	A
Gain-Bandwidth Product	f_T	10			0.2		–	4.0	–	MHz
Switching Time: Rise (See Figs. 10, 12, & 13.)	t_s				1.0	0.1 (I_{B1}) −0.5 (I_{B2})	–	0.35	–	μs
Storage (See Figs. 11, 12, & 13.)	I_S				1.0	0.1 (I_{B1}) −0.5 (I_{B2})	–	1.4	–	μs
Fall (See Figs. 9, 12, & 13.)	t_f				1.0	0.1 (I_{B1}) −0.5 (I_{B2})	–	0.15	–	μs
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$	10			5		–	–	1.4	°C/W

[a] Pulsed; pulse duration $\leq$350 μs, duty factor = 2%

[b]CAUTION: The sustaining voltage $V_{CEO}(sus)$ MUST NOT be measured on a curve tracer. The sustaining voltage should be measured by means of the test circuit shown in Fig. 3.

[c] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward-biased for transistor operation in the active region.

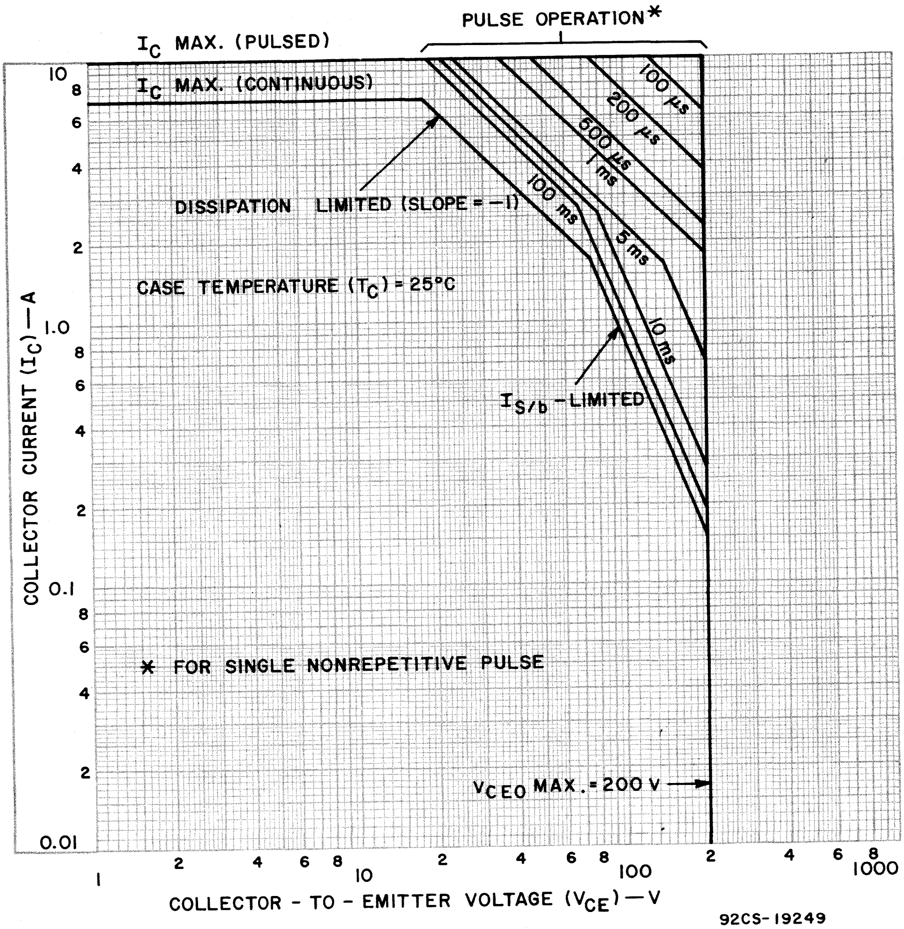


Fig.2—Maximum operating areas.

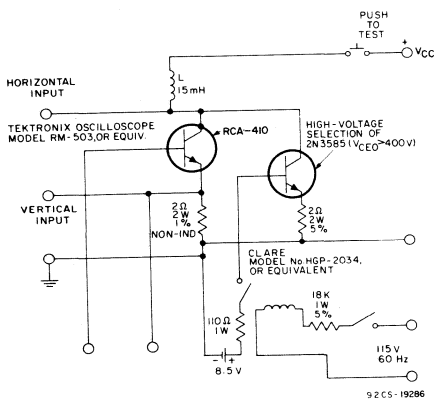


Fig.3—Circuit used to measure sustaining voltage, $V_{CEO}(sus)$.

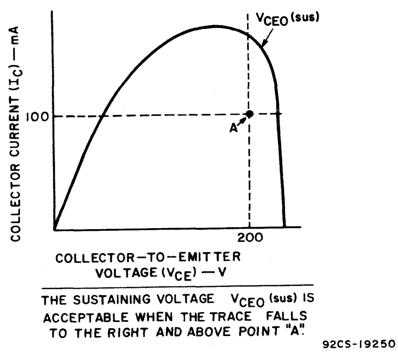


Fig.4—Oscilloscope display for measurement of sustaining voltage (test circuit shown in Fig. 3).

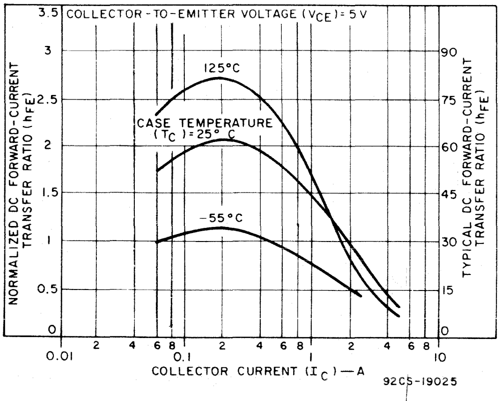


Fig.5—Typical dc beta characteristics.

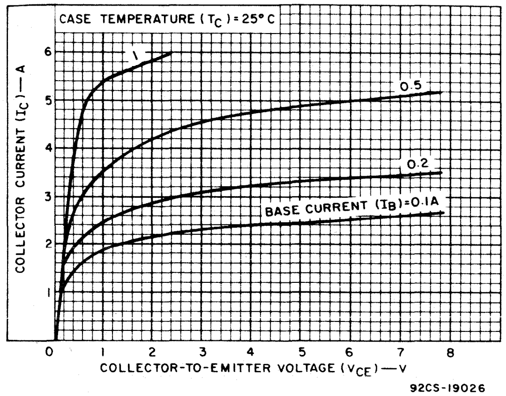


Fig.6—Typical output characteristics.

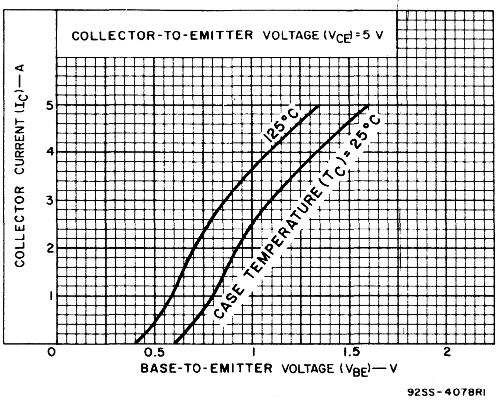


Fig.7—Typical transfer characteristics.

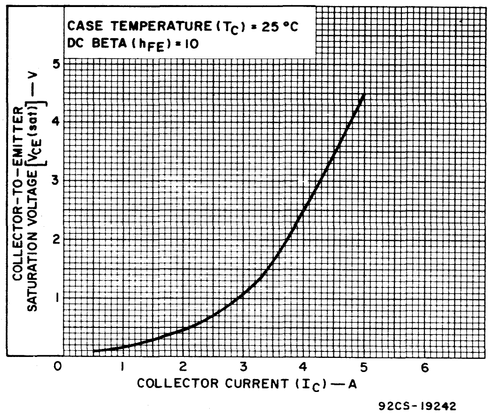


Fig.8—Typical saturation voltage characteristic.

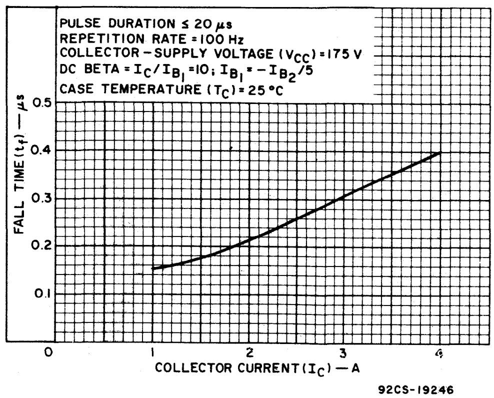


Fig.9—Typical fall time vs. collector current.

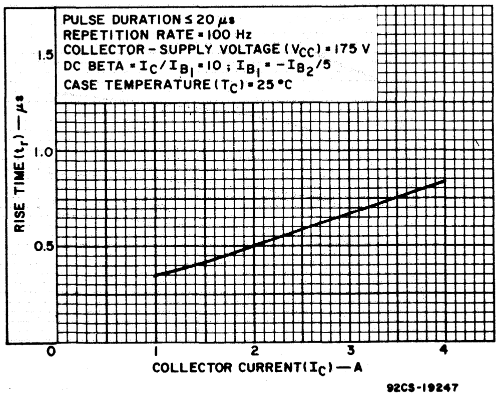


Fig. 10—Typical rise time vs. collector current.

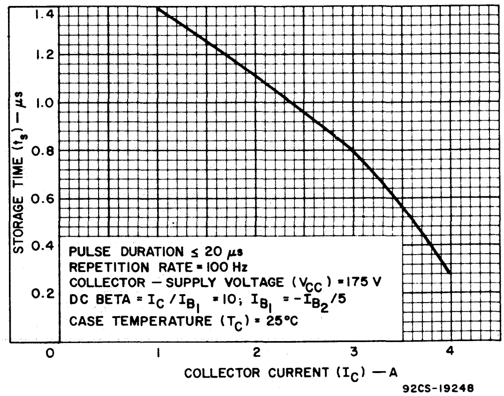
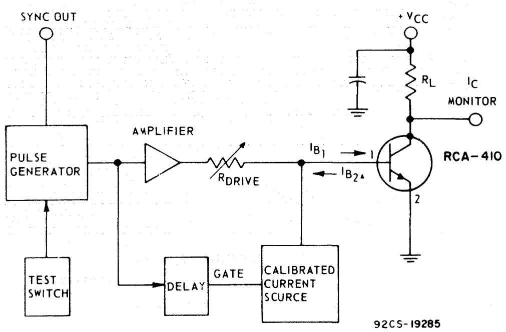


Fig. 11—Typical storage time vs. collector current.



*I_{B_1} AND I_{B_2} MEASURED WITH TEKTRONIX CURRENT PROBE P6019 OR EQUIVALENT

Fig. 12—Circuit used to measure switching times.

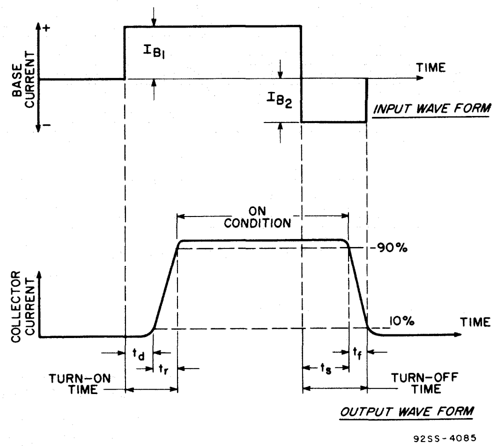
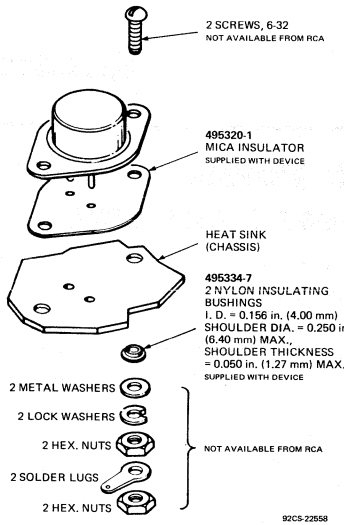


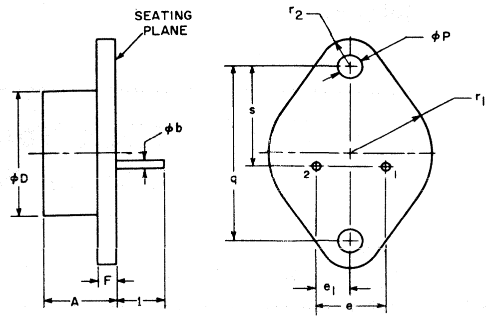
Fig. 13—Phase relationship between input and output currents showing reference points for specification of switching times. Test circuit shown in Fig. 12).



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 14—Suggested mounting hardware.

DIMENSIONAL OUTLINE
JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
ϕb	0.038	0.043	0.97	1.09	2
ϕD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e_1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
l	0.312		7.92		2
ϕP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r_1		0.525		13.34	
r_2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. **These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.**
2. **Two pins.**

92CS-15222

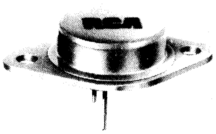
TERMINAL CONNECTIONS

Pin 1 — Base
Pin 2 — Emitter
Mounting Flange, Case — Collector

Solid State Division

Power Transistors

RCA411



JEDEC TO-3

H-1570

High-Voltage, High-Power Silicon N-P-N Power Transistor

For Switching and Linear Applications in Military, Industrial, and Commercial Equipment

Features:

- **Maximum safe-area-of-operation curves**
- **Low saturation voltage: V_{CE}(sat) = 0.8 V (max.)**
- **High voltage rating: V_{CEO}(sus) = 300 V**
- **High dissipation rating: P_T = 125 W**

RCA-411 is an epitaxial silicon n-p-n power transistor utilizing a multiple-emitter-site structure. This device employs the popular JEDEC TO-3 package.

Featuring high breakdown-voltage ratings and low saturation-voltage values, the RCA-411 is especially suitable for use in inverters, deflection circuits, switching regulators, high-voltage bridge amplifiers, ignition circuits, and other high-voltage switching applications.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	300	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE: With base open, V_{CEO}(sus)	300	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}	5	V
COLLECTOR CURRENT:		
Continuous, I_C	7	A
Peak	10	A
BASE CURRENT (Continuous), I_B	2	A
TRANSISTOR DISSIPATION, P_T:		
At case temperatures up to 25 °C and V_{CE} up to 75 V	125	W
At case temperatures up to 25 °C and V_{CE} above 75 V	See Fig. 2.	
At case temperatures above 25 °C and V_{CE} above 75 V	See Figs. 1 & 2.	
TEMPERATURE RANGE:		
Storage & Operating (Junction)	−65 to +200	°C
PIN TEMPERATURE (During Soldering):		
At distances ≥ 1/32 in. (0.8 mm) from case for 10 s max.	230	°C

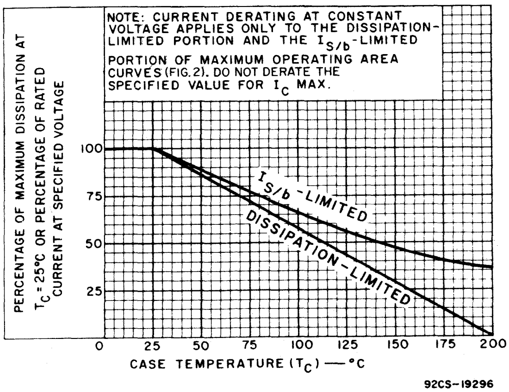


Fig. 1—Dissipation and current derating curves.

11-73

ELECTRICAL CHARACTERISTICS, Case Temperature (T_C) = 25°C Unless Otherwise Specified

Characteristic	Symbol	Test Conditions: DC Collector Voltage (V)	Test Conditions: DC Emitter or Base Voltage (V)		Test Conditions: DC Current (A)		Limits			Units
		V_{CE}	V_{EB}	V_{BE}	I_C	I_B	Min.	Typ.	Max.	
Collector-Cutoff Current: With base open	I_{CEO}	300					–	–	0.25	mA
With base-emitter junction reverse-biased	I_{CEV}	300		−1.5			–	–	0.25	mA
With base-emitter junction reverse-biased & T_C = 125°C	I_{CEV}	300		−1.5			–	–	0.5	mA
Emitter-Cutoff Current	I_{EBO}		5				–	–	5.0	mA
DC Forward-Current Transfer Ratio	h_{FE}	5 5			1.0[a] 2.5[a]		30 10	– –	90 –	
Collector-to-Emitter Sustaining Voltage: With base open (See Figs. 3 & 4.)	$V_{CEO}(sus)$[b]				0.1		300[b]	–	–	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$				1.0[a]	0.1	–	0.9	1.5	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				1.0[a]	0.1	–	0.2	0.8	V
Second-Breakdown Collector Current: (With base forward-biased) Pulse duration (non-repetitive) = 1 s	$I_{S/b}$[c]	150					0.3	–	–	A
Gain-Bandwidth Product	f_T	10			0.2		–	2.5	–	MHz
Switching Time: Rise (See Figs. 10, 12, & 13.)	t_r				1.0	0.1 (I_{B1}) −0.5 (I_{B2})	–	0.35	–	μs
Storage (See Figs. 11, 12, & 13.)	t_s				1.0	0.1 (I_{B1}) −0.5 (I_{B2})	–	1.4	–	μs
Fall (See Figs. 9, 12, & 13.)	t_f				1.0	0.1 (I_{B1}) −0.5 (I_{B2})	–	0.15	–	μs
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$	10			5		–	–	1.4	°C/W

[a] Pulsed; pulse duration $\leq$ 350 μs, duty factor = 2%.

[b] CAUTION: The sustaining voltage $V_{CEO}(sus)$ MUST NOT be measured on a curve tracer. The sustaining voltage should be measured by means of the test circuit shown in Fig. 3.

[c] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward-biased for transistor operation in the active region.

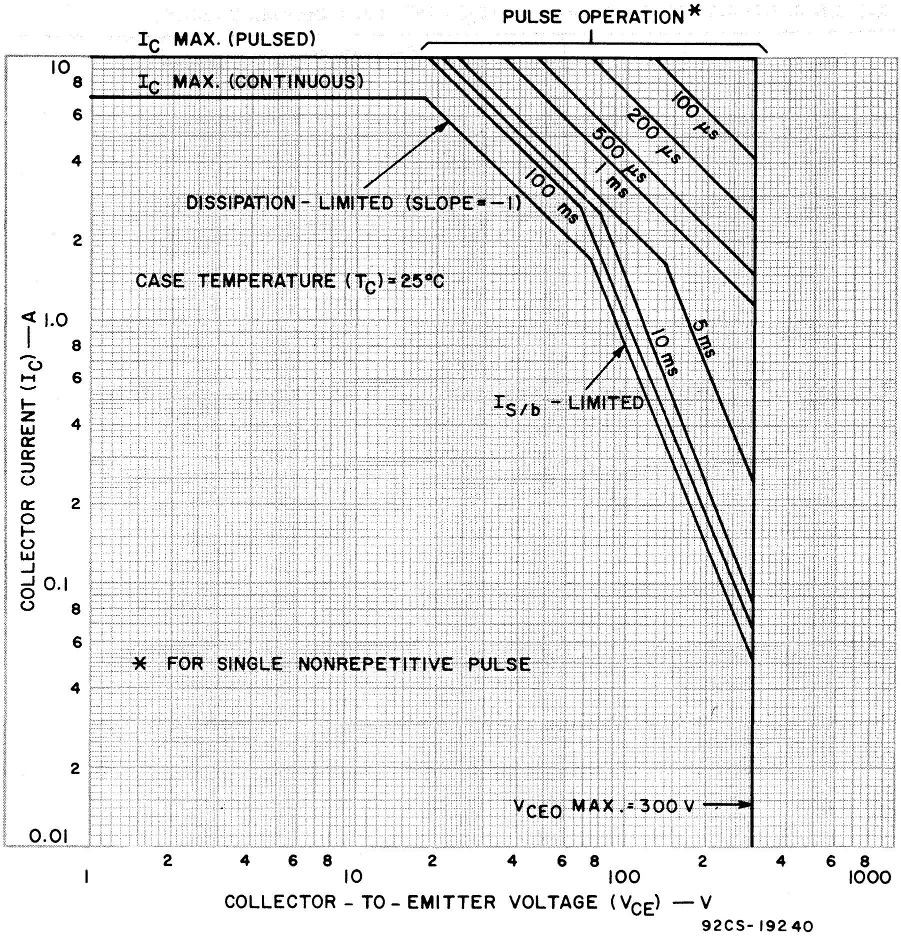


Fig.2—Maximum operating areas.

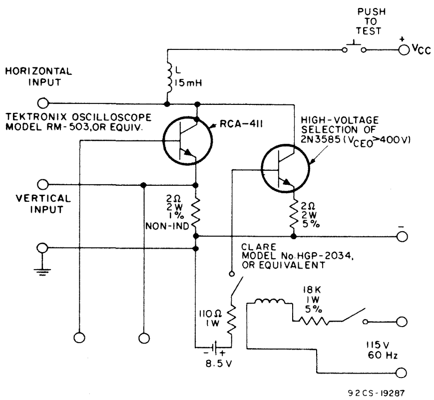


Fig.3—Circuit used to measure sustaining voltage, V_{CEO}(sus).

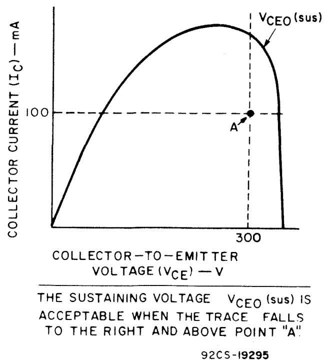


Fig.4—Oscilloscope display for measurement of sustaining voltage (test circuit shown in Fig.3).

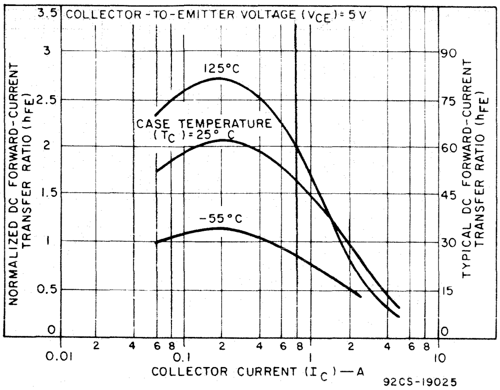


Fig.5—Typical dc beta characteristics.

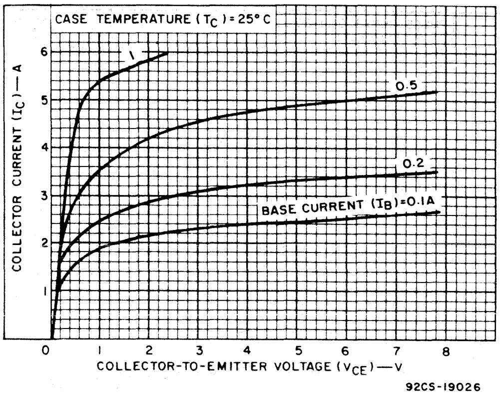


Fig.6—Typical output characteristics.

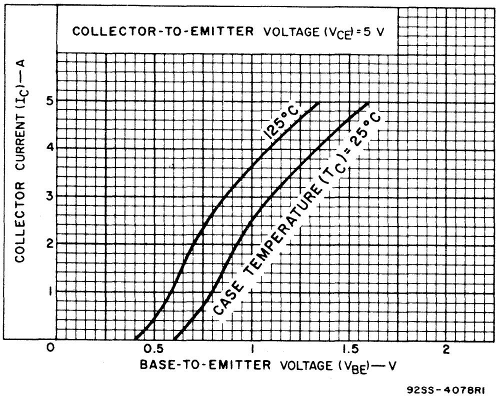


Fig.7—Typical transfer characteristics.

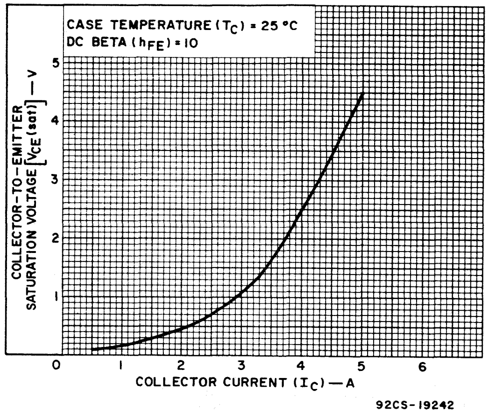


Fig.8—Typical saturation voltage characteristic.

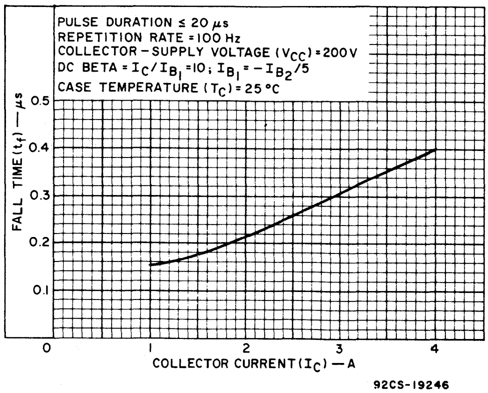


Fig.9—Typical fall time vs. collector current.

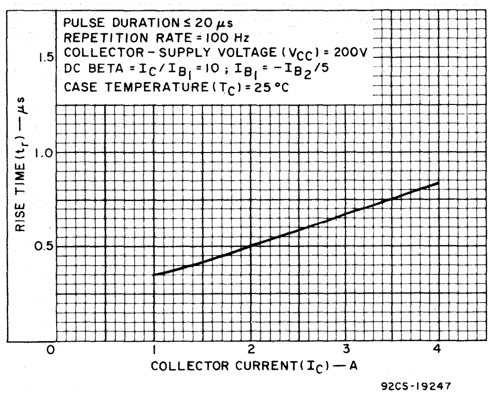


Fig. 10—Typical rise time vs. collector current.

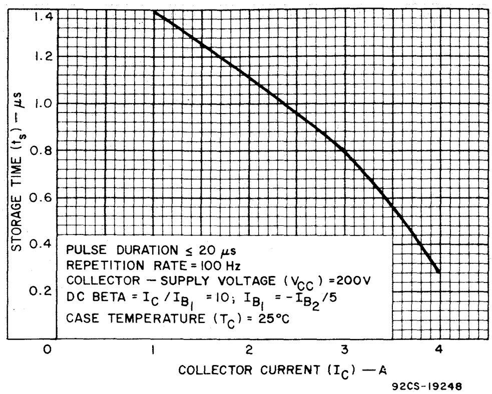


Fig. 11—Typical storage time vs. collector current.

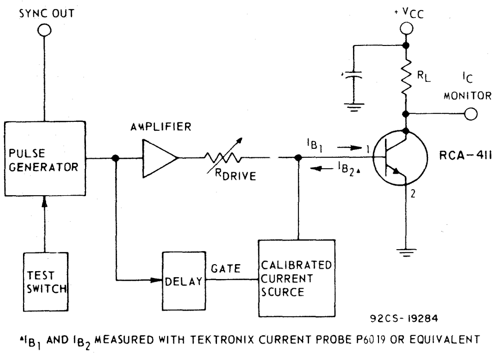


Fig. 12—Circuit used to measure switching times.

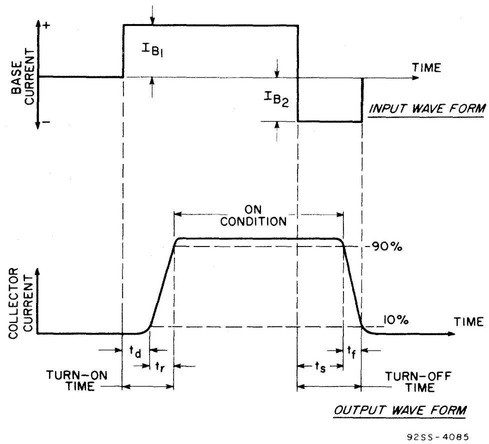
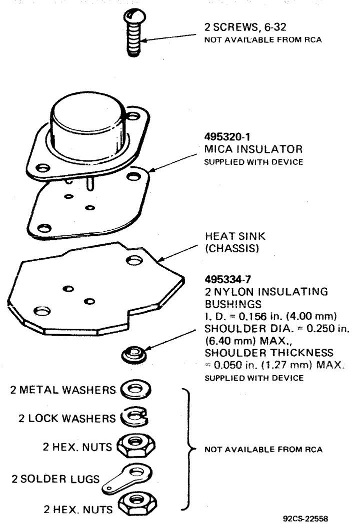


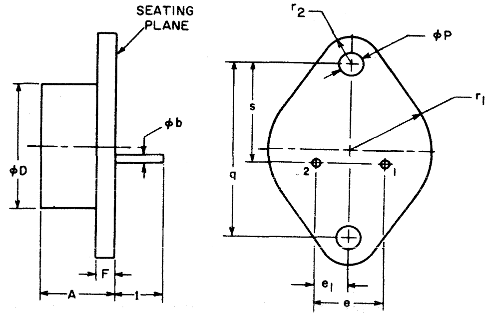
Fig. 13—Phase relationship between input and output currents showing reference points for specification of switching times. Test circuit shown in Fig. 12).



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.14 — Suggested mounting hardware.

DIMENSIONAL OUTLINE
JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
φb	0.038	0.043	0.97	1.09	2
φD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e_1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
l	0.312		7.92		2
φP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r_1		0.525		13.34	
r_2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS-15222

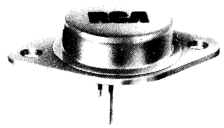
TERMINAL CONNECTIONS

Pin 1 — Base
Pin 2 — Emitter
Mounting Flange, Case — Collector

Solid State Division

Power Transistors

RCA413



JEDEC TO-3

H-1570

High-Voltage, High-Power Silicon N-P-N Power Transistor

For Switching and Linear Applications in Military, Industrial, and Commercial Equipment

Features:

- **Maximum safe-area-of-operation curves**
- **Low saturation voltage: $V_{CE}(sat)$ = 0.8 V (max.)**
- **High voltage rating: $V_{CEO}(sus)$ = 325 V**
- **High dissipation rating: P_T = 125 W**

RCA-413 is an epitaxial silicon n-p-n power transistor utilizing a multiple-emitter-site structure. This device employs the popular JEDEC TO-3 package.

Featuring high breakdown-voltage ratings and low saturation-voltage values, the RCA-413 is especially suitable for use in inverters, deflection circuits, switching regulators, high-voltage bridge amplifiers, ignition circuits, and other high-voltage switching applications.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	400	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE With base open, $V_{CEO}(sus)$	325	V
COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE: With base open, $V_{(BR)CEO}$	400	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}	5	V
COLLECTOR CURRENT: Continuous, I_C	7	A
Peak	10	A
BASE CURRENT (Continuous), I_B	2	A
TRANSISTOR DISSIPATION, P_T: At case temperatures up to 25°C and V_{CE} up to 75 V	125	W
At case temperatures up to 25°C and V_{CE} above 75 V	See Fig. 2.	
At case temperatures above 25°C and V_{CE} above 75 V	See Figs. 1 & 2.	
TEMPERATURE RANGE: Storage & Operating (Junction)	−65 to +200	°C
PIN TEMPERATURE (During Soldering): At distances ≥ 1/32 in. (0.8 mm) from case for 10 s max.	230	°C

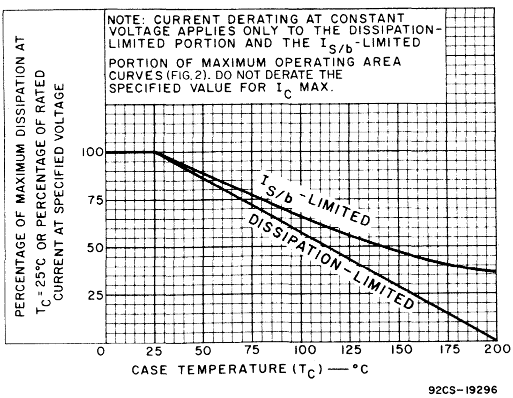


Fig. 1—Dissipation and current derating curves.

ELECTRICAL CHARACTERISTICS, Case Temperature (T_C) = 25°C Unless Otherwise Specified

Characteristic	Symbol	Test Conditions					Limits			Units
		DC Collector Voltage (V)	DC Emitter or Base Voltage (V)		DC Current (A)					
		V_{CE}	V_{EB}	V_{BE}	I_C	I_B	Min.	Typ.	Max.	
Collector-Cutoff Current: With base open	I_{CEO}	400					–	–	0.25	
With base-emitter junction reverse-biased	I_{CEV}	400		−1.5			–	–	0.25	mA
With base-emitter junction reverse-biased & T_C = 125°C	I_{CEV}	400		−1.5			–	–	0.5	
Emitter-Cutoff Current	I_{EBO}		5				–	–	5.0	mA
DC Forward-Current Transfer Ratio	h_{FE}	5 5			0.5[a] 1.0[a]		20 15	– –	80 –	
Collector-to-Emitter Sustaining Voltage: With base open (See Figs. 3 & 4.)	$V_{CEO}(sus)$[b]				0.1		325[b]	–	–	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$				0.5[a]	0.05	–	0.8	1.5	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				0.5[a]	0.05	–	0.15	0.8	V
Second-Breakdown Collector Current: (With base forward-biased) Pulse duration (non-repetitive) = 1 s	$I_{S/b}$[c]	150					0.3	–	–	A
Gain-Bandwidth Product	f_T	10			0.2		–	4.0	–	MHz
Switching Time: Rise (See Figs. 10, 12, & 13.)	t_r				1.0	0.1 (I_{B1}) −0.5 (I_{B2})	–	0.35	–	
Storage (See Figs. 11, 12, & 13.)	t_s				1.0	0.1 (I_{B1}) −0.5 (I_{B2})	–	1.4	–	μs
Fall (See Figs. 9, 12, & 13.)	t_f				1.0	0.1 (I_{B1}) −0.5 (I_{B2})	–	0.15	–	
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$	10			5		–	–	1.4	°C/W

[a] Pulsed; pulse duration $\leq$350 μs, duty factor = 2%

[b] CAUTION: The sustaining voltage $V_{CEO}(sus)$ MUST NOT be measured on a curve tracer. The sustaining voltage should be measured by means of the test circuit shown in Fig. 3.

[c] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward-biased for transistor operation in the active region.

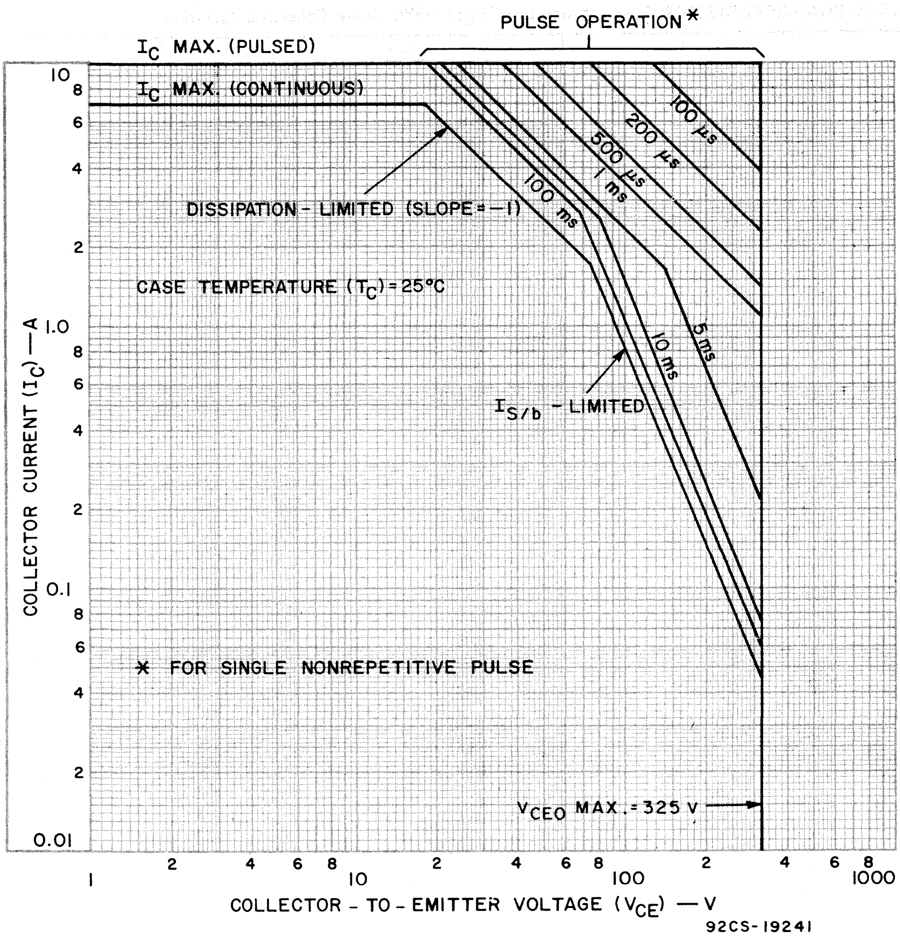


Fig.2—Maximum operating areas.

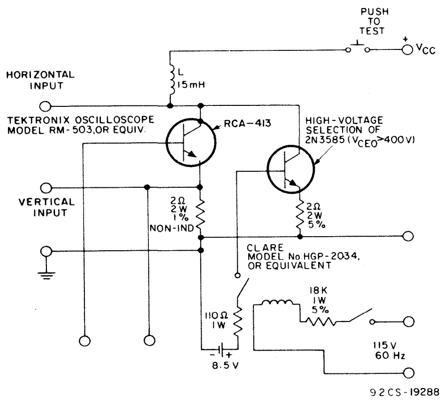


Fig.3—Circuit used to measure sustaining voltage, V_{CEO}(sus).

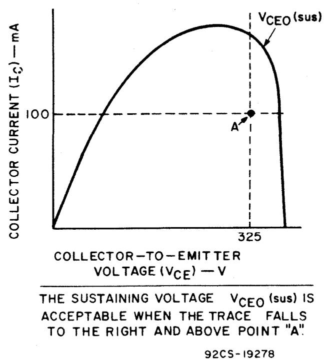


Fig.4—Oscilloscope display for measurement of sustaining voltage (test circuit shown in Fig. 3).

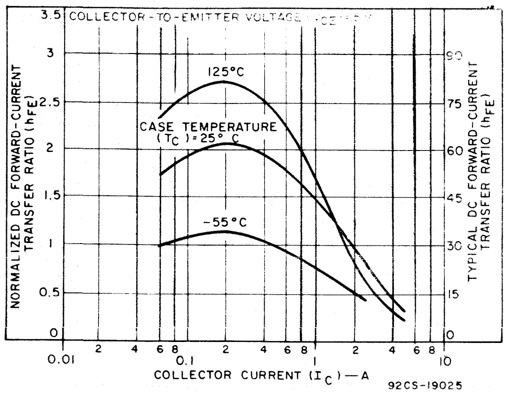


Fig.5—Typical dc beta characteristics.

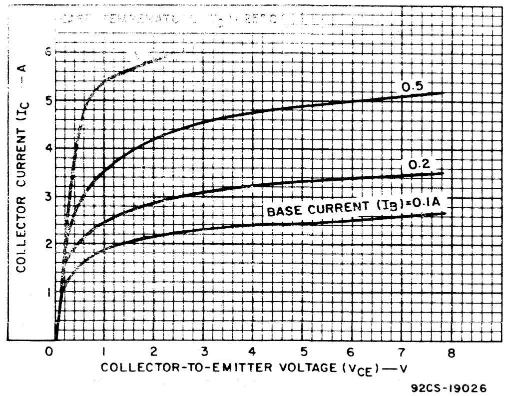


Fig.6—Typical output characteristics.

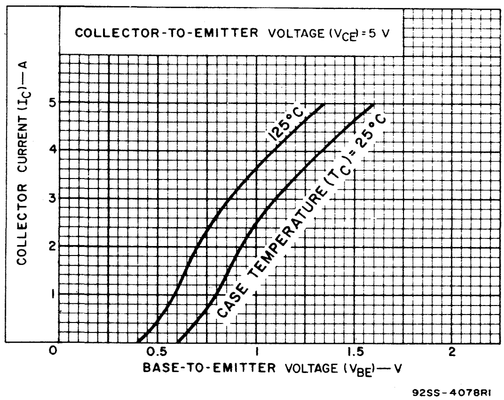


Fig.7—Typical transfer characteristics.

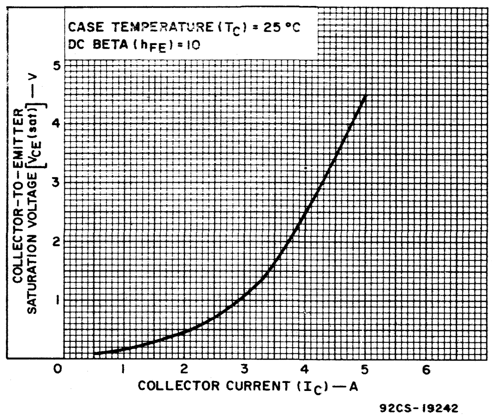


Fig.8—Typical saturation voltage characteristic.

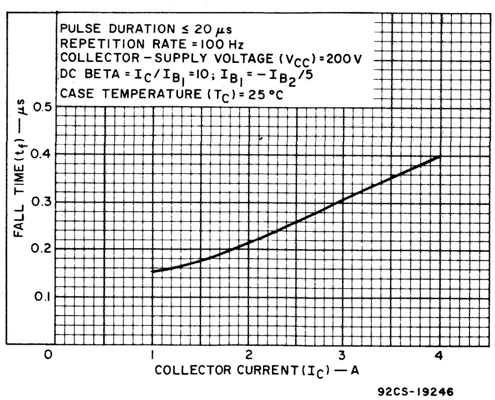


Fig.9—Typical fall time vs. collector current.

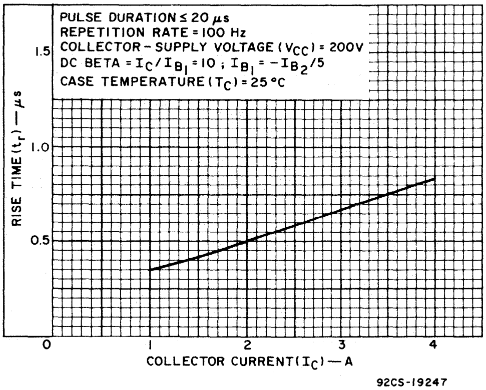


Fig.10—Typical rise time vs. collector current.

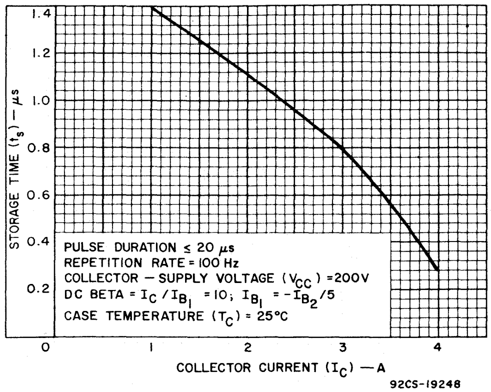


Fig.11—Typical storage time vs. collector current.

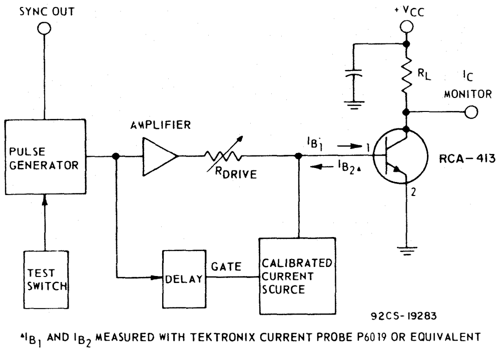


Fig.12—Circuit used to measure switching times.

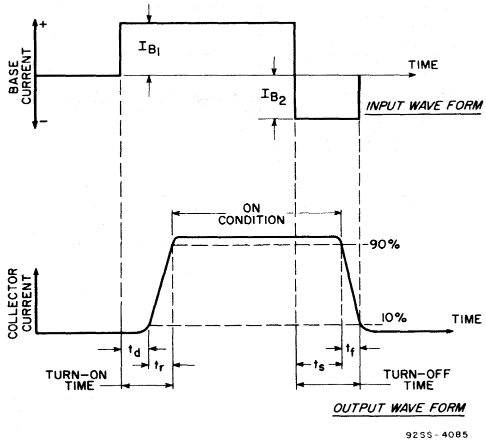
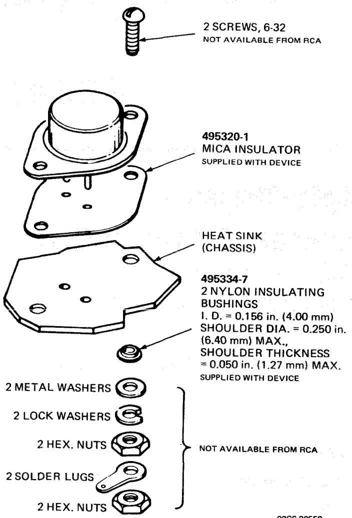


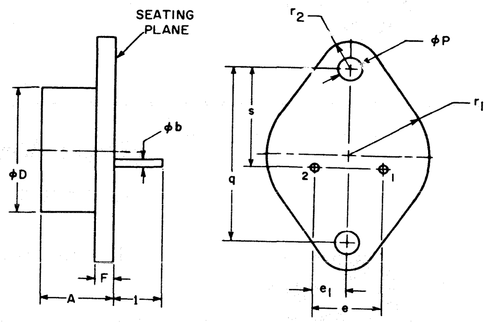
Fig.13—Phase relationship between input and output currents showing reference points for specification of switching times. (Test circuit shown in Fig.12).



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.14 – Suggested mounting hardware.

DIMENSIONAL OUTLINE
JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
ϕb	0.038	0.043	0.97	1.09	2
ϕD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
l	0.312		7.92		2
ϕP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r1		0.525		13.34	
r2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS-15222

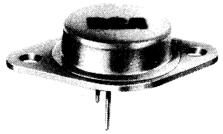
TERMINAL CONNECTIONS

Pin 1 – Base
Pin 2 – Emitter
Mounting Flange, Case – Collector

RCA Solid State Division

Power Transistors

RCA423



JEDEC TO-3

H-1570

High-Voltage, High-Power Silicon N-P-N Power Transistor

For Switching and Linear Applications in Military, Industrial, and Commercial Equipment

Features:

- **Maximum safe-area-of-operation curves**
- **Low saturation voltage: $V_{CE}(sat)$ = 0.8 V (max.)**
- **High voltage rating: $V_{CEO}(sus)$ = 325 V**
- **High dissipation rating: P_T = 125 W**

RCA-423 is an epitaxial silicon n-p-n power transistor utilizing a multiple-emitter-site structure. This device employs the popular JEDEC TO-3 package.

Featuring high breakdown-voltage ratings and low saturation-voltage values, the RCA-423 is especially suitable for use in inverters, deflection circuits, switching regulators, high-voltage bridge amplifiers, ignition circuits, and other high-voltage switching applications.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	400	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE: With base open, $V_{CEO}(sus)$	325	V
COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE: With base open, $V_{(BR)CEO}$	400	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}	5	V
COLLECTOR CURRENT: Continuous, I_C	7	A
Peak	10	A
BASE CURRENT (Continuous), I_B	2	A
TRANSISTOR DISSIPATION, P_T: At case temperatures up to 25 °C and V_{CE} up to 75 V	125	W
At case temperatures up to 25 °C and V_{CE} above 75 V	See Fig. 2.	
At case temperatures above 25 °C and V_{CE} above 75 V	See Figs. 1 & 2.	
TEMPERATURE RANGE: Storage & Operating (Junction)	−65 to +200	°C
PIN TEMPERATURE (During Soldering): At distances ≥ 1/32 in. (0.8 mm) from case for 10 s max.	230	°C

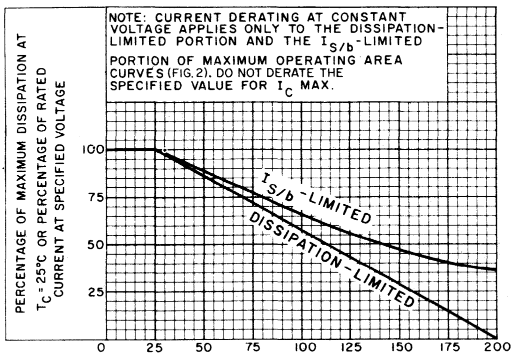


Fig. 1—Dissipation and current derating curves.

11-73

ELECTRICAL CHARACTERISTICS, Case Temperature (T_C) = 25°C Unless Otherwise Specified

Characteristic	Symbol	Test Conditions					Limits			Units
		DC Collector Voltage (V)	DC Emitter or Base Voltage (V)		DC Current (A)					
		V_{CE}	V_{EB}	V_{BE}	I_C	I_B	Min.	Typ.	Max.	
Collector-Cutoff Current: With base open	I_{CEO}	400					–	–	0.25	
With base-emitter junction reverse-biased	I_{CEV}	400		−1.5			–	–	0.25	mA
With base-emitter junction reverse-biased & T_C = 125°C	I_{CEV}			−1.5			–	–	0.5	
Emitter-Cutoff Current	I_{EBO}		5				–	–	5.0	mA
DC Forward-Current Transfer Ratio	h_{FE}	5 5			1.0[a] 2.5[a]		30 10	– –	90 –	
Collector-to-Emitter Sustaining Voltage: With base open (See Figs. 3 & 4.)	$V_{CEO}(sus)$[b]				0.1		325[b]	–	–	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$				1.0[a]	0.1	–	0.9	1.5	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				1.0[a]	0.1	–	0.2	0.8	V
Second-Breakdown Collector Current: (With base forward-biased) Pulse duration (non-repetitive) = 1 s	$I_{S/b}$[c]	150					0.3	–	–	A
Gain-Bandwidth Product	f_T	10			0.2		–	4.0	–	MHz
Switching Time: Rise (See Figs. 10, 12, & 13.)	t_r				1.0	0.1 (I_{B1}) −0.5 (I_{B2})	–	0.35	–	
Storage (See Figs. 11, 12, & 13.)	t_s				1.0	0.1 (I_{B1}) −0.5 (I_{B2})	–	1.4	–	μs
Fall (See Figs. 9, 12, & 13.)	t_f				1.0	0.1 (I_{B1}) −0.5 (I_{B2})	–	0.15	–	
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$	10			5		–	–	1.4	°C/W

[a] Pulsed; pulse duration $\leq$350 μs, duty factor = 2%.

[b] CAUTION: The sustaining voltage $V_{CEO}(sus)$ MUST NOT be measured on a curve tracer. The sustaining voltage should be measured by means of the test circuit shown in Fig. 3.

[c] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward-biased for transistor operation in the active region.

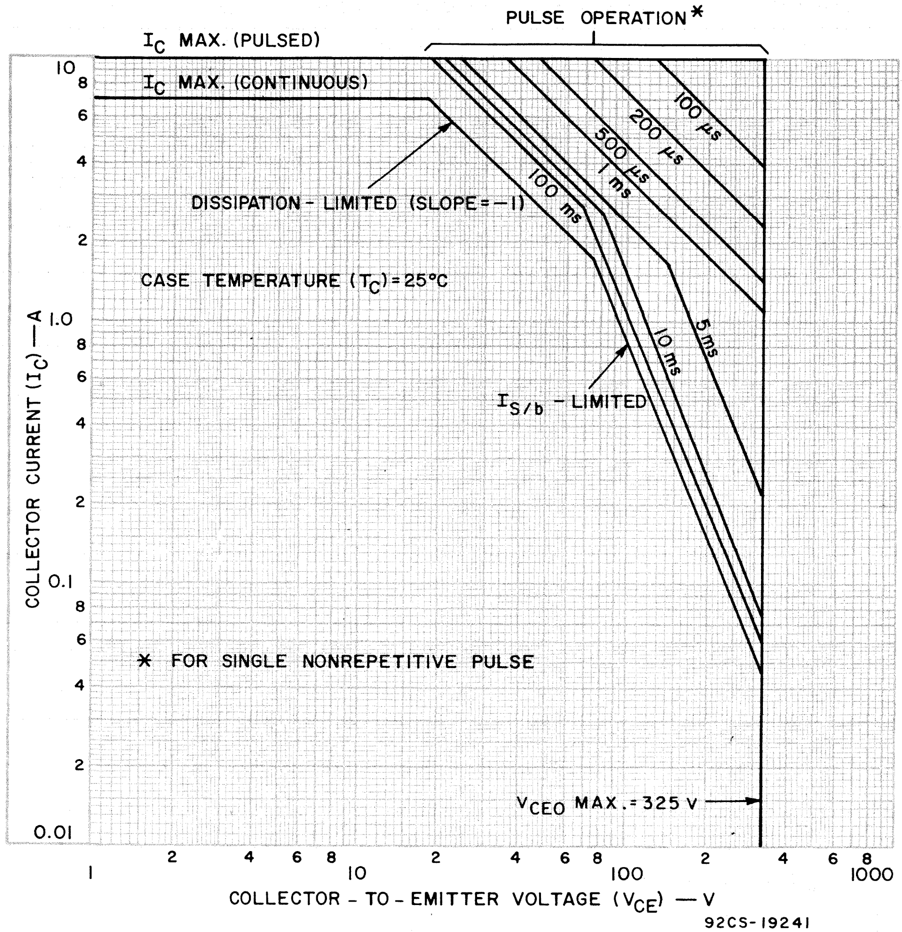


Fig.2—Maximum operating areas.

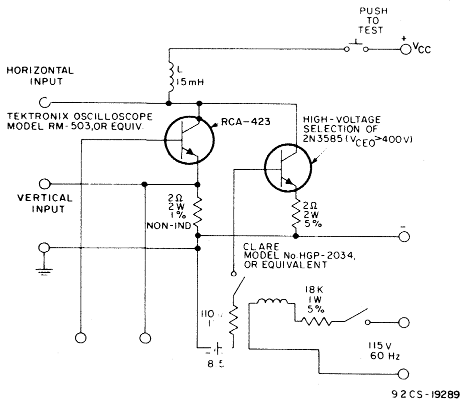


Fig.3—Circuit used to measure sustaining voltage, V_{CEO}(sus).

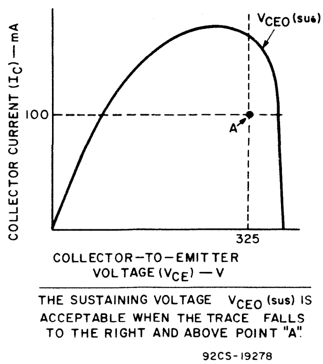


Fig.4—Oscilloscope display for measurement of sustaining voltage (test circuit shown in Fig.3).

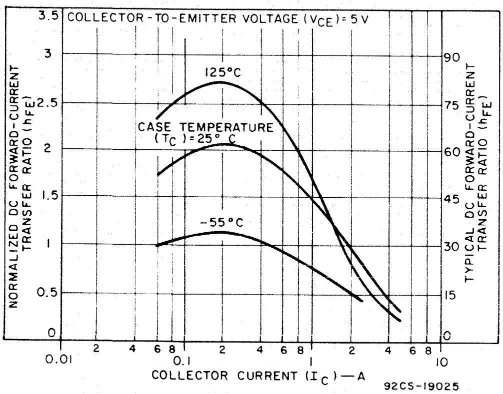


Fig.5—Typical dc beta characteristics.

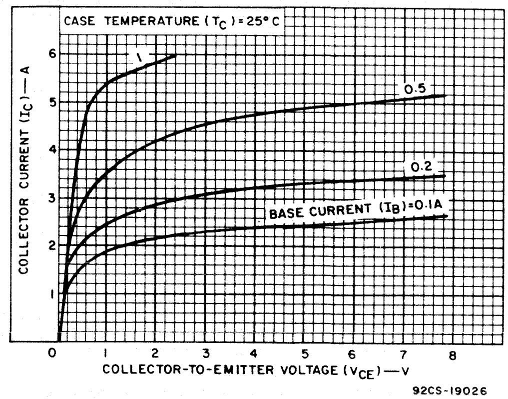


Fig.6—Typical output characteristics.

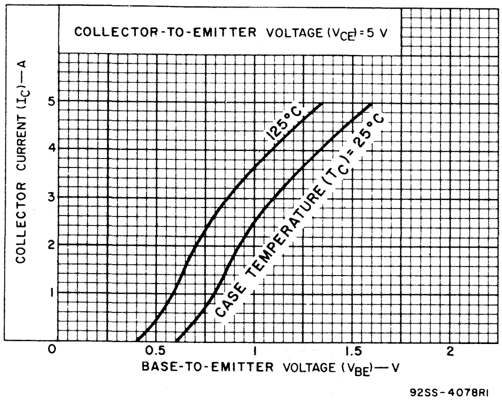


Fig.7—Typical transfer characteristics.

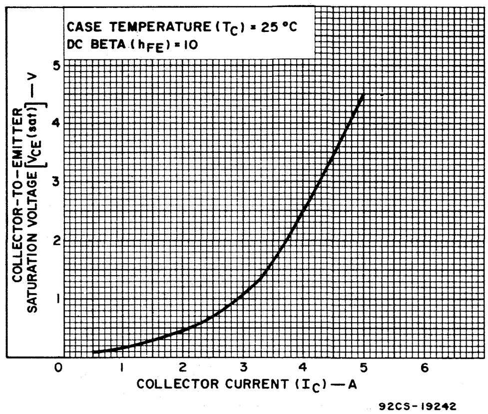


Fig.8—Typical saturation voltage characteristic.

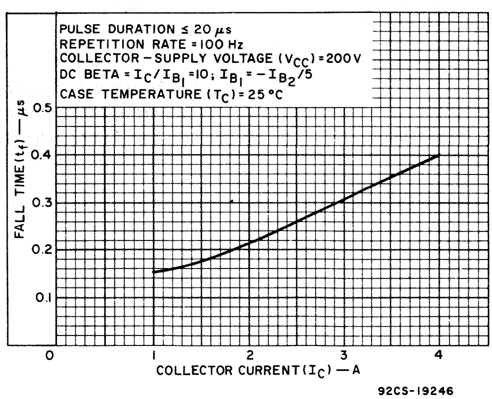


Fig.9—Typical fall time vs. collector current.

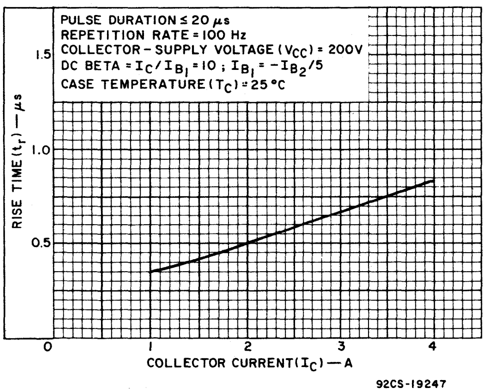


Fig.10—Typical rise time vs. collector current.

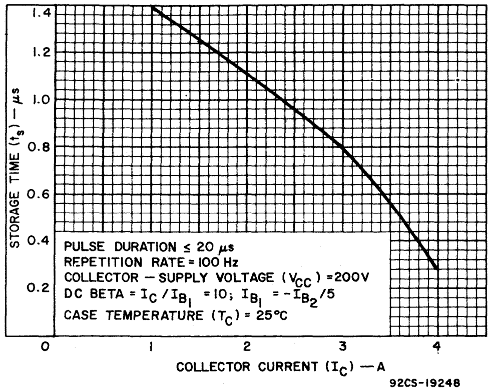
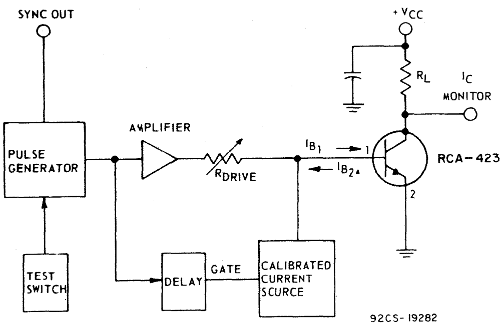


Fig.11—Typical storage time vs. collector current.



*I_{B_1} AND I_{B_2} MEASURED WITH TEKTRONIX CURRENT PROBE P6019 OR EQUIVALENT

Fig.12—Circuit used to measure switching times.

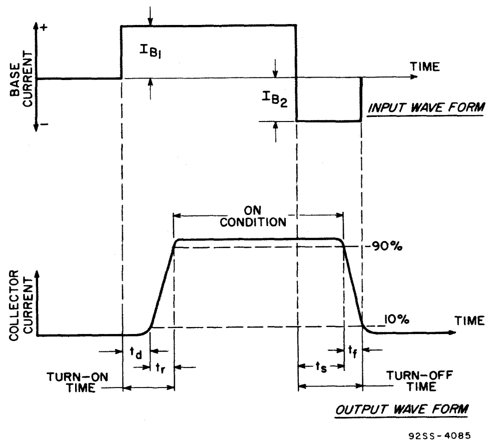
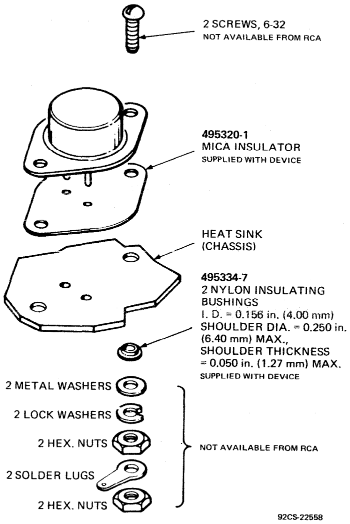


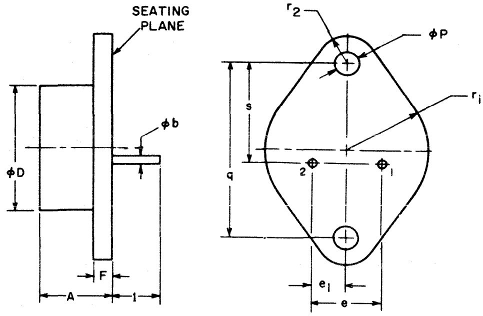
Fig.13—Phase relationship between input and output currents showing reference points for specification of switching times. (Test circuit shown in Fig.12).



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 14—Suggested mounting hardware.

DIMENSIONAL OUTLINE
JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
φb	0.038	0.043	0.97	1.09	2
φD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e_1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
l	0.312		7.92		2
φP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r_1		0.525		13.34	
r_2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. **These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.**
2. **Two pins.**

92CS-15222

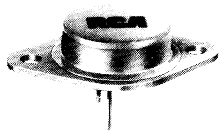
TERMINAL CONNECTIONS

Pin 1 — Base
Pin 2 — Emitter
Mounting Flange, Case — Collector

RCA
Solid State Division

Power Transistors

RCA431



JEDEC TO-3

H-1570

High-Voltage, High-Power Silicon N-P-N Power Transistor

For Switching and Linear Applications in Military, Industrial, and Commercial Equipment

Features:

- **Maximum safe-area-of operation curves**
- **Low saturation voltage: V_{CE}(sat) = 0.7 V (max.)**
- **High voltage rating: V_{CEO}(sus) = 325 V**
- **High dissipation rating: P_T = 125 W**

RCA-431 is an epitaxial silicon n-p-n power transistor utilizing a multiple-emitter-site structure. This device employs the popular JEDEC TO-3 package.

Featuring high breakdown-voltage ratings and low saturation-voltage values, the RCA-431 is especially suitable for use in inverters, deflection circuits, switching regulators, high-voltage bridge amplifiers, ignition circuits, and other high-voltage switching applications.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	400	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE		
With base open, V_{CEO}(sus)	325	V
COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE:		
With base open, $V_{(BR)CEO}$	400	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}	5	V
COLLECTOR CURRENT:		
Continuous, I_C	7	A
Peak	10	A
BASE CURRENT (Continuous), I_B	2	A
TRANSISTOR DISSIPATION, P_T:		
At case temperatures up to 25°C and V_{CE} up to 75 V	125	W
At case temperatures up to 25°C and V_{CE} above 75 V	See Fig. 2.	
At case temperatures above 25°C and V_{CE} above 75 V	See Figs. 1 & 2.	
TEMPERATURE RANGE:		
Storage & Operating (Junction)	−65 to +200	°C
PIN TEMPERATURE (During Soldering):		
At distances ≥ 1/32 in. (0.8 mm) from case for 10 s max.	230	°C

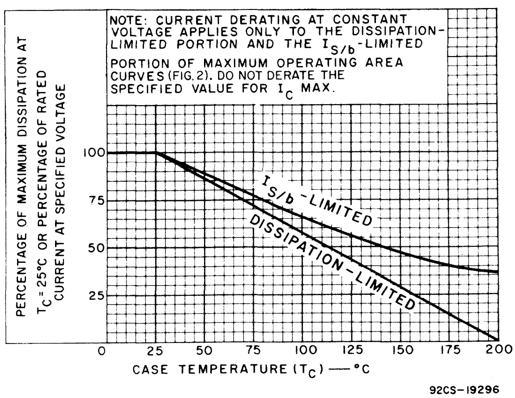


Fig. 1—Dissipation and current derating curves.

ELECTRICAL CHARACTERISTICS, Case Temperature (T_C) = 25°C Unless Otherwise Specified

Characteristic	Symbol	Test Conditions					Limits			Units
		DC Collector Voltage (V)	DC Emitter or Base Voltage (V)		DC Current (A)					
		V_{CE}	V_{EB}	V_{BE}	I_C	I_B	Min.	Typ.	Max.	
Collector-Cutoff Current: With base open	I_{CEO}	400					–	–	2.5	mA
With base-emitter junction reverse-biased	I_{CEV}	400		−1.5			–	–	2.5	mA
With base-emitter junction reverse-biased & T_C = 125°C	I_{CEV}	400		−1.5			–	–	5.0	mA
Emitter-Cutoff Current	I_{EBO}		5				–	–	2.0	mA
DC Forward-Current Transfer Ratio	h_{FE}	5 5			2.5[a] 3.5[a]		15 10	– –	35 –	
Collector-to-Emitter Sustaining Voltage: With base open (See Figs. 3 & 4.)	$V_{CEO}(sus)$[b]				0.1		325[b]	–	–	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$				2.5[a]	0.5	–	–	1.5	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				2.5[a]	0.5	–	0.25	0.7	V
Second-Breakdown Collector Current: (With base forward-biased) Pulse duration (non-repetitive) = 1 s	$I_{S/b}$[c]	150					0.3	–	–	A
Gain-Bandwidth Product	f_T	10			0.2		–	4.0	–	MHz
Switching Time: Rise (See Figs. 10, 12, & 13.)	t_r				2.5	0.5 (I_{B1})[d]	–	0.35	–	μs
Storage (See Figs. 11, 12, & 13.)	t_s				2.5	0.5 (I_{B1})[d]	–	1.8	–	μs
Fall (See Figs. 9, 12, & 13.)	t_f				2.5	0.5 (I_{B1})[d]	–	0.4	–	μs
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$	10			5		–	–	1.4	°C/W

[a] Pulsed; pulse duration ≤350 μs, duty factor = 2%

[b] CAUTION: The sustaining voltage $V_{CEO}(sus)$ MUST NOT be measured on a curve tracer. The sustaining voltage should be measured by means of the test circuit shown in Fig. 3.

[c] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward-biased for transistor operation in the active region.

[d] $I_{B1} = -I_{B2}$ = value shown.

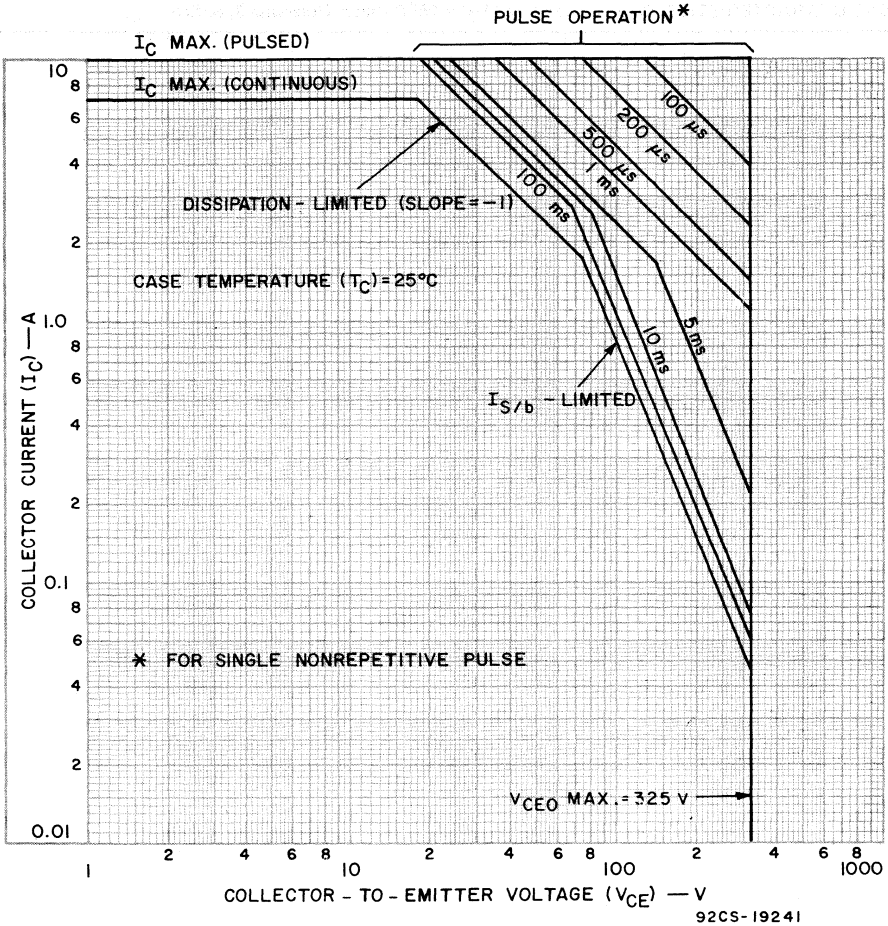


Fig.2—Maximum operating areas.

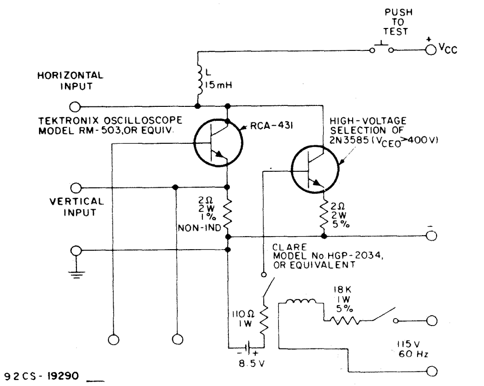


Fig.3—Circuit used to measure sustaining voltage, V_{CEO}(sus).

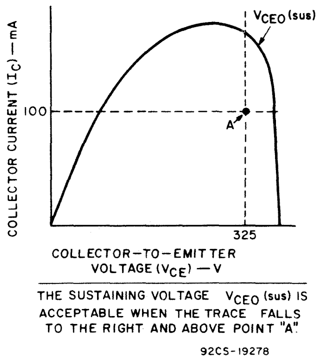


Fig.4—Oscilloscope display for measurement of sustaining voltage (test circuit shown in Fig. 3).

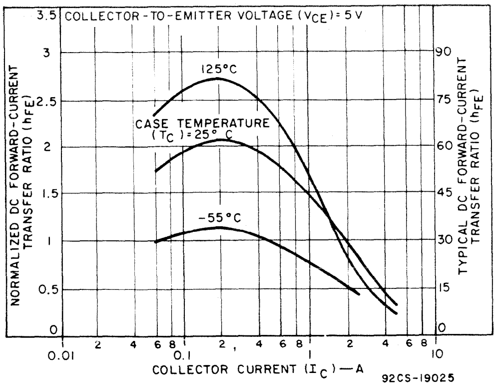


Fig.5—Typical dc beta characteristics.

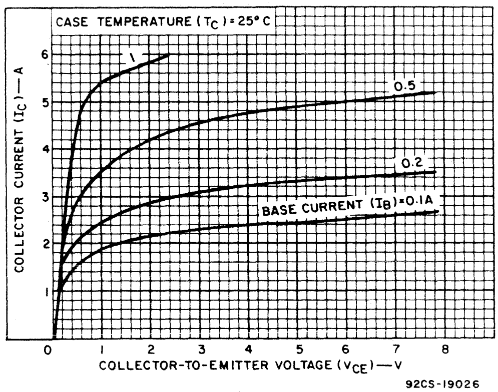


Fig.6—Typical output characteristics.

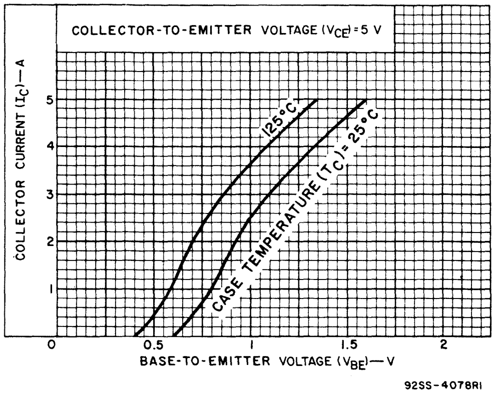


Fig.7—Typical transfer characteristics.

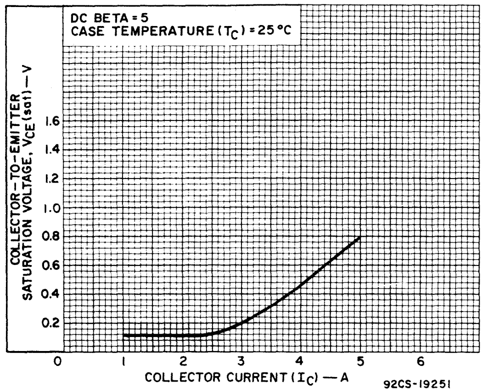


Fig.8—Saturation voltage vs. collector current.

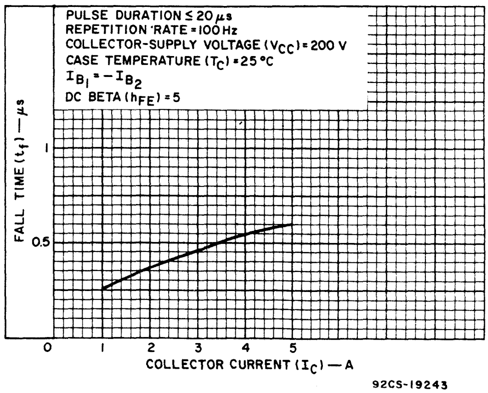


Fig.9—Typical fall-time characteristic.

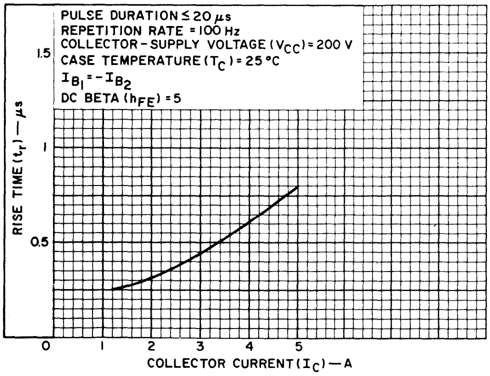


Fig.10—Typical rise-time characteristic.

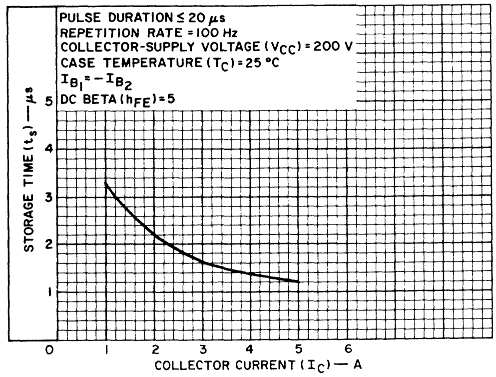
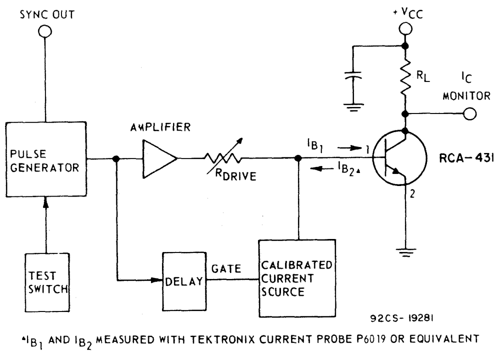


Fig.11—Typical storage-time characteristic (with constant forced gain).



*IB1 AND IB2 MEASURED WITH TEKTRONIX CURRENT PROBE P6019 OR EQUIVALENT

Fig.12—Circuit used to measure switching times.

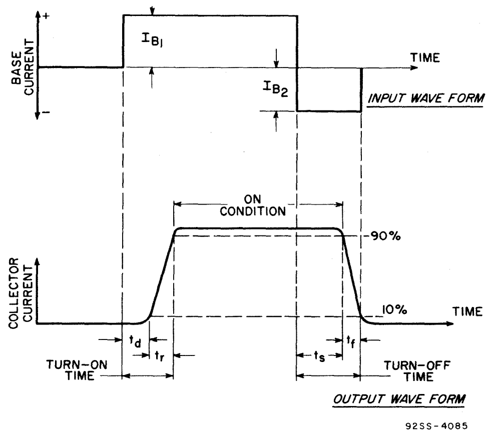
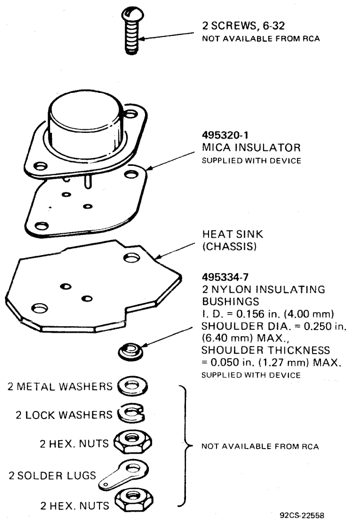


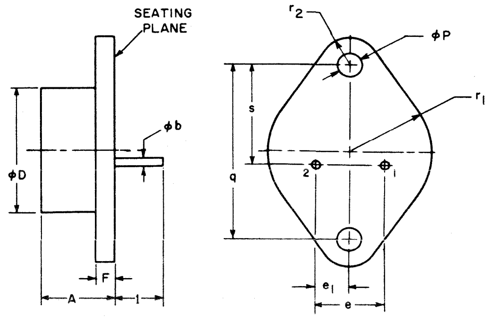
Fig.13—Phase relationship between input and output currents showing reference points for specification of switching times. (Test circuit shown in Fig.12).



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 14 — Suggested mounting hardware.

DIMENSIONAL OUTLINE
JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
φb	0.038	0.043	0.97	1.09	2
φD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
l	0.312		7.92		2
φP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r1		0.525		13.34	
r2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS-15222

TERMINAL CONNECTIONS

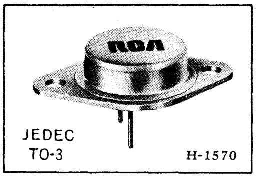
Pin 1 — Base
Pin 2 — Emitter
Mounting Flange, Case — Collector

Solid State
Division

Power Transistors

2N5838
2N5839
2N5840

SILICON N-P-N POWER TRANSISTORS



High-Voltage High-Power Types For Switching and Linear Applications in Military, Industrial, and Commercial Equipment

RCA 2N5838, 2N5839 and 2N5840** are epitaxial silicon n-p-n power transistors utilizing a multiple-emitter-site structure. These devices employ the popular JEDEC TO-3 package; they differ mainly in voltage, current-gain, and V_{CE}(sat) ratings.

Featuring high breakdown voltage ratings and low-saturation voltage values, the 2N5838, 2N5839 and 2N5840 are especially suitable for use in inverters, deflection circuits, switching regulators, high-voltage bridge amplifiers, ignition circuits, and other high-voltage switching applications.

** Formerly RCA Dev. types TA7513, TA7530, and TA7420 respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	2N5838	2N5839	2N5840	
*COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	275	300	375	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:				
* With base open, V_{CEO}(sus)	250	275	350	V
With reverse bias (V_{BE}) of -1.5 V, V_{CEV}(sus)▲	275	300	375	V
With external base-to-emitter resistance (R_{BE}) $\leq$ 50 Ω, V_{CER}(sus)	275	300	375	V
*EMITTER-TO-BASE VOLTAGE, V_{EBO}	6	6	6	V
*COLLECTOR CURRENT, I_C				
Continuous	3	3	3	A
Peak	5	5	5	A
*CONTINUOUS BASE CURRENT, I_B	1.5	1.5	1.5	A
*TRANSISTOR DISSIPATION, P_T:				
At case temperature up to 25° C and V_{CE} up to 40 V	100	100	100	W
At case temperatures up to 25° C and V_{CE} above 40 V	See Fig. 2.			
At case temperatures above 25° C and V_{CE} above 40 V	See Figs. 1 & 2.			
*TEMPERATURE RANGE:				
Storage & Operating (Junction)	-65 to +200			°C
*PIN TEMPERATURE (During Soldering):				
At distances $\geq$ 1/32 in. (0.8 mm) from case for 10 s max	230			°C

* In accordance with JEDEC registration data format (JS-6, RDF-1).
▲ Shown as V_{CEX}(sus) in JEDEC Registration Data.

Features:

- **Maximum safe-area-of-operation curves**
- **Low saturation voltages**
- **High voltage ratings**
  V_{CER}(sus) = 375 V (2N5840)
  300 V (2N5839)
  275 V (2N5838)
- **High dissipation rating**
  P_T = 100 W

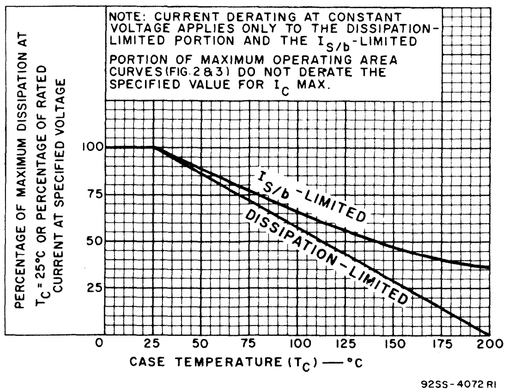


Fig. 1 - Derating curves for all types.

ELECTRICAL CHARACTERISTICS, *Case Temperature* (T_C) = 25°C

Characteristic	Symbol	Test Conditions: DC Collector Voltage (V)	Test Conditions: DC Emitter or Base Voltage (V)		Test Conditions: DC Current (A)			Limits: Type 2N5838			Limits: Type 2N5839			Limits: Type 2N5840			Units
		V_{CE}	V_{EB}	V_{BE}	I_C	I_B	I_E	Min.	Max.	Typ.	Min.	Max.	Typ.	Min.	Max.	Typ.	
Collector-Cutoff Current: With base open	I_{CEO}	200 250						- -	2 -	- -	- -	- 2	- -	- -	- 2	- -	mA
* With base-emitter junction reverse biased	I_{CEV}	265 290 360		-1.5 -1.5 -1.5				- - -	5 - -	- - -	- - -	- 2 -	- - -	- - -	- - 2	- - -	mA
* With base-emitter junction reverse biased	I_{CEV} T_C = 100 °C	265 290 360		-1.5 -1.5 -1.5				- - -	8 - -	- - -	- - -	- 5 -	- - -	- - -	- - 5	- - -	mA
* Emitter-Cutoff Current	I_{EBO}		6					-	1	-	-	1	-	-	1	-	mA
* Collector-to-Emitter Sustaining Voltage: *(See Figs. 4, 5, & 6)* With base open	$V_{CEO}(sus)$[a]				0.2			250[b]	-	-	275[b]	-	-	350[b]	-	-	V
* With base-emitter junction reversed biased	$V_{CEX}(sus)$[a]			-1.5	0.1			275[b]	-	-	300[b]	-	-	375[b]	-	-	V
With external base-to-emitter resistance (R_{BE}) = 50 Ω	$V_{CER}(sus)$[a]				0.2			275[b]	-	-	300[b]	-	-	375[b]	-	-	V
* Emitter-to-Base Voltage	V_{EBO}				0.02			6	-	-	6	-	-	6	-	-	V
* DC Forward-Current Transfer Ratio	h_{FE}	5 3 2			0.5[b] 2[b] 3[b]			20 - 8	- - 40	- - -	20 10 -	- 50 -	- - -	20 10 -	- 50 -	- - -	
* Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$				2 3	0.2 0.375		- -	- 2	- -	- -	2 -	- -	- -	2 -	- -	V
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				2 3	0.2 0.375		- -	- 1	- -	- -	1.5 -	- -	- -	1.5 -	- -	V
Output Capacitance (At 1 MHz)	C_{obo}		10				0	-	150	-	-	150	-	-	150	-	pF
* Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward-Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	10			0.2			5	-	-	5	-	-	5	-	-	
Second Breakdown Collector Current (With base forward biased) Pulse duration (non-repetitive) = 1 s	$I_{S/b}$[c]	40						2.5	-	-	2.5	-	-	2.5	-	-	A
Second Breakdown[c] Energy (With base reverse biased) R_B = 50 Ω, L = 100 μH	$E_{S/b}$[d]			-4				0.45	-	-	0.45	-	-	0.45	-	-	mJ
Switching Times: Delay *(See Figs. 11, 15, & 16)*	t_d	V_{CC} = 200			2 3	0.2[e] 0.375[e]		- -	- -	- 0.06	- -	- -	0.07 -	- -	- -	0.07 -	μs
* Rise *(See Figs. 12, 15, & 16)*	t_r	V_{CC} = 200			2 3	0.2[e] 0.375[e]		-	- 1.5	- 0.8	- -	1.5 -	0.6 -	- -	1.75 -	0.6 -	μs
* Storage *(See Figs. 13, 15, & 16)*	t_s	V_{CC} = 200			2 3	0.2[e] 0.375[e]		- -	- 3.0	- 1.0	- -	3.75 -	1.75 -	- -	3.0 -	1.75 -	μs
* Fall *(See Figs. 14, 15, & 16)*	t_f	V_{CC} = 200			2 3	0.2[e] 0.375[e]		- -	- 1.5	- 0.4	- -	1.5 -	0.35 -	- -	1.5 -	0.35 -	μs
Thermal Resistance (Junction-to-Case)	θ_{J-C}	10			5				1.75	-	-	1.75	-	-	1.75		°C/W

a Pulsed; pulse duration ≲ 350 μs, Duty factor = 2%.

b CAUTION: Ths sustaining voltages $V_{CEO}(sus)$, $V_{CEX}(sus)$ and $V_{CER}(sus)$, MUST NOT be measured on a curve tracer. These sustaining voltages should be measured by means of the test circuit shown in Fig. 4.

c $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward biased for transistor operation in the active region.

d $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse bias conditions. $E_{S/b} = 1/2\ LI^2$ where L is a series load or leakage inductance, and I is the peak collector current.

e $I_{B1} = I_{B2}$ = value shown.

* In accordance with JEDEC registration data format (JS-6 RDF-1).

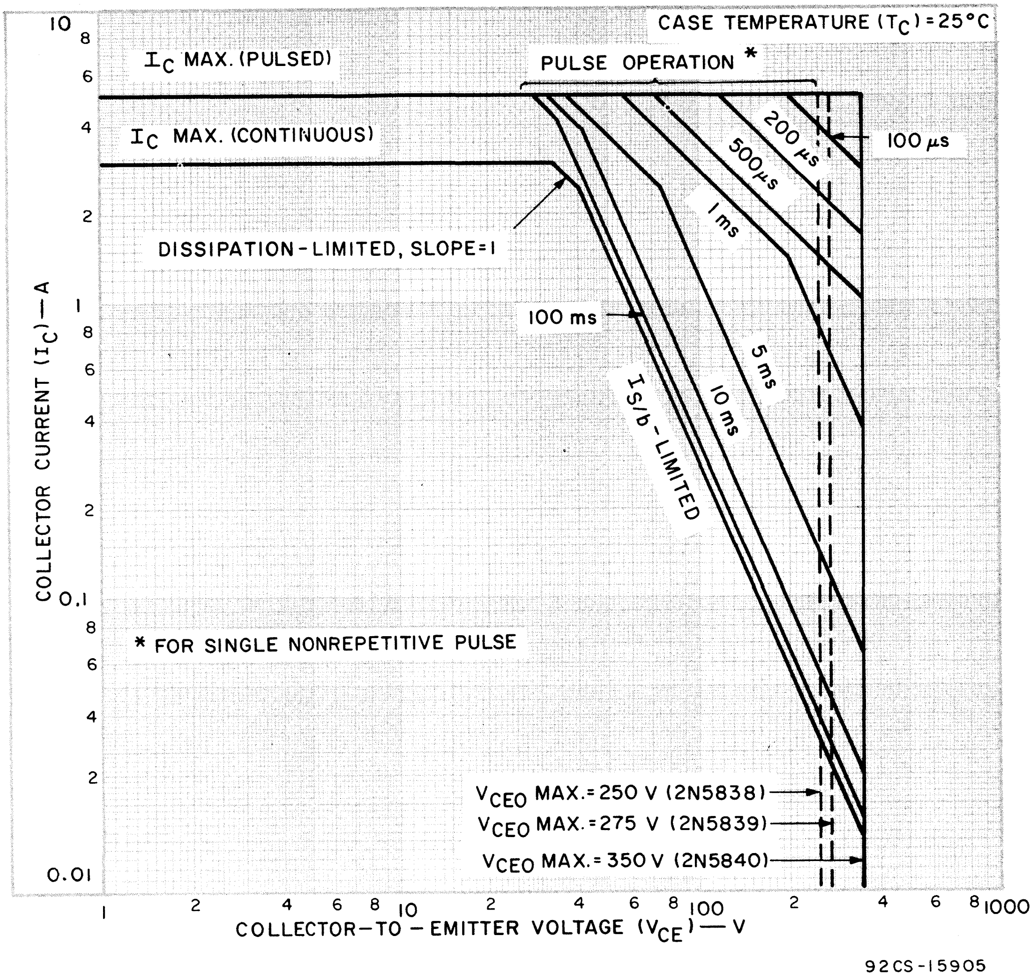
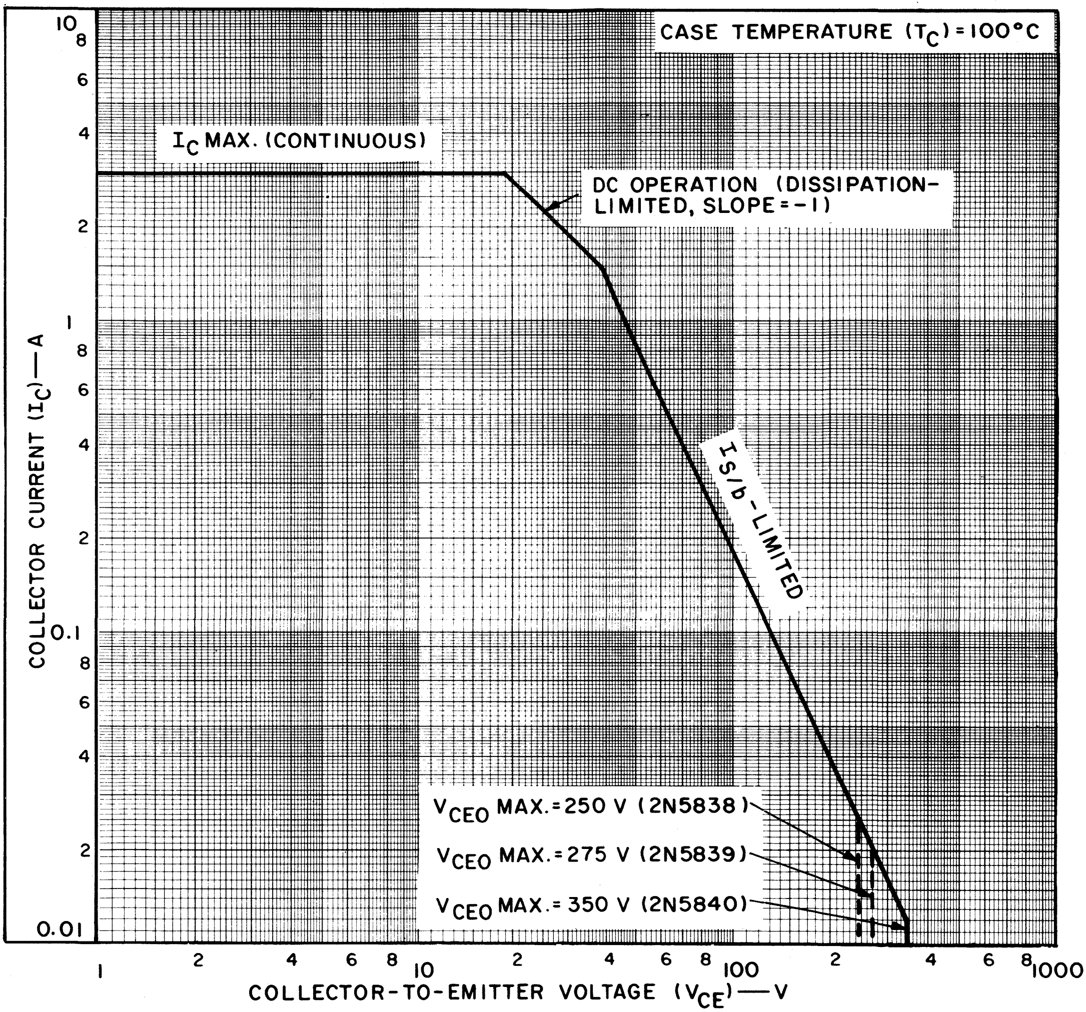


Fig. 2 - Maximum operating areas for all types.


CASE TEMPERATURE (T_C) = 100°C
I_C MAX. (CONTINUOUS)
DC OPERATION (DISSIPATION-LIMITED, SLOPE = -1)
Is/b-LIMITED
V_{CEO} MAX. = 250 V (2N5838)
V_{CEO} MAX. = 275 V (2N5839)
V_{CEO} MAX. = 350 V (2N5840)
COLLECTOR CURRENT (I_C) — A
COLLECTOR-TO-EMITTER VOLTAGE (V_{CE}) — V
10
8
6
4
2
1
0.1
0.01
100
1000

92CS-15906

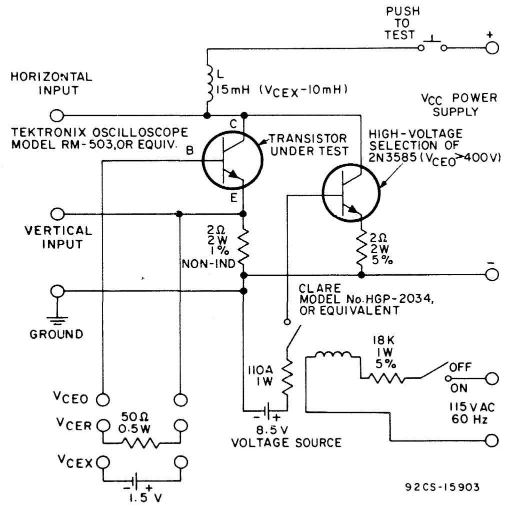


Fig. 4 - Circuit used to measure sustaining voltages $V_{CEO}(sus)$, $V_{CER}(sus)$, and $V_{CEX}(sus)$ for all types.

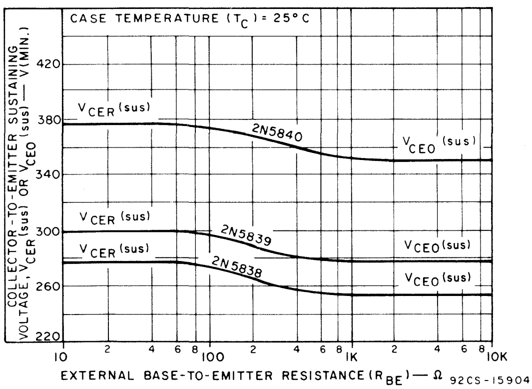


Fig. 6 - Collector-to-emitter sustaining voltage characteristics for all types.

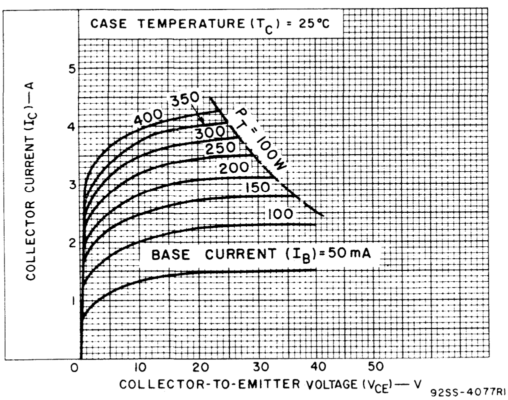
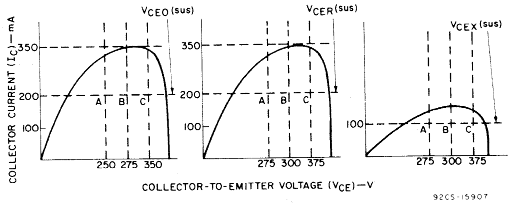


Fig. 8 - Typical output characteristics for all types.



The sustaining voltages $V_{CEO}(sus)$, $V_{CER}(sus)$, and $V_{CEX}(sus)$ are acceptable when the traces fall to the right and above point "A" for type 2N5838, point "B" for type 2N5839, and point "C" for type 2N5840.

Fig. 5 - Oscilloscope display for measurement of sustaining voltages (test circuit shown in Fig. 4).

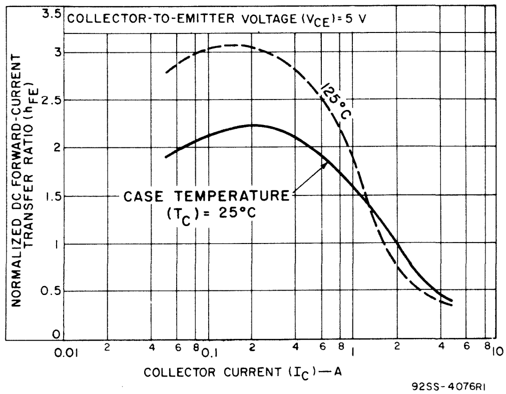


Fig. 7 - Typical normalized dc beta characteristics for all types.

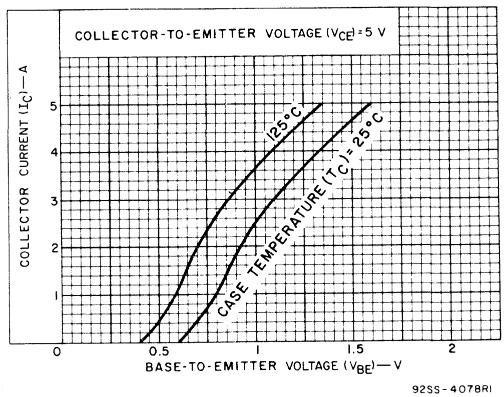


Fig. 9 - Typical transfer characteristics for all types.

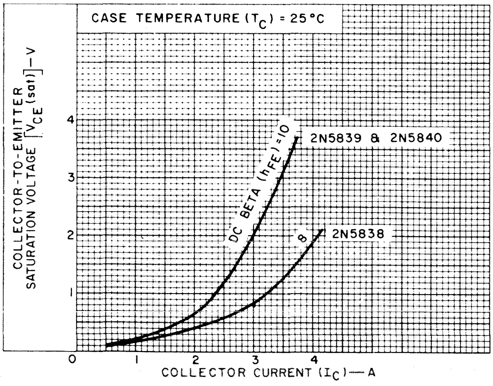


Fig. 10 - Typical saturation voltage characteristics for all types.

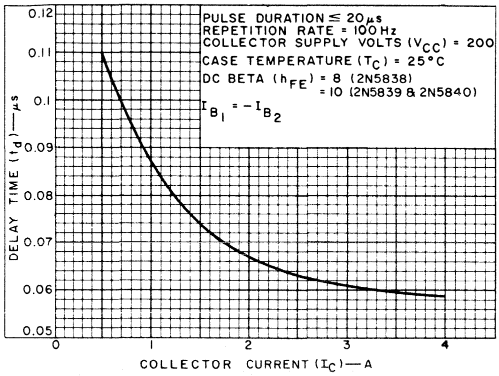


Fig. 11 - Typical delay-time characteristic for all types.

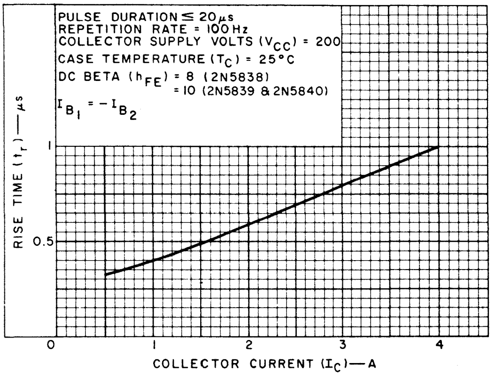


Fig. 12 - Typical rise-time characteristic for all types.

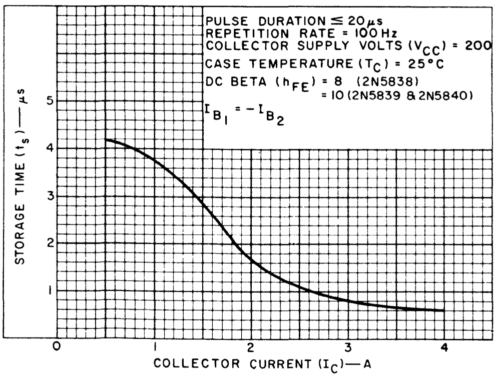


Fig. 13 - Typical storage-time characteristic for all types.

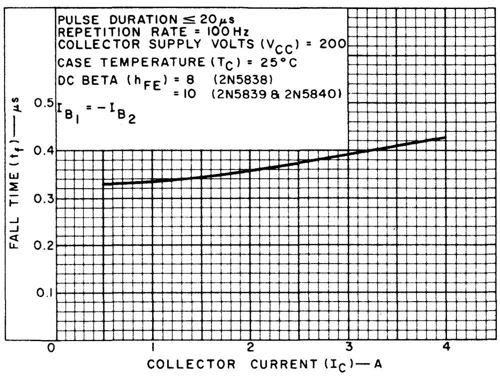
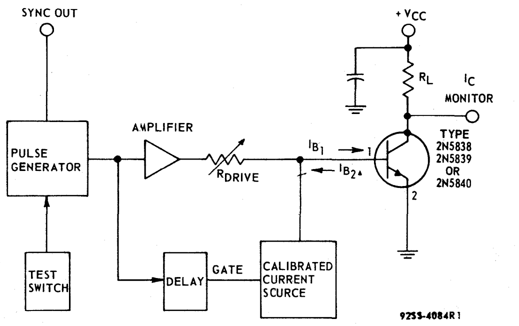


Fig. 14 - Typical fall-time characteristic for all types.



*IB1 AND IB2 MEASURED WITH TEKTRONIX CURRENT PROBE P6019 OR EQUIVALENT

Fig. 15 - Circuit used to measure switching times for all types.

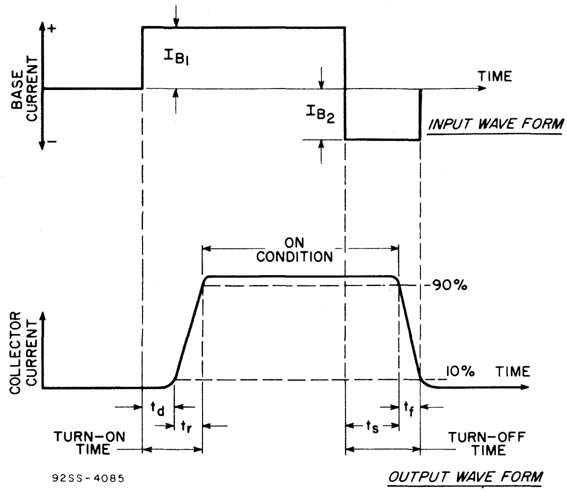
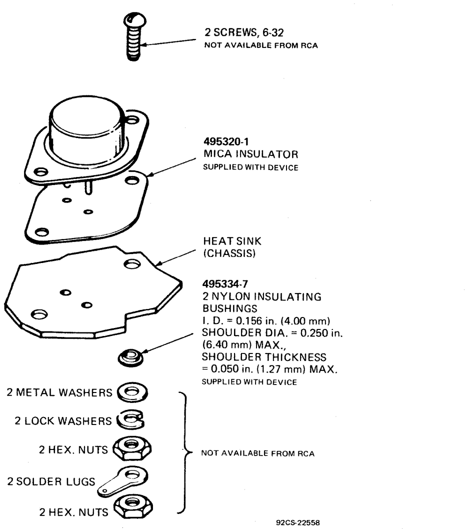


Fig. 16 - Phase relationship between input and output currents showing reference points for specification of switching times. (Test circuit shown in Fig. 15).



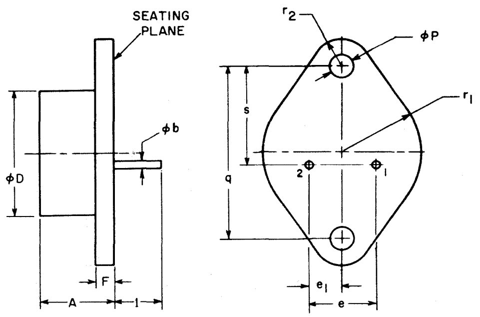
In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 17 - Suggested mounting hardware for all types.

TERMINAL CONNECTIONS

Pin 1 - Base
Pin 2 - Emitter
Mounting Flange, Case - Collector

DIMENSIONAL OUTLINE
FOR TYPES 2N5838, 2N5839, 2N5840
JEDEC TO-3



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	.250	.450	6.35	11.43	
ϕb	.038	.043	.97	1.09	2
ϕD		.875		22.23	
e	.420	.440	10.67	11.18	
e_1	.205	.225	5.21	5.72	
F		.135		3.43	
1	.312		7.92		2
ϕP	.151	.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r_1		.525		13.34	
r_2		.188		4.78	
s	.655	.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS-15222

Solid State Division

Power Transistors

BU106

JEDEC TO-3

H-1570

Epitaxial-Base Silicon N-P-N Transistor

For Horizontal Deflection for Small-Screen Black-and-White TV

Features:

- **Maximum safe-area-of-operation curves**
- **Low saturation voltages**
- **High voltage ratings**
- **High dissipation rating**

BU106 is a silicon n-p-n transistor with a pi-nu epitaxial-layer construction. This device is supplied in a JEDEC TO-3 hermetic package. The BU106 is primarily intended for use in horizontal-deflection output stages in small-screen black-and-white television receivers.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	325	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:			
With base open	V_{CEO}(sus)	140	V
With base reverse-biased (V_{BE}) between −2 V ~ 8 V	V_{CEV}(sus)	325	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	8	V
CONTINUOUS COLLECTOR CURRENT	I_C	7	A
PEAK COLLECTOR CURRENT		10	A
CONTINUOUS BASE CURRENT	I_B	4	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25°C and V_{CE} up to 40 V		75	W
At case temperatures up to 25°C and V_{CE} above 40 V		See Fig.1	
At case temperatures above 25°C and V_{CE} above 40 V.		See Figs. 1 & 2	
TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to +200	°C
PIN TEMPERATURE (During Soldering):			
At distances ≥ 1/32 in. (0.8 mm) from seating plane for 10 s max. .		230	°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS						LIMITS		UNITS
		VOLTAGE V dc			CURRENT A dc			BU106		
		V_{CE}	V_{EB}	V_{BE}	I_C	I_B	I_E	MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	100				0		–	2	mA
With base-emitter junction reverse-biased	I_{CEV}	325		−1.5				–	2	mA
With base-emitter junction reverse-biased and T_C = 100°C	I_{CEV}	325		−1.5				–	5	mA
Emitter-Cutoff Current	I_{EBO}		8		0			–	10	mA
Collector-to-Emitter Sustaining Voltage (See Figs. 4 and 5): With base open	$V_{CEO}(sus)$				0.1[a]	0		140	–	V
With base-emitter junction reverse-biased	$V_{CEV}(sus)$			−2	0.05[a]			325	–	V
Emitter-to-Base Voltage	V_{EBO}				0.01			8	–	V
DC Forward-Current Transfer Ratio	h_{FE}	5			4[a]			8	–	
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$				4[a]	0.5		–	1.5	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				4[a]	0.5		–	5	V
Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	10			0.2			3	–	
Common Base Output Capacitance (f = 1 MHz)	C_{ob}	V_{CB} = 10					0	150	–	pF
Forward-Bias Second Breakdown Collector Current (1-s non-repetitive pulse)	$I_{S/b}$[c]	40						1.85	–	A
Switching Time: Storage (V_{CC} = 40 V)	t_s				4	0.5[e]		–	3	μs
Fall (V_{CC} = 40 V)	t_f	2			0.1			–	1.5	μs
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	10			5			–	2.34	°C/W

a Pulsed; pulse duration $\leq$ 350 μs, Duty factor = 2%.

b CAUTION: The sustaining voltages $V_{CEO}(sus)$, $V_{CEX}(sus)$ and $V_{CER}(sus)$, MUST NOT be measured on a curve tracer. These sustaining voltages should be measured by means of the test circuit shown in Fig.4.

c $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward biased for transistor operation in the active region.

d $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse bias conditions. $E_{S/b} = 1/2\ LI^2$ where L is a series load or leakage inductance, and I is the peak collector current.

e $I_{B1} = I_{B2}$ = value shown.

f Fall time is measured when V_{CE} has reached a value of 2 V and I_C has increased to 100 mA. A typical measurement circuit is shown in Fig.10.

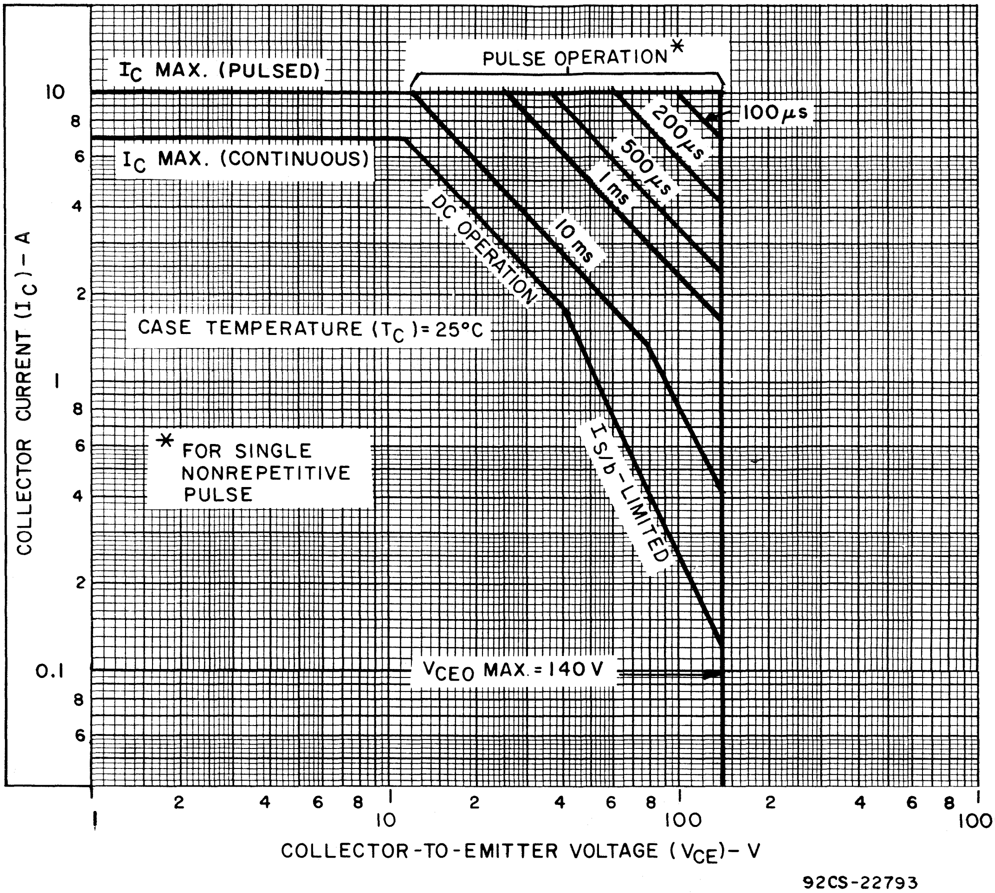


Fig.1 — Maximum operating areas.

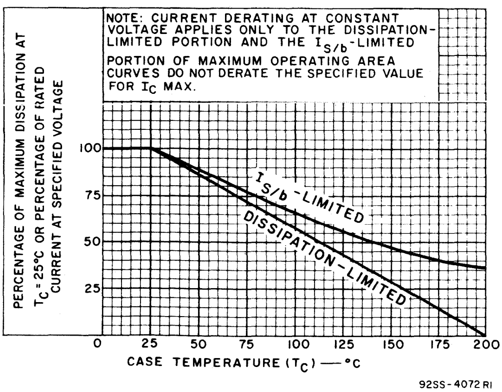


Fig.2 — Derating curve.

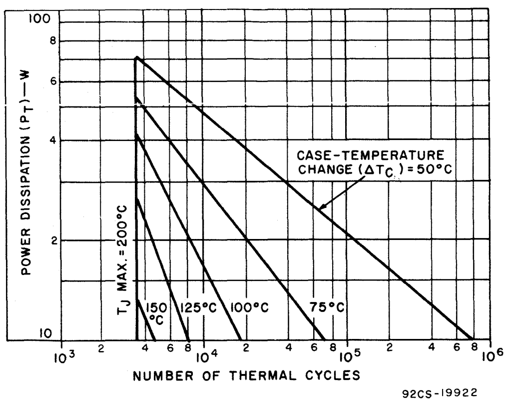


Fig.3 — Thermal-cycling rating chart.

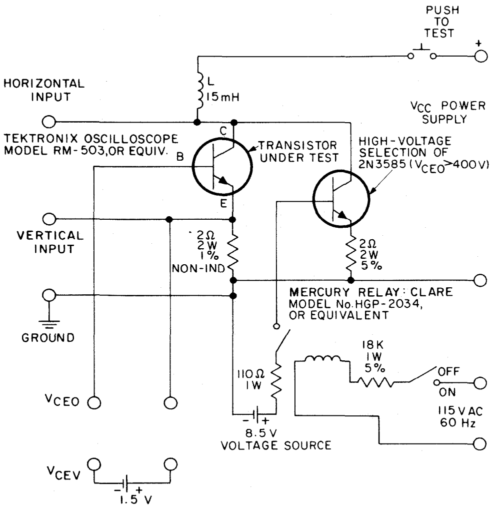
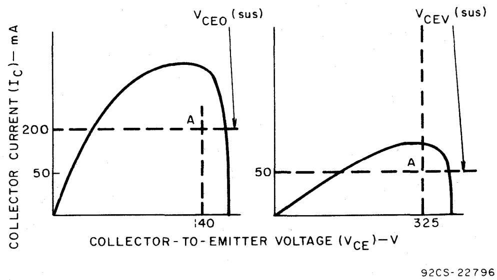


Fig.4 — Circuit used to measure sustaining voltages $V_{CEO}(sus)$ and $V_{CEV}(sus)$.



The sustaining voltages V_{CEO}(sus) and V_{CEV}(sus) are acceptable when the traces fall to the right and above point "A".

Fig.5 — Oscilloscope display for measurement of sustaining voltages (test circuit shown in Fig.4).

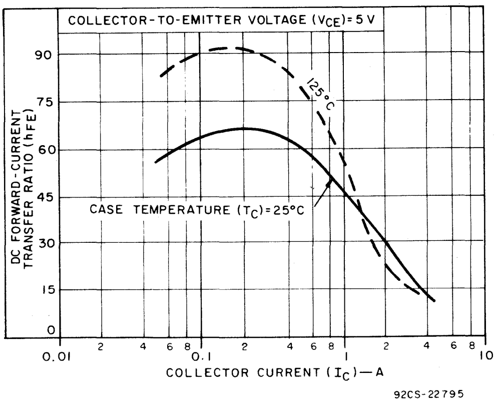


Fig.6 — Typical dc beta characteristics.

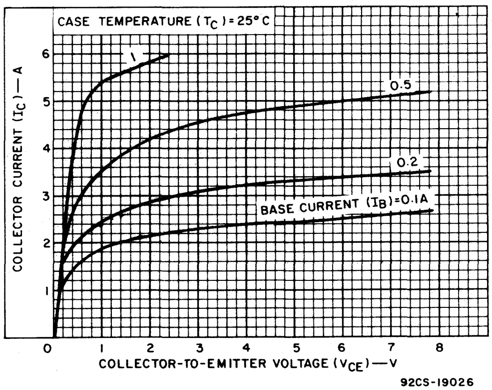


Fig.7 — Typical output characteristics.

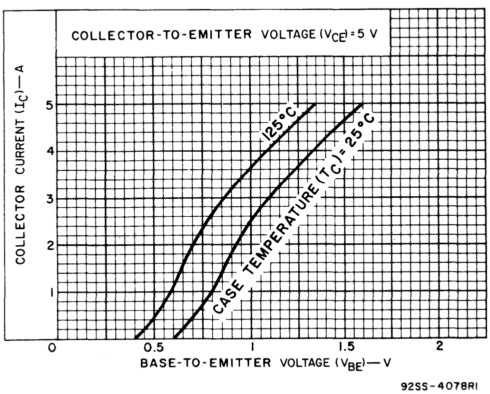


Fig.8 — Typical transfer characteristics.

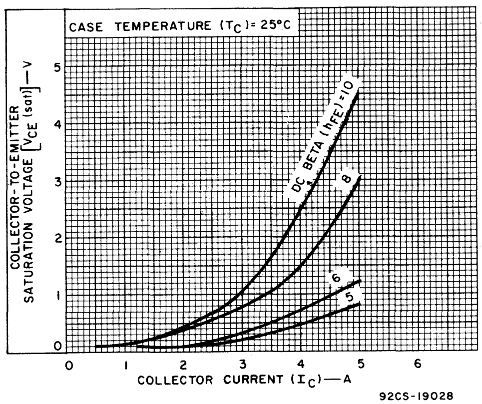


Fig.9 — Typical saturation voltage characteristics.

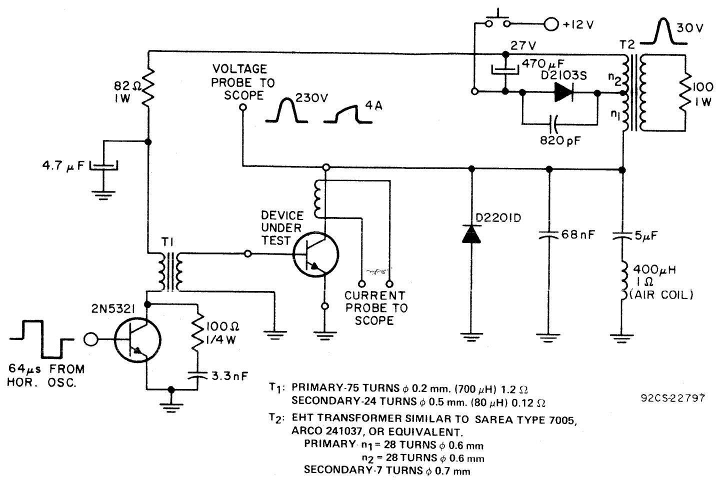


Fig. 10 – Circuit for fall-time measurement.

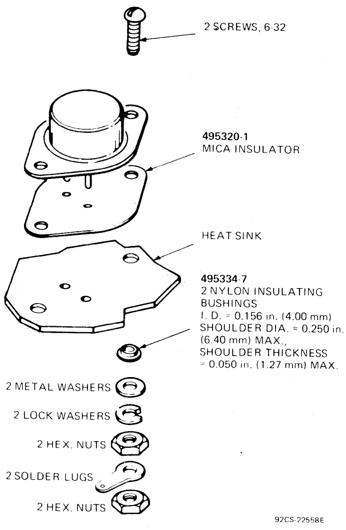
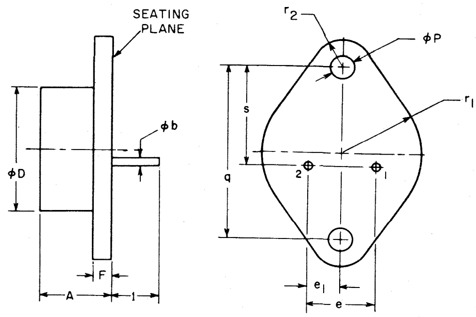


Fig. 11 – Suggested mounting hardware.

TERMINAL CONNECTIONS

Pin 1 – Base
Pin 2 – Emitter
Case – Collector
Mounting Flange – Collector

DIMENSIONAL OUTLINE – JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
ϕb	0.038	0.043	0.97	1.09	2
ϕD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
l	0.312		7.92		2
ϕP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r1		0.525		13.34	
r2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS–15222

RCA
Solid State
Division

Power Transistors

40850 40851
40852 40853
40854

40850
40851

JEDEC TO-66

40852
40853
40854

JEDEC TO-3

450-V Silicon N-P-N Types

For Off-Line Switching-Regulator Type Power-Supply Applications

Features:
- **High-voltage ratings for operation from power lines without a step-down transformer**
- **Popular JEDEC TO-3 and TO-66 hermetic packages**

Applications:
- **For use in switching-regulator supplies which feature:**
  - **A substantial reduction in size and weight due to elimination of the 60-Hz power transformer.**
  - **Operation with a substantial reduction of heat**
- **5-V, off-line supplies with current ratings of 25, 50, 100, or 200 A**
- **30-V, off-line supplies with current ratings of 5, 10, 20, or 40 A**

RCA 40850–40854, inclusive, are silicon n-p-n power transistors,selected from RCA's line of silicon power transistors,for power-supply applications. Their high-voltage ratings (450 V) permit operation directly off the power line thereby eliminating the heavy and bulky 60-Hz power transformer.

Their fast switching speeds (t_r plus t_f equal to less than 2.0 μs) permit operation above the audio-frequency range (20 to 30 kHz) for quiet performance, and permit the use of small ferrite-core transformers for changing the voltage level.

These types have sufficient voltage capability to be used as push-pull inverters or pulse-width-modulated inverters operating directly off the 120-V power line.

Types 40850–40854 have sufficient voltage capability to operate as switching regulators off a 240-V line; for 120-V lines, the prototypes can be used.

A brief description of these types, together with prototype identification, is given in the tables on pages 2, 3, and 4.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	40850	40851	40852■	40853	40854	
COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	450	450	450	450	450	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:						
With base open, V_{CEO}(sus)	300	350	350	300	300	V
With external base-to-emitter resistance (R_{BE}) ≤ 50 Ω, V_{CER}(sus)	400	375	375	375	325	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}	6	9	9	6	6	V
COLLECTOR CURRENT, I_C						
Continuous and Average	2	7	7	10	15	A
Peak (10 ms max.)	5	10	10	15	30	A
CONTINUOUS BASE CURRENT, I_B	1	4	4	5	10	A

■ Formerly RCA-40832.

Continued on following page.

MAXIMUM RATINGS (cont'd):

	40850	40851	40852■	40853	40854	
TRANSISTOR DISSIPATION, P_T:						
(Power Dissipation-Limited Region*)						
At case temperaures up to 25°C	35	45	100	100	175	W
At case temperaures above 25°C and in the $I_{S/b}$-Limited Region*	See derating curves in prototype bulletins.					
TEMPERATURE RANGE:						
Storage & Operating (Junction)	← -65 to +200 °C →					
PIN TEMPERATURE (During Soldering):						
At distances ≥1/32 in. (0.8 mm) from case for 10 s max.	← 230°C →					

* Safe-operating-area curves for prototype devices should be extended to the maximum values of collector current given for these devices.
■ Formerly RCA-40832

Type 40850 (For 5-V, 25-A & 30-V, 5-A Power Supplies)
Package: JEDEC TO-66
Application Information: See "RCA Power Circuits" manual SP-52 and RCA Application Note AN3065

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector-Cutoff Current:	I_{CEV}	V_{CE} = 450 V, V_{BE} = -1.5 V	–	0.2	mA
With base reverse biased	I_{CEV}	V_{CE} = 450 V, V_{BE} = -1.5 V, T_C = 125°C	–	2	mA
Collector-to-Emitter Voltage With base open	V_{CEO}[a]	I_C = 0.2 A, I_B = 0	300	–	V
Collector-to-Emitter Voltage With external base-to-emitter resistance (R_{BE})	V_{CER}[a]	I_C = 0.2 A, R_{BE} = 50 Ω	400	–	V
Emitter-to-Base Voltage	V_{EBO}	I_E = 5 mA, I_C = 0	6	–	V
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 0.75 A, V_{CE} = 10 V	25	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 2 A, I_B = 0.4 A	–	2.0	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$	I_C = 2 A, I_B = 0.4 A	–	2.0	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$[a]	V_{CE} = 100 V	0.35	–	A
Second-Breakdown Energy: With base reversed biased	$E_{S/b}$[a]	L = 100 μH, I_C(PEAK) = 2 A, R = 20 Ω V_{BE} = -4 V	0.2	–	mJ

[a] For characteristics curves and test conditions, refer to published data for prototype 2N3585 (File 138).

Type 40851 (For 5-V, 50-A & 30-V, 10-A Power Supplies)
Package: JEDEC TO-66
Applications Information: See "RCA Power Circuits" manual SP-52 and RCA Application Note AN4509

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector-Cutoff Current:	I_{CEV}	V_{CE} = 450 V, V_{BE} = -1.5 V	–	0.5	mA
With base reverse biased	I_{CEV}	V_{CE} = 450 V, V_{BE} = -1.5 V, T_C = 125°C	–	5	mA
Collector-to-Emitter Voltage With base open	V_{CEO}[a]	I_C = 0.2 A, I_B = 0	350	–	V
Collector-to-Emitter Voltage With external base-to-emitter resistance (R_{BE})	V_{CER}[a]	I_C = 0.2 A, R_{BE} = 50 Ω	375	–	V
Emitter-to-Base Voltage	V_{EBO}	I_E = 1 mA, I_C = 0	9	–	V
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 1.2 A, V_{CE} = 1.0 V	12	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 4 A, I_B = 0.8 A	–	3	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$	I_C = 4 A, I_B = 0.8 A	–	2	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$[a]	V_{CE} = 50 V	0.9	–	A
Second-Breakdown Energy: With base reversed biased	$E_{S/b}$[a]	L = 100 μH, $I_C(PEAK)$ = 3 A, R = 50 Ω V_{BE} = -4 V	0.45	–	mJ

[a] For characteristics curves and test conditions, refer to published data for prototype 2N6079 (File 492).

Type 40852 (For 5-V, 50-A & 30-V, 10-A Power Supplies)
Package: JEDEC TO-3
Applications Information: See "RCA Power Circuits" manual SP-52 and RCA Application Note AN4509

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector-Cutoff Current:	I_{CEV}	V_{CE} = 450 V, V_{BE} = -1.5 V	–	0.5	mA
With base reverse biased	I_{CEV}	V_{CE} = 450 V, V_{BE} = -1.5 V, T_C = 125°C	–	5	mA
Collector-to-Emitter Voltage With base open	V_{CEO}[a]	I_C = 0.2 A, I_B = 0	350	–	V
Collector-to-Emitter Voltage With external base-to-emitter resistance (R_{BE})	V_{CER}[a]	I_C = 0.2 A, R_{BE} = 50 Ω	375	–	V
Emitter-to-Base Voltage	V_{EBO}	I_E = 1 mA, I_C = 0	9	–	V
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 1.2 A, V_{CE} = 1.0 V	12	–	
Collector-to-Emitter Saturation Voltage	V_{CE} (sat)	I_C = 4 A, I_B = 0.8 A	–	3.0	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$	I_C = 4 A, I_B = 0.8 A	–	2.0	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$[a]	V_{CE} = 40 V	2.5	–	A
Second-Breakdown Energy: With base reversed biased	$E_{S/b}$[a]	L = 100 μH, $I_C(PEAK)$ = 3 A, R = 50 Ω V_{BE} = -4 V	0.45	–	mJ

[a] For characteristics curves and test conditions, refer to published data for prototype 2N5840 (File 410).

Type 40853 (For 5-V, 100-A & 30-V, 20-A Power Supplies)
Package: JEDEC TO-3
Applications Information: See "RCA Power Circuits" manual SP-52

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector-Cutoff Current: With base reverse biased	I_{CEV}	V_{CE} = 450 V, V_{BE} = -1.5 V	–	1.0	mA
	I_{CEV}	V_{CE} = 450 V, V_{BE} = -1.5 V, T_C = 125°C	–	10	mA
Collector-to-Emitter Voltage With base open	V_{CEO}[a]	I_C = 0.2 A, I_B = 0	300	–	V
Collector-to-Emitter Voltage With external base-to-emitter resistance (R_{BE})	V_{CER}[a]	I_C = 0.2 A, R_{BE} = 50 Ω	375	–	V
Emitter-to-Base Voltage	V_{EBO}	I_E = 5 mA, I_C = 0	6	–	V
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 5 A, V_{CE} = 4 V	10	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 8 A, I_B = 1.6 A	–	3.0	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$	I_C = 8 A, I_B = 1.6A	–	2.0	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$[a]	V_{CE} = 50 V	2.2	–	A
Second-Breakdown Energy: With base reversed biased	$E_{S/b}$[a]	L = 50 μH, I_C(PEAK) = 5 A, R = 20 Ω V_{BE} = -4 V	0.62	–	mJ

[a] For characteristics curves and test conditions, refer to published data for prototype 2N5805 (File 407).

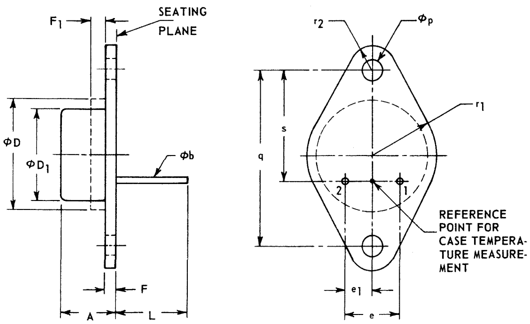
Type 40854 (For 5-V, 200-A & 30-V, 40-A Power Supplies)
Package: JEDEC TO-3
Applications Information: See "RCA Power Circuits" manual SP-52

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector-Cutoff Current: With base reverse biased	I_{CEV}	V_{CE} = 450 V, V_{BE} = -1.5 V	–	1.0	mA
	I_{CEV}	V_{CE} = 450 V, V_{BE} = -1.5 V, T_C = 125°C	–	10	mA
Collector-to-Emitter Voltage With base open	V_{CEO}[a]	I_C = 0.2 A, I_B = 0	300	–	V
Collector-to-Emitter Voltage With external base-to-emitter resistance (R_{BE})	V_{CER}[a]	I_C = 0.2 A, R_{BE} = 50 Ω	325	–	V
Emitter-to-Base Voltage	V_{EBO}	I_E = 5 mA, I_C = 0	6	–	V
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 A, V_{CE} = 4 V	8	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 16 A, I_B = 3.2 A	–	3.0	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$	I_C = 16 A, I_B = 3.2 A	–	3.0	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$[a]	V_{CE} = 30 V	5.8	–	A
Second-Breakdown Energy: With base reversed biased	$E_{S/b}$[a]	L = 50 μH, I_C(PEAK) = 10 A, R = 50 Ω V_{BE} = -4 V	2.5	–	mJ

[a] For characteristics curves and test conditions, refer to published data for prototype 2N6251 (File 523).

DIMENSIONAL OUTLINE (JEDEC TO-66)



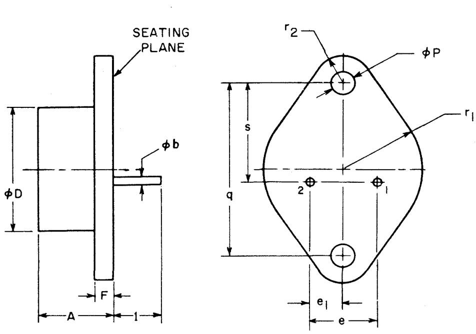
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.340	6.35	8.64	
φb	0.028	0.034	0.711	0.863	
φD		0.620		15.75	
φD1	0.470	0.500	11.94	12.70	
e	0.190	0.210	4.83	5.33	
e1	0.093	0.107	2.36	2.72	
F	0.050	0.075	1.27	1.91	2
F1		0.050		1.27	1
L	0.360		9.14		
φp	0.142	0.152	3.61	3.86	
q	0.958	0.962	24.33	24.43	
r1		0.350		8.89	
r2		0.145		3.68	
s	0.570	0.590	14.48	14.99	

NOTES:

1. The outline contour is optional within zone defined by φD and F1.
2. Dimensions does not include sealing flanges.

92SS-3738

DIMENSIONAL OUTLINE (JEDEC TO-3)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
φb	0.038	0.043	0.97	1.09	2
φD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
l	0.312		7.92		2
φP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r1		0.525		13.34	
r2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS—15222

TERMINAL CONNECTIONS (All Types)

Pin 1 - Base

Pin 2 - Emitter

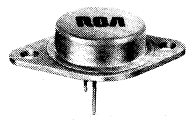
Mounting Flange, Case - Collector

File No. 321

RCA Solid State Division

Power Transistors

2N5239
2N5240



JEDEC TO-3

H-1570

Silicon N-P-N Power Transistors

High-Voltage, High-Power Types for Applications in Industrial and Commercial Service

Features:

- **High voltage ratings: $V_{CER}(sus) = 350\,V, R_{BE} \leq 50\,\Omega$ (2N5240)**
  $= 250\,V, R_{BE} \leq 50\,\Omega$ (2N5239)
- **High power dissipation rating: $P_T = 100\,W$ at $V_{CE} = 150\,V, T_C = 25^\circ C$**
- **For switching applications where circuit values and operating conditions require a transistor with a high second breakdown rating ($I_{S/b}$) (limit line begins at 150 V)**
- **Maximum area-of-operation curves for dc and pulse operation**

RCA-2N5239 and 2N5240* are multiple epitaxial silicon n-p-n power transistors employing a new overlay construction with several emitter sites. Both devices employ the popular JEDEC TO-3 package; they differ in breakdown-voltage and leakage-current values.

The high breakdown voltage ratings and exceptional second-breakdown capabilities of these transistors make them especially suitable for use in series regulators, power amplifiers, inverters, deflection circuits, switching regulators, and high-voltage bridge amplifiers.

*RCA Dev. Nos. TA2765 and TA2765A, respectively.

MAXIMUM RATINGS, ***Absolute-Maximum Values:***

	2N5239	2N5240	
*COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	300	375	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:			
* With base open, $V_{CEO}(sus)$	225	300	V
With external base-to-emitter resistance (R_{BE}) $\leq 50\,\Omega$, $V_{CER}(sus)$	250	350	V
*EMITTER-TO-BASE VOLTAGE, V_{EBO}	6	6	V
*COLLECTOR CURRENT, I_C	5	5	A
*BASE CURRENT, I_B	−2	−2	A
*TRANSISTOR DISSIPATION, P_T:			
At case temperatures up to 25° C and V_{CE} up to 150 V	100	100	W
At case temperatures up to 25° C and V_{CE} above 150 V	See Fig 2.		
At case temperatures above 25° C and V_{CE} above 150 V	See Figs. 1 & 2		
*TEMPERATURE RANGE:			
Storage & Operating (Junction)	−65 to +200		°C
*PIN TEMPERATURE (During Soldering)			
At distances $\geq$ 1/32 in. from seating plane for 10 s max		230	°C

*In accordance with JEDEC registration data format (JS-6,RDF-2)

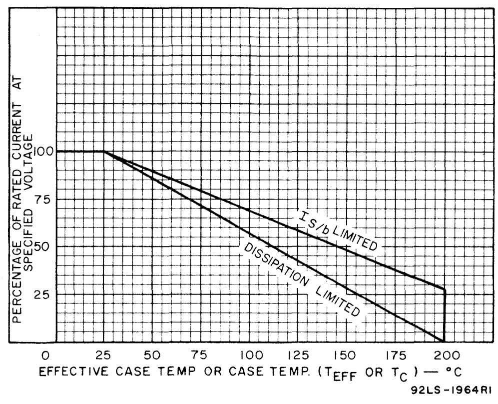


Fig. 1 - Dissipation derating curves for types 2N5239 & 2N5240

11-73

ELECTRICAL CHARACTERISTICS, ***Case Temperature (T_C) = 25°C Unless Otherwise Specified***

Characteristic	Symbol	TEST CONDITIONS							LIMITS				Units
		DC Collector Voltage (V)		DC Emitter or Base Voltage (V)		DC Current (A)			Type 2N5239		Type 2N5240		
		V_{CB}	V_{CE}	V_{EB}	V_{BE}	I_C	I_E	I_B	Min.	Max.	Min.	Max.	
Collector-Cutoff Current	I_{CEO}	–	200	–	–	–	–	0	–	5.0	–	2.0	mA
*	I_{CEV}	–	300	–	−1.5	–	–	–	–	4.0	–	–	mA
*	I_{CEV}	–	375	–	−1.5	–	–	–	–	–	–	2.0	mA
	I_{CEV} (T_C=150° C)	–	300	–	−1.5	–	–	–	–	5.0	–	3.0	mA
* Emitter-Cutoff Current	I_{EBO}	–	–	5.0	–	0	–	–	–	5.0	–	1.0	mA
Collector-to-Emitter Sustaining Voltage: *(See Figs. 3 & 4)* * With base open	$V_{CEO}(sus)$	–	–	–	–	0.2	–	0	225[b]	–	300[b]	–	V
With external base-to-emitter resistance (R_{BE}) ≤ 50 Ω	$V_{CER}(sus)$	–	–	–	–	0.2	–	0	250[b]	–	350[b]	–	V
* Emitter-to-Base Voltage	V_{EBO}	–	–	–	–	–	–	0.02	6	–	6	–	V
* Base-to-Emitter Voltage	V_{BE}	–	10	–	–	2.0[a]	–	–	–	3.0	–	3.0	V
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	– –	– –	– –	– –	2.0[a] 4.5[a]	– –	0.25 1.125	– –	2.5 5	– –	2.5 5	V
DC Forward-Current Transfer Ratio * *	h_{FE}	– – –	10 10 10	– – –	– – –	0.4[a] 2.0[a] 4.5[a]	– – –	– – –	20 20 5	80 80 –	20 20 5	80 80 –	
Output Capacitance (At 1 MHz)	C_{ob}	10	–	–	–	–	0	–	–	150	–	150	pF
* Second-Breakdown[c] Collector Current[d] (With base forward biased)	$I_{S/b}$[c]	–	150	–	–	–	–	–	0.67	–	0.67	–	A
Second-Breakdown Energy (With base reverse biased) R_{BE} = 50Ω, L = 0.2 mH	$E_{S/b}$[e]	–	–	4.0	–	4.0	–	–	1.6	–	1.6	–	mJ
Gain-Bandwidth Product	f_T	–	10	–	–	0.2	–	–	5.0	–	5.0	–	MHz
* Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (at 1 MHz)	$\|h_{fe}\|$	–	10	–	–	0.2	–	–	5.0	–	5.0	–	
* Common-Emitter, Small-Signal Short-Circuit, Forward-Current Transfer Ratio (at 1 kHz)	h_{fe}	–	10	–	–	4.0	–	–	20	–	20	–	
Thermal Resistance (Junction-to-Case)	$\theta_{J\text{-}C}$	–	–	–	–	–	–	–	–	1.75	–	1.75	°C/W

[a] Pulsed; pulse duration ≤ 350 μs, duty factor = 2%.

[b] CAUTION: The sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$ MUST NOT be measured on a curve tracer. These sustaining voltages should be measured by means of the test circuit shown in *Fig. 3.*

[c] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward biased for transistor operation in the active region.

[d] Pulsed; 1-s, non-repetitive pulse.

[e] $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse bias conditions. $E_{S/b} = 1/2LI^2$, where L is a series load or leakage inductance and I is the peak collector current.

*In accordance with JEDEC registration data format (JS-6, RDF-2)

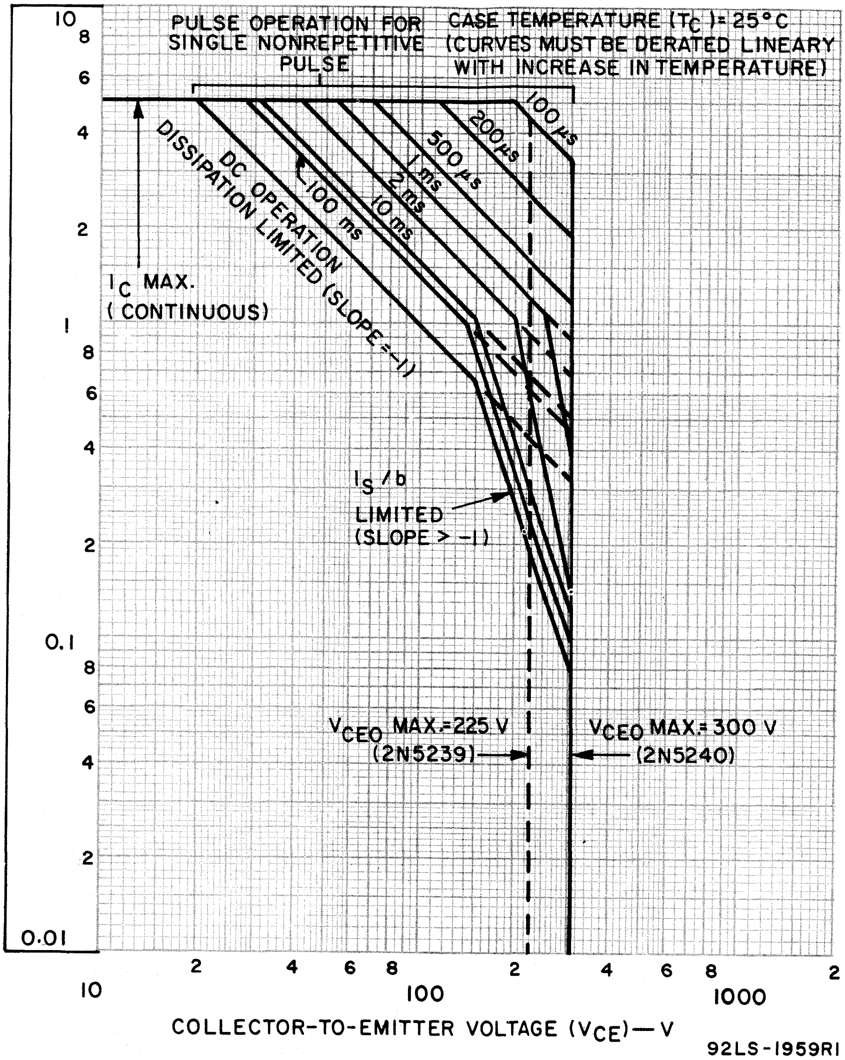


Fig. 2 - Maximum operating area for types 2N5239 & 2N5240

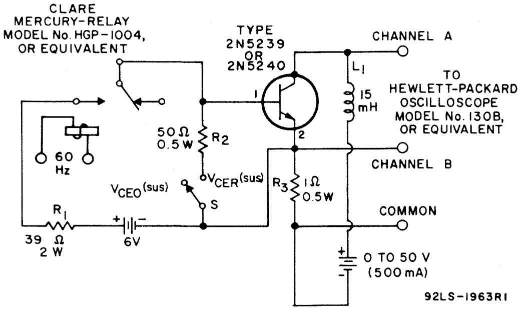
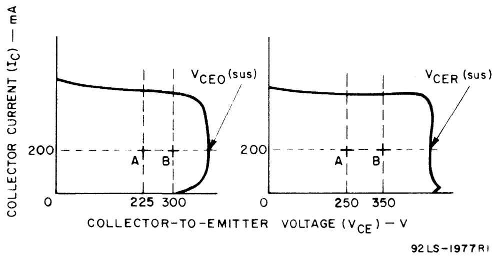


Fig. 3 - Circuit used to measure sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$ for types 2N5239 & 2N5240



Note: The sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$ are acceptable when the traces fall to the right and above points "A" and "B" for types 2N5239 and 2N5240

Fig. 4 - Oscilloscope display for measurement of sustaining voltages. (Test circuit shown in Fig. 3.)

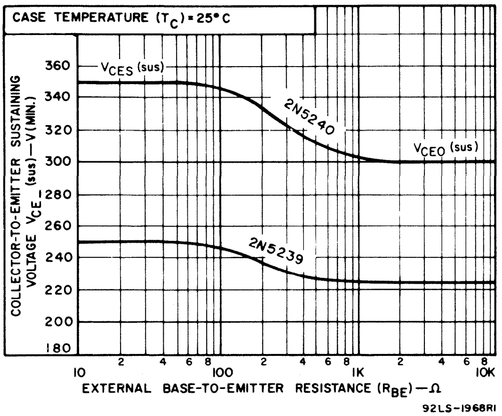


Fig. 5 - Sustaining voltage vs. base-to-emitter resistance for types 2N5239 & 2N5240

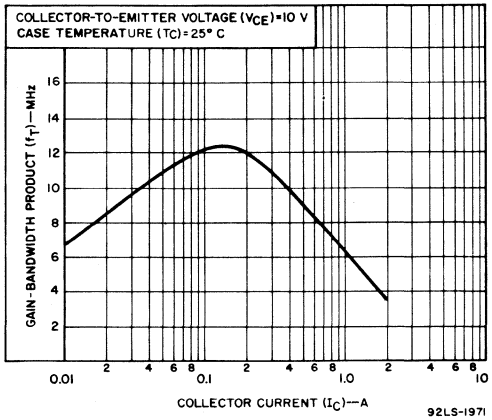


Fig. 6 - Typical gain-bandwidth product for types 2N5239 & 2N5240

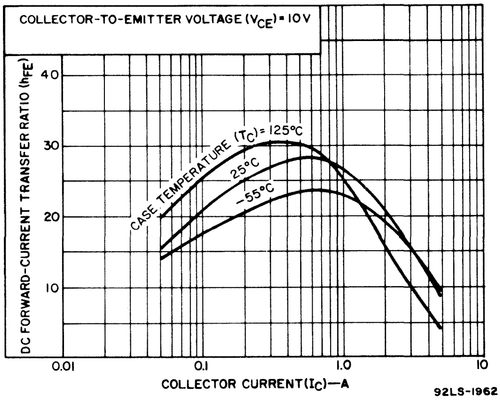


Fig. 7 - Typical DC beta for types 2N5239 & 2N5240

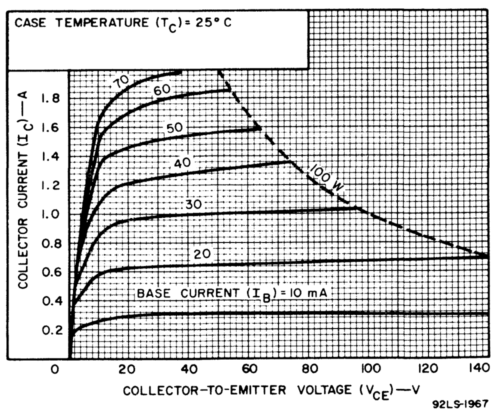


Fig. 8 - Typical output characteristics for types 2N5239 & 2N5240

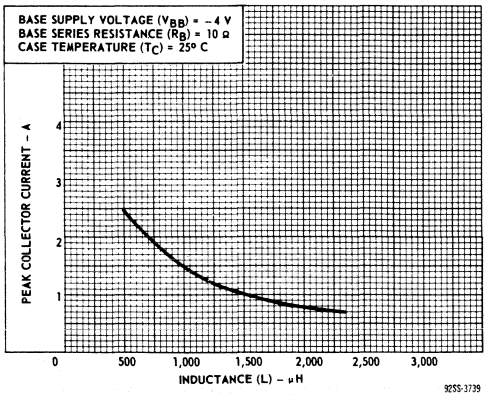


Fig. 9 - Typical reverse-bias, second breakdown characteristic for types 2N5239 & 2N5240

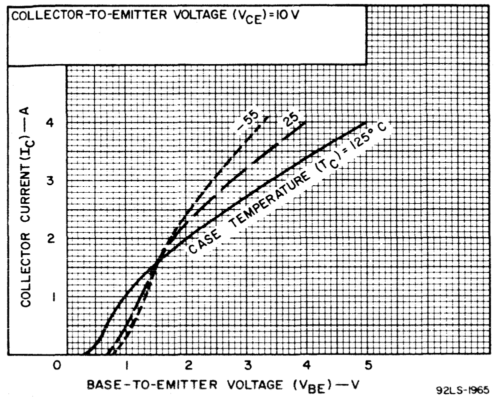


Fig. 12 - Typical transfer characteristics for types 2N5239 & 2N5240

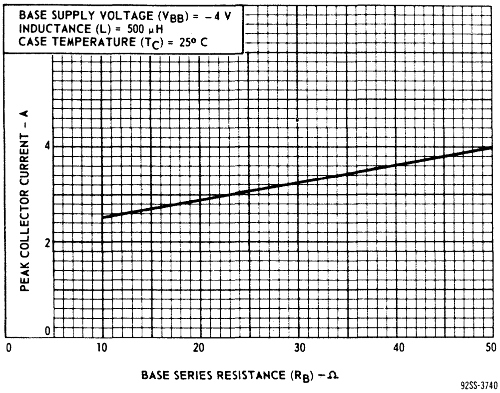


Fig. 10 - Typical reverse-bias, second breakdown characteristic for types 2N5239 & 2N5240

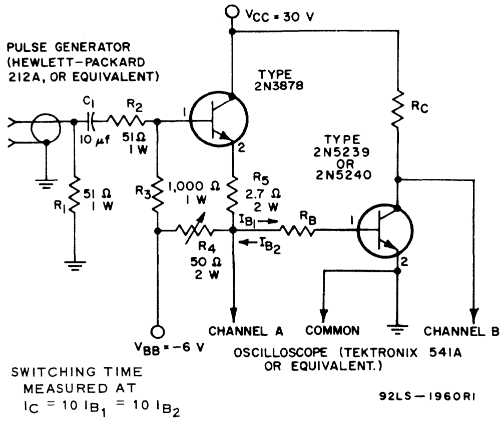


Fig. 13 - Circuit used to measure switching times for types 2N5239 & 2N5240

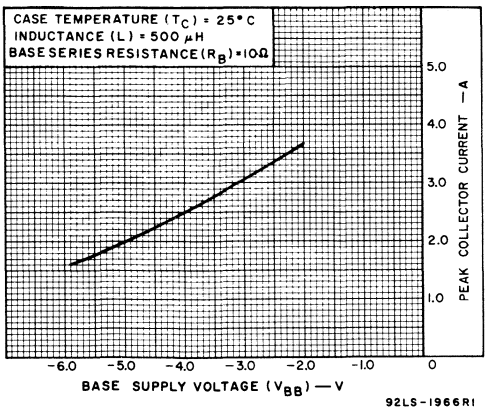


Fig. 11 - Typical reverse-bias, second breakdown characteristic for types 2N5239 & 2N5240

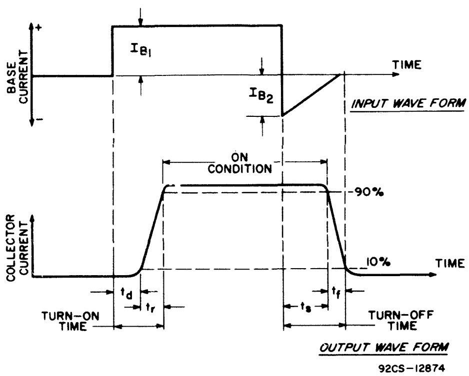


Fig. 14 - Oscilloscope display of switching times. (Test circuit shown in Fig. 13.)

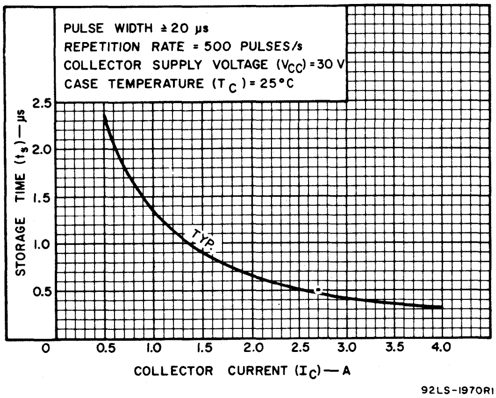


Fig. 15 - Saturated switching time (storage) vs. collector current for types 2N5239 & 2N5240

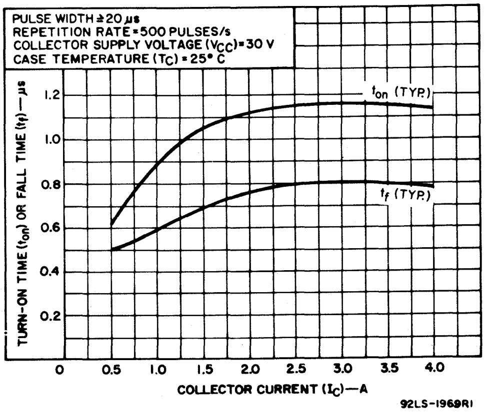
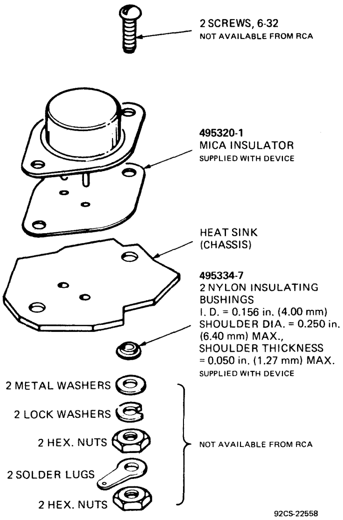


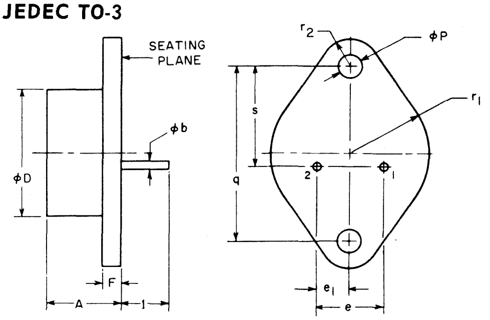
Fig. 16 - Saturated switching times (turn-on and fall) vs. collector current for types 2N5239 & 2N5240



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 17 - Suggested hardware for types 2N5239 & 2N5240

DIMENSIONAL OUTLINE FOR TYPES 2N5239 & 2N5240 JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
φb	0.038	0.043	0.97	1.09	2
φD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e_1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
1	0.312		7.92		2
φP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r_1		0.525		13.34	
r_2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27mm) to 0.055 in. (1.40mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS-15222

TERMINAL CONNECTIONS

Pin 1 - Base
Pin 2 - Emitter
Case, Flange - Collector

RCA

Solid State Division

Power Transistors

2N5804
2N5805

JEDEC TO-3 H-1570

High-Voltage, High-Power Silicon N-P-N Power Transistors

For Switching and Amplifier Applications

Features:

- **Power dissipation (P_T) = 110 W at 50 V**
- **High-voltage ratings:**
  V_{CEO}(sus) = 300 V max. (2N5805)
  = 225 V max. (2N5804)
- **Maximum-operating-area curves. .for selection of maximum operating conditions for operation free from second breakdown.**

RCA types 2N5804 and 2N5805** are silicon n-p-n transistors with high breakdown-voltage ratings and fast switching speeds. Both devices employ the popular TO-3 package; they differ in breakdown-voltage ratings and leakage-current values.

These transistors are especially suitable for power-switching circuits, switching regulators, converters, inverters, and power amplifiers.

**Formerly RCA Dev. Nos. TA7130 and TA7130A, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N5804	2N5805	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	300	375	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:				
* With 1.5 volts (V_{BE}) of reverse bias, and external base-to-emitter resistance (R_{BE}) = 50Ω	V_{CEX}(sus)	300	375	V
With base open	V_{CEO}(sus)	225	300	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	6	6	V
*CONTINUOUS COLLECTOR CURRENT	I_C	5	5	A
PEAK COLLECTOR CURRENT		15	15	A
*CONTINUOUS BASE CURRENT	I_B	2	2	A
*TRANSISTOR DISSIPATION:	P_T			
At case temperatures up to 25° C and V_{CE} up to 50 V		110	110	W
At case temperatures up to 25° C and V_{CE} above 50 V		See Fig. 1		
At case temperatures above 25° C and V_{CE} above 50 V		See Figs. 1 & 3		
*TEMPERATURE RANGE:				
Storage & Operating (Junction)		-65 to +200		°C
*PIN TEMPERATURE (During Soldering):				
At distances ≥ 1/32 in. (0.8 mm) from seating plane for 10 s max		+230		°C

*In accordance with JEDEC registration data format (JS-6 RDF-1)

11-73

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS							LIMITS				UNITS
		DC COLLECTOR VOLTAGE (V)		DC EMITTER OR BASE VOLTAGE (V)		DC CURRENT (A)			2N5804		2N5805		
		V_{CB}	V_{CE}	V_{EB}	V_{BE}	I_C	I_E	I_B	MIN.	MAX.	MIN.	MAX.	
Collector-Cutoff Current: With base open	I_{CEO}		150					0	–	15	–	5	mA
* With base-emitter junction reverse biased	I_{CEV}		270		−1.5				–	5	–	–	mA
			340		−1.5				–	–	–	5	
(T_C = 100°C)			270		−1.5				–	15	–	–	mA
			340		−1.5				–	–	–	15	
* Emitter-Cutoff Current	I_{EBO}			6		0			–	30	–	30	mA
				5		0			–	5	–	5	
* DC Forward-Current Transfer Ratio	h_{FE}[a]		10			0.5			25	250	25	250	
			4			5.0			10	100	10	100	
* Collector-to-Emitter Sustaining Voltage: (See Fig. 5, 6, & 7) With base open	$V_{CEO}(sus)$[b]					0.2		0	225	–	300	–	V
* With external base-to-emitter resistance (R_{BE}) = 50 Ω	$V_{CEX}(sus)$[b,g]				−1.5	0.2		0	300	–	375	–	V
Emitter-to-Base Voltage	V_{EBO}							0.03	6	–	6	–	V
* Base-to-Emitter Sat. Voltage	$V_{BE}(sat)$[a]					5.0		0.5	–	2	–	2	V
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$[a]					5.0		0.5	–	2	–	2	V
Output Capacitance (At 1 MHz)	C_{obo}	10					0		–	450	–	450	pF
* Second-Breakdown[c] Collector Current (With base forward biased)	$I_{S/b}$[d,e]		50						2.2	–	2.2	–	A
Second-Breakdown[c] Energy (With base reverse biased) R_B = 20 Ω, L = 50 μH	$E_{S/b}$[f]			−4.0		5.0			0.62	–	0.62	–	mJ
* Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward-Current Transfer Ratio (f = 5 MHz)	h_{fe}		10			1.0			3	–	3	–	
Saturated Switching Time: Turn-On (Delay Time + Rise Time)	t_{on}		200			5.0		0.5	–	0.5	–	0.5	μs
Storage (See Figs. 13 & 14)	t_s		200			5.0		0.5	–	3.5	–	3.5	μs
Fall (See Figs. 13 & 16)	t_f		200			5.0		0.5	–	2.0	–	2.0	μs
** Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$		10			5			–	1.6	–	1.6	°C/W

[a]Pulsed; pulse duration ≤ 350 μs, duty factor = 2%

[b]CAUTION: The sustaining voltages $V_{CEO}(sus)$ and $V_{CEX}(sus)$ MUST NOT be measured on a curve tracer. These sustaining voltages should be measured by means of the test circuit shown in Fig. 6.

[c]Safe-operating region for forward- and reverse-bias operation is explained in the RCA Solid-State Power Circuits Designer's Handbook (SP-52)

[d]$I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward biased for transistor operation in the active region at the specified collector current.

[e]Pulsed; 1-s non-repetitive pulse.

[f]$E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse bias conditions. $E_{S/b} = 1/2LI^2$ where L is a series load or leakage inductance and I is the peak collector current.

[g]Pulsed: pulse duration = 8.33 ms; duty factor = 50%

*In accordance with JEDEC registration data format (JS-6 RDF-1).

**Specified in JEDEC registration data as a derating factor of 0.625 W/°C.

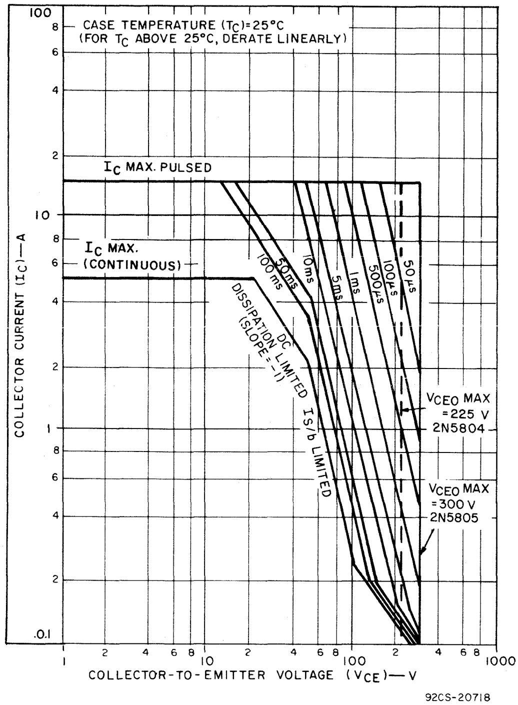


Fig. 1—Maximum operating areas for both types.

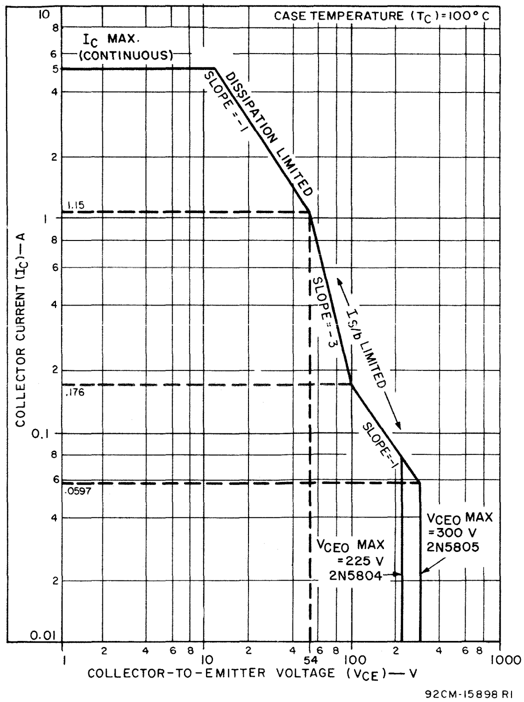


Fig. 2—Maximum operating areas for both types.

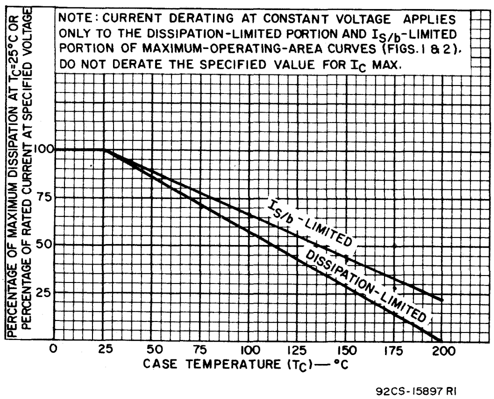


Fig. 3—Derating curves for both types.

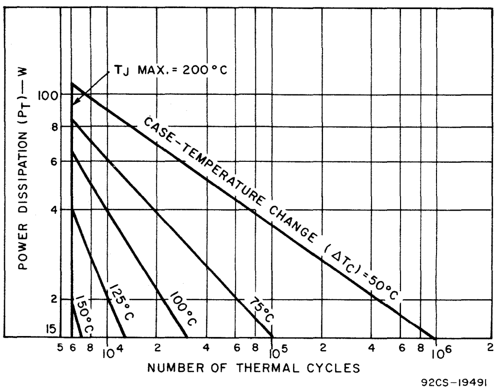


Fig. 4—Thermal-cycling rating chart.

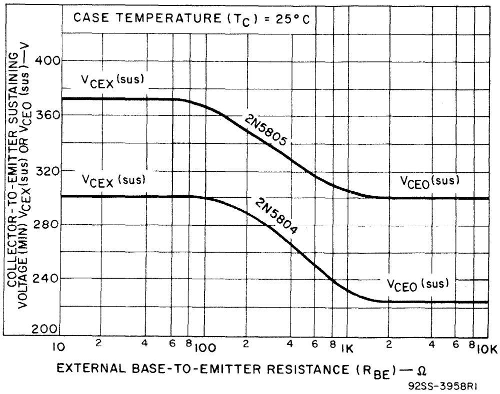


Fig. 5—Collector-to-emitter sustaining voltage characteristics.

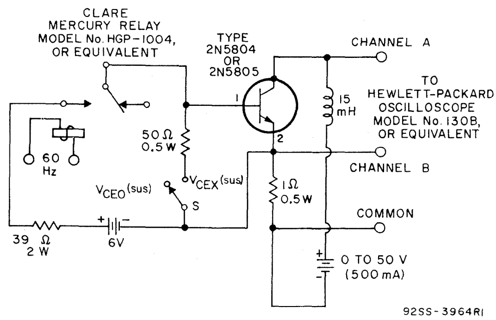


Fig. 6—Circuit used to measure sustaining voltages V_{CEO}(sus) and V_{CEX}(sus).

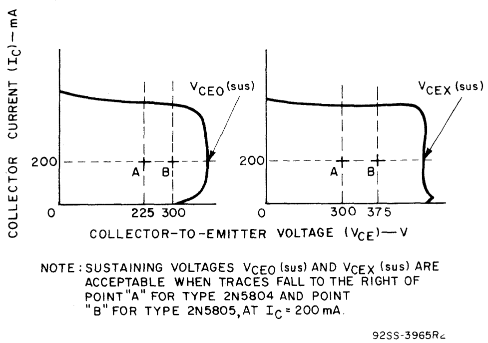


Fig. 7—Oscilloscope display for measurement of sustaining voltages (test circuit shown in Fig. 6).

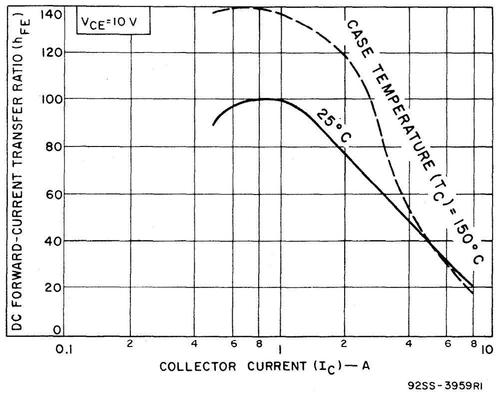


Fig. 8—Typical dc beta characteristics.

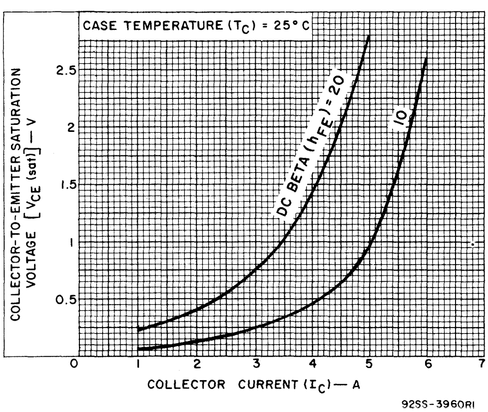


Fig. 9—Typical saturation-voltage characteristics.

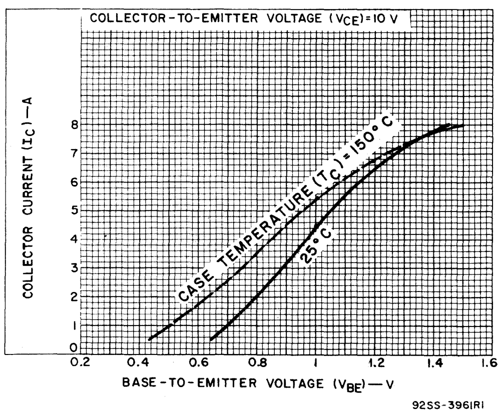


Fig. 10—Typical transfer characteristics.

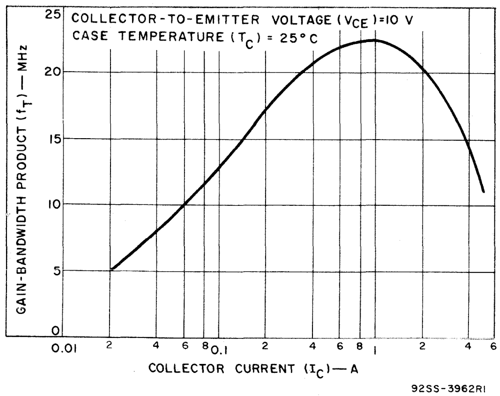


Fig. 11—Typical gain-bandwidth product.

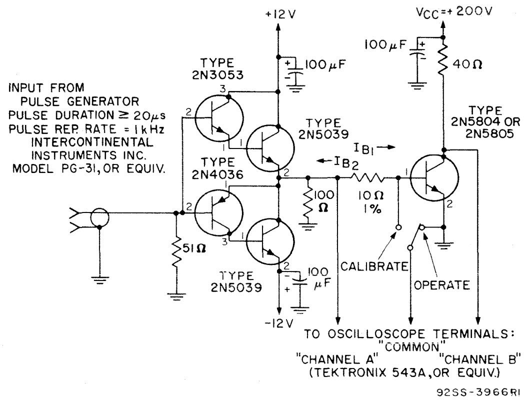


Fig. 12—Circuit used to measure switching times.

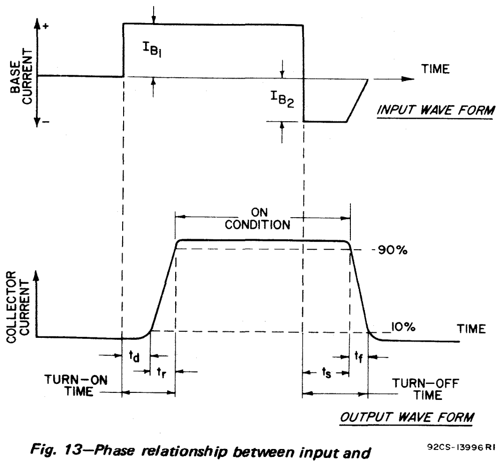


Fig. 13—Phase relationship between input and output currents showing reference points for specification of switching times (test circuit shown in Fig. 12).

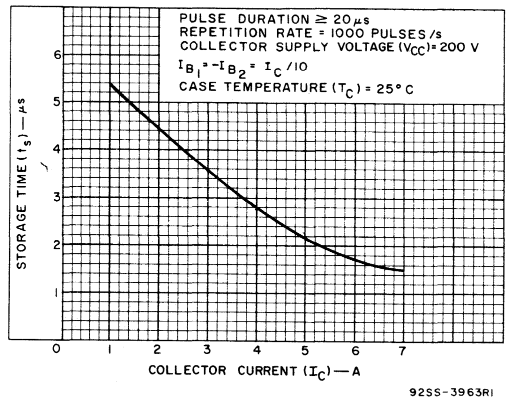


Fig. 14—Typical storage-time characteristic.

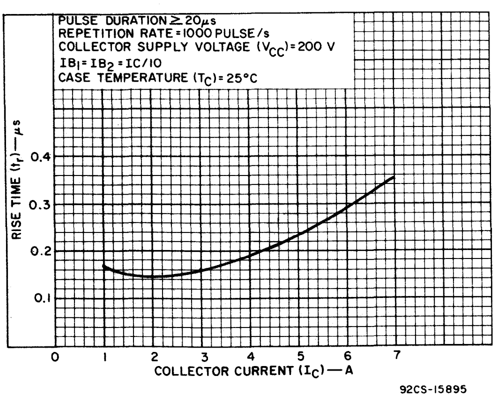


Fig. 15—Typical rise-time characteristic.

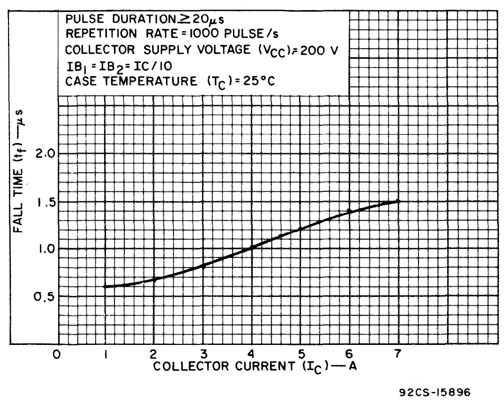
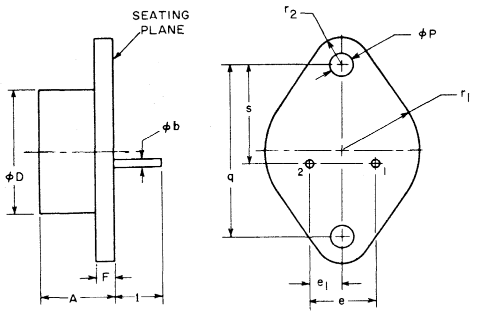


Fig. 16—Typical fall-time characteristic.

DIMENSIONAL OUTLINE
JEDEC TO-3



TERMINAL CONNECTIONS

Pin 1 — Base
Pin 2 — Emitter
Case — Collector
Mounting Flange — Collector

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
ϕb	0.038	0.043	0.97	1.09	2
ϕD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e_1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
1	0.312		7.92		2
ϕP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r_1		0.525		13.34	
r_2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS–15222

RCA
Solid State
Division

Power Transistors
2N6249
2N6250
2N6251

JEDEC TO-3

H-1570

450-V, 30-A, 175-W Silicon N-P-N Switching Transistors

For Switching Applications in Industrial and Commercial Equipment

Features:

- **High voltage ratings:**
  V_{CBO} = 450 V (2N6251)
  375 V (2N6250)
  300 V (2N6249)
- **High dissipation rating: P_T = 175 W**
- **Low saturation voltages**
- **Maximum safe-area-of-operation curves**

RCA-2N6249, 2N6250, and 2N6251● are multiple epitaxial silicon n-p-n power transistors utilizing a multiple-emitter-site structure. Multiple-epitaxial construction maximizes the volt-ampere characteristic of the device and provides fast switching speeds. Multiple-emitter-site design assures uniform current flow throughout the structure, which produces a high $I_{S/b}$ and a large safe- operation area.

These devices use the popular JEDEC TO-3 package; they differ mainly in voltage ratings, leakage-current limits, and V_{CE}(sat) ratings.

The exceptional second-breakdown capabilities and high voltage-breakdown ratings make these transistors especially suitable for off-line inverters, switching regulators, motor controls, and deflection circuit applications.

The high gain and high $E_{S/b}$ energy-handling capability of the 2N6249 make it an excellent choice for motor-control applications in which large winding inductances are encountered and high surge currents are required to start the motor.

The high breakdown voltages, low saturation voltages, and fast-switching capability of the 2N6250 and 2N6251 make them especially suitable for inverter circuits operating directly off the rectified 115-V power line or in a bridge configuration operating from the rectified 220-V line.

● Formerly RCA Dev. Nos. TA7005, TA7006, and TA7007.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N6249	2N6250	2N6251	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	300	375	450	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:					
With base open	V_{CEO}(sus)	200	275	350	V
* With reverse bias (V_{BE}) = 0 V (with base-emitter shorted)	V_{CEX}(sus)	225	300	375	V
With external base-to-emitter resistance (R_{BE}) $\leq$ 50 Ω	V_{CER}(sus)	225	300	375	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	6	6	6	V
COLLECTOR CURRENT:	I_C				
* Continuous		10	10	10	A
Peak		30	30	30	A
*CONTINUOUS BASE CURRENT	I_B	10	10	10	A
TRANSISTOR DISSIPATION:	P_T				
At case temperatures up to 25°C and V_{CE} up to 30 V		175	175	175	W
At case temperatures up to 25°C and V_{CE} above 30 V		← See Fig. 1 →			
* At case temperatures above 25°C and V_{CE} above 30 V		← See Figs. 1, 2, & 4 →			
*TEMPERATURE RANGE:					
Storage & Operating (Junction)		← -65 to +200 →			°C
*PIN TEMPERATURE (During Soldering):					
At distances $\geq$ 1/32 in. (0.8 mm) from case for 10 s max.		← 230 →			°C

* In accordance with JEDEC registration data format (JS-6, RDF-1).

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C unless otherwise specified*

Characteristic	Symbol	Test Conditions: DC Collector or Emitter Voltage (V) V_{CE}	V_{BE}	DC Current (A) I_C	I_B	I_E	Limits: Type 2N6249 Min.	Typ.	Max.	Type 2N6250 Min.	Typ.	Max.	Type 2N6251 Min.	Typ.	Max.	Units
Collector-Cutoff Current: With base open	I_{CEO}	150			0		–	–	5	–	–	–	–	–	–	mA
		225			0		–	–	–	–	–	5	–	–	–	
		300			0		–	–	–	–	–	–	–	–	5	
* With base-emitter junction reverse-biased	I_{CEV}	225	−1.5				–	–	5	–	–	–	–	–	–	
		300	−1.5				–	–	–	–	–	5	–	–	–	
		375	−1.5				–	–	–	–	–	–	–	–	5	
* With base-emitter junction reverse-biased	I_{CEV} T_C = 125°C	225	−1.5				–	–	10	–	–	–	–	–	–	
		300	−1.5				–	–	–	–	–	10	–	–	–	
		375	−1.5				–	–	–	–	–	–	–	–	10	
* Emitter-Cutoff Current	I_{EBO}		−6				–	–	1	–	–	1	–	–	1	mA
* Collector-to-Emitter Sustaining Voltage *(see Figs. 15 & 16)* With base open	$V_{CEO}(sus)^b$			0.2			200[b]	–	–	275[b]	–	–	350[b]	–	–	V
With external base-to-emitter resistance (R_{BE}) = 50 Ω	$V_{CER}(sus)^b$			0.2			225[b]	–	–	300[b]	–	–	375[b]	–	–	V
* Emitter-to-Base Voltage	V_{EBO}					0.001	6	–	–	6	–	–	6	–	–	V
* DC Forward-Current Transfer Ratio	h_{FE}	3		10			10	–	50	–	–	–	–	–	–	
		3		10			–	–	–	8	–	50	–	–	–	
		3		10			–	–	–	–	–	–	6	–	50	
* Base-to-Emitter Saturation Voltage	$V_{BE}(sat)^a$			10	1		–	–	2.25	–	–	–	–	–	–	V
				10	1.25		–	–	–	–	–	2.25	–	–	–	
				10	1.67		–	–	–	–	–	–	–	–	2.25	
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)^a$			10	1		–	–	1.5	–	–	–	–	–	–	V
				10	1.25		–	–	–	–	–	1.5	–	–	–	
				10	1.67		–	–	–	–	–	–	–	–	1.5	
* Magnitude of Common Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	10		1			2.5	8	–	2.5	8	–	2.5	8	–	
Second Breakdown Collector Current (With base forward-biased) Pulse duration (non-repetitive) = 1 s	$I_{S/b}^c$	30					5.8	–	–	5.8	–	–	5.8	–	–	A
* Second Breakdown[c] Energy (With base reverse-biased) R_B = 50 Ω, L = 50 μH	$E_{S/b}^d$		−4	10			2.5	–	–	2.5	–	–	2.5	–	–	mJ
* Switching Times: Rise *(See Figs. 13, 17, & 18)*	t_r^e	V_{CC} = 200 V		10	1		–	0.8	2	–	–	–	–	–	–	μs
				10	1.25		–	–	–	–	0.8	2	–	–	–	
				10	1.67		–	–	–	–	–	–	–	0.8	2	
Storage *(See Figs. 11, 12, 17, & 18)*	t_s^e	V_{CC} = 200 V		10	1		–	1.8	3.5	–	–	–	–	–	–	
				10	1.25		–	–	–	–	1.8	3.5	–	–	–	
				10	1.67		–	–	–	–	–	–	–	1.8	3.5	
Fall *(See Figs. 14, 17, & 18)*	t_f^e	V_{CC} = 200 V		10	1		–	0.5	1	–	–	–	–	–	–	
				10	1.25		–	–	–	–	0.5	1	–	–	–	
				10	1.67		–	–	–	–	–	–	–	0.5	1	
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$	10		5			–	–	1	–	–	1	–	–	1	°C/W

[a] Pulsed; pulse duration $\leq$350 μs, duty factor = 2%.

[b] CAUTION: The sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$ MUST NOT be measured on a curve tracer. These sustaining voltages should be measured by means of the test circuit shown in Fig. 15.

[c] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward-biased for transistor operation in the active region.

[d] $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse-bias conditions. $E_{S/b} = 1/2\ LI^2$ where L is a series load or leakage inductance, and I is the peak collector current.

[e] $I_{B1} = I_{B2}$ = value shown.

* In accordance with JEDEC registration data format (JS-6 RDF-1).

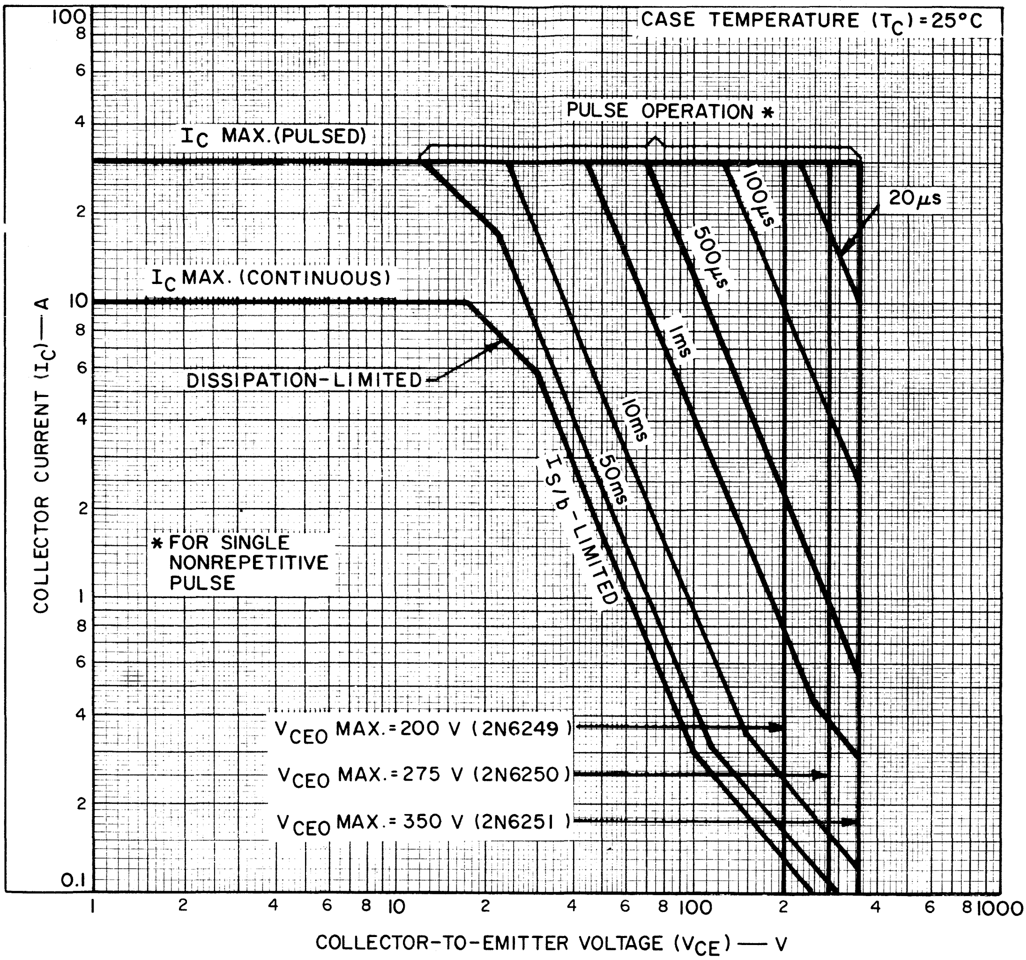


Fig. 1—Maximum operating areas for all types.

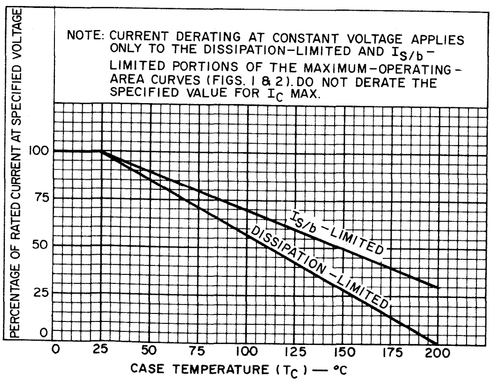


Fig. 2 —Dissipation derating and $I_{S/b}$ derating for all types.

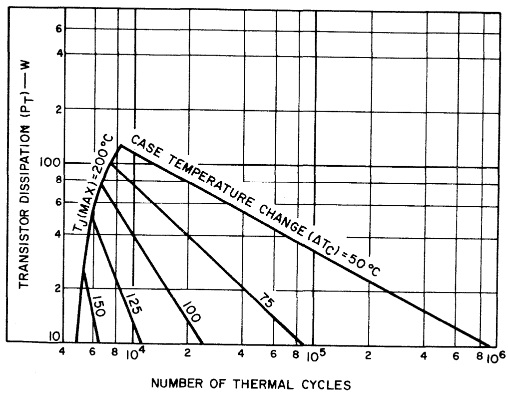


Fig. 3 —Thermal-cycle rating chart for all types.

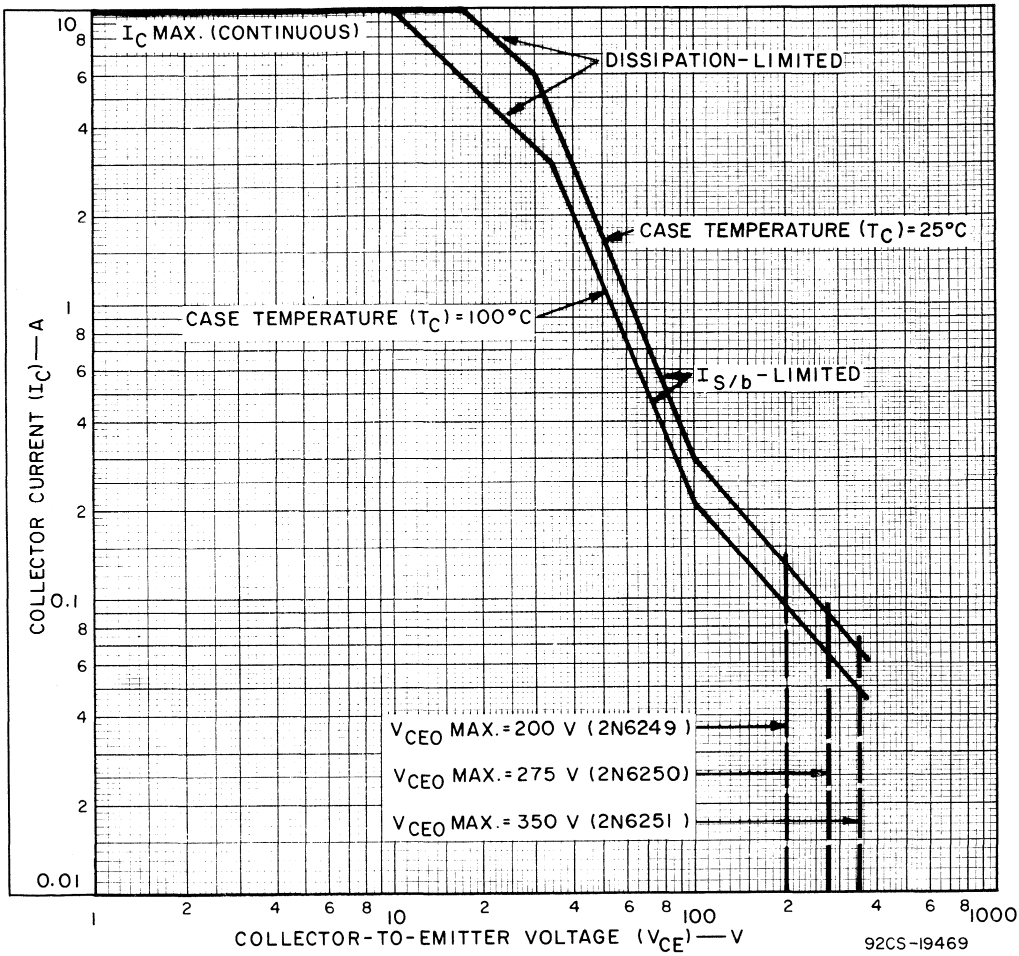


Fig.4 —Maximum operating areas for all types.

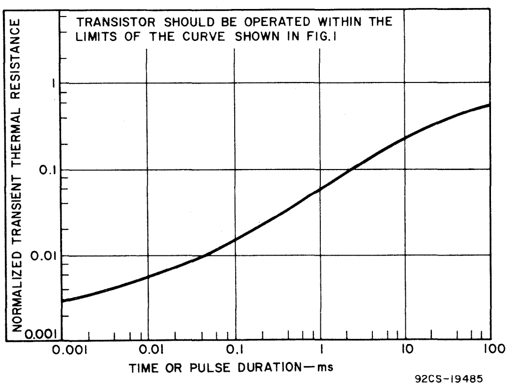


Fig.5—Typical thermal response characteristic for all types.

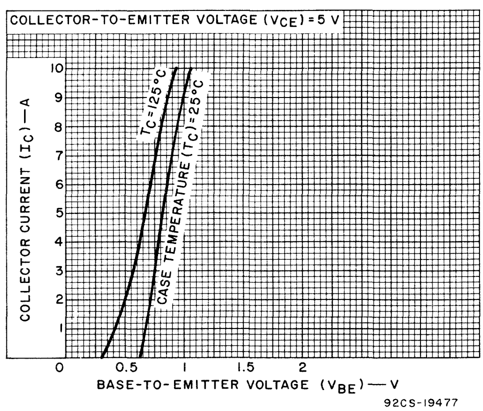


Fig.6—Typical transfer characteristics for all types.

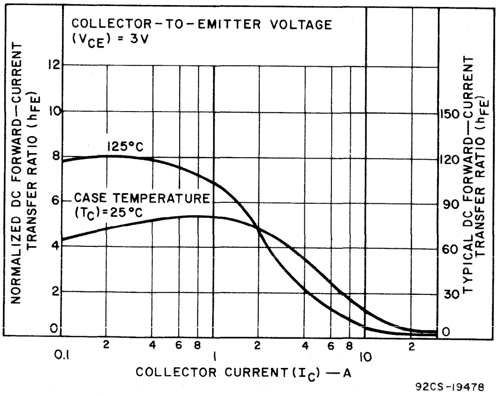


Fig.7—Typical normalized dc beta characteristics for all types.

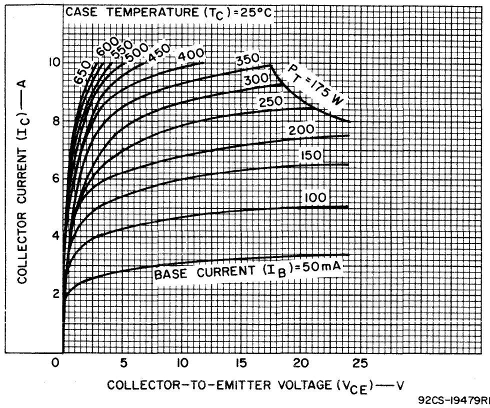


Fig.8—Typical output characteristics for all types.

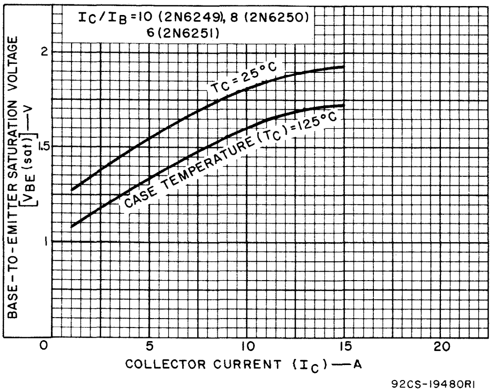


Fig.9—Typical base-to-emitter saturation voltage characteristics for all types.

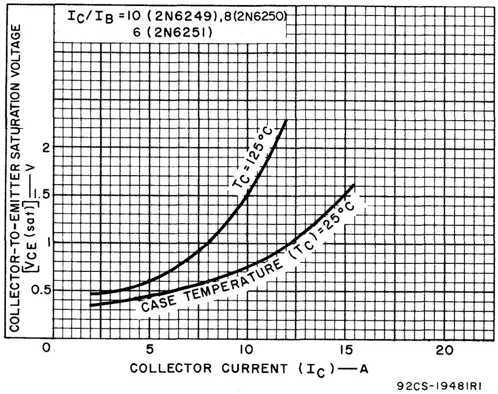


Fig.10—Typical collector-to-emitter saturation voltage characteristics for all types.

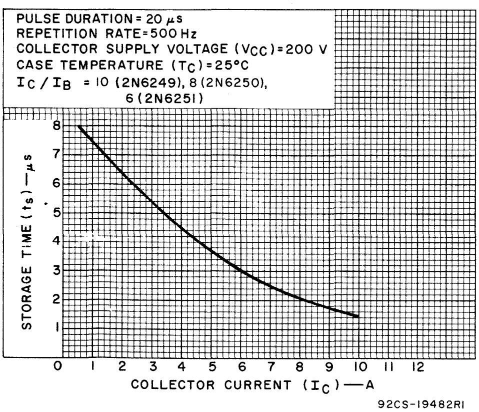


Fig.11—Typical storage-time characteristics for all types (with constant forced gain).

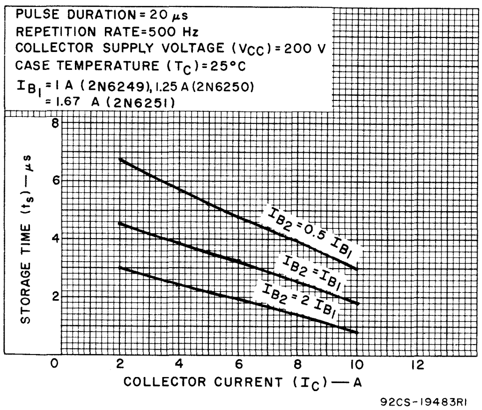


Fig.12—Typical storage-time characteristics for all types (with constant base drive).

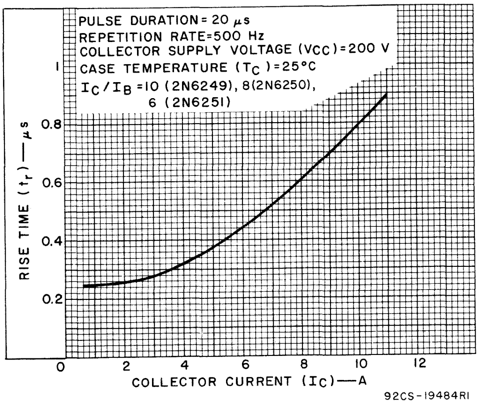


Fig. 13—Typical rise-time characteristic for all types.

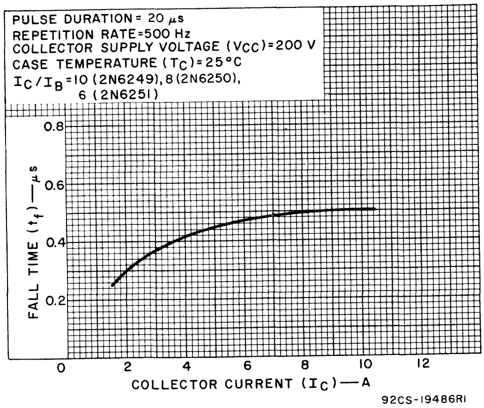


Fig. 14—Typical fall-time characteristic for all types.

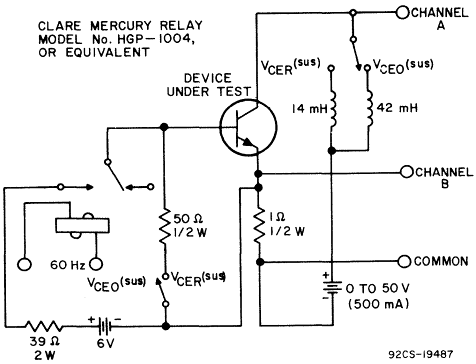
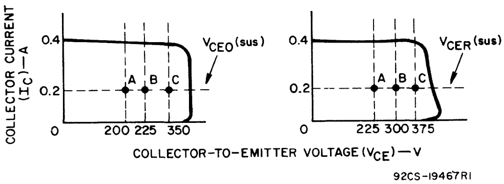


Fig. 15—Circuit used to measure sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$ for all types.



The sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$ are acceptable when the traces fall to the right of point "A" for type 2N6249, point "B" for type 2N6250, and point "C" for type 2N6251 (I_C = 0.2 A).

Fig. 16—Oscilloscope display for measurement of sustaining voltages. (Test circuit shown in Fig. 15).

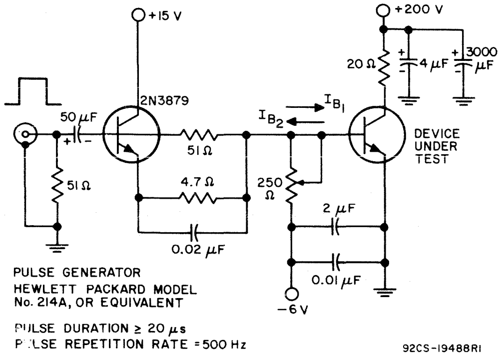


Fig. 17—Circuit used to measure switching times for all types.

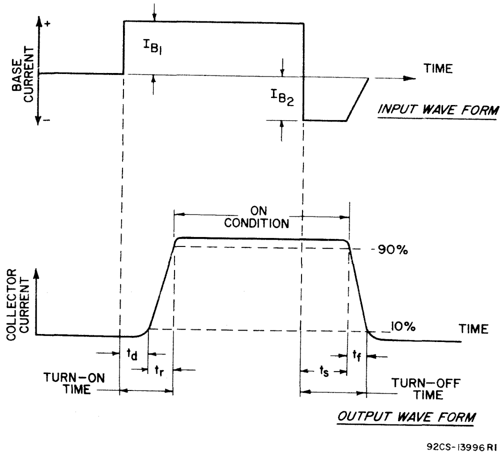


Fig. 18—Phase relationship between input and output currents showing reference points for specification of switching times (Test circuit shown in Fig. 17).

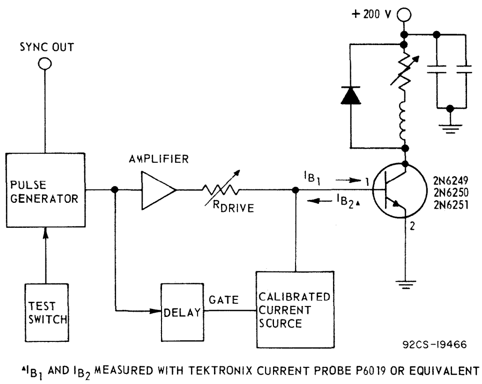


Fig. 19—Circuit used to measure inductive-load switching times for all types.

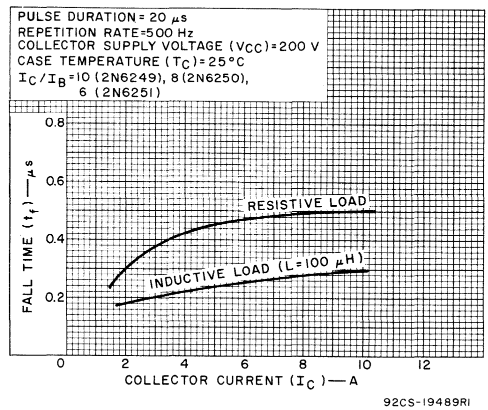
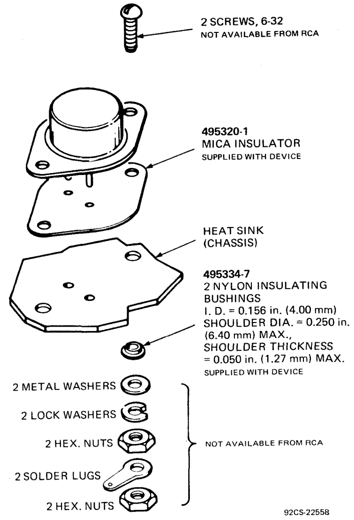


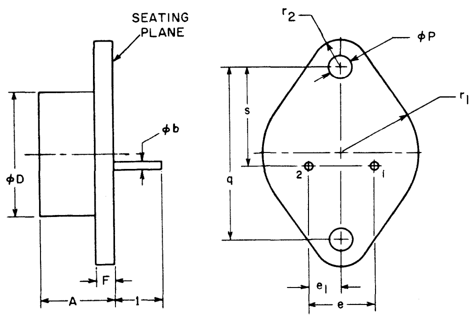
Fig. 20—Typical inductive- and resistive-load fall-time characteristics for all types.



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.21—Suggested mounting hardware.

DIMENSIONAL OUTLINE
JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
φb	0.038	0.043	0.97	1.09	2
φD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e_1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
l	0.312		7.92		2
φP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r_1		0.525		13.34	
r_2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS—15222

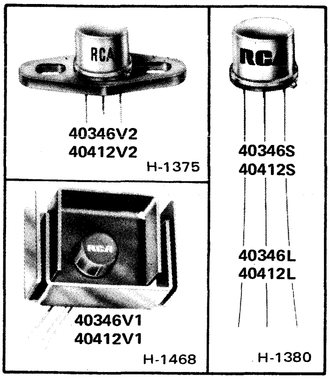
TERMINAL CONNECTIONS

Pin 1 — Base
Pin 2 — Emitter
Case — Collector
Mounting Flange — Collector

RCA
Solid State
Division

Power Transistors

40346 40346V1 40346V2 40412 40412V1 40412V2



Medium-Power Silicon N-P-N Planar Transistors

For High-Voltage Switching and Linear-Amplifier Applications

Features:

- **For operation at junction temperature up to 200°C**
- **Planar construction for low noise and low leakage**

These devices are generally available with ½-inch leads (TO-39 package). They are also available in the U.S.A., Canada, Latin America, and Far East with 1½-inch leads (TO-5 package); the shorter-lead versions are specified by a suffix letter "S" after the type number, and the longer-lead versions by a suffix letter "L".

RCA-40346, -40346V1, -40346V2, -40412, -40412V1, and -40412V2 are silicon n-p-n transistors having high breakdown voltages, high frequency-response capability, and fast switching speeds.

These transistors are intended for a wide variety of low- and medium-power, high-voltage applications. Types 40346, 40346V1, and 40346V2 are especially useful in such devices as neon indicator and NIXIE* driver circuits and in differential and operational amplifiers. Types 40412, 40412V1, and 40412V2 are especially suited for class-A ac/dc audio-amplifier service.

Types 40346 and 40412 are supplied in a JEDEC TO-39 (S) or TO-5 (L) package; types 40346V1 and 40412V1, with a factory-attached heat radiator for greater free-air dissipation, capability; and types 40346V2 and 40412V2 are supplied with an attached flange for increased power dissipation and mounting convenience.

* Nixie is a Registered Trademark of Burroughs Corporation, Electronic Components Division, Plainfield, N. J.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		40346	40346V1	40346V2	40412	40412V1	40412V2	
COLLECTOR-TO-EMITTER VOLTAGE:	$V_{CER(sus)}$							
With R_{BE} = 1,000 Ω		175	175	175	–	–	–	V
With R_{BE} = 10,000 Ω		–	–	–	250	250	250	V
COLLECTOR CURRENT	I_C	1	1	1	1	1	1	A
BASE CURRENT	I_B	0.5	0.5	0.5	0.5	0.5	0.5	A
TRANSISTOR DISSIPATION:	P_T							
At case temperatures up to 25°C		10	–	10	10	–	10	W
At free-air temperatures up to 50°C		1	–	–	1	–	–	W
At free-air temperatures up to 25°C		–	4	–	–	4	–	W
At other temperatures		See Fig. 1						
TEMPERATURE RANGE:								
Storage and Operating		–65 to +200						°C

9-73

ELECTRICAL CHARACTERISTICS, *Case Temperature (T_C) = 25°C, Unless Otherwise Specified*

Characteristic	Symbol	DC Collector Volts		DC Emitter Volts	DC Current (mA)			LIMITS												UNITS
								40346		40346V1		40346V2		40412		40412V1		40412V2		
		V_{CE}	V_{CB}	V_{EB}	I_C	I_E	I_B	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Collector-Cutoff Current:																				
With base open	I_{CEO}	100	–	–	–	–	–	–	5	–	5	–	5	–	–	–	–	–	–	μA
With R = 10,000 ohms	I_{CER}	100	–	–	–	–	–	–	–	–	–	–	–	–	1	–	1	–	1	mA
With base reverse-biased:																				
T_C=25° C	I_{CEV}	200	–	1.5	–	–	–	–	10	–	10	–	10	–	–	–	–	–	–	μA
T_C=150° C	I_{CEV}	200	–	1.5	–	–	–	–	1	–	1	–	1	–	–	–	–	–	–	mA
T_C=150° C	I_{CEV}	150	–	1.5	–	–	–	–	–	–	–	–	–	–	2	–	2	–	2	mA
Emitter-Cutoff Current	I_{EBO}	–	–	4	–	–	–	–	5	–	5	–	5	–	–	–	–	–	–	μA
	I_{EBO}	–	–	3	–	–	–	–	–	–	–	–	–	–	100	–	100	–	100	μA
Collector-To-Emitter Sustaining Voltage: With external base-emitter resistor																				
R_{BE}=1,000 ohms	$V_{CER(sus)}$	–	–	–	50	–	–	175	–	175	–	175	–	–	–	–	–	–	–	V
R_{BE}=10,000 ohms	$V_{CER(sus)}$	–	–	–	50	–	–	–	–	–	–	–	–	250	–	250	–	250	–	V
Collector-To-Emitter Saturation Voltage	$V_{CE(sat)}$	–	–	–	10	–	1	–	0.5	–	0.5	–	0.5	–	–	–	–	–	–	V
Base-To-Emitter Voltage	V_{BE}	10	–	–	10	–	–	–	1	–	1	–	1	–	–	–	–	–	–	V
Second-Breakdown Current (Safe-operating region)	$I_{S/b}$●	200	–	–	–	–	–	–	–	–	–	–	–	50	–	50	–	50	–	mA
DC Forward-Current Transfer Ratio	h_{FE}	10	–	–	10	–	–	25	–	25	–	25	–	–	–	–	–	–	–	
	h_{FE}	20	–	–	30	–	–	–	–	–	–	–	–	40	–	40	–	40	–	
Small-Signal Forward-Current Transfer Ratio at F=5 MHz	h_{fe}	10	–	–	10	–	–	2	–	2	–	2	–	2	–	2	–	2	–	
Output Capacitance (At 1 MHz)	C_{ob}	–	10	–	–	0	–	–	–	–	–	–	–	–	10	–	10	–	10	pF
Thermal Resistance: Junction-to-case	θ_{J-C}	–	–	–	–	–	–	–	15	–	–	–	15	–	15	–	–	–	15	°C/W
Junction-to-free air	θ_{J-FA}	–	–	–	–	–	–	–	–	–	45	–	–	–	–	–	45	–	–	°C/W

● $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage.

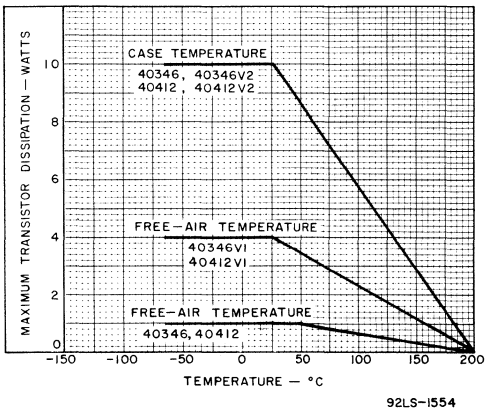


Fig.1 — Dissipation derating curves.

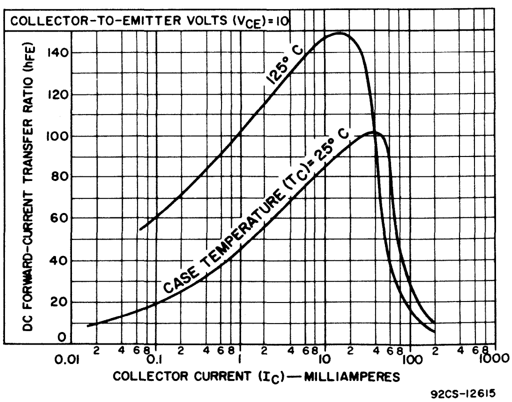
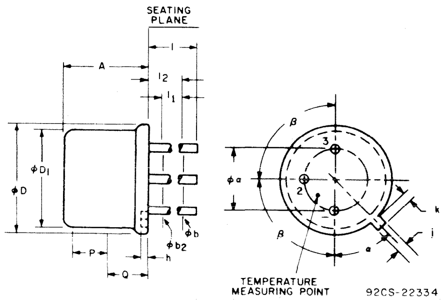


Fig.2 — Typical dc-beta characteristics for all types.

DIMENSIONAL OUTLINE FOR 40346 AND 40412



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
ϕa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
ϕb	0.016	0.021	0.406	0.533	2
ϕb_2	0.016	0.019	0.406	0.483	2
ϕD	0.350	0.370	8.89	9.40	
ϕD_1	0.305	0.335	8.00	8.51	
h	0.009	0.041	0.229	1.04	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
L {long lead	1.500		38.10		2
L {short lead	0.500		12.70		2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

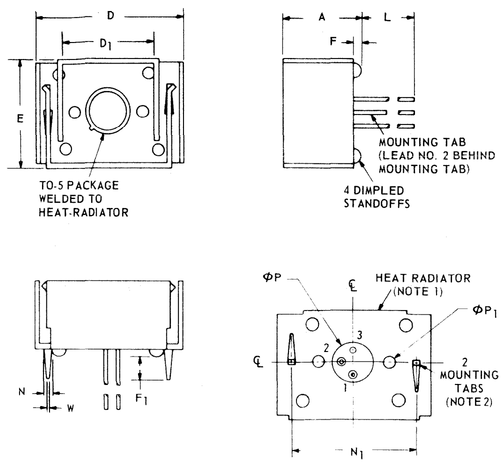
Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and l. Diameter is uncontrolled in l_1.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

DIMENSIONAL OUTLINE FOR 40346V1 AND 40412V1



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	0.630	–	16.00	
D	1.205	1.235	30.61	31.37	
D_1	0.775	0.785	19.69	19.93	
E	0.875	0.905	22.22	22.99	
F	0.040	0.055	1.02	1.40	
F_1	0.160	0.195	4.06	4.95	
L {long lead	1.410	–	35.81	–	
L {short lead	0.410	–	10.41	–	
ϕP	0.295	0.305	7.493	7.747	
ϕP_1	0.093	0.095	2.362	2.413	
N	0.048	0.062	1.21	1.57	
N_1	0.998	1.002	25.349	25.450	3
W	0.048	0.052	1.219	1.320	

NOTES:

1. **0.035 C.R.S., finish—electroless nickel plate.**
2. **Recommended hole size for printed-circuit board is** 0.070 in. (1.78 mm) dia.
3. **Measured at bottom of heat-radiator.** 92CS-22335

TERMINAL CONNECTIONS

Lead 1 — Emitter
Lead 2 — Base
Case, Lead 3 — Collector

TERMINAL CONNECTIONS

Lead 1 — Emitter
Lead 2 — Base
Heat Radiator, , Lead 3 — Collector

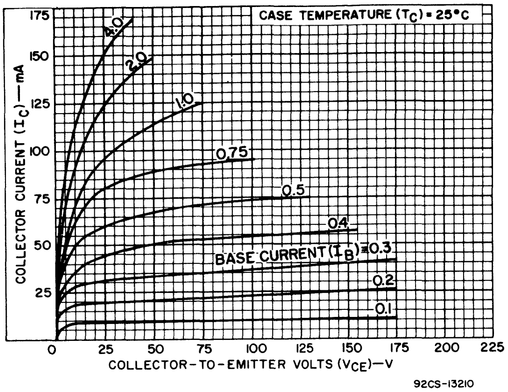


Fig.3 — Typical output characteristics for all types.

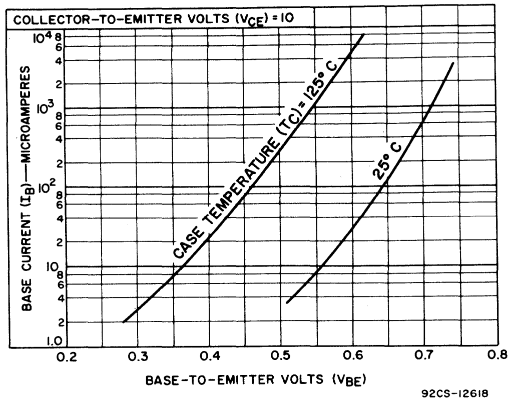


Fig.4 — Typical input characteristics for all types.

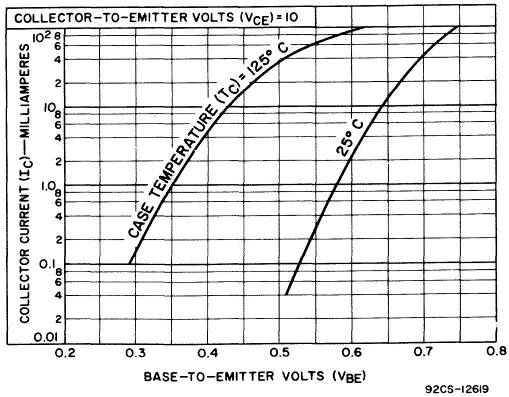
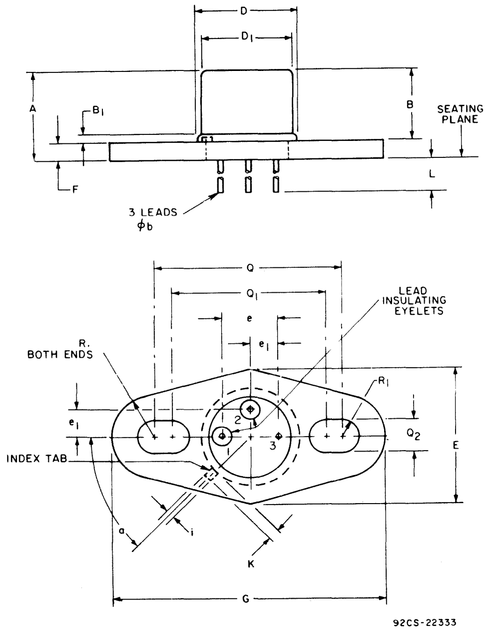


Fig.5 — Typical transfer characteristics for all types.

DIMENSIONAL OUTLINE FOR 40346V2 AND 40412V2



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	0.328	–	8.33	
B	0.240	0.260	6.10	6.60	
B_1	0.009	0.125	0.229	3.18	
ϕ_b	0.016	0.019	0.406	0.483	
D	0.335	0.370	8.51	9.40	
D_1	0.305	0.335	7.75	8.51	
E	0.495	0.505	12.57	12.83	
e	0.200 T.P.		5.08 T.P.		1
e_1	0.100 T.P.		2.54 T.P.		1
F	0.062	0.068	1.57	1.74	
G	0.995	1.005	25.27	25.53	
i	0.028	0.034	0.711	0.864	
k	0.029	0.045	0.737	1.14	
L {long lead	1.430	–	36.32	–	
L {short lead	0.430	–	10.92	–	
Q	0.685	0.691	17.40	17.55	
Q_1	0.559	0.565	14.20	14.35	
Q_2	0.128	0.132	3.25	3.35	
R	0.156 T.P.		3.96 T.P.		1
R_1	0.064	0.066	1.63	1.67	
α	45° T.P.				1, 2

NOTES:
1. True position.
2. Tab centerline.

TERMINAL CONNECTIONS

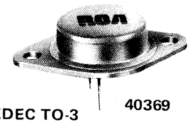
Lead 1 — Emitter
Lead 2 — Base
Flange, Lead 3 — Collector

RCA

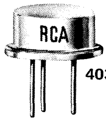
Solid State
Division

Power Transistors

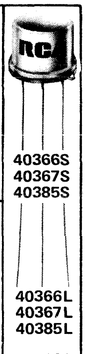
40366-40369
40385



JEDEC TO-3 40369
H-1570



40368
H-1015
JEDEC TO-8



40366S
40367S
40385S

40366L
40367L
40385L

H-1380

High-Reliability Silicon N-P-N Power Transistors

For Power Switching and Amplifier Applications

Features

- High reliability assured by five preconditioning steps
- Group A test data included*
- Transistors utilize JEDEC hermetic packages;
  40369 – TO-3
  40368 – TO-8
  40366, 40367, 40385 } See Note at right

Note:

These devices are generally available with ½-inch leads (TO-39 package). They are also available in the U.S.A., Canada, Latin America, and Far East with 1½-inch leads (TO-5 package); the shorter-lead versions are specified by a suffix letter "S" after the type number, and the longer-lead versions by a suffix letter "L".

RCA-40366–40369 and 40385 are silicon n-p-n power transistors derived from JEDEC types 2N2102, 2N1482, 2N1486, 2N1490, and 2N3439. They are specially preconditioned for use in power-switching and amplifier applications in those instances where high reliability is a requisite.

- High voltage ratings:
  V_{CER} = 80 V max. (40366)
  V_{CEV} = 100 V max. (40367, 40368 & 40369)
  V_{CEO} = 350 V max. (40385)
- High power-dissipation capability:
  P_T = 5 W max. (40366, 40367 & 40385)
  = 25 W max. (40368)
  = 75 W max. (40369)

* Group A test data shown on pages 2 & 3.

MAXIMUM RATINGS, *Absolute-Maximum Values:*		40366	40367	40368	40369	40385	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	120	100	100	100	450	V
COLLECTOR-TO-EMITTER VOLTAGE:							
With external base-to-emitter resistance (R_{BE}) $\leq$ 10 Ω	V_{CER}	80	–	–	–	–	V
With –1.5 V (V_{BE}) of reverse bias	V_{CEV}	–	100	100	100	–	V
With base open	V_{CEO}	65	55	55	55	350	V
EMITTER-TO-BASE VOLTAGE...........	V_{EBO}	7	12	12	10	7	V
CONTINUOUS COLLECTOR CURRENT....	I_C	1	1.5	3	6	1	A
CONTINUOUS BASE CURRENT	I_B	–	1	1.5	3	–	A
TRANSISTOR DISSIPATION:	P_T						
At case temperature up to 25°C		5	5	25	75	10	W
At free-air temperature up to 25°C		1	1	–	–	1	W
At temperatures above 25°C		← Derate linearly to 0 watts at 200°C →					
TEMPERATURE RANGE:							
Storage & Operating (Junction)..........		← –65 to 200 →					°C
PIN or LEAD TEMPERATURE (During soldering):							
At distances $\geq$ 1/32 in. (0.79 mm) from seating plane for 10 s max.....		255	255	235	235	255	°C

9-73

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C) = 25°C

Characteristic	Symbol	TEST CONDITIONS						LIMITS										Units
		DC Collector Volts		DC Emitter Volts	DC Current (Milliamperes)			Type 40366		Type 40367		Type 40368		Type 40369		Type 40385		
		V_{CB}	V_{CE}	V_{EB}	I_C	I_E	I_B	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Collector-Cutoff Current	I_{CBO}	30				0		–	–	–	4.0	–	9.0	–	10	–	–	μA
		60				0		–	2.0	–	–	–	–	–	–	–	–	nA
	I_{CEO}		300				0	–	–	–	–	–	–	–	–	–	20	μA
	I_{CEV}		450	1.5				–	–	–	–	–	–	–	–	–	500	μA
Emitter-Cutoff Current	I_{EBO}			5	0			–	5.0	–	–	–	–	–	–	–	–	nA
				6	0			–	–	–	–	–	–	–	–	–	20	μA
				10	0			–	–	–	–	–	–	–	6.0	–	–	μA
				12	0			–	–	–	2.0	–	5.0	–	–	–	–	μA
DC Forward-Current Transfer Ratio	h_{FE}		4		200			–	–	35	100	–	–	–	–	–	–	
			4		750			–	–	–	–	35	100	–	–	–	–	
			4		1500			–	–	–	–	–	–	25	75	–	–	
			10		0.01			10	–	–	–	–	–	–	–	–	–	
			10		0.1			20	–	–	–	–	–	–	–	–	–	
			10		2			–	–	–	–	–	–	–	–	30	–	
			10		20			–	–	–	–	–	–	–	–	40	160	
			10		150•			40	120	–	–	–	–	–	–	–	–	
			10		500•			25	–	–	–	–	–	–	–	–	–	
			10		1000•			10	–	–	–	–	–	–	–	–	–	
Collector-to-Base Breakdown Voltage	BV_{CBV}			1.5	0.1			120	–	–	–	–	–	–	–	–	–	V
Collector-to-Emitter Breakdown Voltage	BV_{CEV}			1.5	0.25			–	–	100	–	100	–	100	–	–	–	V
Emitter-to-Base Breakdown Voltage	BV_{EBO}					0.1		7.0	–	–	–	–	–	–	–	–	–	V
Collector-to-Emitter Sustaining Voltage: With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{CER}(sus)$				100•			80	–	–	–	–	–	–	–	–	–	V
With base open	$V_{CEO}(sus)$				50		0	–	–	55	–	–	–	–	–	350	–	V
					100•		0	65	–	–	–	–	–	–	–	–	–	
					100		0	–	–	–	–	55	–	55	–	–	–	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				50		4	–	–	–	–	–	–	–	–	–	0.5	V
					150•		15	–	0.5	–	–	–	–	–	–	–	–	
					200		10	–	–	–	1.4	–	–	–	–	–	–	
					750		40	–	–	–	–	–	0.75	–	–	–	–	
					1300		100	–	–	–	–	–	–	–	1.0	–	–	
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$				150•		15	–	1.1	–	–	–	–	–	–	–	–	V
					50		4	–	–	–	–	–	–	–	–	–	1.3	
Base-to-Emitter Voltage	V_{BE}		4		200		–	–	–	–	3.0	–	–	–	–	–	–	V
			4		750		–	–	–	–	–	–	2.5	–	–	–	–	
			4		1500		–	–	–	–	–	–	–	–	2.5	–	–	

•Pulsed; pulse duration = 300 μs, duty factor = 1.8%.

GROUP-A TESTS (IN ACCORDANCE WITH MIL-S-19500)

TEST METHOD PER MIL-STD-750	EXAMINATION OR TEST	CONDITIONS	LTPD*	SYMBOL	LIMITS										UNITS
					40366		40367		40368		40369		40385		
					Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
2071	**Subgroup 1** Visual and Mechanical Examination	–	10 –	–	–	–	–	–	–	–	–	–	–	–	–
3036D	**Subgroup 2** Collector-Cutoff Current	V_{CB} = 30V, I_E = 0	5	I_{CBO}	–	–	–	4.0	–	9.0	–	10	–	–	μA
		V_{CB} = 60V, I_E = 0	–	I_{CBO}	–	2.0	–	–	–	–	–	–	–	–	nA
3041A	Collector-Cutoff Current	V_{CE} = 450V, V_{BE} = -1.5V	–	I_{CEV}	–	–	–	–	–	–	–	–	–	500	μA
3041D	Collector-Cutoff Current	V_{CE} = 300V, I_E = 0	–	I_{CEO}	–	–	–	–	–	–	–	–	–	20	μA

GROUP-A TESTS (CONT.)

TEST METHOD PER MIL-STD-750	EXAMINATION OR TEST	CONDITIONS	LTPD*	SYMBOL	LIMITS 40366 Min.	40366 Max.	40367 Min.	40367 Max.	40368 Min.	40368 Max.	40369 Min.	40369 Max.	40385 Min.	40385 Max.	UNITS
3061D	Emitter-Cutoff Current	V_{EB} = 5V, I_C = 0	–	I_{EBO}	–	5.0	–	–	–	–	–	–	–	–	nA
		V_{EB} = 6V, I_C = 0	–	I_{EBO}	–	–	–	–	–	–	–	–	–	20	μA
		V_{EB} = 10V, I_C = 0	–	I_{EBO}	–	–	–	–	–	–	–	6.0	–	–	μA
		V_{EB} = 12V, I_C = 0	–	I_{EBO}	–	–	–	2.0	–	5.0	–	–	–	–	μA
3001A	Collector-to-Base Breakdown Voltage	I_C = 100μA, V_{EB} = 1.5V	–	BV_{CBV}	120	–	–	–	–	–	–	–	–	–	V
3026D	Emitter-to-Base Breakdown Voltage	I_E = 100μA, I_C = 0	–	BV_{EBO}	7.0	–	–	–	–	–	–	–	–	–	V
3011A	Collector-to-Emitter Breakdown Voltage	I_C = 0.25mA, V_{EB} = 1.5V	–	BV_{CEV}	–	–	100	–	100	–	–	–	–	–	V
		I_C = 0.5mA, V_{EB} = 1.5V	–	BV_{CEV}	–	–	–	–	–	–	100	–	–	–	V
3011D	Collector-to-Emitter Sustaining Voltage	I_C = 50mA, I_B = 0	–	$V_{CEO}(sus)$	–	–	55	–	–	–	–	–	350	–	V
		I_C = 100mA●, I_B = 0	–	$V_{CEO}(sus)$	65	–	–	–	–	–	–	–	–	–	V
		I_C = 100mA, I_B = 0	–	$V_{CEO}(sus)$	–	–	–	–	55	–	55	–	–	–	V
3011B	Collector-to-Emitter Sustaining Voltage	I_C = 100mA●, R_{BE} = 10Ω	–	$V_{CER}(sus)$	80	–	–	–	–	–	–	–	–	–	V
3071	Subgroup 3 Collector-to-Emitter Saturation Voltage	I_C = 50mA, I_B = 4mA	–	$V_{CE}(sat)$	–	–	–	–	–	–	–	–	–	0.5	V
		I_C = 150mA●, I_B = 15mA	5	$V_{CE}(sat)$	–	0.5	–	–	–	–	–	–	–	–	V
		I_C = 200mA, I_B = 10mA	–	$V_{CE}(sat)$	–	–	–	1.4	–	–	–	–	–	–	V
		I_C = 750mA, I_B = 40mA	–	$V_{CE}(sat)$	–	–	–	–	–	0.75	–	–	–	–	V
		I_C = 1.5A, I_B = 100mA	–	$V_{CE}(sat)$	–	–	–	–	–	–	–	1.0	–	–	V
3066A	Base-to-Emitter Saturation Voltage	I_C = 50mA, I_B = 4mA	–	$V_{BE}(sat)$	–	–	–	–	–	–	–	–	–	1.3	V
		I_C = 150mA●, I_B = 15mA	–	$V_{BE}(sat)$	–	1.1	–	–	–	–	–	–	–	–	V
3066A	Base-to-Emitter Voltage	I_C = 200mA, V_{CE} = 4V	–	V_{BE}	–	–	–	3.0	–	–	–	–	–	–	V
		I_C = 750mA, V_{CE} = 4V	–	V_{BE}	–	–	–	–	–	2.5	–	–	–	–	V
3076	DC Forward-Current Transfer Ratio	I_C = 0.01mA, V_{CE} = 10V	–	h_{FE}	10	–	–	–	–	–	–	–	–	–	
		I_C = 0.1mA, V_{CE} = 10V	–	h_{FE}	20	–	–	–	–	–	–	–	–	–	
		I_C = 2mA, V_{CE} = 10V	–	h_{FE}	–	–	–			–	–	–	30	–	
		I_C = 20mA, V_{CE} = 10V	–	h_{FE}	–	–			–	–	–	–	15	60	
		I_C = 150mA●, V_{CE} = 10V	–	h_{FE}	40	120	–	–	–	–	–	–	–	–	
		I_C = 200mA, V_{CE} = 4V	–	h_{FE}	–	–	35	100	–	–	–	–	–	–	
		I_C = 500mA●, V_{CE} = 10V	–	h_{FE}	25	–	–	–	–	–	–	–	–	–	
		I_C = 750mA, V_{CE} = 4V	–	h_{FE}	–	–	–	–	35	100	–	–	–	–	
		I_C = 1A●, V_{CE} = 10V	–	h_{FE}	10	–	–	–	–	–	–	–	–	–	
		I_C = 1.5A, V_{CE} = 4V	–	h_{FE}	–	–	–	–	–	–	25	75	–	–	

●Pulsed; pulse duration = 300μs, duty factor = 1.8%. *Lot tolerance per cent defective.

The RCA-40366, 40367, 40368, 40369, and 40385 are high-reliability versions of the RCA-2N2102, 2N1482, 2N1486, 2N1490 and 2N3439*, respectively. These transistors are intended for medium- and high-power switching and amplifier applications in military and industrial equipment.

The 40366 and 40385 are silicon n-p-n types with a power-dissipation capability of 5 watts each. The 40367 is a silicon n-p-n hometaxial type with a power-dissipation capability of 5 watts. These devices are available with either 1-½-inch leads (TO-5 package) or ½-inch leads (TO-39 package).

The 40368 is a silicon n-p-n hometaxial type in a JEDEC TO-8 package with a power-dissipation capability of 25 watts.

The 40369 is a silicon n-p-n hometaxial type in the popular JEDEC TO-3 package and has a dissipation capability of 75 watts.

The 40366, the high-reliability version of the 2N2102, features linear beta characteristics which are controlled over a wide range of collector currents (0.01 mA to 1 A).

The 40367, 40368, and 40369, the high-reliability versions of the 2N1482, 2N1486, and 2N1490, respectively, feature rugged construction, low saturation voltage, and high beta at high currents, and are designed to assure freedom from forward-bias second breakdown when operated with specified limits.

Typical applications for these transistors include: power-switching circuits such as dc-to-dc converters, inverters, choppers, solenoid- and relay-controls; oscillator, regulator, and pulse-amplifier circuits; Class A and Class B push-pull audio- and servo-amplifiers.

* Complete data for types 2N1482, 2N1486, 2N1490, 2N2102 and 2N3439 are given in separate technical bulletins (Files 135, 137, 139, 106, and 64, respectively). Bulletins are available upon request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.

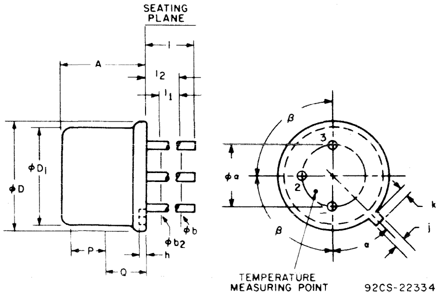
RELIABILITY TESTING

Each RCA-40366, 40367, 40368, 40369 and 40385 is subjected to the following preconditioning steps:

1. Temperature Cycling-Method 102A of MIL-STD-202, 5 cycles, –65° C to 200° C
2. Bake, 72 hours min., 200° C
3. Helium Leak, 1 x 10^{-8} cc/s max.
4. (a) Methanol Bomb, 70 psig, 16 hours min. (For 40366)
   (b) Bubble Test (Per MIL-STD-202, COND. A), 125° C min., 1 minute, ethylene glycol (For 40367, 40368, 40369 & 40385)
5. Serialization
6. (a) Record I_{CBO} and h_{FE} (150 mA) (For 40366)
   (b) Record I_{CBO} and h_{FE} (For 40367, 40368, & 40369)
   (c) Record I_{CEV} and h_{FE} (20 mA) (For 40385)
7. (a) Power Age, T_{FA} = 25° C, V_{CB} = 60 V, t= 168 hours, P_T = 1 W, free-air (For 40366 & 40367)
   (b) Power Age, T_C = 125° C, V_{CB} = 24 V, t= 168 hours, P_T = 10.5 W, with heat-sink (For 40368) P_T = 32 W, with heat-sink (For 40369)
   (c) Power Age, T_{FA}= 25° C, V_{CB}= 200 V, t= 168 hours, P_T= 800 mW, free air (For 40385)
8. (a) For 40366, †record I_{CBO}, h_{FE}(150 mA), BV_{CBV}, $V_{CEO}(sus)$, BV_{EBO}, $V_{CE}(sat)$. Data furnished with transistor.
   (b) For 40367, 40368, & 40369, †record I_{CBO}, h_{FE}, BV_{CEV}, $V_{CEO}(sus)$, I_{EBO}, $V_{CE}(sat)$. Data furnished with transistors.
   (c) For 40385, †record I_{CEO}, I_{EBO}, $V_{CEO}(sus)$, I_{CEV}, $V_{CE}(sat)$, and h_{FE}(20 mA). Data furnished with transistor.

† **Delta criteria after 168 hours Power Age:**
$\Delta h_{FE} \pm 25\%$ (For all types) ΔI_{CBO} + 1 μA (For 40367, 40368, & 40369)

DIMENSIONAL OUTLINE FOR 40366, 40367, AND 40385



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
ϕa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
ϕb	0.016	0.021	0.406	0.533	2
ϕb_2	0.016	0.019	0.406	0.483	2
ϕD	0.350	0.370	8.89	9.40	
ϕD_1	0.305	0.335	8.00	8.51	
h	0.009	0.041	0.229	1.04	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
L {long lead	1.500		38.10		2
L {short lead	0.500		12.70		2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and l. Diameter is uncontrolled in l_1.

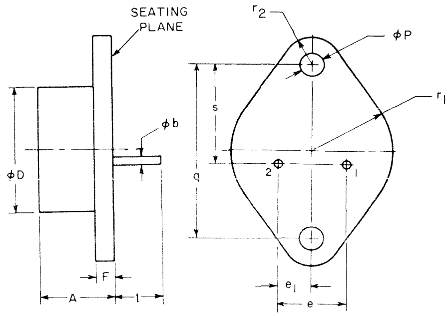
Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

TERMINAL CONNECTIONS

Pin 1 — Emitter
Pin 2 — Base
Case, Pin 3 — Collector

DIMENSIONAL OUTLINE FOR 40369 JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
ϕb	0.038	0.043	0.97	1.09	2
ϕD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e_1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
l	0.312		7.92		2
ϕP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r_1		0.525		13.34	
r_2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

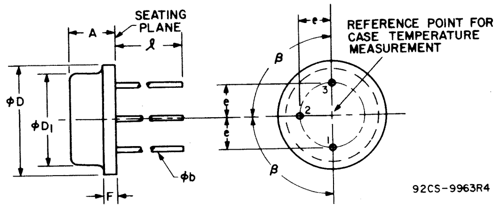
1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS–15222

TERMINAL CONNECTIONS

Pin 1 — Base
Pin 2 — Emitter
Case — Collector
Mounting Flange — Collector

DIMENSIONAL OUTLINE FOR 40368
JEDEC TO-8



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.270	0.330	6.86	8.38	–
φb	0.027	0.033	0.686	0.838	1
φD	0.550	0.650	13.97	16.51	–
φD1	0.444	0.524	11.28	13.31	–
e	0.136	0.146	3.45	3.71	–
F	–	0.115	–	2.92	–
ℓ	0.360	0.440	9.14	11.18	1
β	90° NOMINAL				

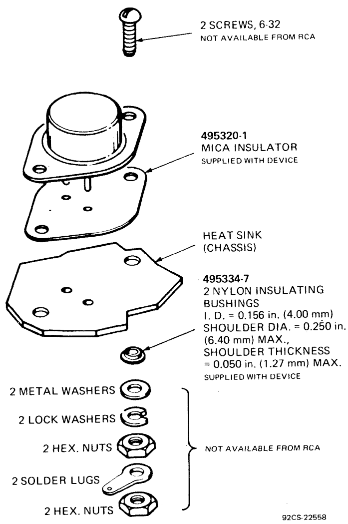
TERMINAL CONNECTIONS

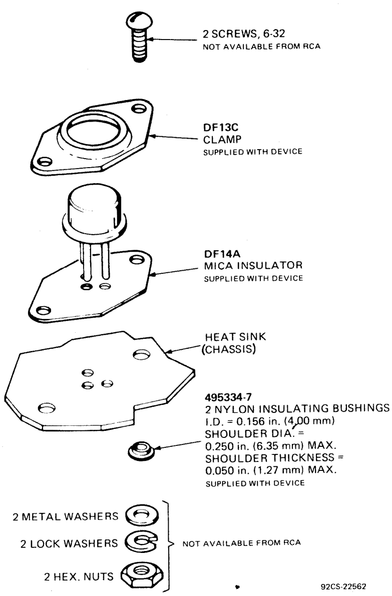
Lead 1 – Emitter
Lead 2 – Base
Case, Lead 3 – Collector

NOTE:

1. Three leads.

When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.





In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.1 – Suggested mounting hardware for use with JEDEC TO-3 package

Fig.2 – Suggested mounting hardware for use with JEDEC TO-8 package

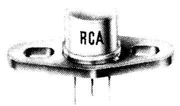
High-Speed Switching Power Transistors

RCA

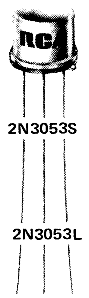
Solid State Division

Power Transistors

2N3053 40389 40392



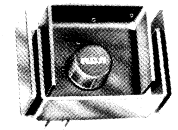
40392 H-1375



2N3053S

2N3053L

H-1380



40389 H-1468

General-Purpose, Medium-Power Silicon N-P-N Planar Transistors

For Small-Signal Applications
In Industrial and Commercial Equipment

Features:

- **Maximum safe-area-of-operation curve**
- **Forward- and reverse-bias operation without second breakdown**
- **Low leakage current**

These devices are generally available with ½-inch leads (TO-39 package). They are also available in the U.S.A., Canada, Latin America, and Far East with 1½-inch leads (TO-5 package); the shorter-lead versions are specified by a suffix letter "S" after the type number, and the longer-lead versions by a suffix letter "L".

RCA-2N3053 is a silicon n-p-n planar transistor useful up to 20 MHz in small-signal, medium-power applications. Type 40389 is a 2N3053 with a factory-attached diamond-shaped mounting flange.

Applications:

- **Audio amplifiers**
- **Controlled amplifiers**
- **Power supplies**
- **Power oscillators**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N3053	40389 40392	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	60	60	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:				
With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{CER}(sus)$	50	50	V
With base open	$V_{CEO}(sus)$	40	40	V
With base-emitter-junction reverse-biased	$V_{CEV}(sus)$	60	60	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	5	V
COLLECTOR CURRENT	I_C	0.7	0.7	A
TRANSISTOR DISSIPATION:	P_T			
At case temperatures up to 25°C		5	7 (40392)	W
At free-air temperatures up to 25°C		1	3.5 (40389)	W
At temperatures above 25°C		See Figs.1, 2, and 3		
TEMPERATURE RANGE:				
Storage and operating (Junction)		← −65 to +200 →		°C
LEAD TEMPERATURE (During soldering):				
At distance ≥ 1/32 in. (0.8 mm) from seating plane for 10 s max.		← 235 →		°C

ELECTRICAL CHARACTERISTICS, *at Case Temperature (T_C) = 25°C unless otherwise specified*

Characteristics	Symbol	TEST CONDITIONS							LIMITS		Units
		DC Collector Voltage V		DC Emitter or Base Voltage V		DC Current mA			Types 2N3053 40389 40392		
		V_{CB}	V_{CE}	V_{EB}	V_{BE}	I_C	I_E	I_B	Min.	Max.	
Collector-Cutoff Current	I_{CBO}	30					0		—	0.25	μA
Emitter-Cutoff Current	I_{EBO}			4		0			—	0.25	μA
DC Forward-Current Transfer Ratio	h_{FE}		10			150[a]			50	250	
Collector-to-Base Breakdown Voltage	BV_{CBO}					0.1	0		60	—	V
Emitter-to-Base Breakdown Voltage	BV_{EBO}					0	0.1		5	—	V
Collector-to-Emitter Sustaining Voltage: With base open	$V_{CEO}(sus)$					100[a]		0	40	—	V
With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{CER}(sus)$					100[a]			50	—	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$					150		15	—	1.7	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					150		15	—	1.4	V
Small-Signal, Forward Current Transfer Ratio (At 20 MHz)	h_{fe}		10			50			5	—	
Output Capacitance	C_{ob}	10					0		—	15	pF
Input Capacitance	C_{ib}			0.5		0			—	80	pF
Thermal Resistance: Junction-to-Case	θ_{J-C}								35(max.) 2N3053		°C/W
									25(max.) 40392		°C/W
Junction-to-Free Air	θ_{J-FA}								175(max.) 2N3053		°C/W
									50(max.) 40389		°C/W

[a]Pulsed; pulse duration = 300μs, duty factor = 1.8%.

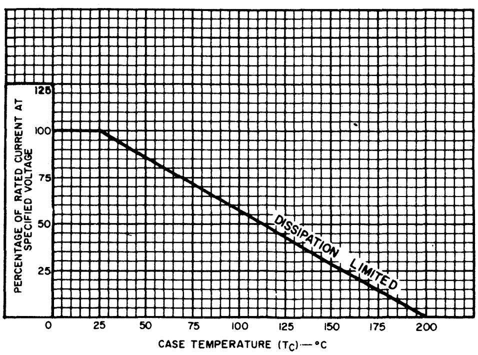


Fig.1 — Derating curve for type 2N3053. 92LS-1469

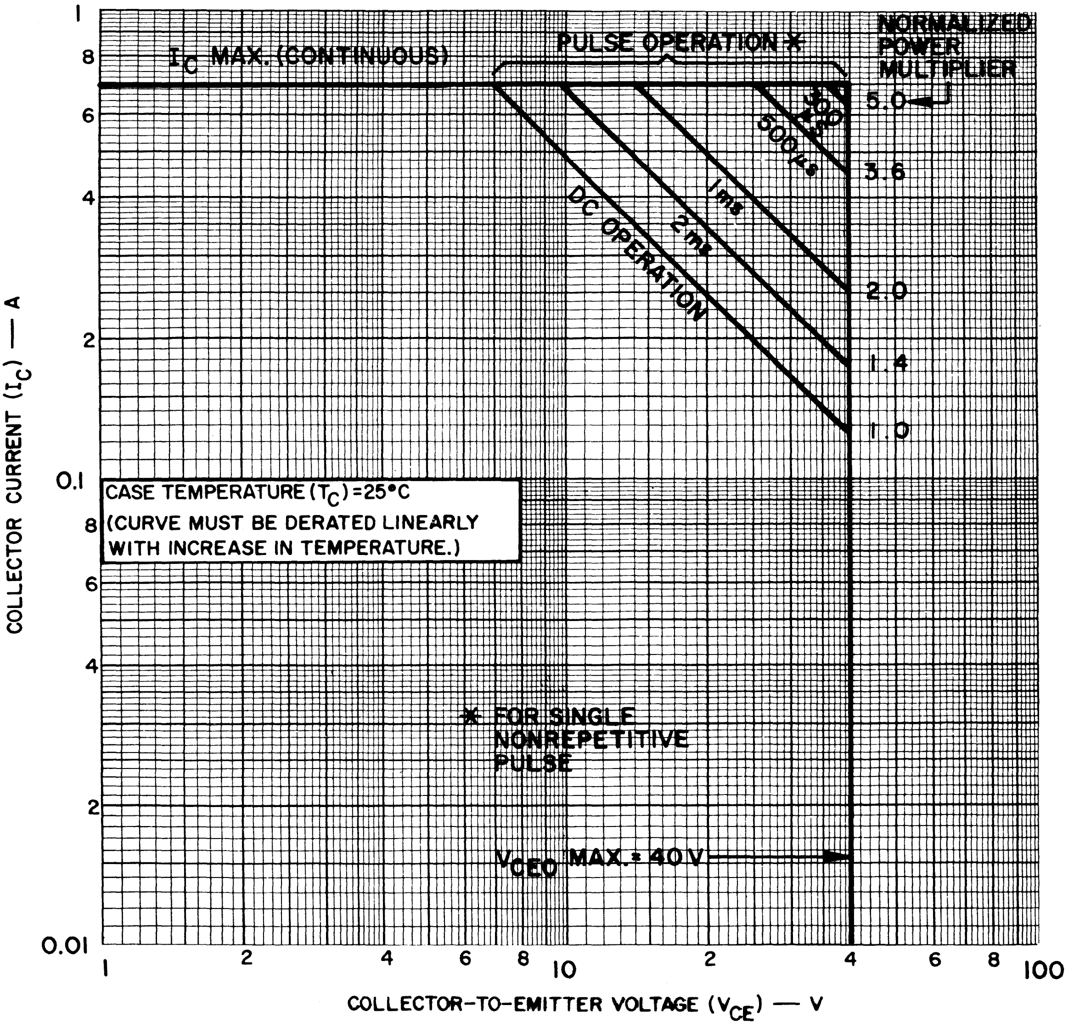


Fig.2 – Maximum operating areas for type 2N3053.

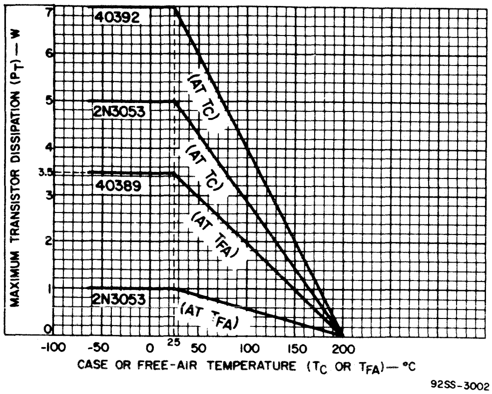


Fig. 3 - Dissipation derating curves for all types.

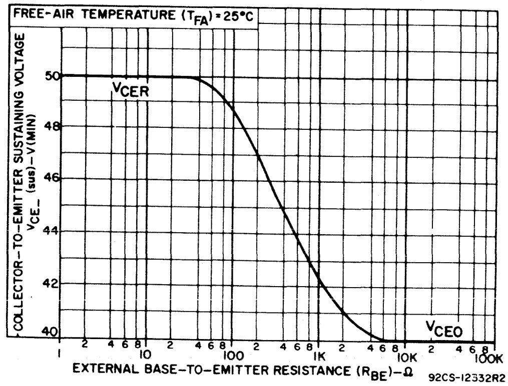


Fig. 4 - Sustaining voltage vs. base-to-emitter resistance for all types.

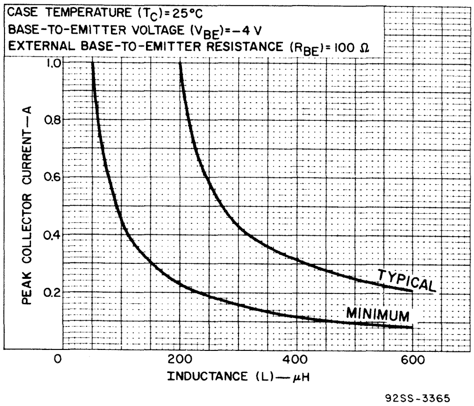


Fig. 5 - Reverse-bias, second-breakdown characteristics for all types.

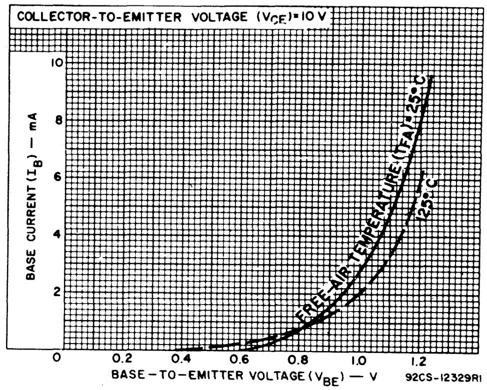


Fig. 6 - Typical dc-beta characteristics for all types.

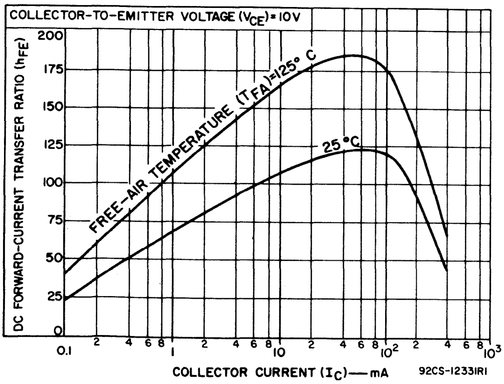


Fig. 7 - Typical input characteristics for all types.

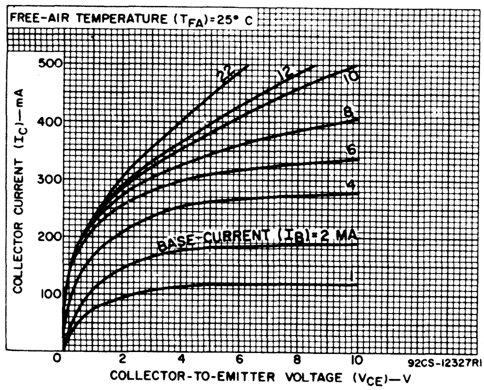


Fig. 8 - Typical output characteristics for all types.

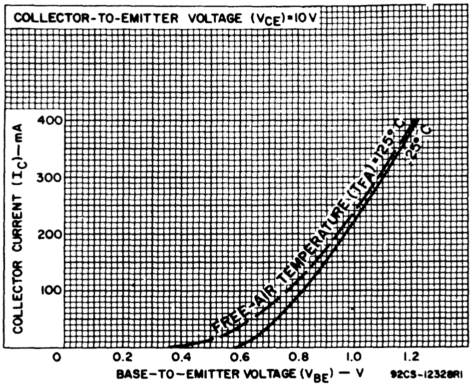


Fig. 9 - Typical transfer characteristics for all types.

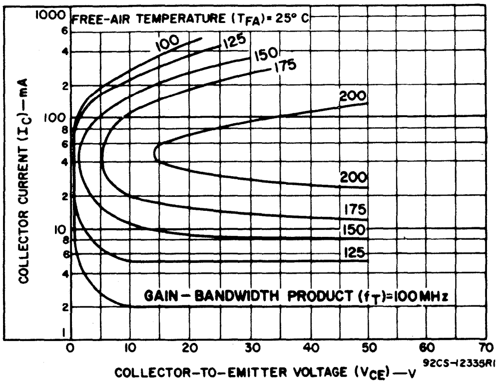


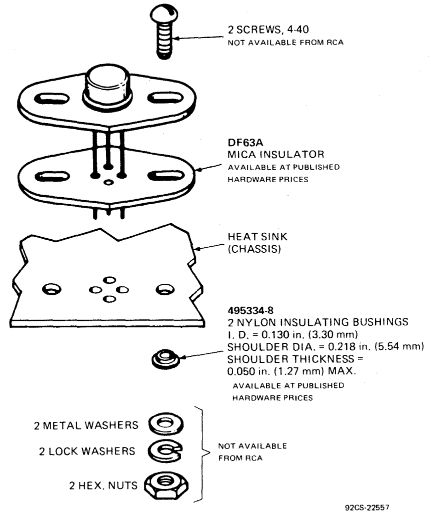
Fig. 10 - Typical variation of gain-bandwidth product with I_C and V_{CE} for all types.

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	0.328	–	8.33	
B	0.240	0.260	6.10	6.60	
B_1	0.009	0.125	0.229	3.18	
ϕ_b	0.016	0.019	0.406	0.483	
D	0.335	0.370	8.51	9.40	
D_1	0.305	0.335	7.75	8.51	
E	0.495	0.505	12.57	12.83	
e	0.200 T.P.		5.08 T.P.		1
e_1	0.100 T.P.		2.54 T.P.		1
F	0.062	0.068	1.57	1.74	
G	0.995	1.005	25.27	25.53	
i	0.028	0.034	0.711	0.864	
k	0.029	0.045	0.737	1.14	
L {long lead	1.430		36.32	–	
L {short lead	0.430	–	10.92	–	
Q	0.685	0.691	17.40	17.55	
Q_1	0.559	0.565	14.20	14.35	
Q_2	0.128	0.132	3.25	3.35	
R	0.156 T.P.		3.96 T.P.		1
R_1	0.064	0.066	1.63	1.67	
α	45° T.P.				1, 2

NOTES:
1. True position.
2. Tab centerline.

TERMINAL CONNECTIONS

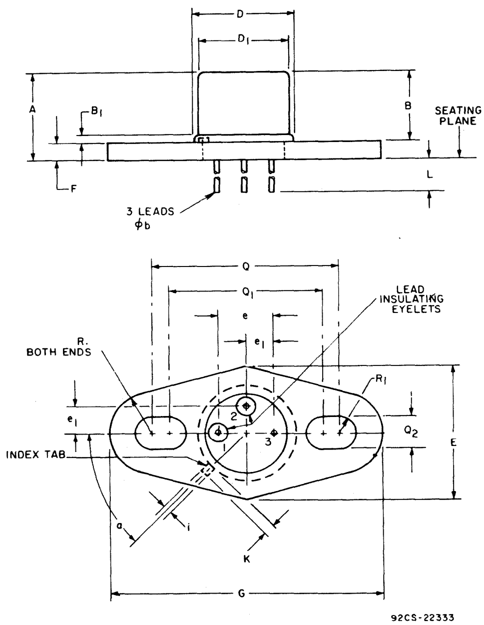
Lead 1 — Emitter
Lead 2 — Base
Flange, Lead 3 — Collector



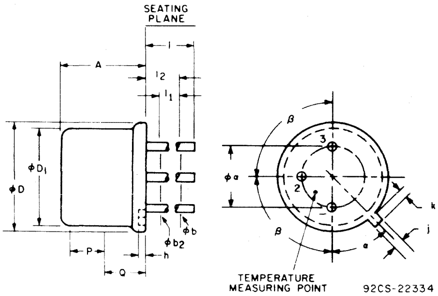
In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.11 — Suggested mounting hardware for type 40392.

DIMENSIONAL OUTLINE FOR 40392



DIMENSIONAL OUTLINE FOR 2N3053



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
φa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
φb	0.016	0.021	0.406	0.533	2
$φb_2$	0.016	0.019	0.406	0.483	2
φD	0.350	0.370	8.89	9.40	
$φD_1$	0.305	0.335	8.00	8.51	
h	0.009	0.041	0.229	1.04	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
L {long lead	1.500		38.10		2
L {short lead	0.500		12.70		2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

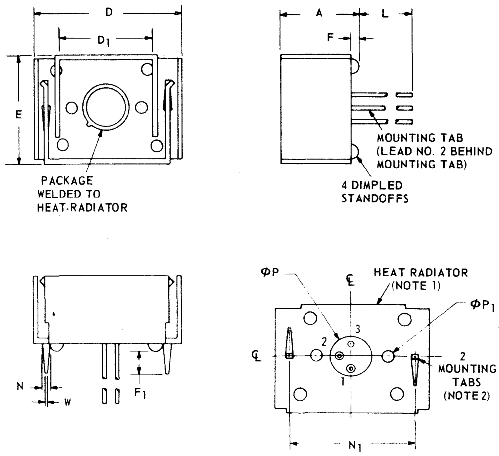
Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads) $φb_2$ applies between l_1 and l_2. φb applies between l_2 and l. Diameter is uncontrolled in l_1.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

DIMENSIONAL OUTLINE FOR 40389



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	0.630	–	16.00	
D	1.205	1.235	30.61	31.37	
D_1	0.775	0.785	19.69	19.93	
E	0.875	0.905	22.22	22.99	
F	0.040	0.055	1.02	1.40	
F_1	0.160	0.195	4.06	4.95	
L {long lead	1.410	–	35.81	–	
L {short lead	0.410	–	10.41	–	
φP	0.295	0.305	7.493	7.747	
$φP_1$	0.093	0.095	2.362	2.413	
N	0.048	0.062	1.21	1.57	
N_1	0.998	1.002	25.349	25.450	3
W	0.048	0.052	1.219	1.320	

NOTES:

1. **0.035 C.R.S., finish—electroless nickel plate.**
2. **Recommended hole size for printed-circuit board is 0.070 in. (1.78 mm) dia.**
3. **Measured at bottom of heat-radiator.** 92CS-22335

TERMINAL CONNECTIONS

Lead 1 – Emitter
Lead 2 – Base
Case, Lead 3 – Collector

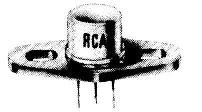
TERMINAL CONNECTIONS

Lead 1 – Emitter
Lead 2 – Base
Heat Radiator, Lead 3 – Collector

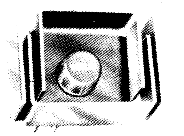
RCA Solid State Division

Power Transistors

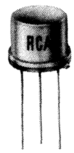
2N4036 2N4037 2N4314 40391 40394



40394 H-1375



40391 H-1468



2N4036 2N4037 2N4314

JEDEC TO-39

H-1381

Medium-Power Silicon P-N-P Planar Transistors

General-Purpose Types for Industrial and Commercial Applications

Features:

- 2N4036, 2N4037 are p-n-p complements of 2N2102[▲▲], 2N3053
- Gain-bandwidth product (f_T) = 60 MHz min
- High breakdown voltages
- Maximum-area-of-operation curves
- Planar construction provides low noise and low leakage
- Low saturation voltages
- High pulsed beta at high collector current
- Fast switching (2N4036)

These devices are generally available with ½-inch leads (TO-39 package). They are also available in the U.S.A., Canada, Latin America, and Far East with 1½-inch leads (TO-5 package); the shorter-lead versions are specified by a suffix letter "S" after the type number, and the longer-lead versions by a suffix letter "L".

The 2N4036, 2N4037, 2N4314[▲], 40391, and 40394 are double-diffused, epitaxial-planar, silicon p-n-p transistors; they differ in breakdown-voltage ratings, leakage-current, and saturation characteristics. The 40391 is a 2N4037 with a factory-attached heat radiator, intended for printed-circuit-board applications. Type 40394 is a 2N4037 with a factory-attached diamond-shaped mounting flange.

These transistors are intended for a wide variety of small-signal medium-power applications. With a minimum gain-bandwidth product (f_T) of 60 MHz, these devices provide useful gain at high frequencies. In addition, the 2N4036 is useful in high-speed saturated switching applications.

▲ Formerly Dev. Nos. TA2651, TA2670, and TA2670A, respectively.

▲▲ 2N2102 is a linear-beta type; the 2N3053 is a general-purpose type. For technical bulletins for these types, write to RCA Solid State Division, Box 3200, Somerville, N. J. 08876.

MAXIMUM RATINGS, *Absolute Maximum Values:*

		2N4036	2N4037 40391, 40394	2N4314	
* COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	−90	−60	−90	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:					
With 1.5 volts (V_{BE}) of reverse bias	$V_{CEV}(sus)$	−85	−60	−85	V
With external base-to-emitter resistance (R_{BE}) ≤200 Ω	$V_{CER}(sus)$	−85	−60	−85	V
* With base open	$V_{CEO}(sus)$	−65	−40	−65	V
* EMITTER-TO-BASE VOLTAGE	V_{EBO}	−7	−7	−7	V
* COLLECTOR CURRENT	I_C	−1.0	−1.0	−1.0	A
* BASE CURRENT	I_B	−0.5	−0.5	−0.5	A
* TRANSISTOR DISSIPATION:	P_T				
At case temperatures up to 25°C		7	7(2N4037)	7	W
		−	7(40394)	−	W
At free-air temperatures up to 25°C		1	3.5(40391)	1	W
		−	1(2N4037, 40394)	−	W
At temperatures above 25°C		←	See Figs. 6 and 7	→	
For pulsed operation		←	See Fig. 1	→	
* TEMPERATURE RANGE:					
Storage & Operating (Junction)		←	−65 to 200	→	°C
* LEAD TEMPERATURE (During soldering):					
At distance ≥ 1/16 in. (1.58 mm) from seating plane for 10 s max.		←	230	→	°C

* In accordance with JEDEC registration data format (JS-6 RDF-1 2N4036; JS-9 RDF-2 2N4037, 2N4314).

ELECTRICAL CHARACTERISTICS, *at Case Temperature (T_C) = 25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS VOLTAGE V dc				TEST CONDITIONS CURRENT mA dc			LIMITS 2N4036		LIMITS 2N4037 40391 40394		LIMITS 2N4314		UNITS
		V_{CB}	V_{CE}	V_{EB}	V_{BE}	I_C	I_E	I_B	Min.	Max.	Min.	Max.	Min.	Max.	
Collector Cutoff Current: With emitter open	I_{CBO}	– 90					0		–	– 0.1*	–	–	–	–	mA
		– 60					0		–	– 0.02	–	– 0.25*	–	– 0.25*	μA
With base open	I_{CEO}		– 30					0	–	– 0.5*	–	– 5*	–	– 5*	μA
With base-emitter junction reverse biased	I_{CEX}		– 85		1.5				–	– 100*	–	–	–	–	mA
T_C = 150°C			– 30		1.5				–	– 0.1*	–	–	–	–	
*Emitter Cutoff Current	I_{EBO}			– 7		0			–	– 0.1*	–	–	–	–	mA
				– 5		0			–	– 0.02	–	– 1*	–	– 1*	μA
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$					– 0.1	0		– 90	–	– 60*	–	– 90*	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$					0	– 0.1		– 7	–	– 7	–	– 7	–	V
Collector-to-Emitter Sustaining Voltage: *(See Figs. 2 and 3)* With base-emitter junction reverse biased	$V_{CEV}(sus)$	•			1.5	– 100			– 85[a]	–	– 60[a]	–	– 85[a]	–	V
With external base-to-emitter resistance (R_{BE}) ≤ 200 Ω	$V_{CER}(sus)$					– 100			– 85[a]	–	– 60[a]	–	– 85[a]	–	V
* With base open	$V_{CEO}(sus)$					– 100		0	– 65[a]	–	– 40[a]	–	– 65[a]	–	V
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					– 150		– 15	–	– 0.65	–	– 1.4	–	– 1.4	V
Base-to-Emitter Voltage	V_{BE}		– 10			– 150			–	– 1.1	–	– 1.5*	–	– 1.5*	V
* Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$					– 150		– 15	–	– 1.4	–	–	–	–	V
* DC Forward-Current Transfer Ratio	h_{FE}		– 2			– 150			20	200	–	–	–	–	
			– 10			– 0.1			20	–	–	–	–	–	
			– 10			– 1.0			–	–	15	–	15	–	
			– 10			– 150[b]			40	140	50	250	50	250	
			– 10			– 500[b]			20	–	–	–	–	–	
Common-Emitter, Small-Signal, Short-Circuit, Forward-Current Transfer Ratio (at f = 20 MHz)	h_{fe}		– 10			– 50			3.0	–	3.0	–	3.0	–	
* Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward-Current Transfer Ratio (at f = 20 MHz)	$\|h_{fe}\|$		10			– 50			3.0	–	3.0	10	3.0	10	
Collector-Base Capacitance (at f = 1 MHz)	C_{cb}	– 10					0		–	30	–	30*	–	30*	pF
Input Capacitance	C_{ib}			– 0.5		0			–	90	–	90	–	90	pF
* Sat. Switching Time: *(See Figs. 10 and 11)* Rise time	t_r		– 30			– 150		– 15	–	70	–	–	–	–	ns
Storage time	t_s		– 30			– 150		– 15	–	600	–	–	–	–	ns
Fall time	t_f		– 30			– 150		– 15	–	100	–	–	–	–	ns
Turn-on time	t_{on}		– 30			– 150		– 15	–	110	–	–	–	–	ns
Turn-off time	t_{off}		– 30			– 150		– 15	–	700	–	–	–	–	ns
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$								–	25*	25 (max.) 2N4037 & 40394		–	25	°C/W
									–	–			–	–	
Junction-to-Ambient	$R_{\theta JA}$								–	165	165 (max.) 2N4037 & 40394		–	165	°C/W
									–	–	50 (max.) 40391		–	–	°C/W

[a] CAUTION: The sustaining voltages $V_{CEO}(sus)$, $V_{CER}(sus)$, and $V_{CEV}(sus)$ MUST NOT be measured on a curve tracer. These sustaining voltages should be measured by means of the test circuit shown in Fig. 2.

[b] Pulsed; pulse duration = 300 μs, duty factor < 2%.

* In accordance with JEDEC registration data format (JS-6 RDF-1 2N4036; JS-9 RDF-2 2N4037, 2N4314).

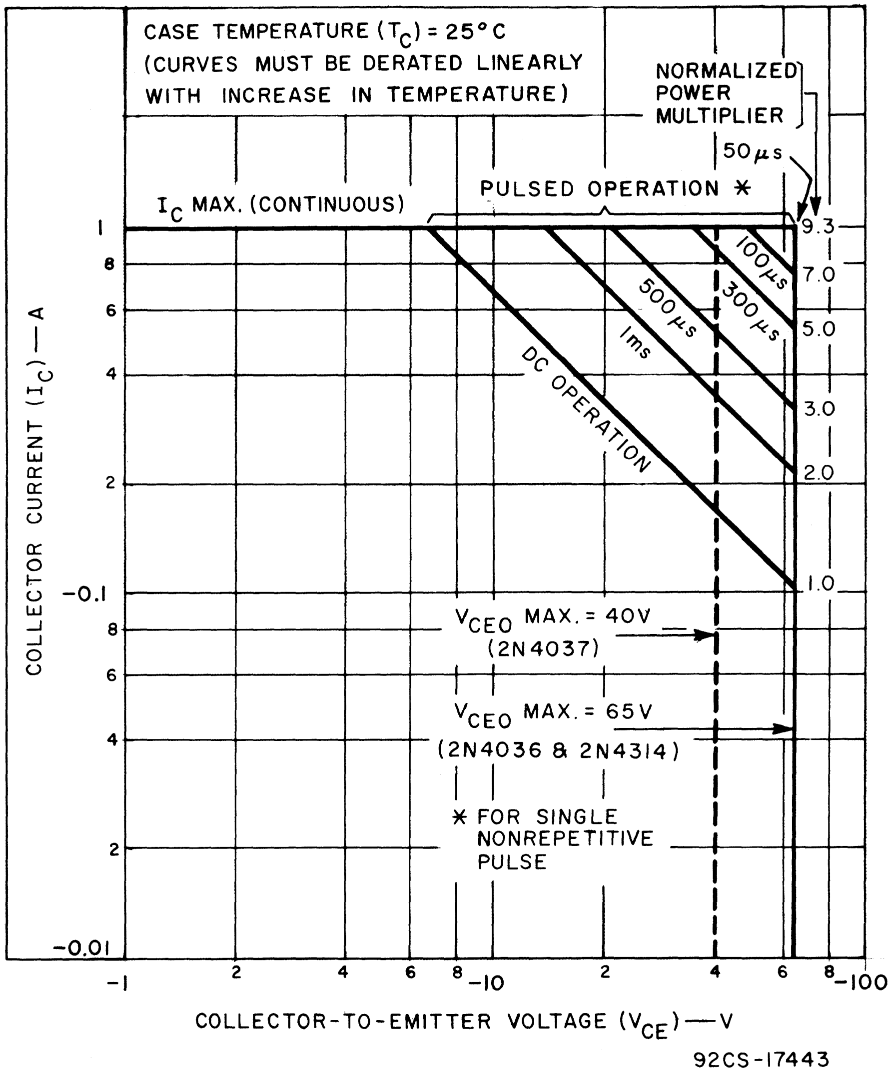


Fig.1 – Maximum operating areas for types 2N4036, 2N4037, and 2N4314.

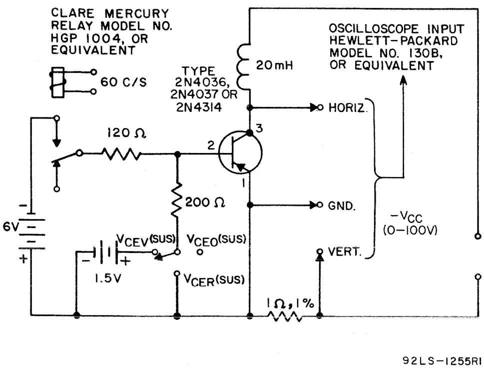
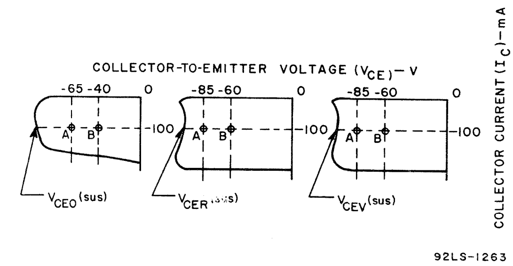


Fig.2 – Circuit used to measure sustaining voltages $V_{CEO}(sus)$, $V_{CER}(sus)$, and $V_{CEV}(sus)$ for all types.



NOTE: The sustaining voltages $V_{CEO}(sus)$, $V_{CER}(sus)$, and $V_{CEV}(sus)$ are acceptable when the traces fall to the left and below point "A" for type 2N4036 and 2N4314, and point "B" for type 2N4037.

Fig.3 – Oscilloscope display for measurement of sustaining voltages (test circuit shown in Fig.2).

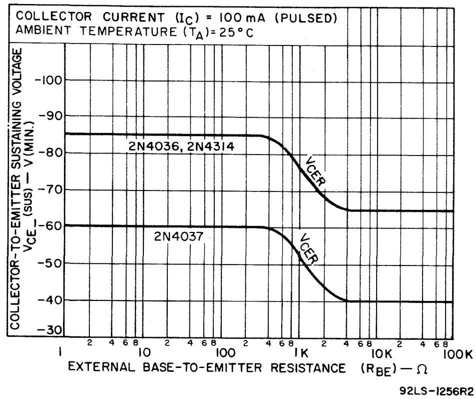


Fig.4 – Sustaining voltage vs. base-to-emitter resistance for all types.

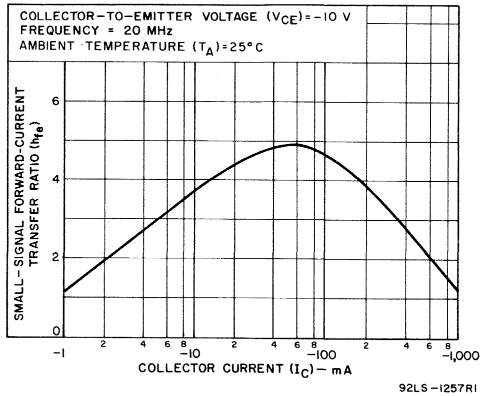


Fig.5 – Typical small-signal beta characteristic for all types.

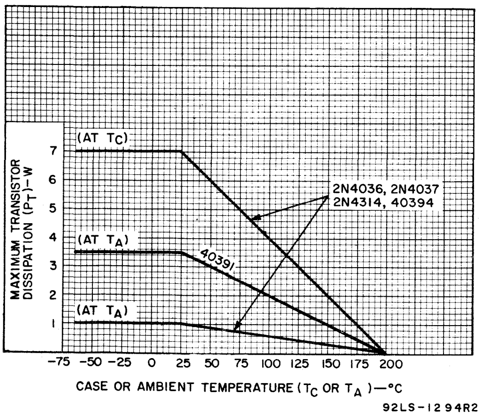


Fig.6 – Dissipation derating curve for all types.

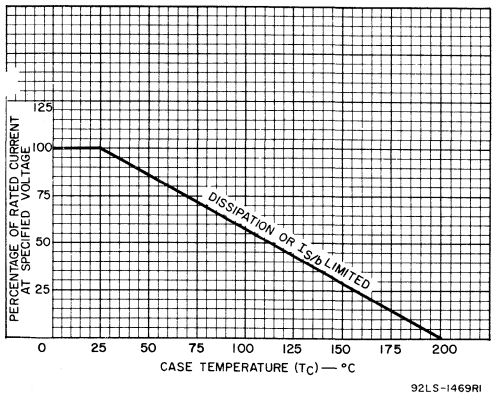


Fig.7 – Dissipation derating curve for types 2N4036, 2N4037, and 2N4314.

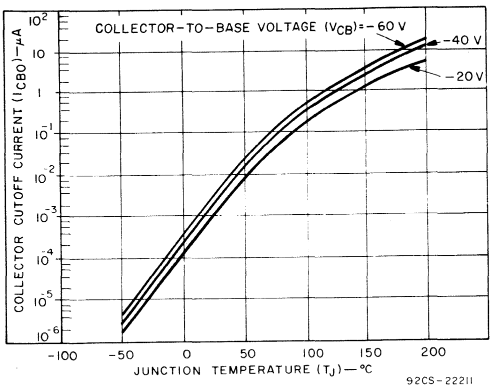


Fig.8 — Typical collector-cutoff current vs. junction temperature for type 2N4036.

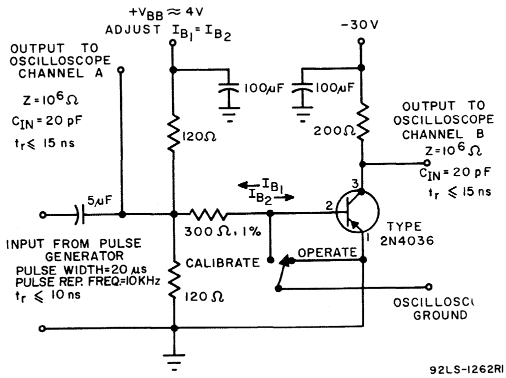


Fig.9 — Circuit used to measure switching times for type 2N4036.

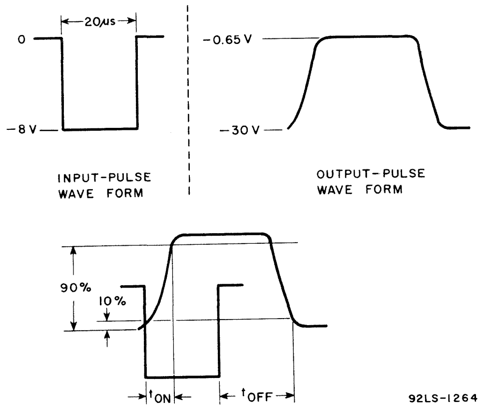


Fig.10 — Oscilloscope display for measurement of switching times test circuit shown in Fig.9).

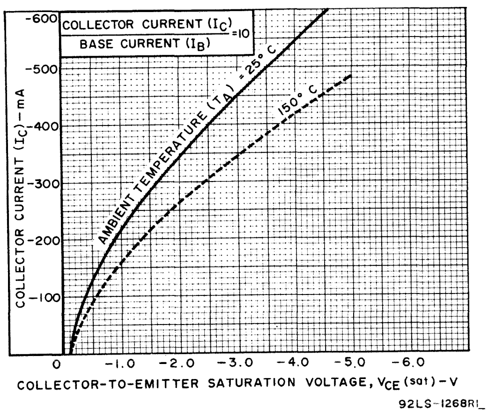


Fig.11 — Typical saturation-voltage characteristics for type 2N4036.

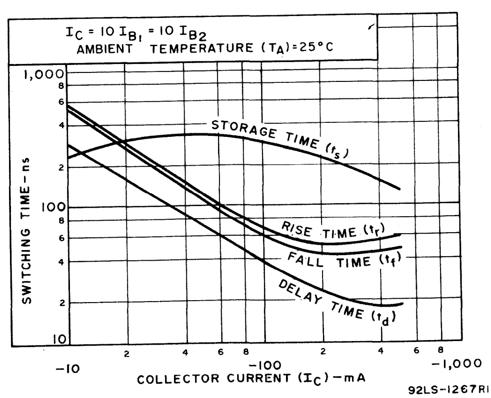


Fig.12 — Typical saturated switching times for type 2N4036.

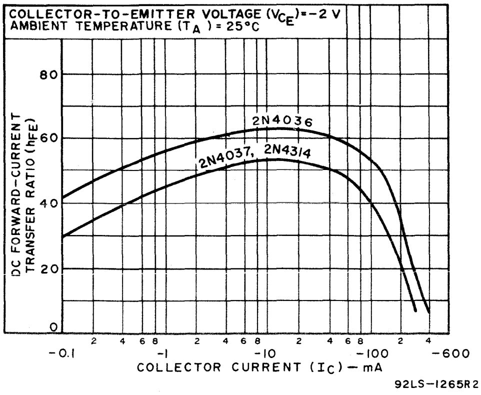


Fig. 13 — Typical dc beta characteristics for all types.

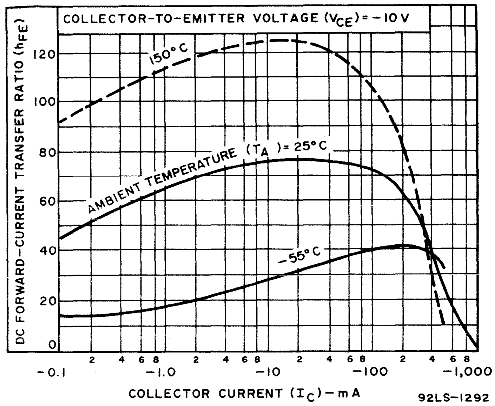


Fig. 14 — Typical dc beta characteristics for types 2N4037 and 2N4314.

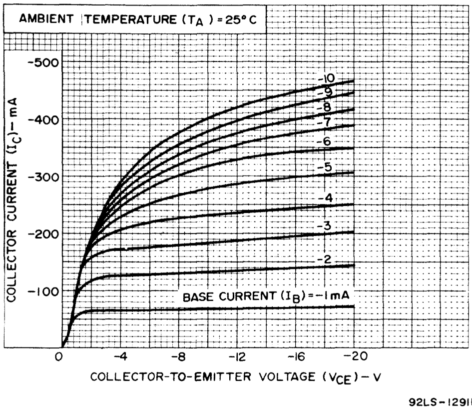


Fig. 15 — Typical output characteristics for types 2N4037 and 2N4314.

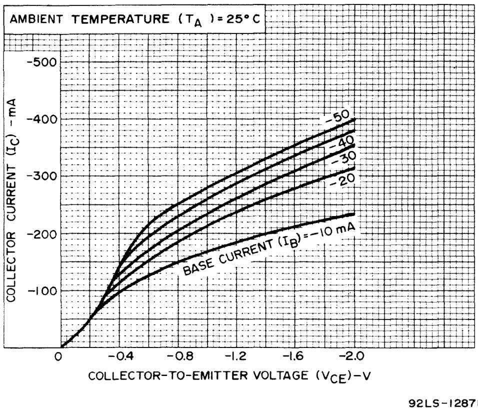


Fig. 16 — Typical output characteristics for types 2N4037 and 2N4314.

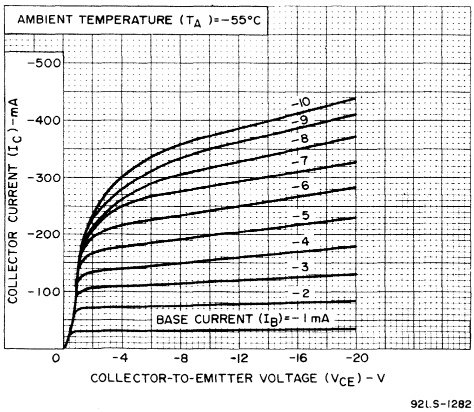


Fig. 17 — Typical output characteristics for types 2N4037 and 2N4314.

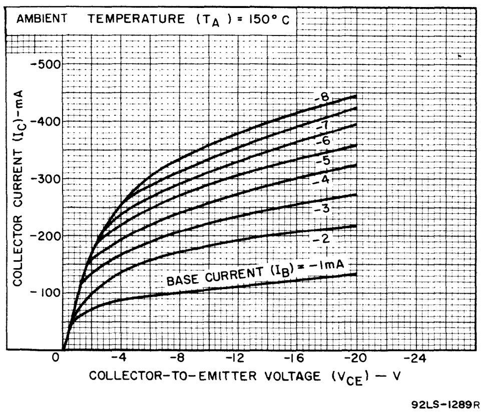


Fig. 18 — Typical output characteristics for types 2N4037 and 2N4314.

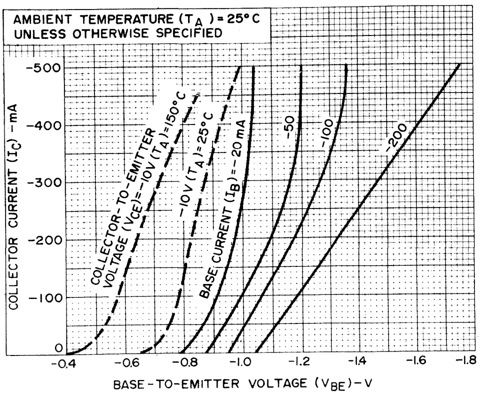
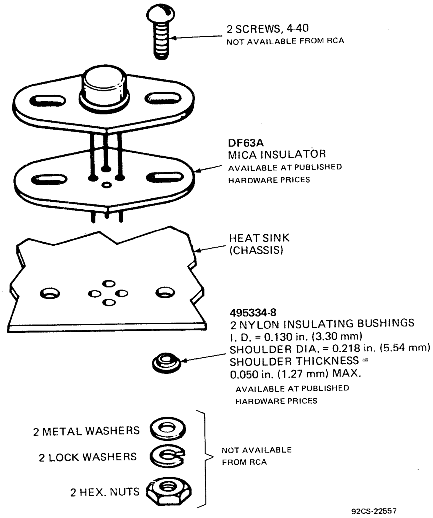


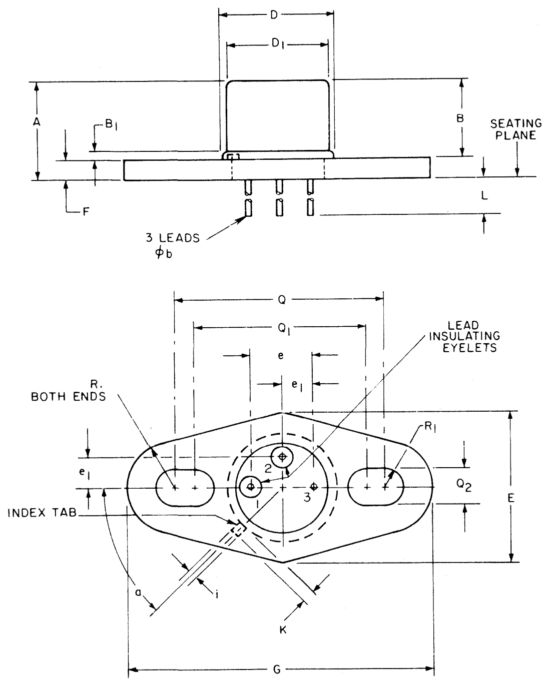
Fig.19 – Typical transfer characteristics for types 2N4037 and 2N4314.



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.20 – Suggested mounting hardware for type 40394.

DIMENSIONAL OUTLINE FOR 40394



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	–	0.328	–	8.33	
B	0.240	0.260	6.10	6.60	
B_1	0.009	0.125	0.229	3.18	
ϕb	0.016	0.019	0.406	0.483	
D	0.335	0.370	8.51	9.40	
D_1	0.305	0.335	7.75	8.51	
E	0.495	0.505	12.57	12.83	
e	0.200 T.P.		5.08 T.P.		1
e_1	0.100 T.P.		2.54 T.P.		1
F	0.062	0.068	1.57	1.74	
G	0.995	1.005	25.27	25.53	
i	0.028	0.034	0.711	0.864	
k	0.029	0.045	0.737	1.14	
L	0.430	–	10.92	–	
Q	0.685	0.691	17.40	17.55	
Q_1	0.559	0.565	14.20	14.35	
Q_2	0.128	0.132	3.25	3.35	
R	0.156 T.P.		3.96 T.P.		1
R_1	0.064	0.066	1.63	1.67	
α	45° T.P.				1, 2

NOTES:

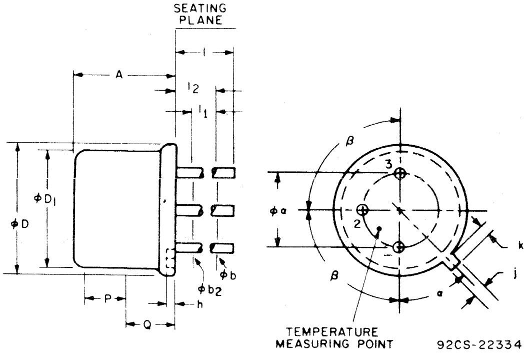
1. True position.
2. Tab centerline.

92CS-22331

TERMINAL CONNECTIONS

Lead 1 – Emitter
Lead 2 – Base
Flange, Lead 3 – Collector

DIMENSIONAL OUTLINE FOR 2N4036, 2N4037, 2N4314 JEDEC TO-39



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
ϕa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
ϕb	0.016	0.021	0.406	0.533	2
ϕb_2	0.016	0.019	0.406	0.483	2
ϕD	0.350	0.370	8.89	9.40	
ϕD_1	0.305	0.335	8.00	8.51	
h	0.009	0.041	0.229	1.04	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
L (long lead)	1.500		38.10		2
L (short lead)	0.500		12.70		2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

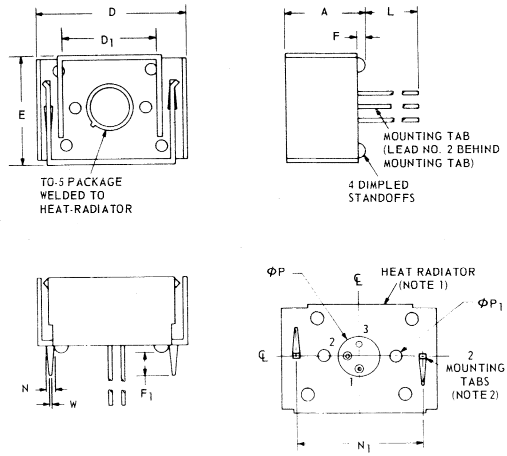
Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and l. Diameter is uncontrolled in l_1.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

DIMENSIONAL OUTLINE FOR 40391



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	–	0.630	–	16.00	
D	1.205	1.235	30.61	31.37	
D_1	0.775	0.785	19.69	19.93	
E	0.875	0.905	22.22	22.99	
F	0.040	0.055	1.02	1.40	
F_1	0.160	0.195	4.06	4.95	
L	0.410	–	10.41	–	
ϕP	0.295	0.305	7.493	7.747	
ϕP_1	0.093	0.095	2.362	2.413	
N	0.048	0.062	1.21	1.57	
N_1	0.998	1.002	25.349	25.450	3
W	0.048	0.052	1.219	1.320	

NOTES:

1. 0.035 C.R.S., finish—electroless nickel plate.
2. Recommended hole size for printed-circuit board is 0.070 dia.
3. Measured at bottom of heat-radiator

92CS-22332

TERMINAL CONNECTIONS

Lead 1 — Emitter
Lead 2 — Base
Case, Lead 3 — Collector

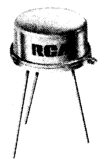
TERMINAL CONNECTIONS

Lead 1 — Emitter
Lead 2 — Base
Heat-Radiator, Lead 3 — Collector

RCA
Solid State
Division

Power Transistors

2N5189



"MODIFIED TO-39"

H-1546

High-Voltage Silicon N-P-N Switching Transistor

For Core-Driver and Line-Driver Service in Data-Processing Equipment and Other Critical Industrial and Military Applications

Features:

- **Excellent power handling capability**
- **High switching speeds at high currents**
- **High breakdown-voltage capabilities**
- **High reliability**

RCA-2N5189● is a double-diffused epitaxial planar transistor of the silicon n-p-n type featuring high breakdown voltages, low saturation voltages, and high switching speeds over a wide range of collector current.

It is especially useful in switching applications of high-performance computers and in other critical industrial applications where high-voltage and high-current-handling capabilities and short "turn-off" and "turn-on" times are important design features. These features also make the 2N5189 particularly useful in class C circuits for mobile and portable equipment.

The 2N5189 is hermetically sealed in a metal package like the JEDEC TO-39 but with a reduced height (0.180 in. max., 0.160 in. min.) and 0.5 in. min. leads.

●Formerly RCA Dev. No. TA7322.

MAXIMUM RATINGS, *Absolute Maximum Values:*

*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	60	V
COLLECTOR-TO-EMITTER VOLTAGE:			
* With base shorted to emitter	V_{CES}	55	V
With base open	V_{CEO}	35	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	V
*CONTINUOUS COLLECTOR CURRENT	I_C	2	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25°C		5	W
At case temperatures above 25°C, derate linearly		28.5	mW/°C
* At ambient temperatures up to 25°C		0.8	W
* At ambient temperatures above 25°C, derate linearly		4.57	mW/°C
*TEMPERATURE RANGE:			
Storage and operating (Junction)		−65 to +200	°C
*LEAD TEMPERATURE (During soldering):			
At distances ≥ 1/32 in. (0.8 mm) from seating plane for 10 s max.		265	°C

* In accordance with JEDEC registration data format JS-8/RDF-7.

ELECTRICAL CHARACTERISTICS, *At Ambient Temperature (T_A) = 25°C*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: VOLTAGE V dc			TEST CONDITIONS: CURRENT A dc			LIMITS 2N5189		UNITS
		V_{CB}	V_{CE}	V_{EB}	I_C	I_E	I_B	MIN.	MAX.	
*Collector Cutoff Current: With emitter open	I_{CBO}	60				0		–	100	μA
With emitter-base junction shorted	I_{CES}		55					–	100	μA
*Emitter Cutoff Current	I_{EBO}			5	0			–	10	μA
*Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$				0.01			35	–	V
*Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				1		0.1	–	1	V
*Base-to-Emitter Voltage	V_{BE}				1		0.1	–	1.5	V
*DC Forward Current Transfer Ratio	h_{FE}		1		1[a]			15	–	
Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 100 MHz)	h_{fe}		10		0.05			2.5	–	
Common-Base, Open-Circuit Output Capacitance (f = 1 MHz)	C_{ob}	10				0		–	15	pF
*Switching Time:					I_C	I_{B_1}	I_{B_2}			
Turn-on ($t_d + t_r$)	t_{on}				1	0.1	–	–	40	ns
Turn-off ($t_s + t_f$)	t_{off}				1	0.1	−0.1	–	70	ns

[a]Pulsed: Pulse duration ≤ 400 μs; duty factor ≤ 0.03.

*In accordance with JEDEC registration data format JS-8/RDF-7.

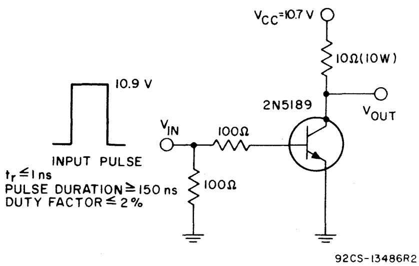


Fig. 1—Circuit used to measure turn-on time.

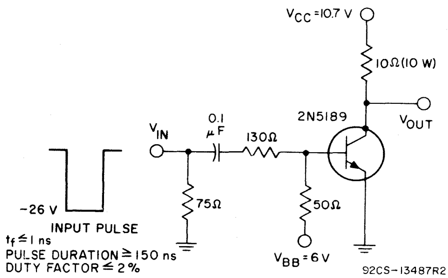


Fig. 2—Circuit used to measure turn-off time.

TYPICAL CHARACTERISTICS

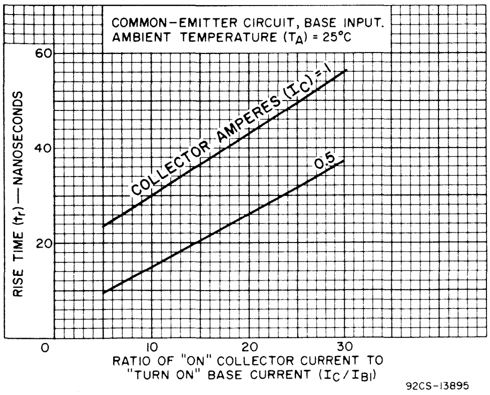


Fig. 3 – Rise Time vs I_C/I_{B1}

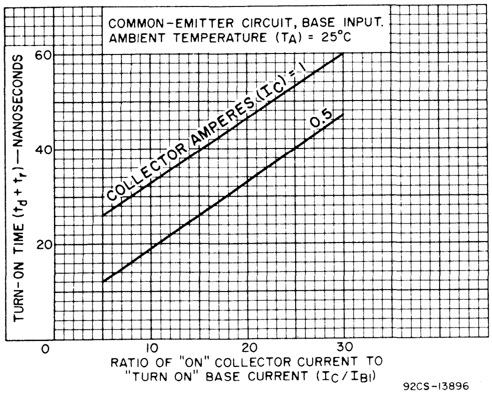


Fig. 4 – Turn-On Time vs I_C/I_{B1}

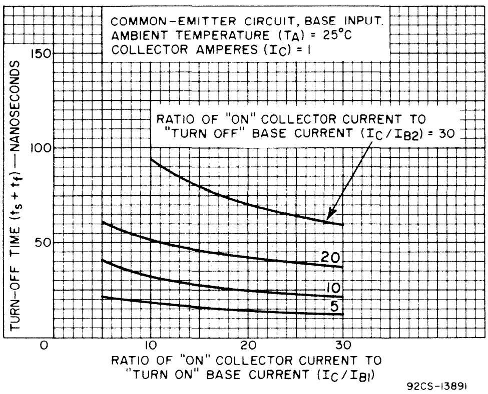


Fig. 5 – Turn-Off Time vs I_C/I_{B1}

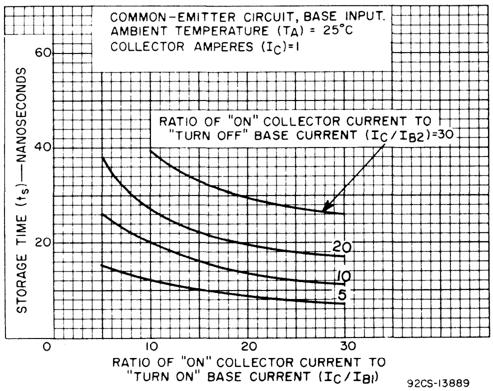


Fig. 6 – Storage Time vs I_C/I_{B1}

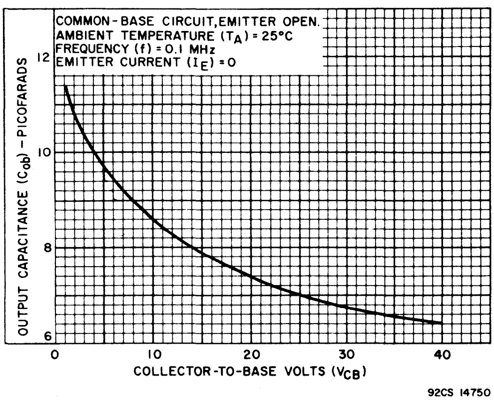


Fig. 7 – Output Capacitance vs Collector-to-Base Voltage

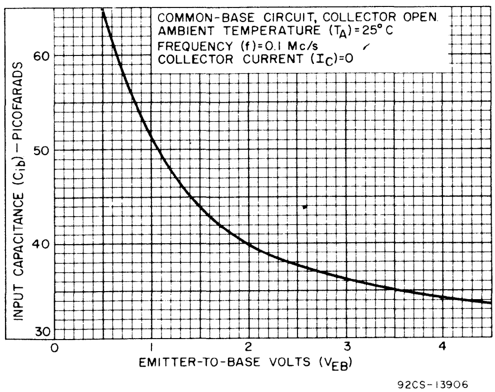


Fig. 8 – Input Capacitance vs Emitter-to-Base Voltage

TYPICAL CHARACTERISTICS

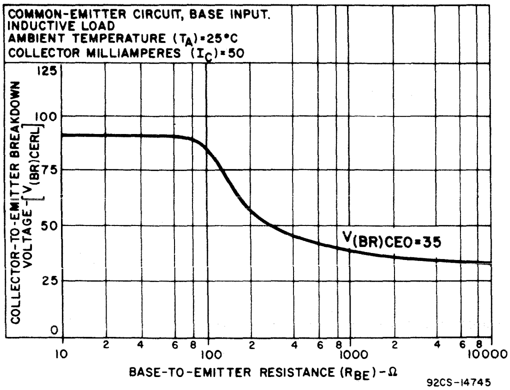


Fig. 9 – Collector-Cutoff Current vs Ambient Temperature

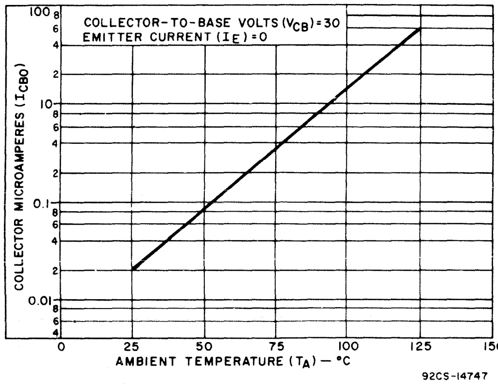


Fig. 10 – Collector-to-Emitter Breakdown Voltage vs Base-to-Emitter Resistance

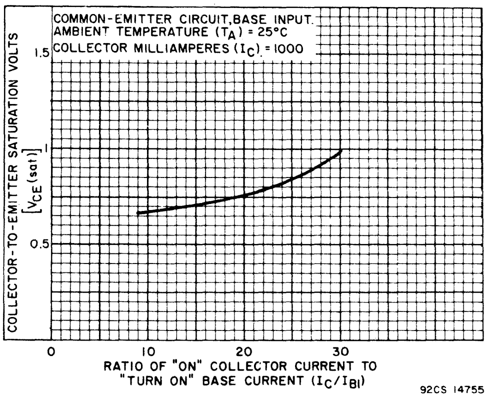


Fig. 11 – Collector-to-Emitter Saturation Voltage vs I_C/I_{B1}

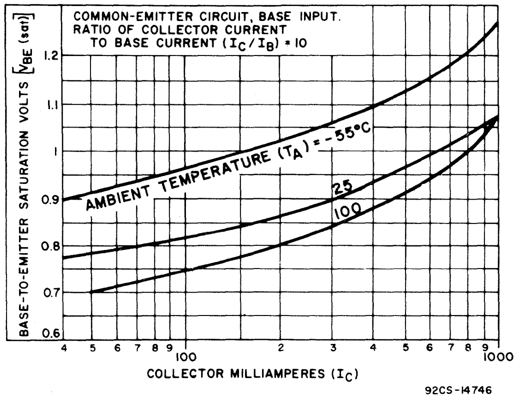


Fig. 12 – Base-to-Emitter Saturation Voltage vs I_C

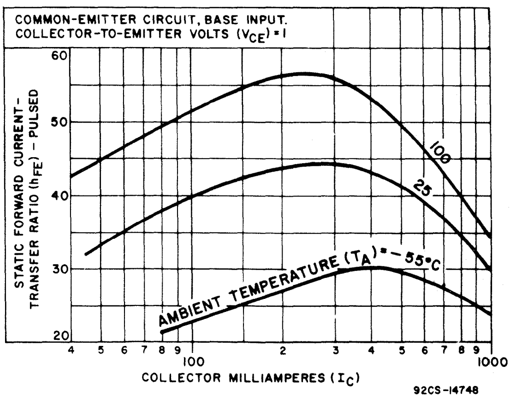


Fig. 13 – Static Forward Current-Transfer Ratio (Pulsed) vs I_C

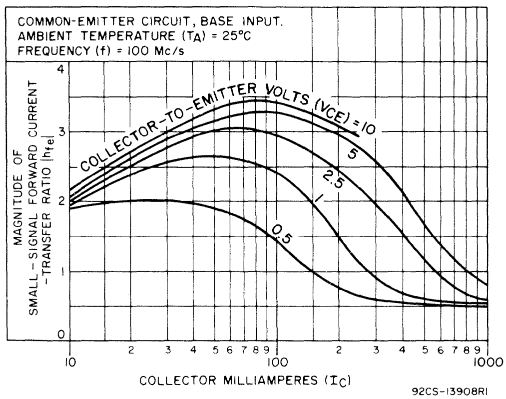
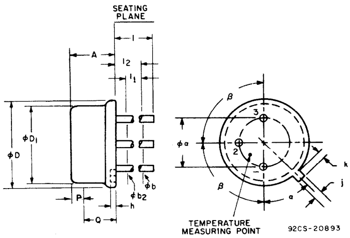


Fig. 14 – Small-Signal Forward Current-Transfer Ratio vs I_C

DIMENSIONAL OUTLINE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
φa	0.190	0.210	4.83	5.33	
A	0.160	0.180	4.07	4.57	
φb	0.016	0.021	0.406	0.533	2
$φb_2$	0.016	0.019	0.406	0.483	2
φD	0.350	0.370	8.89	9.40	
$φD_1$	0.315	0.335	8.00	8.51	
h	0.009	0.125	0.229	3.18	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
l	0.500		12.70		2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
P					1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads) $φb_2$ applies between l_1 and l_2. φb applies between l_2 and 0.5 in. (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond 0.5 in. (12.70 mm) from seating plane.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

TERMINAL CONNECTIONS

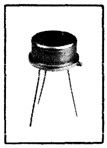
LEAD 1 – EMITTER
LEAD 2 – BASE
LEAD 3 – COLLECTOR, CASE

RCA Solid State Division

Power Transistors

2N5262

SILICON N-P-N HIGH-VOLTAGE ULTRA-HIGH-SPEED TRANSISTOR



For Memory Driver Service in Data-Processing Equipment and Other Critical Industrial Applications

RCA-2N5262* is a silicon n-p-n, epitaxial planar transistor with characteristics which make it exceptionally desirable for high-speed, high-voltage, high-current switching applications. In addition, the 2N5262 features very short turn-on and turn-off times and low saturation voltages. It is also controlled for freedom from second breakdown under both forward-bias and reverse-bias conditions, when operated within specified maximum ratings.

The 2N5262 meets the requirements of the basic military specification MIL-S-19500, and is hermetically sealed in a metal low-profile JEDEC TO-39 package.

RCA-2N5262 is primarily intended for use as a driver for "2-1/2D" coincident-current and word-organized magnetic-memory systems, and in the other critical industrial applications requiring switching of large currents through inductive loads.

* Developmental number TA-7238 is a reduced-height version of the former developmental number TA-2626.

Maximum Ratings, *Absolute-Maximum Values*

COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	75 max.	V
COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO}	50 max.	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}	5 max.	V
Continuous	2 max.	A
Instantaneous (See Fig. 4)	3 max.	A
TRANSISTOR DISSIPATION, P_T:		
For case temperatures[a] — up to 25°C	5 max.	W
For case temperatures[a] — above 25°C	Derate at 28.5 mw/°C	
For ambient temperatures — up to 25°C	1 max.	W
For ambient temperatures — above 25°C	Derate at 5.7 mw/°C	
TEMPERATURE RANGE:		
Storage and Operating (Junction)	-65 to +200	°C
LEAD TEMPERATURE (During Soldering):		
At distances ≥ 1/32" from seating surface for 10 seconds max	265 max.	°C

a Measured at center of seating surface.

Features

- high dc beta at high collector current
  h_{fe} = 25 min at I_C = 1 A
- controlled for safe operation without damage due to second breakdown under both forward-and reverse-bias conditions
- meets the requirements of Military Specification MIL-S-19500
- excellent power handling capability—
  P_T = 5 W max. at T_C = 25°C
  P_T = 1 W max. at T_A = 25°C
- high switching speeds at high currents—
  t_{on} = 30 ns max. at I_C = 1 A
  t_{off} = 60 ns max. at I_C = 1 A
- high breakdown-voltage capabilities—
  $V_{(BR)CBO}$ = 75 V min.
  $V_{(BR)CEO}$ = 50 V min.
- hermetically sealed low-profile TO-39 metal package
- low saturation voltage at high current—
  V_{CE} = 0.5 V typ. at I_C = 1 A

ELECTRICAL CHARACTERISTICS, $T_A = 25^0 C$ *unless otherwise specified*

Characteristics	Symbols	TEST CONDITIONS					LIMITS 2N5262			UNITS
		f	V_{CE}	I_C	I_E	I_B				
		MHz	Volts	mA			Min.	Typ.	Max.	
Collector-Cutoff Current	I_{CES}		60				-	-	10	μA
			30				-	0.4	1	μA
			30▲				-	-	100	μA
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0.1			75	110	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$			10			50	56	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$				-0.1		5	8	-	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$			1000		100	-	0.5	0.8	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$			1000		100	-	1	1.4	V
Static Forward Current-Transfer Ratio	h_{FE}		1	100			35	55	-	
			1	500			40	65	-	
			1	1000*			25	45	-	
Small-Signal Forward Current Transfer Ratio	h_{fe}	100	10	50			2.5	3.5	-	
Common-Base, Open-Circuit Output Capacitance	C_{ob}	0.1 to 1	V_{CB} = 10		0		-	9	12	pF
				I_C	I_{B1}	I_{B2}				
Turn-On Time Delay Time + Rise Time	$t_{on} = (t_d + t_r)$			1000	100	-	-	18	30	ns
Turn-Off Time Storage Time + Fall Time	$t_{off} = (t_s + t_f)$			1000	100	-100	-	35	60	ns

* Pulsed condition - Pulse duration ≤ 400 μs, duty factor ≤ 0.03. ▲ $T_A = 100^0C$

CIRCUIT USED TO MEASURE TURN-ON TIME (t_{on})

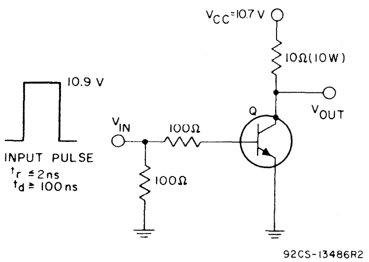


Fig.1

CIRCUIT USED TO MEASURE TURN-OFF TIME (t_{off})

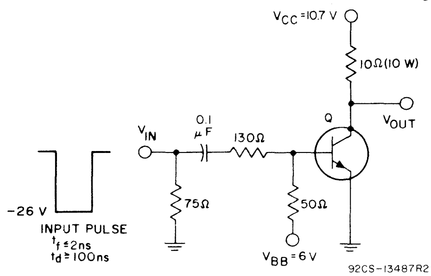


Fig.2

RATING CHART

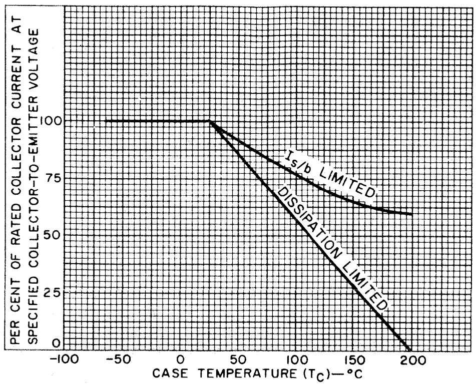


Fig.3

SECOND BREAKDOWN CHARACTERISTICS AND RATINGS

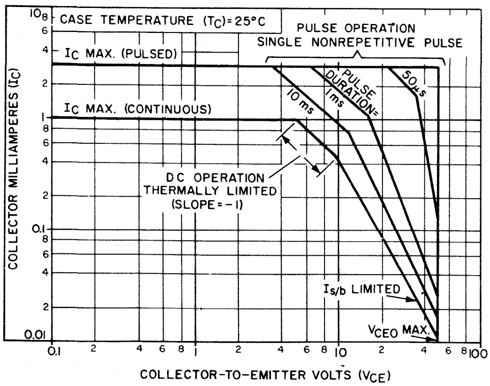


Fig.4

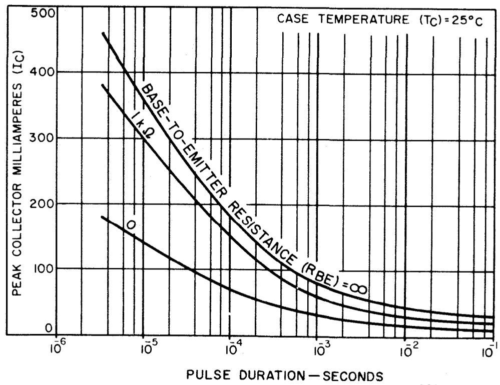


Fig.5

TYPICAL CHARACTERISTICS

h_{fe} vs I_C

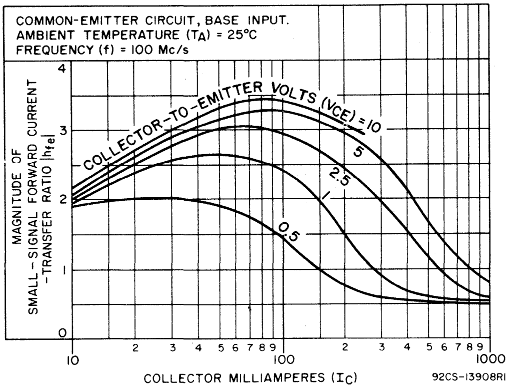


Fig.6

h_{FE} vs I_C

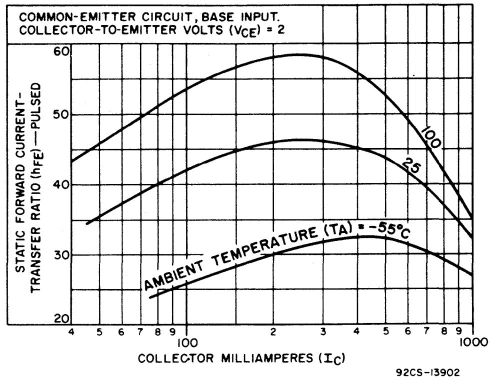


Fig.7

$V_{CE}(sat)$ vs I_C/I_B

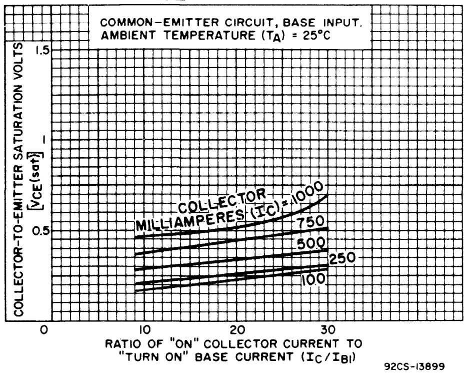


Fig.8

$V_{CE}(sat)$ vs β_T/β_C

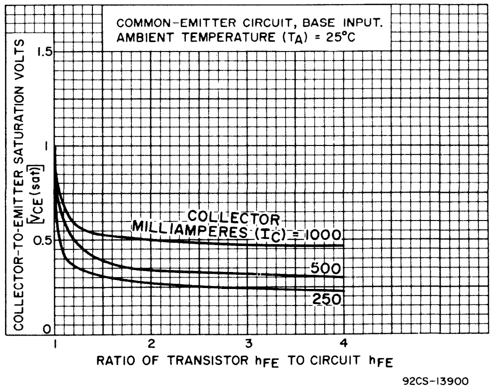


Fig.9

$V_{BE}(sat)$ vs I_C

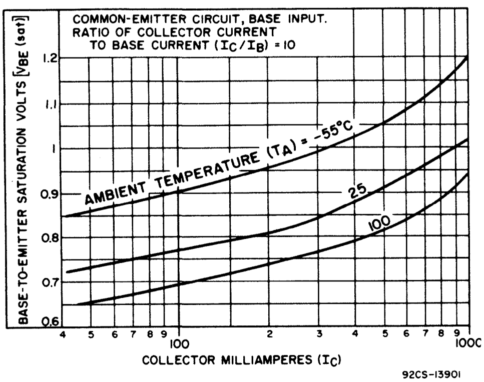


Fig.10

I_C & I_B vs V_{BE}

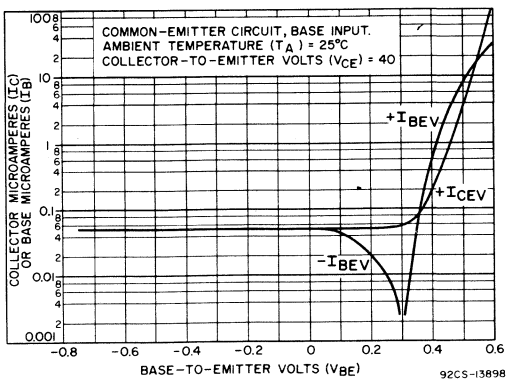


Fig.11

TYPICAL CHARACTERISTICS

t_r vs I_C/I_{B1}

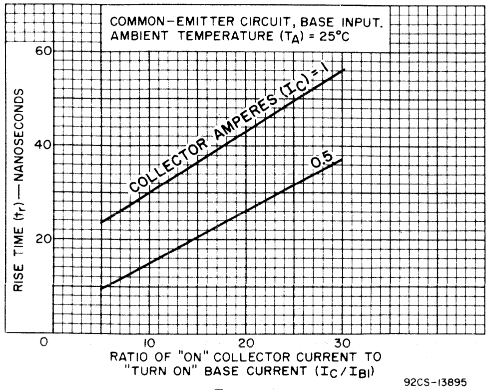


Fig.12

t_s vs I_C/I_{B1}

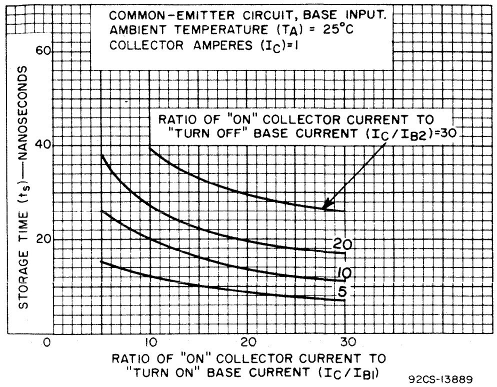


Fig.13

t_{on} vs I_C/I_{B1}

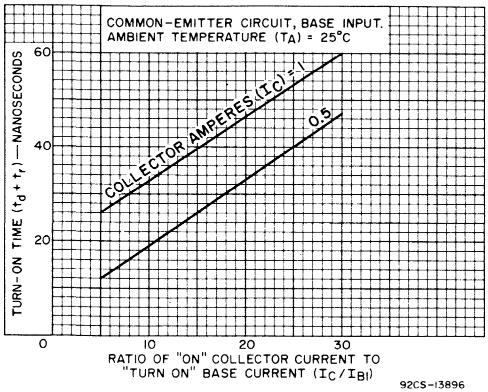


Fig.14

t_{off} vs I_C/I_{B1}

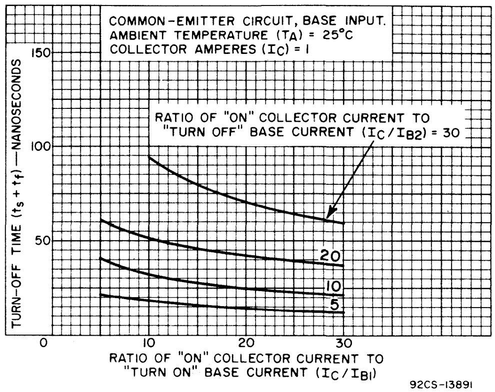


Fig.15

I_{CES} vs T_A

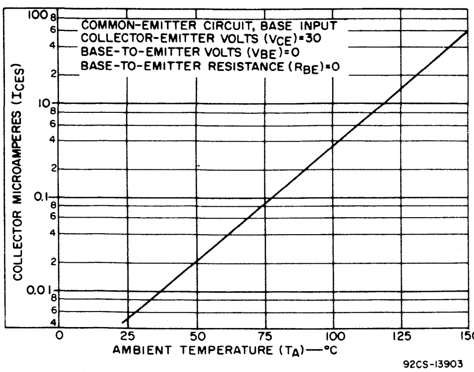


Fig.16

BV_{CERL} vs R_{BE}

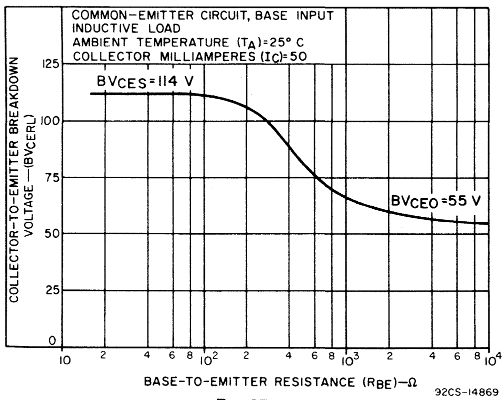


Fig.17

TYPICAL CHARACTERISTICS

C_{ob} vs V_{CB}

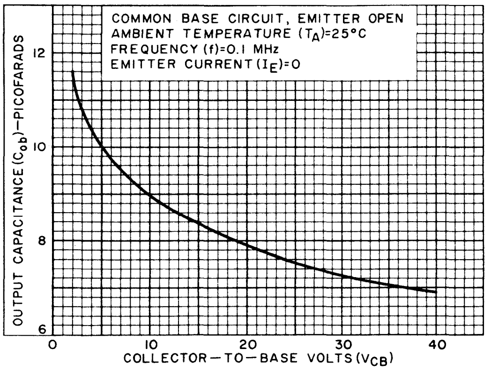


Fig. 18

C_{ib} vs V_{EB}

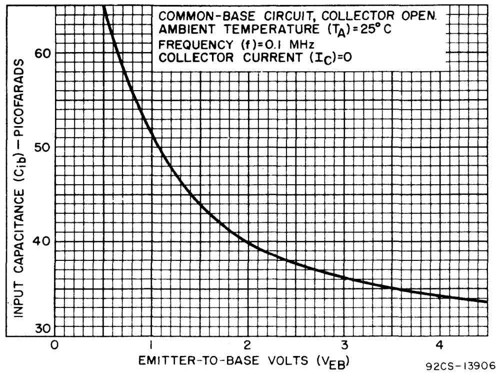
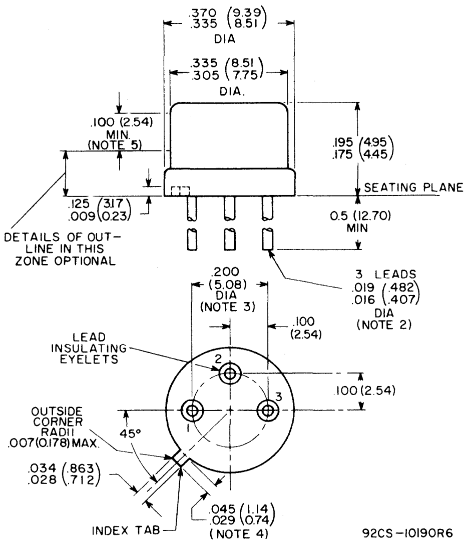


Fig. 19

DIMENSIONAL OUTLINE



Dimensions in Inches and Millimeters

Note 1: *Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.*

Note 2: The specified lead diameter applies in the zone between 0.050" (1.27 mm) and 0.250" (6.35 mm) from the seating plane. From 0.250" (6.35 mm) to the end of the lead a maximum diameter of 0.021" (0.533 mm) is held. Outside of these zones, the lead diameter is not controlled.

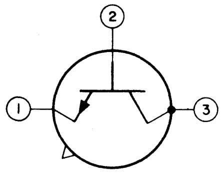
Note 3: Leads having a maximum diameter of 0.019" (0.482 mm) at a gauging plane of 0.054" (1.372 mm) + 0.001" (0.025 mm) - 0.000" (0.000 mm) below seating plane shall be within 0.007" (0.178 mm) of their true position (location) relative to a maximum width of tab.

Note 4: Measured from actual maximum diameter.

Note 5: This zone is controlled for automatic handling. The variation in actual diameter within the zone shall not exceed 0.010" (0.25 mm).

TERMINAL DIAGRAM

Bottom View



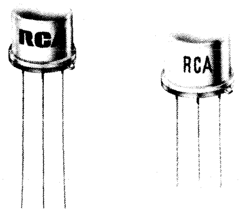
LEAD 1 — EMITTER

LEAD 2 — BASE

LEAD 3 — COLLECTOR, CASE

RCA
Solid State
Division

Power Transistors
2N5320 2N5321 2N5322 2N5323



2N5320L	2N5320S
2N5321L	2N5321S
2N5322L	2N5322S
2N5323L	2N5323S
JEDEC TO-5	JEDEC TO-39
H-1380	H-1381

Complementary N-P-N & P-N-P Silicon Power Transistors

General-Purpose Types for Small-Signal, Medium-Power Applications

Features:

- 2N5322, 2N5323 P–N–P Complements of: 2N5320, 2N5321
- Maximum safe-area-of-operation curves
- Planar construction for low-noise and low-leakage characteristics
- Low saturation voltage
- High beta at high collector current

These devices are generally available with ½-inch leads (TO-39 package). They are also available in the U.S.A., Canada, Latin America, and Far East with 1½-inch leads (TO-5 package); the shorter-lead versions are specified by a suffix letter "S" after the type number, and the longer-lead versions by a suffix letter "L".

RCA-2N5320, 2N5321, 2N5322 and 2N5323 are double-diffused epitaxial-planar silicon power transistors intended for small-signal medium-power applications. The 2N5320 and 2N5321 n-p-n types are actually high-current, high-dissipation versions of the 2N2102 with all of the salinet features of that device. The 2N5322 and 2N5323, p-n-p complements of the 2N5320 and 2N5321, are actually high-current, high-power versions of the 2N4036 with all of its additional outstanding features. (Technical data on the 2N2102 and 2N4036 are shown in RCA Data Bulletin File Nos. 106 and 216, respectively).

ALSO AVAILABLE ....

On special request, these transistor types can be supplied with a factory-attached heat radiator or mounting flange, as illustrated on page 6.

Please submit requirements to your RCA Technical Sales Representative, or write to RCA, Low-Frequency Transistor Marketing, Somerville, N. J. 08876.

MAXIMUM RATINGS, *Absolute-Maximum Values:*		2N5321	2N5323	2N5320	2N5322	
* COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	75	-75	100	-100	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:						
With 1.5 volts (V_{BE}) of reverse bias............	$V_{CEV}(sus)$	75	-75	100	-100	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$	65	-65	90	-90	V
* With base open	$V_{CEO}(sus)$	50	-50	75	-75	V
* EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	-5	7	-7	V
* COLLECTOR CURRENT	I_C	2	-2	2	-2	A
* BASE CURRENT	I_B	1	-1	1	-1	A
* TRANSISTOR DISSIPATION:	P_T					
At case temperatures up to 25° C		10	10	10	10	W
At case temperatures above 25° C		See Figs. 3 & 6 Derate linearly at 0.057 W/°C				
* TEMPERATURE RANGE:						
Storage and operating (Junction)..............		-65 to + 200				°C
* LEAD TEMPERATURE (During soldering): At distance ≥ 1/32 in. (0.8 mm) from seating plane for 10 s max		230				°C

*In accordance with JEDEC registration data format (JS-6 RDF-1)

9-73

ELECTRICAL CHARACTERISTICS, Case Temperature (T_C) = 25° C, unless otherwise specified

CHARACTERISTIC	Symbol	TEST CONDITIONS: DC Collector Voltage V, V_{CB}	V_{CE}	DC Emitter or Base Voltage V, V_{EB}	V_{BE}	DC Current mA, I_C	I_E	I_B	LIMITS: Type 2N5320 Min.	Max.	Type 2N5321 Min.	Max.	Type 2N5322 Min.	Max.	Type 2N5323 Min.	Max.	Units
Collector-Cutoff Current: With base open	I_{CBO}	80					0		-	0.5	-	-	-	-	-	-	µA
		60					0		-	-	-	5	-	-	-	-	
		-80					0		-	-	-	-	-	-0.5	-	-	
		-60					0		-	-	-	-	-	-	-	-5	
* With base-emitter Junction reverse biased	I_{CEX}		100		-1.5				-	0.1	-	-	-	-	-	-	mA
			75		-1.5				-	-	-	0.1	-	-	-	-	
			-100		1.5				-	-	-	-	-	-0.1	-	-	
			-75		1.5				-	-	-	-	-	-	-	-0.1	
T_C=150°C			70		-1.5				-	5	-	-	-	-	-	-	mA
			45		-1.5				-	-	-	5	-	-	-	-	
			-70		1.5				-	-	-	-	-	-5	-	-	
			-45		1.5				-	-	-	-	-	-	-	-5	
* Emitter-Cutoff Current	I_{EBO}			7		0			-	0.1	-	-	-	-	-	-	mA
				5		0			-	-	-	0.1	-	-	-	-	
				-7		0			-	-	-	-	-	-0.1	-	-	
				-5		0			-	-	-	-	-	-	-	-0.1	
				5		0			-	0.1	-	-	-	-	-	-	µA
				4		0			-	-	-	0.5	-	-	-	-	
				-5		0			-	-	-	-	-	-0.1	-	-	
				-4		0			-	-	-	-	-	-	-	-0.5	
Collector-to-Emitter Breakdown Voltage: With base-emitter junction reverse biased	$V_{(BR)CEV}$				-1.5	0.1			100	-	75	-	-	-	-	-	V
					1.5	-0.1			-	-	-	-	-100	-	-75	-	
Collector-to-Emitter Sustaining Voltage: With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)^a$					100			90	-	65	-	-	-	-	-	V
						-100			-	-	-	-	-90	-	-65	-	
* With base open	$V_{CEO}(sus)^a$					100		0	75	-	50	-	-	-	-	-	V
						-100		0	-	-	-	-	-75	-	-50	-	
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					500		50	-	0.5	-	0.8	-	-	-	-	V
						-500		-50	-	-	-	-	-	-0.7	-	-1.2	
* Base-to-Emitter Voltage	V_{BE}		4			500			-	1.1	-	1.4	-	-	-	-	V
			-4			-500			-	-	-	-	-	-1.1	-	-1.4	
* DC Forward Current Transfer Ratio	h_{FE}^b See NOTE		4			500			30	130	40	250	-	-	-	-	
			-4			-500			-	-	-	-	30	130	40	250	
			2			1000			10	-	-	-	-	-	-	-	
			-2			-1000			-	-	-	-	10	-	-	-	
Gain-Bandwidth Product	f_T		4			50			50	-	50	-	-	-	-	-	MHz
			-4			-50			-	-	-	-	50	-	50	-	
* Magnitude of common-emitter, small-signal, short circuit, forward current transfer ratic (f=10 MHz)	$\|h_{fe}\|$		4			50			5	-	5	-	-	-	-	-	
			-4			-50			-	-	-	-	5	-	5	-	

ELECTRICAL CHARACTERISTICS, (Cont'd)

CHARACTERISTIC	Symbol	TEST CONDITIONS							LIMITS								Units
		DC Collector Voltage V		DC Emitter or Base Voltage V		DC Current mA			Type 2N5320		Type 2N5321		Type 2N5322		Type 2N5323		
		V_{CB}	V_{CE}	V_{EB}	V_{BE}	I_C	I_E	I_B	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Second Breakdown Collector Current[c,e] (With base forward biased)	$I_{S/b}$[d]		50 -35						200 -	- -	200 -	- -	- -285	- -	- -285	- -	mA
* Sat. Switching Time: *(See Fig.11.)* Turn-on Time	t_{on}		30 -30			500 -500		50 -50	- -	80 -	- -	80 -	- -	- 100	- -	- 100	ns
Turn-off Time	t_{off}		30 -30			500 -500		50 -50	- -	800 –	- -	800 -	– –	– 1000	- -	- 1000	ns
* Thermal Resistance: Junction-to-Case	θ_{J-C}								-	17.5	-	17.5	-	17.5	-	17.5	$^oC/W$
Junction-to-Ambient	θ_{J-A}								–	150	-	150	-	150	-	150	$^oC/W$

[a] CAUTION: The sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$ MUST NOT be measured on a curve tracer.

[b] Pulsed; pulse duration $\leq$ 300 μs, duty factor $\leq$ 0.02.

[c] Safe operating regions for forward-bias operation are shown on pages 4 & 5.

[d] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward biased for transistor operation in the active region.

[e] Pulsed; 0.4s non-repetitive pulse.

*In accordance with JEDEC registration data format (JS-6 RDF-1)

NOTE: RCA 2N5320, 2N5321, 2N5322, and 2N5323 can be shipped with color dots on the device case to indicate the following ranges of beta values within the beta limits specified for each device.

Color Code	Beta Range	Color Code	Beta Range
Brown	25-38	Green	73-110
Red	33-50	Blue	95-145
Orange	43-65	Violet	125-190
Yellow	56-85	White	165-250

Specific beta distributions or beta matching are available as custom types only on special order. For further details, contact your local RCA Sales office.

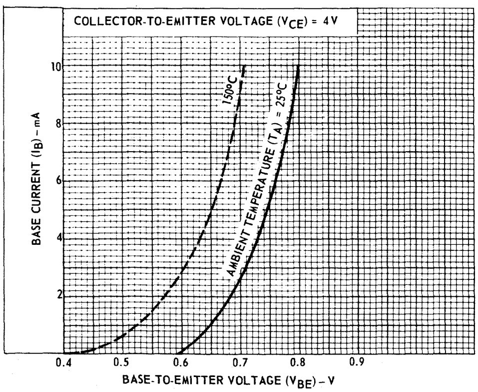


Fig. 1 - Typical input characteristics for types 2N5320 and 2N5321.

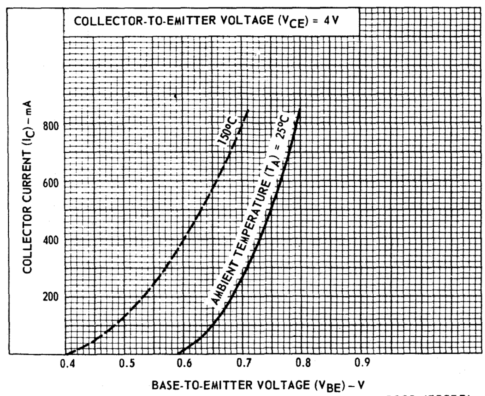


Fig. 2 - Typical transfer characteristics for types 2N5320 and 2N5321.

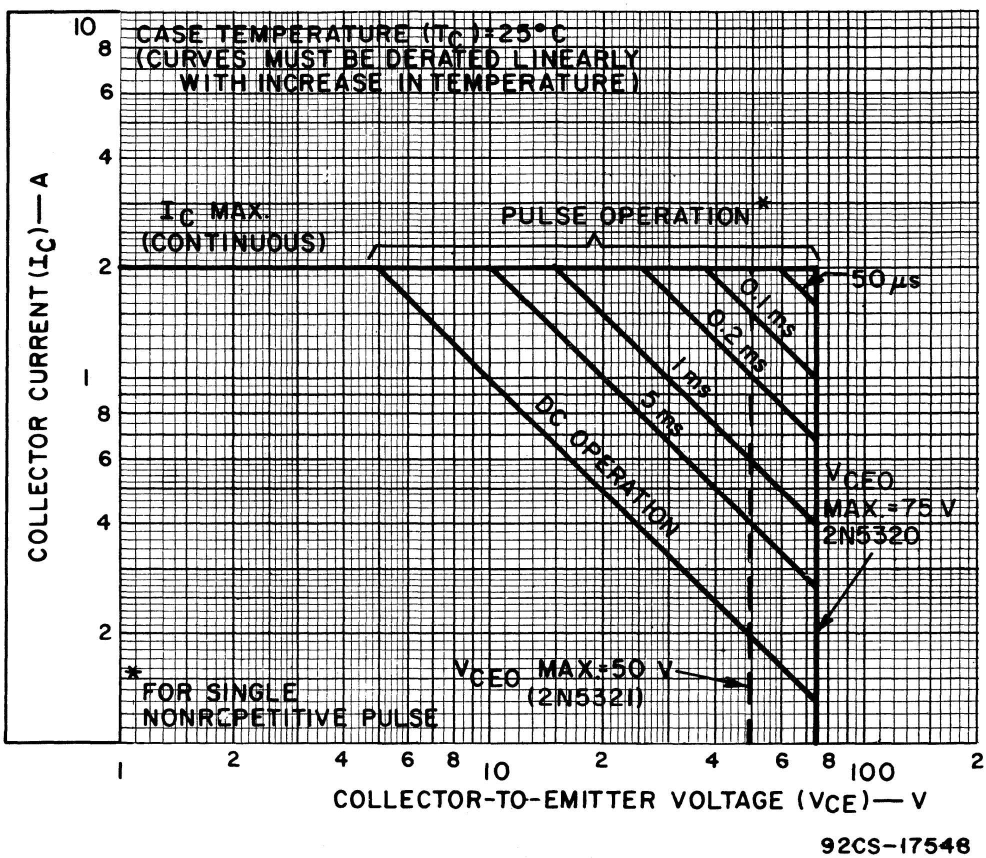


Fig. 3 - Maximum operating areas for types 2N5320 and 2N5321.

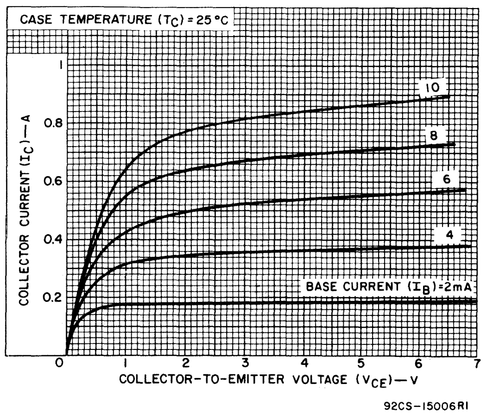


Fig. 4 - Typical output characteristics for types 2N5320 and 2N5321.

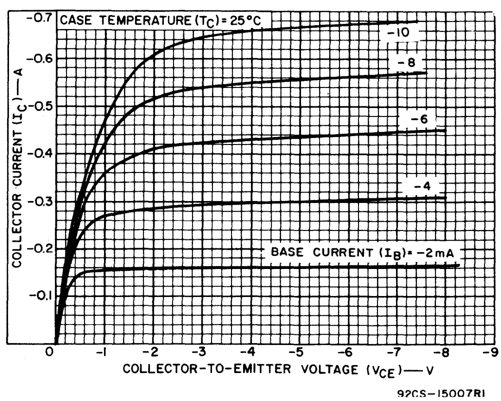


Fig. 5 - Typical output characteristics for types 2N5322 and 2N5323.

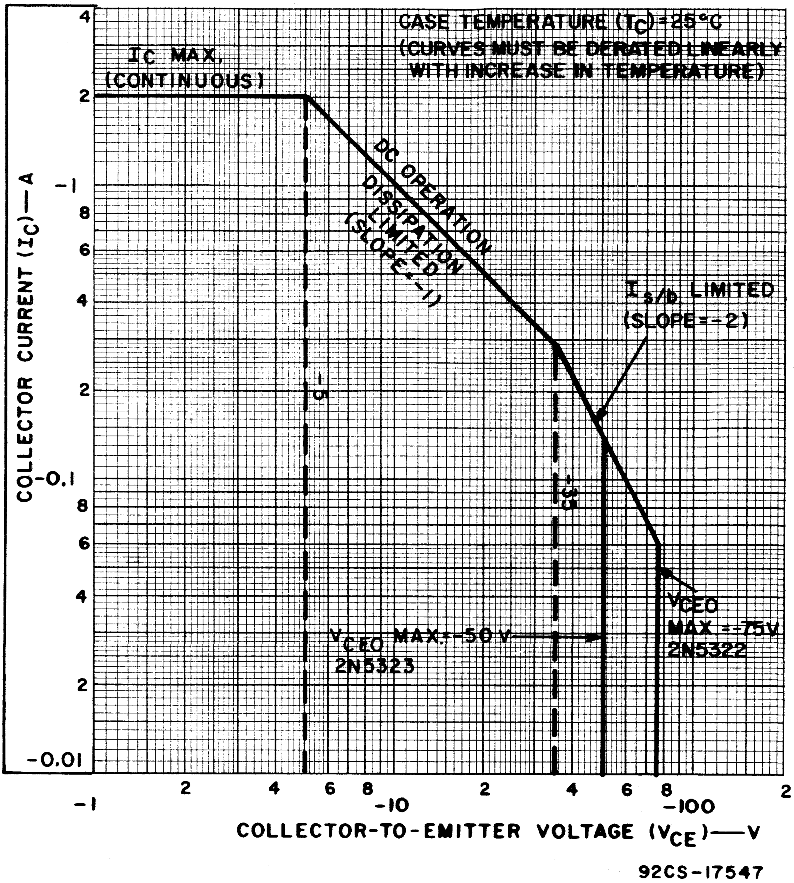


Fig. 6 - Maximum operating areas for types 2N5322 and 2N5323.

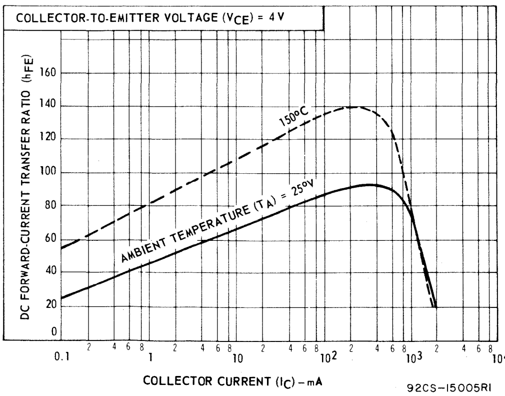


Fig. 7 - Typical static beta characteristics for types 2N5320 and 2N5321.

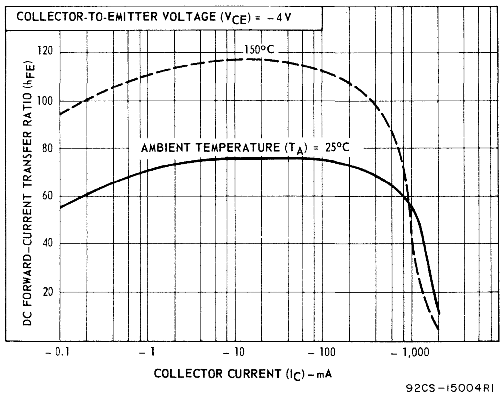


Fig. 8 - Typical static beta characteristics for types 2N5322 and 2N5323.

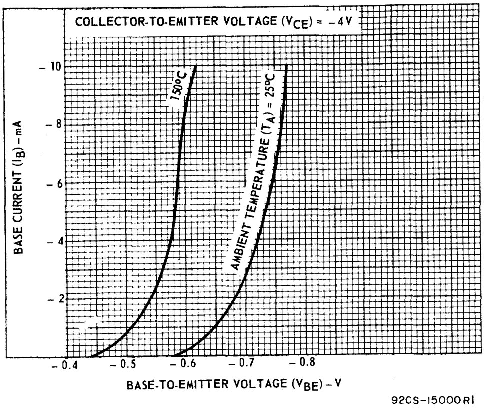


Fig. 9 - Typical input characteristics for types 2N5322 and 2N5323.

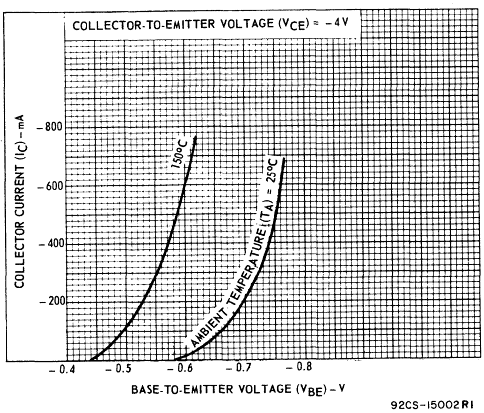
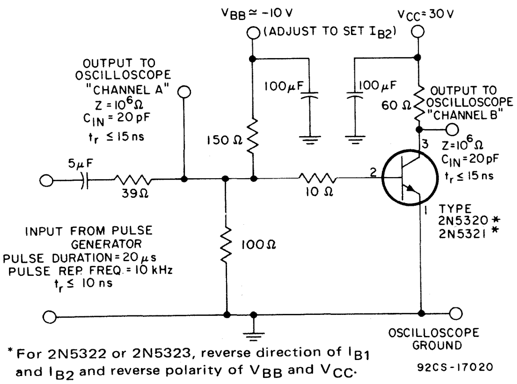


Fig. 10 - Typical transfer characteristics for types 2N5322 and 2N5323.



*For 2N5322 or 2N5323, reverse direction of I_{B1} and I_{B2} and reverse polarity of V_{BB} and V_{CC}.

Fig. 11 - Circuit used to measure switching times for all types.

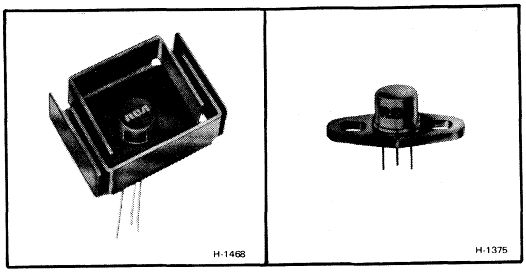
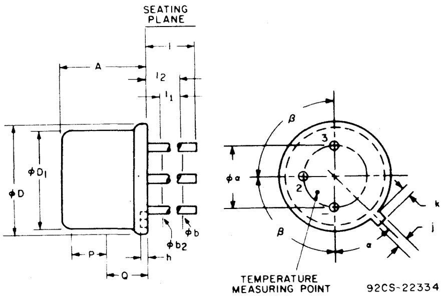


Fig. 12 - 2N5320 - 23 with factory-attached heat radiator or mounting flange, available upon special request. (See page 1.).

DIMENSIONAL OUTLINE FOR ALL TYPES



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
φa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
φb	0.016	0.021	0.406	0.533	2
φb2	0.016	0.019	0.406	0.483	2
φD	0.350	0.370	8.89	9.40	
φD1	0.305	0.335	8.00	8.51	
h	0.009	0.041	0.229	1.04	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
L long lead	1.500		38.10		2
L short lead	0.500		12.70		2
l1		0.050		1.27	2
l2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads) φb2 applies between l1 and l2. φb applies between l2 and l. Diameter is uncontrolled in l1.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

TERMINAL CONNECTIONS

Lead 1 – Emitter Lead 2 – Base Lead 3 – Collector, Case

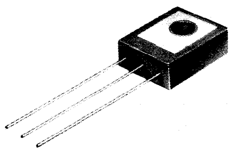
RCA Solid State Division

Power Transistors

2N6178 2N6180 2N6179 2N6181

Silicon N-P-N & P-N-P Power Transistors

"Plastic TO-5" General-Purpose Types for Large-Signal, Medium-Power Applications



"Plastic TO-5"

H-1642

Features:

- Maximum area-of-operation curves
- Planar construction for low-noise and low-leakage characteristics
- Low saturation voltage (2N6178, 2N6180)
- High beta (2N6179, 2N6181)
- Fast switching (2N6178, 2N6179)
- "Plastic TO-5" package with insulated mounting hole

RCA types 2N6178, 2N6179, 2N6180, and 2N6181● are silicon power transistors intended for large-signal, medium-power applications in industrial and commercial equipment.

The 2N6178 and 2N6179 are triple-diffused silicon n-p-n planar types. These types have features similar to the popular 2N2102 plus higher collector-current ratings and dissipation capability.

Types 2N6180 and 2N6181 (p-n-p complements of the 2N6178 and 2N6179, respectively) are double-diffused, epitaxial-planar devices. These types have features similar to the 2N4036 plus higher collector-current ratings and dissipation capability.

Complementary N-P-N & P-N-P Types...

2N6178, 2N6179 } N-P-N   2N6180, 2N6181 } P-N-P

In addition, these types utilize the new RCA-developed "Plastic TO-5" package. This plastic package has an insulated mounting hole for ease of mounting and heat sinking for optimum thermal contact.

● Formerly RCA Dev. Nos. TA7554–TA7557, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N6179	2N6181	2N6178	2N6180	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	75	-75	100	-100	V
COLLECTOR-TO-EMITTER VOLTAGE:						
* With 1.5 volts (V_{BE}) of reverse bias	V_{CEX}	75	-75	100	-100	V
With external base-to-emitter resistance (R_{BE}) = 100Ω, sustaining	V_{CER}(sus)	65	-65	90	-90	V
With base open, sustaining	V_{CEO}(sus	50	-50	75	-75	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	-5	7	-7	V
*CONTINUOUS COLLECTOR CURRENT	I_C	2	-2	2	-2	A
*CONTINUOUS BASE CURRENT	I_B	1	-1	1	-1	A
*TRANSISTOR DISSIPATION:	P_T					
At case temperatures up to 25°C		25	25	25	25	W
At case temperatures above 25°C			See Figs. 1, 2, & 3			
At case temperatures up to 100°C		10	10	10	10	W
At case temperatures above 100°C			See Figs. 3, 4, & 5			
*TEMPERATURE RANGE:						
Storage and operating (Junction)		←	-65 to 150		→	°C
*LEAD TEMPERATURE (During soldering): At distance ≥1/32 in (0.8 mm) from seating plane for 10 s max		←	230		→	°C

*In accordance with JEDEC registration data format JS-6/RDF-1.

11-73

ELECTRICAL CHARACTERISTICS, *at case temperature (T_C) = 25°C, unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS							LIMITS								UNITS
		DC Collector Voltage (V)		DC Emitter or Base Voltage (V)		DC Current (mA)			Type 2N6178		Type 2N6179		Type 2N6180		Type 2N6181		
		V_{CB}	V_{CE}	V_{EB}	V_{BE}	I_C	I_E	I_B	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Collector-Cutoff Current With emitter open	I_{CBO}	80					0		–	0.5	–	–	–	–	–	–	µA
		60					0		–	–	–	0.5	–	–	–	–	
		–80					0		–	–	–	–	–	–0.5	–	–	
		–60					0		–	–	–	–	–	–	–	–0.5	
With base open	I_{CEO}		60					0	–	1	–	–	–	–	–	–	mA
			45					0	–	–	–	1	–	–	–	–	
			–60					0	–	–	–	–	–	–1	–	–	
			–45					0	–	–	–	–	–	–	–	–1	
* With base reverse-biased	I_{CEV}		100		–1.5				–	0.1	–	–	–	–	–	–	mA
			75		–1.5				–	–	–	0.1	–	–	–	–	
			–100		1.5				–	–	–	–	–	–0.1	–	–	
			–75		1.5				–	–	–	–	–	–	–	–0.1	
* With base reverse-biased and T_C = 100°C	I_{CEV}		70		–1.5				–	0.5	–	–	–	–	–	–	mA
			45		–1.5				–	–	–	0.5	–	–	–	–	
			–70		1.5				–	–	–	–	–	–0.5	–	–	
			–45		1.5				–	–	–	–	–	–	–	–0.5	
* Emitter-Cutoff Current	I_{EBO}			7		0			–	0.1	–	–	–	–	–	–	mA
				5		0			–	–	–	0.1	–	–	–	–	
				–7		0			–	–	–	–	–	–0.1	–	–	
				–5		0			–	–	–	–	–	–	–	–0.1	
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$					0	0.1		7	–	5	–	–	–	–	–	V
						0	–0.1		–	–	–	–	–7	–	–5	–	
* Collector-to-Emitter Breakdown Voltage: With base-emitter junction reverse-biased	$V_{(BR)CEV}$				–1.5	0.1			100	–	75	–	–	–	–	–	V
					1.5	–0.1			–	–	–	–	–100	–	–75	–	
* With base open	$V_{(BR)CEO}$					100		0	75	–	50	–	–	–	–	–	V
						–100		0	–	–	–	–	–75	–	–50	–	
Collector-to-Emitter Sustaining Voltage: With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)^a$					100			90	–	65	–	–	–	–	–	V
						–100			–	–	–	–	–90	–	–65	–	
With base open	$V_{CEO}(sus)^a$					100		0	75	–	50	–	–	–	–	–	V
						–100		0	–	–	–	–	–75	–	–50	–	
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					500		50	–	0.5	–	0.8	–	–	–	–	V
						–500		–50	–	–	–	–	–	–0.7	–	–1.2	
* Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$					500		50	–	1.2	–	1.5	–	–	–	–	V
						–500		–50	–	–	–	–	–	–1.2	–	–1.5	
Output Capacitance (At 1 MHz)	C_{obo}	10							12	20	12	20	–	–	–	–	pF
		–10							–	–	–	–	25	40	25	40	
* DC Forward-Current Transfer Ratio	h_{FE}		4			50			–	–	30	–	–	–	–	–	
			–4			–50			–	–	–	–	–	–	30	–	
			2			500[b]			30	130	40	250	–	–	–	–	
			–2			–500[b]			–	–	–	–	30	130	40	250	
			2			1000[b]			10	–	–	–	–	–	–	–	
			–2			–1000[b]			–	–	–	–	10	–	–	–	
Second-Breakdown Collector Current [c, d] (With base forward-biased)	$I_{S/b}^e$		V_{CC}= 50						200	–	200	–	–	–	–	–	mA
			–50						–	–	–	–	–150	–	–150	–	
Gain-Bandwidth Product	f_T		4			50			50	–	50	–	–	–	–	–	MHz
			–4			–50			–	–	–	–	50	–	50	–	
* Magnitude of Common Emitter, Small-Signal, Short-Circuit Forward-Current Transfer Ratio (f = 10 MHz)	$\|h_{fe}\|$		4			50			5	–	5	–	–	–	–	–	
			–4			–50			–	–	–	–	5	–	5	–	

Chart continued on page 3.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS							LIMITS								UNITS
		DC Collector Voltage (V)		DC Emitter or Base Voltage (V)		DC Current (mA)			Type 2N6178		Type 2N6179		Type 2N6180		Type 2N6181		
		V_{CB}	V_{CE}	V_{EB}	V_{BE}	I_C	I_E	I_B	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
* Saturated Switching Time: (See Fig. 30 & 31) Turn-on Time	t_{on}		V_{CC}= 30 −30			500 −500		50 −50	– –	80 –	– –	80 –	– –	– 100	– –	– 100	ns
Turn-off Time	t_{off}		V_{CC}= 30 −30			500 −500		50 −50	– –	800 –	– –	800 –	– –	– 1000	– –	– 1000	ns
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$								–	5	–	5	–	5	–	5	°C/W
Junction-to-Ambient	$R_{\theta JA}$								–	156	–	156	–	156	–	156	°C/W

* In accordance with JEDEC registration data format JS-6/RDF-1.

[a] CAUTION: The sustaining voltages V_{CEO}(sus) and V_{CER}(sus) MUST NOT be measured on a curve tracer.

[b] Pulsed; pulse duration ≤300 μs, duty factor ≤0.02.

[c] Safe operating regions for forward-bias operation are shown on Figs. 1, 2, 4, and 5.

[d] Pulsed: 0.4s, non-repetitive pulse.

[e] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward biased for transistor operation in the active region.

N-P-N

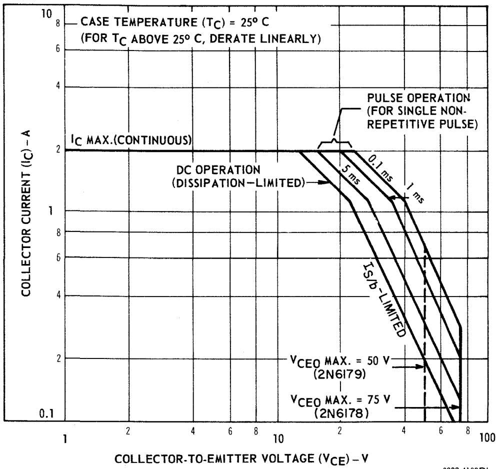


Fig.1—Maximum operating areas for 2N6178 and 2N6179 at T_C=25°C.

P-N-P

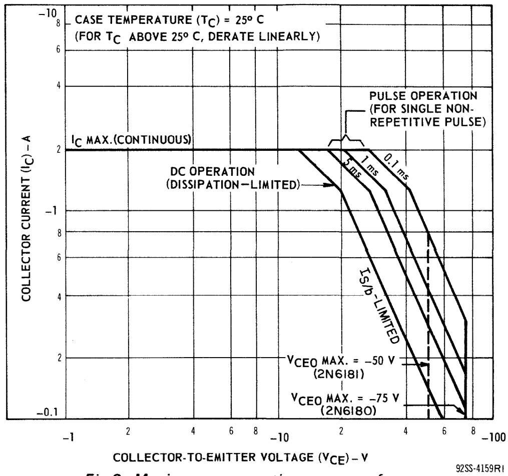


Fig.2—Maximum operating areas for 2N2180 and 2N6181 at T_C=25°C.

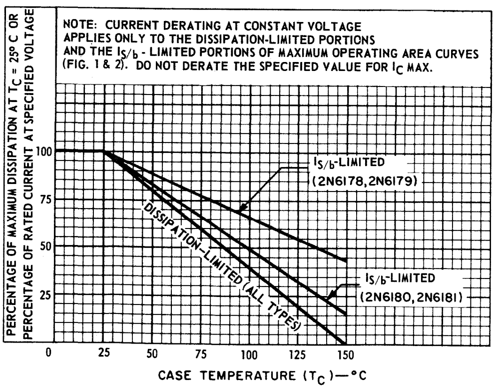


Fig.3—Derating curves for all types.

N-P-N

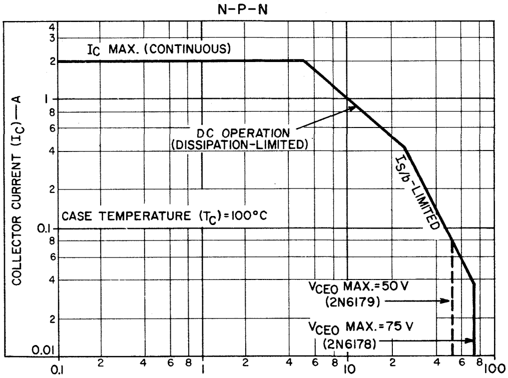


Fig.4—Maximum operating areas for 2N6178 and 2N6179 at T_C=100°C.

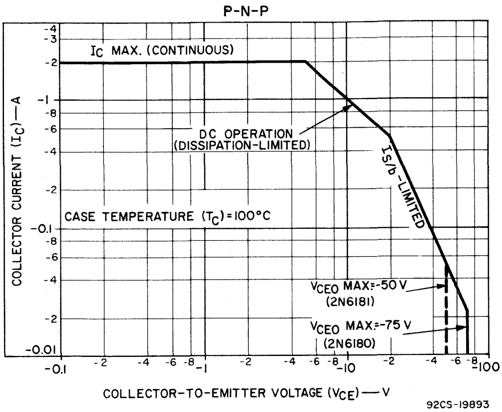


Fig.5—Maximum operating areas for 2N6180 and 2N6181 at T_C=100°C.

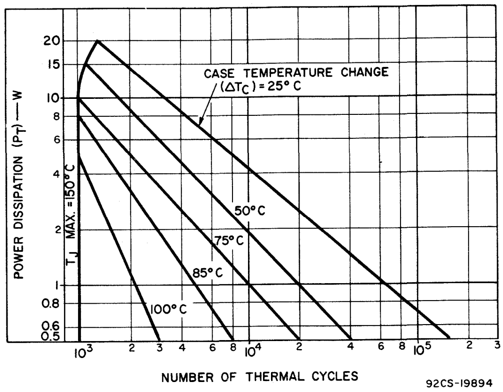


Fig.6—Thermal-cycling rating chart for all types.

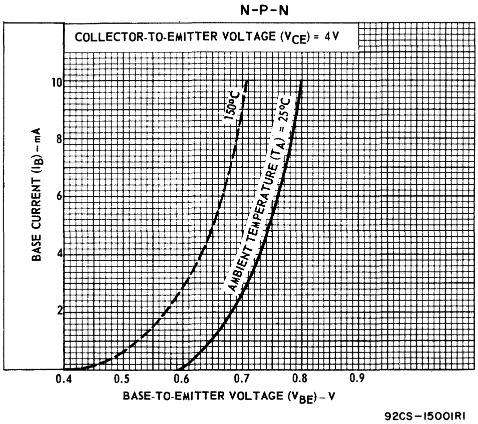


Fig.7—Typical input characteristics for 2N6178 and 2N6179.

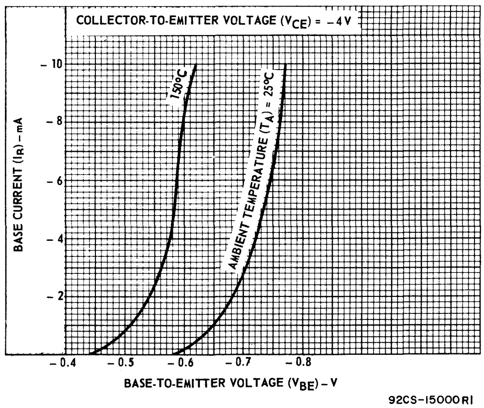


Fig.8—Typical input characteristics for 2N6180 and 2N6181.

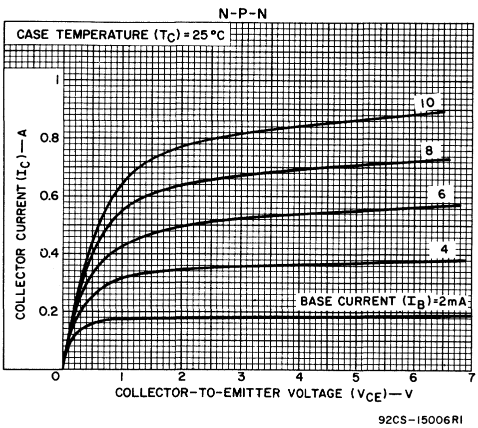


Fig.9—Typical output characteristics for 2N6178 and 2N6179.

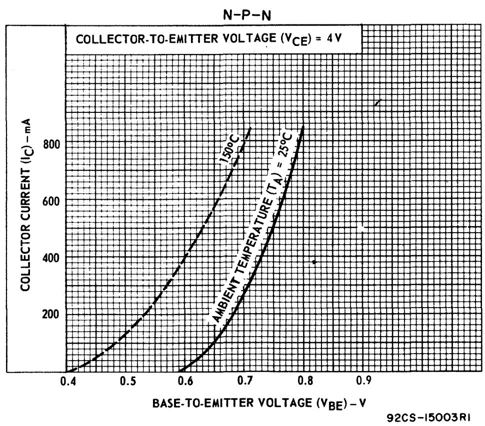


Fig.10—Typical transfer characteristics for 2N6178 and 2N6179.

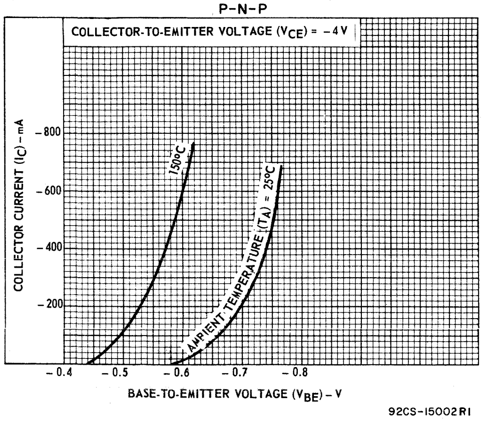


Fig.11—Typical transfer characteristics for 2N6180 and 2N6181.

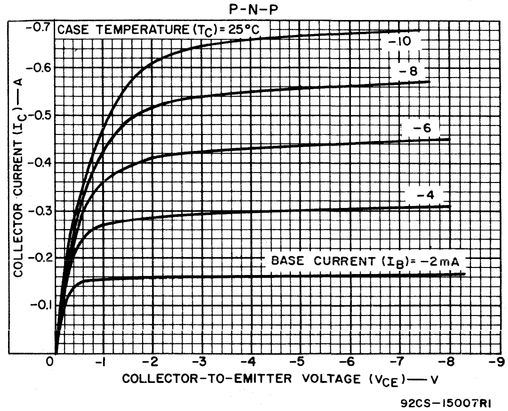


Fig.12—Typical output characteristics for 2N6180 and 2N6181.

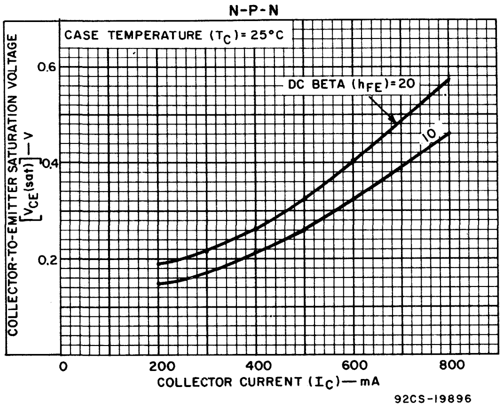


Fig.13—Typical saturation-voltage characteristics for 2N6178 and 2N6179.

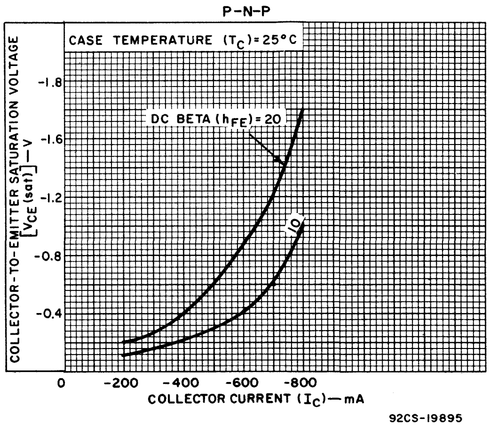


Fig.14—Typical saturation-voltage characteristics for 2N6180 and 2N6181.

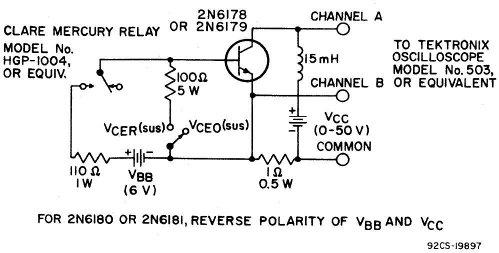


Fig.15—Circuit used to measure sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$.

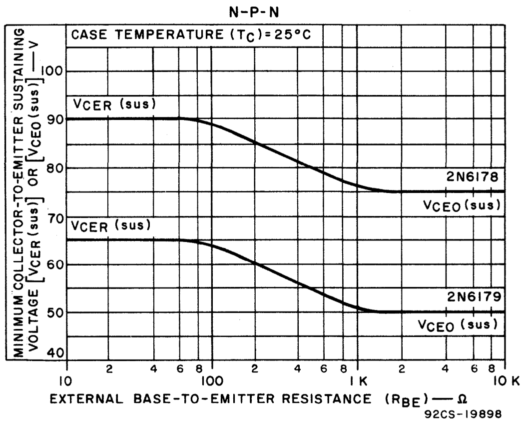


Fig.16—Collector-to-emitter sustaining voltage characteristics for 2N6178 and 2N6179.

P-N-P

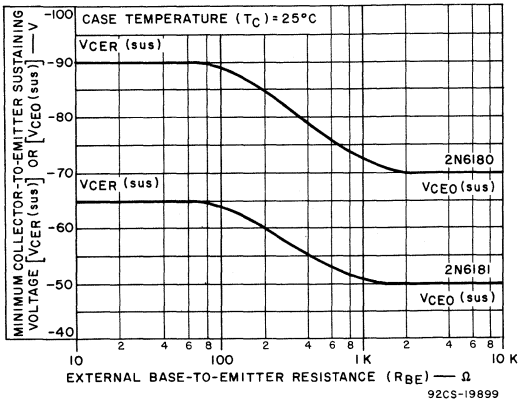
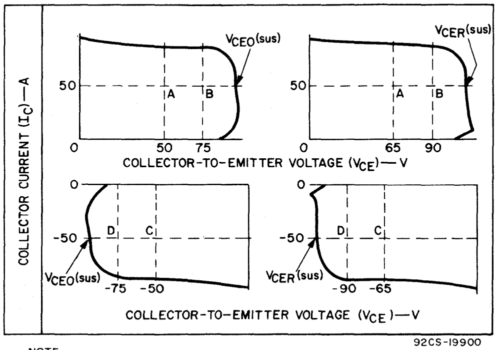


Fig.17—Collector-to-emitter sustaining voltage characteristics for 2N6180 and 2N6181.



NOTE:
SUSTAINING VOLTAGES V_{CEO}(sus) AND V_{CER}(sus) ARE ACCEPTABLE WHEN TRACES FALL TO THE RIGHT AND ABOVE POINTS "A" FOR TYPE 2N6179, POINTS "B" FOR TYPE 2N6178, TO THE LEFT AND BELOW POINTS "C" FOR TYPE 2N6181, AND POINTS "D" FOR TYPE 2N6180.

Fig.18—Oscilloscope display for measurement of sustaining voltages (test circuit shown in Fig.15).

N-P-N

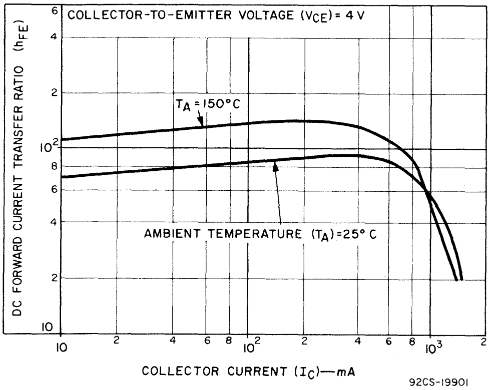


Fig.19—Typical dc beta characteristics for 2N6178 and 2N6179.

P-N-P

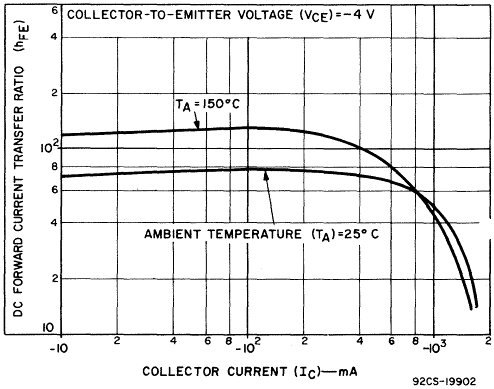


Fig.20—Typical dc beta characteristics for 2N6180 and 2N6181.

N-P-N

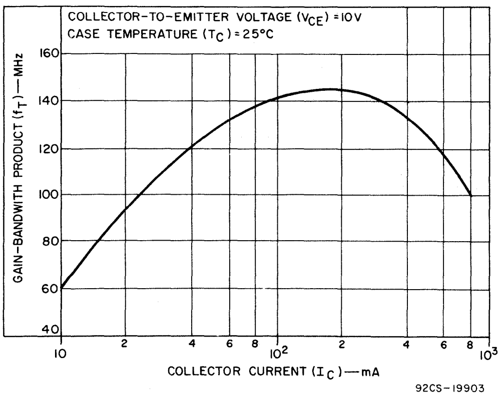


Fig.21—Typical gain-bandwidth product for 2N6178 and 2N6179.

N-P-N

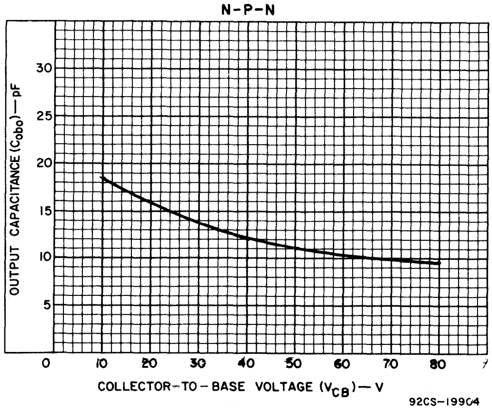


Fig.22—Typical output capacitance vs. collector-to-base voltage for 2N6178 and 2N6179.

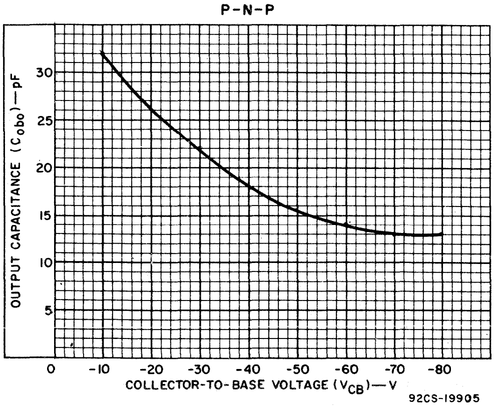


Fig.23—Typical output capacitance vs. collector-to-base voltage for 2N6180 and 2N6181.

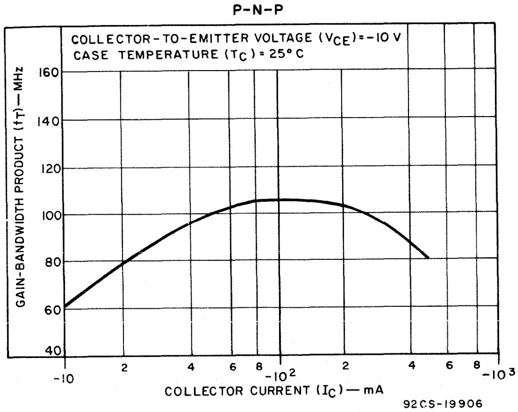


Fig.24—Typical gain-bandwidth product for 2N6180 and 2N6181.

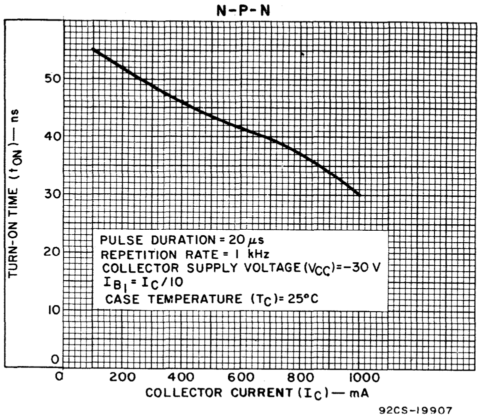


Fig.25—Typical turn-on time for 2N6178 and 2N6179.

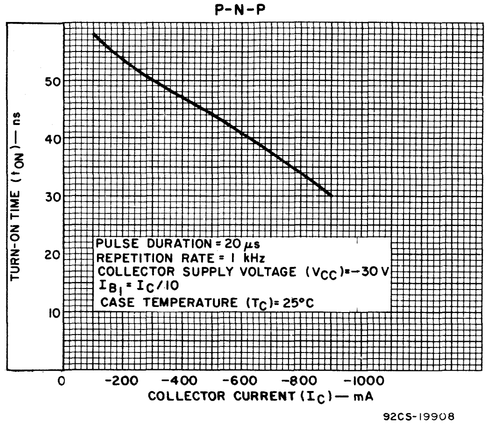


Fig.26—Typical turn-on time for 2N6180 and 2N6181.

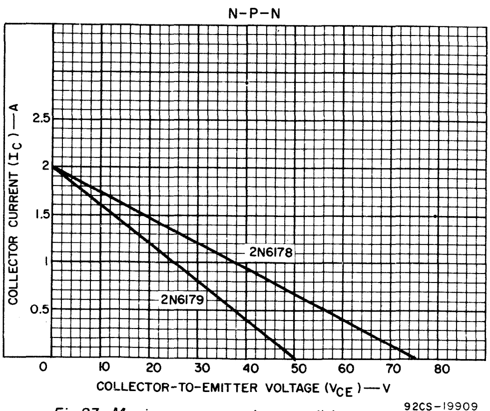


Fig.27—Maximum operating conditions, resistive-load switching between saturation and cutoff for 2N6178 and 2N6179.

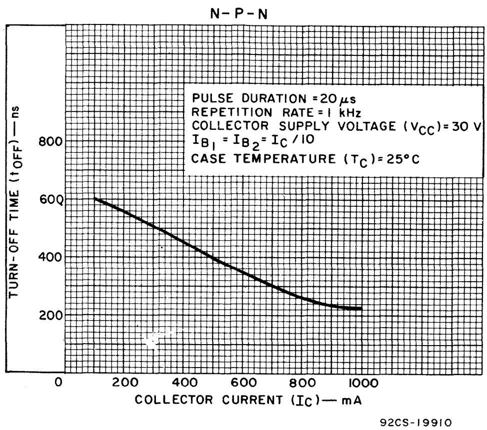


Fig.28—Typical turn-off time for 2N6178 and 2N6179.

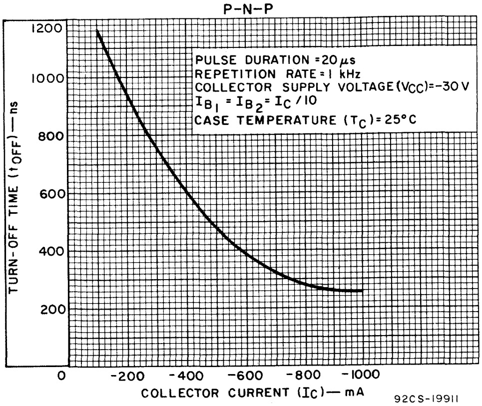


Fig.29—Typical turn-off time for 2N6180 and 2N6181.

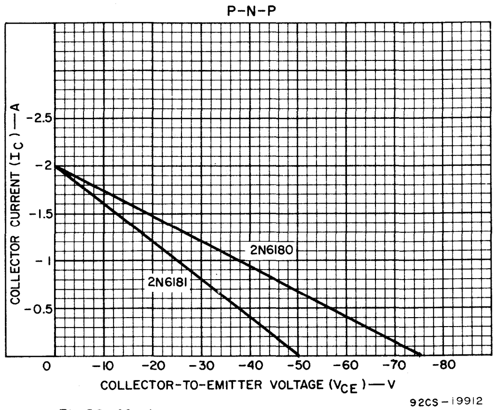


Fig.30—Maximum operating conditions, resistive-load switching between saturation and cutoff for 2N6180 and 2N6181.

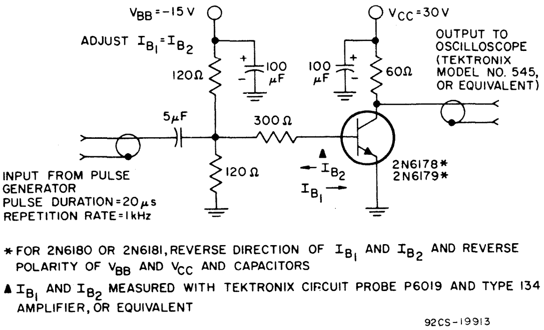


Fig.31—Circuit used to measure switching times for all types.

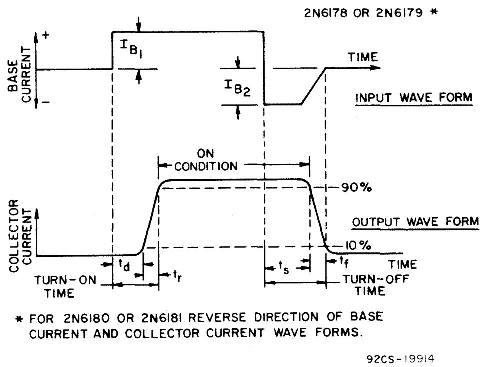
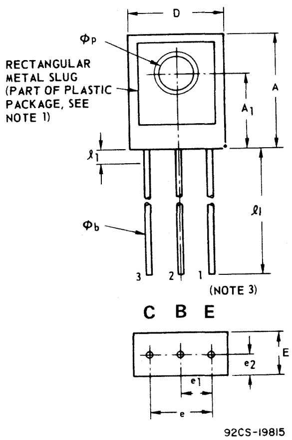


Fig.32—Phase relationship between input current and output voltage showing reference points for specification of switching times (test circuit shown in Fig.31).

DIMENSIONAL OUTLINE
"Plastic TO-5"



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	0.385	0.395	9.78	10.03	
A1	0.251	0.261	6.37	6.63	
φb	0.016	0.019	0.41	0.48	2
D	0.305	0.315	7.75	8.00	
E	0.145	0.155	3.68	3.94	
e	0.195	0.205	4.95	5.21	
e1	0.095	0.105	2.41	2.67	
e2	0.070	0.080	1.78	2.03	
ℓ	0.725	0.745	18.41	18.91	
ℓ1	0.125	0.250	3.17	6.35	
φp	0.112	0.118	2.84	2.99	

NOTE 1: To attach to heat sink, use a 4-40 binding-head screw and a No. 4 flat washer. The recommended screw torque (for even distribution of mounting pressure and optimum thermal contact) is 6 in.-lb.
NOTE 2: Three leads. Leads are pretinned to the ℓ1 dimension.
NOTE 3: Lead numbering from right to left with rectangular metal slug facing observer.

TERMINAL CONNECTIONS
Lead 1 — Emitter
Lead 2 — Base
Lead 3 — Collector
Rectangular Metal Slug-Collector

RCA
Solid State
Division

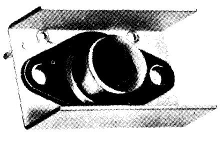
Power Transistors

2N3878 2N5202
2N3879 40375

RCA-2N3878, 2N3879, 2N5202* are epitaxial silicon n-p-n transistors. The 2N3878 is an amplifier type intended for audio-, ultrasonic-, and radio-frequency circuits. Types 2N3879 and 2N5202 are switching transistors intended for use in high-current, high-speed switching circuits.

Typical applications for these transistors include: low-distortion power amplifiers, oscillators, switching regulators, series regulators, converters, and inverters.

Formerly RCA Dev. Type Nos. TA2509, TA2509A, and TA7285, respectively.

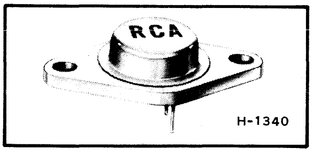

H-1470A
40375

ALSO AVAILABLE . . .

Type 40375 is a 2N3878 with a factory-attached heat radiator; it is intended for printed circuit-board applications.

SILICON N-P-N TRANSISTORS

Amplifier and Switching Types for Industrial and Commercial Applications



H-1340

2N3878, 2N3879, & 2N5202 (JEDEC TO-66)

- Maximum operating-area curves for DC and pulse operation.
  $I_{S/b}$-limit line begins at: 36 V (2N3878)
  28 V (2N3879)
  23 V (2N5202)
- $V_{CER}(sus)$ = 90 V (2N3879)
  75 V (2N5202)
  65 V (2N3878)
- V_{CBO} = 120 V Max. (2N3878, 2N3879, 2N5202)
- Rated for safe operation in both forward- and reverse-bias conditions.
- Total saturated switching time typically less than 1 μs at 4 A for 2N3879 and 2N5202.

MAXIMUM RATINGS

Absolute-Maximum Values:		2N3878 40375	2N3879	2N5202	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	120	120	120	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:					
With external base-to-emitter resistance (R_{BE}) = 50 Ω	$V_{CER}(sus)$	65	90	75	V
With base open	$V_{CEO}(sus)$	50	75	–	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	7	7	7	V
CONTINUOUS COLLECTOR CURRENT	I_C	7	7	4	A
PEAK COLLECTOR CURRENT		10	10	5	A
CONTINUOUS BASE CURRENT	I_B	5	5	2	A
TRANSISTOR DISSIPATION:	P_T				
At case temperatures up to 25° C and V_{CE}					
up to 36 V		35 (2N3878)	–	–	W
28 V		–	35	–	W
23 V		–	–	35	W
At case temperatures up to 25° C and V_{CE}					
above 36 V		See *Fig.5*	–	–	
28 V		–	See *Fig.6*	–	
23 V		–	–	See *Fig.6*	
At case temperatures above 25° C and V_{CE}					
above 36 V		See *Figs.4 & 5*	–	–	
28 V		–	See *Figs.4 & 6*	–	
23 V		–	–	See *Figs.4 & 6*	
At free-air temperatures up to 25° C		5.8 (40375)	–	–	W
At free-air temperatures above 25° C		See *Fig.7*	–	–	
TEMPERATURE RANGE:					
Storage & Operating (Junction)		–65 to 200			°C
PIN TEMPERATURE (During soldering):					
At distances ≥ 1/32 in. from seating plane for 10 s max.		255			°C

11-73

ELECTRICAL CHARACTERISTICS *Case Temperature (T_C) = 25° Unless Otherwise Specified*

Characteristic	Symbol	TEST CONDITIONS: DC Collector Volts V_{CB}	DC Collector Volts V_{CE}	DC Emitter or Base Volts V_{EB}	DC Emitter or Base Volts V_{BE}	DC Current (Amperes) I_C	DC Current (Amperes) I_E	DC Current (Amperes) I_B	LIMITS: Types 2N3878 40375 Min.	Types 2N3878 40375 Max.	Type 2N3879 Min.	Type 2N3879 Max.	Type 2N5202 Min.	Type 2N5202 Max.	Units
Collector-Cutoff Current	I_{CEO}		40					0	–	5	–	5	–	–	mA
	I_{CEV}		100		−1.5				–	4	–	4	–	10	mA
	I_{CEV} (T_C = 150° C)		100		−1.5				–	4	–	4	–	10	mA
Emitter-Cutoff Current	I_{EBO}			4 6		0 0			– –	4 –	– –	2 –	– –	– 10	mA
DC Forward-Current Transfer Ratio	h_{FE}		1.2 2 5 5			4 4 0.5 4			– 8 50 20	– – 200 –	– 12 40 20	– – – 80	10 – – –	100 – – –	
Collector-to-Emitter Sustaining Voltage: *(See Fig. 1 & 2)* With base open	$V_{CEO}(sus)$					0.2		0	50[a]	–	75[a]	–	–	–	V
With external base-to-emitter resistance (R_{BE}) = 50 Ω	$V_{CER}(sus)$					0.2			65[a]	–	90[a]	–	75[a]	–	V
Base-to-Emitter Voltage	V_{BE}		1.2 2			4 4			– –	– 2.5	– –	– 1.8	– –	1.9 –	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					4 4		0.4 0.5	– –	– 2.0	– –	1.2 –	– –	1.2 –	V
Output Capacitance (At 1 MHz)	C_{ob}	10					0		–	175	–	175	–	175	pF
Second-Breakdown[b] Collector Current[d] (With base forward biased)	$I_{S/b}$[c]		40						750	–	500	–	400	–	mA
Second-Breakdown[b] Energy: With base reverse biased, R_B = 50 Ω, L = 50 μH	$E_{S/b}$[e]				V_{BB} = −4				–	–	–	–	0.4	–	mJ
With base reverse biased, R_B = 50 Ω, L = 125 μH					V_{BB} = −4				1	–	1	–	–	–	mJ
Small-Signal, Forward-Current Transfer Ratio (At 10 MHz)	h_{fe}		10			0.5			6.0	–	6.0	–	6.0	–	
Sat. Switching Turn-On Time: Delay Time	t_d		V_{CC} = 30			4		0.4[f]	–	–	–	40	–	40	ns
Rise Time *(See Fig. 24, 25, & 26)*	t_r					4		0.4[f]	–	–	–	400	–	400	ns
Sat. Switching Storage Time *(See Fig. 24, 25, & 27)*	t_s		V_{CC} = 30			4		−0.4[g]	–	–	–	800	–	800	ns
Sat. Switching Fall Time *(See Fig. 24, 25, & 28)*	t_f		V_{CC} = 30			4		−0.4[g]	–	–	–	400	–	400	ns
Thermal Resistance (Junction-to-Case)	θ_{J-C}								5 Max. 2N3878		–	5	–	5	°C/W
(Junction-to-Free Air)	θ_{J-FA}								30 Max. 40375		–	–	–	–	°C/W

CIRCUIT USED TO MEASURE SUSTAINING VOLTAGES $V_{CEO}(sus)$ & $V_{CER}(sus)$ FOR TYPES 2N3878, 2N3879, & 2N5202

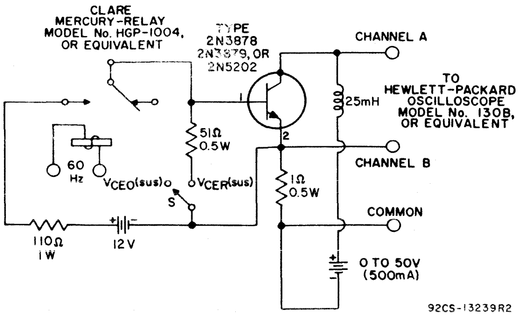
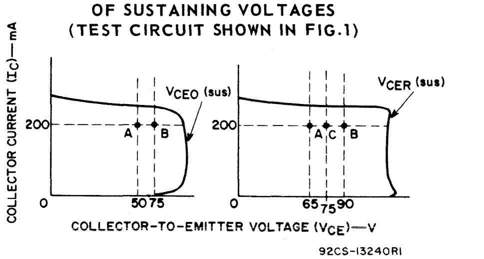


Fig. 1

OSCILLOSCOPE DISPLAY FOR MEASUREMENT OF SUSTAINING VOLTAGES (TEST CIRCUIT SHOWN IN FIG.1)



The sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$ are acceptable when the traces fall to the right and above point "A" for type 2N3878; and point "B" for type 2N3879. The sustaining voltage $V_{CER}(sus)$ is acceptable when the trace falls to the right and above point "C" for type 2N5202.

Fig. 2

SUSTAINING VOLTAGE vs. BASE-TO-EMITTER RESISTANCE FOR TYPES 2N3878 & 2N3879

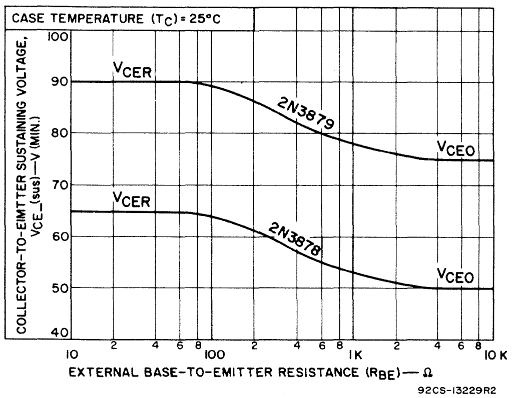


Fig. 3

DISSIPATION DERATING CURVE FOR TYPES 2N3878, 2N3879, & 2N5202

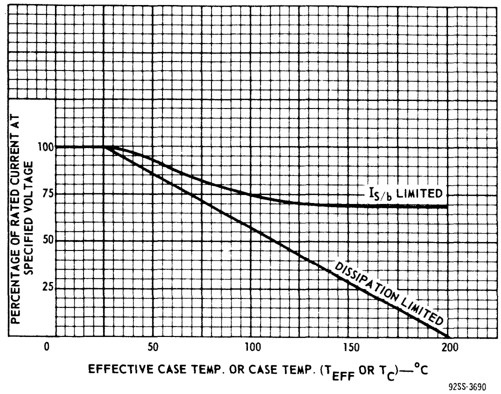


Fig. 4

FOOTNOTES (For Table of Electrical Characteristics)

[a] CAUTION: The sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$ MUST NOT be measured on a curve tracer. These sustaining voltages should be measured by means of the test circuit shown in *Fig.1*.

[b] Safe-operating region for forward- and reverse-bias operation is explained on pages 4 and 8.

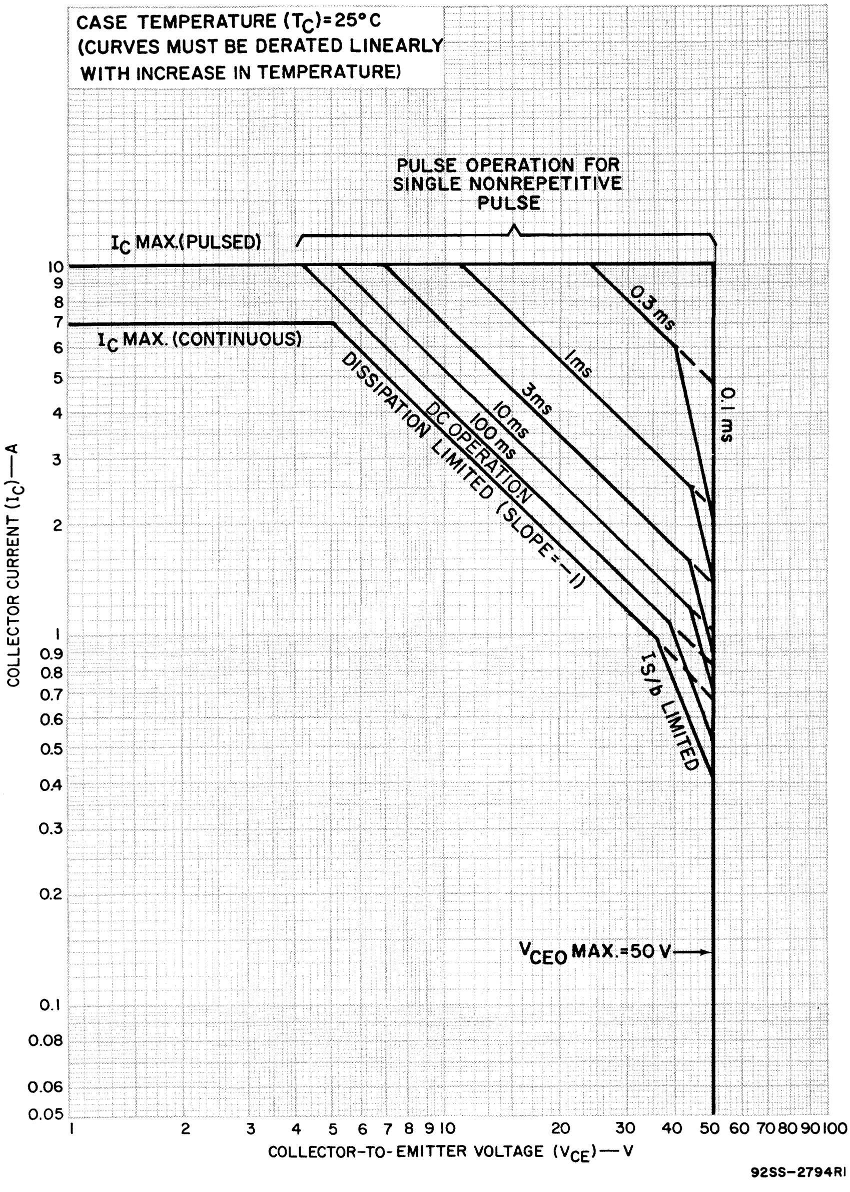
[c] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward biased for transistor operation in the active region.

[d] Pulsed; 1-s, non-repetitive pulse.

[e] $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse bias conditions. $E_{S/b} = 1/2LI^2$. where L is a series load or leakage inductance and I is the peak collector current.

[f] I_{B1} value (turn-on base current).

[g] I_{B2} value (turn-off base current).



CASE TEMPERATURE (T_C)=25°C
(CURVES MUST BE DERATED LINEARLY
WITH INCREASE IN TEMPERATURE)
PULSE OPERATION FOR SINGLE NONREPETITIVE PULSE
I_C MAX.(PULSED)
I_C MAX. (CONTINUOUS)
0.3 ms
1ms
3ms
10 ms
100 ms
DC OPERATION
DISSIPATION LIMITED (SLOPE=−1)
0.1 ms
IS/b LIMITED
V_{CEO} MAX.=50 V
COLLECTOR CURRENT (I_C)—A
COLLECTOR-TO-EMITTER VOLTAGE (V_{CE})—V
92SS-2794R1

Fig. 5

MAXIMUM OPERATING AREAS FOR TYPES 2N3879 & 2N5202

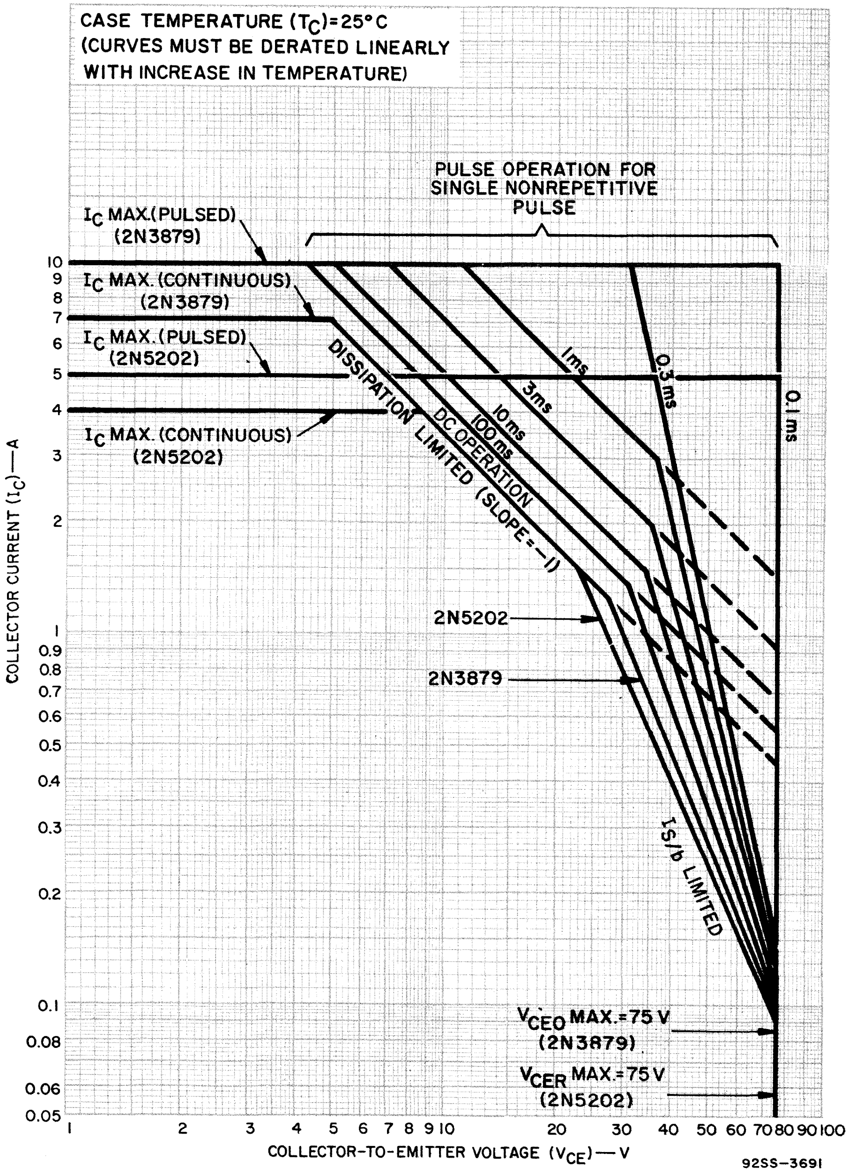


Fig. 6

MAXIMUM OPERATING AREAS FOR TYPE 40375

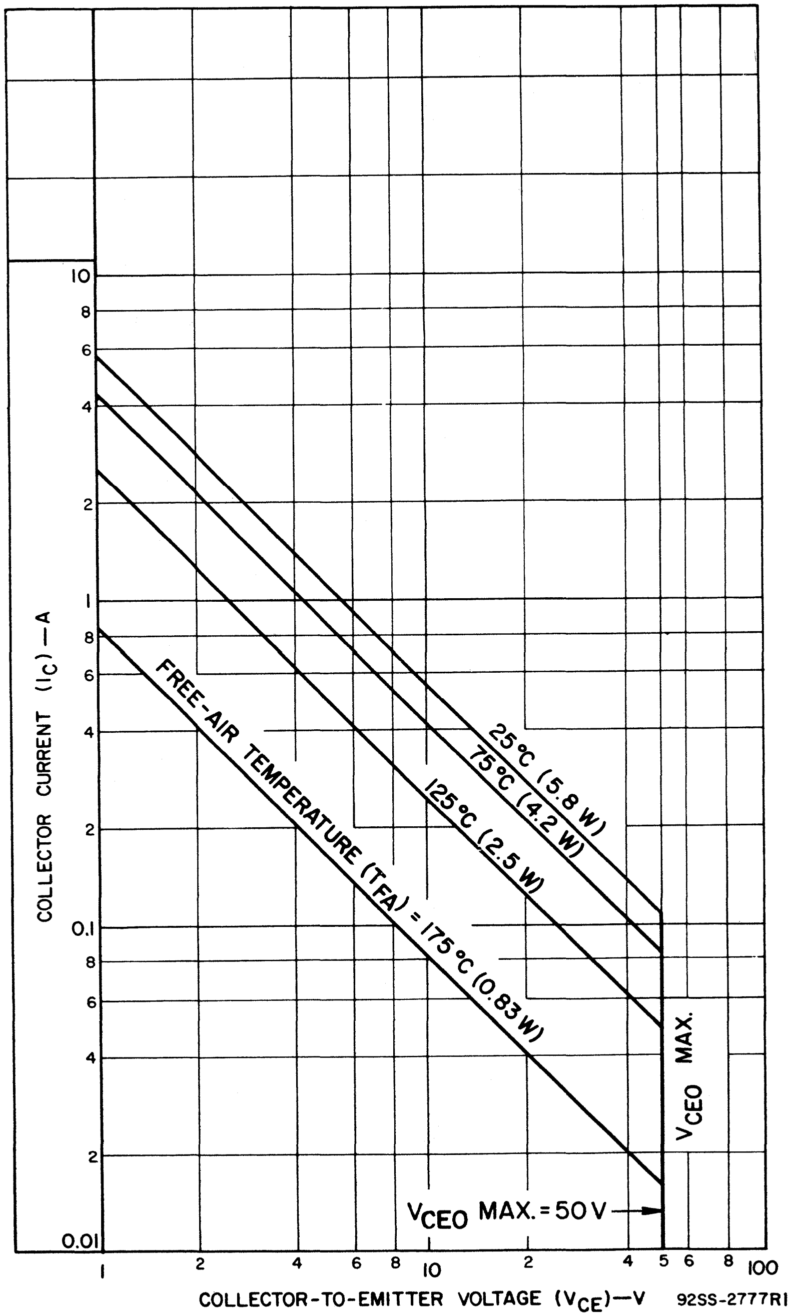


Fig. 7

REVERSE-BIAS OPERATION

The energy required to induce second breakdown when the transistor is turned off depends on the current during the "on" condition, the emitter-to-base voltage and resistance when the transistor is turned off, and the amount of inductance in series with the collector. The curves shown in *Fig. 8, 9, 10* (2N3878, 2N3879) or *Fig. 11, 12, 13* (2N5202) should prove useful in the design of circuits having inductive loads (such as solenoid- or relay-control circuits, magnetic-amplifier and -deflection circuits, and switching regulators) without protective zener diodes across the collector-to-emitter terminals. Also, these curves can be used when designing circuits where some leakage inductance is present (such as in inverters, converters, and transformer-coupled power amplifiers.)

In general, reverse-bias, second breakdown energy ($E_{S/b}$) capability increases with a decrease in inductance. Therefore, the allowable energy shown in the above-mentioned curves (calculated from $E_{S/b} = 1/2LI^2$, where L is a series load or leakage inductance and I is the peak collector current from the curves) will be conservative for smaller inductive loads. For further information on second breakdown, consult RCA "Silicon Power Circuits Manual" Form No. (SP-50) and SMA-30, "Second Breakdown in Transistors Under Conditions of Cut-off."

REVERSE-BIAS, SECOND-BREAKDOWN CHARACTERISTICS FOR TYPES 2N3878 & 2N3879

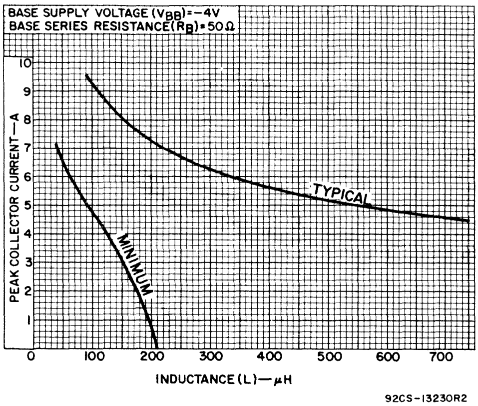


Fig. 8

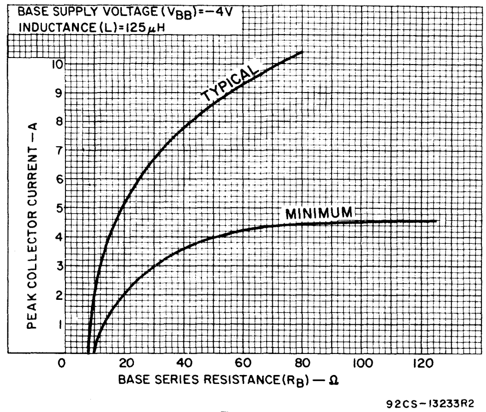


Fig. 9

REVERSE-BIAS, SECOND-BREAKDOWN CHARACTERISTICS FOR TYPES 2N3878 & 2N3879

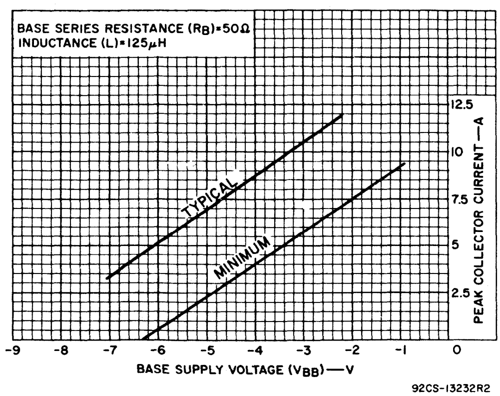


Fig. 10

REVERSE-BIAS, SECOND-BREAKDOWN CHARACTERISTICS FOR TYPE 2N5202

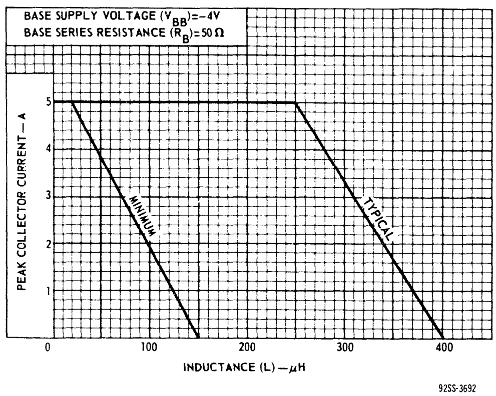


Fig. 11

REVERSE-BIAS, SECOND-BREAKDOWN CHARACTERISTICS FOR TYPE 2N5202

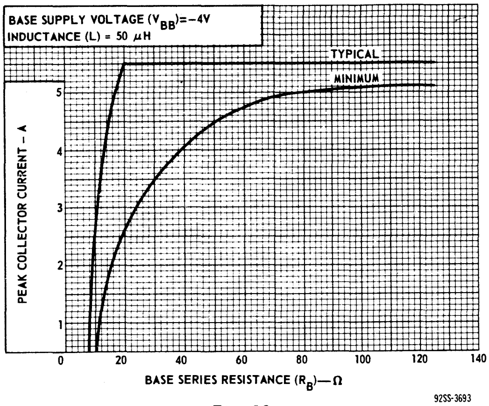


Fig. 12

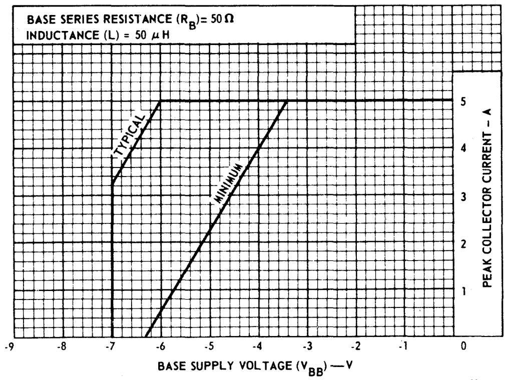


Fig. 13

TYPICAL DC BETA FOR TYPES 2N3878 & 2N3879

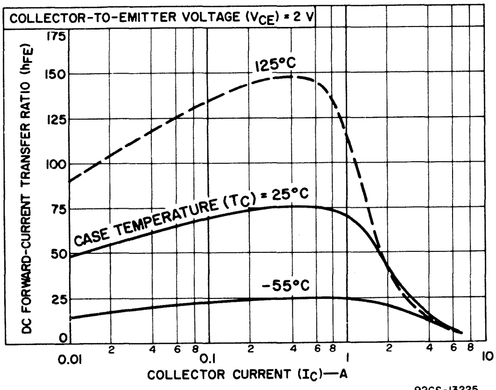


Fig. 14

TYPICAL DC BETA FOR TYPES 2N3878 & 2N3879

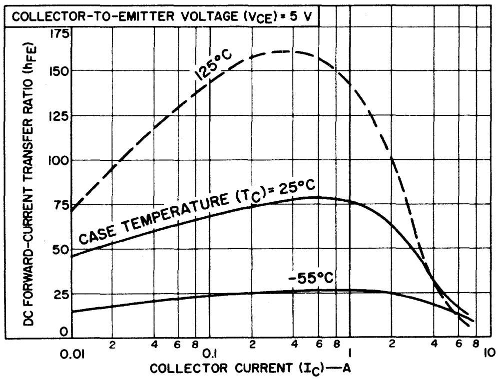


Fig. 15

TYPICAL DC BETA FOR TYPE 2N5202

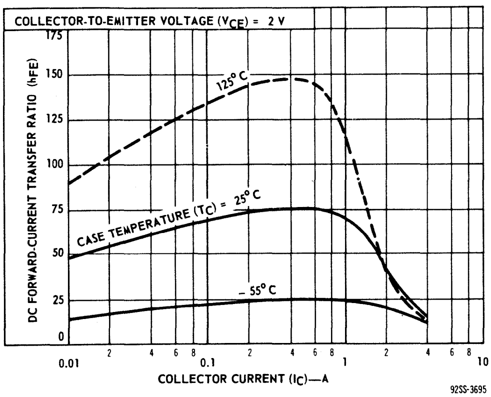


Fig. 16

TYPICAL DC BETA FOR TYPE 2N5202

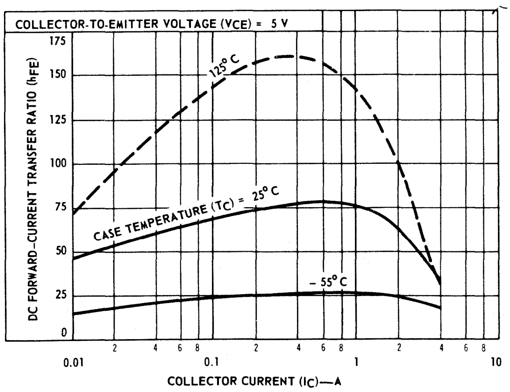


Fig. 17

TYPICAL INPUT CHARACTERISTICS FOR TYPES 2N3878, 2N3879, & 2N5202

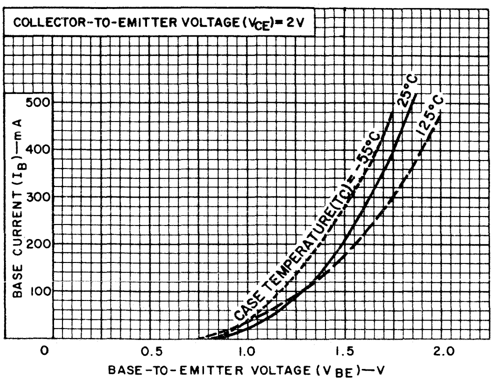


Fig. 18

TYPICAL OUTPUT CHARACTERISTICS FOR TYPES 2N3878, 2N3879, & 2N5202

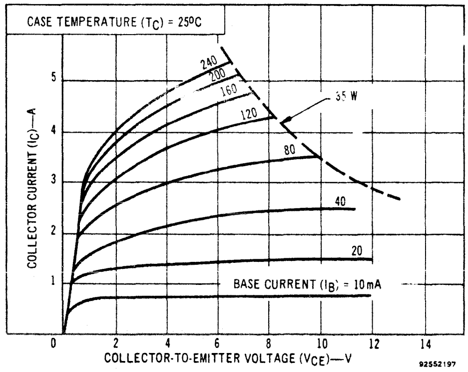


Fig. 19

TYPICAL TRANSFER CHARACTERISTICS FOR TYPES 2N3878, 2N3879, & 2N5202

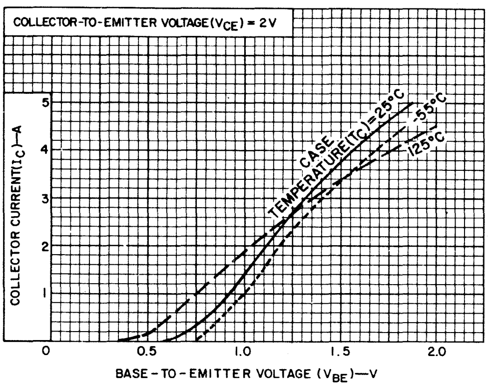


Fig. 20

TYPICAL GAIN-BANDWIDTH PRODUCT FOR TYPES 2N3878, 2N3879, & 2N5202

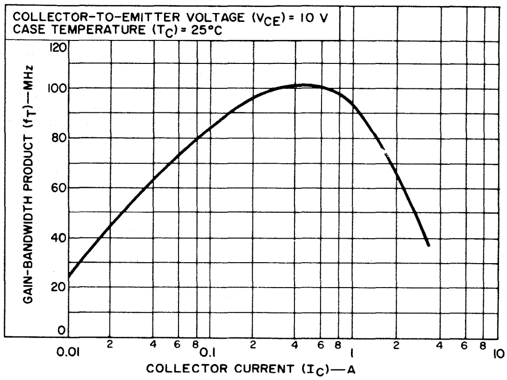


Fig. 21

TYPICAL SATURATION VOLTAGE CHARACTERISTICS FOR TYPES 2N3878 & 2N3879

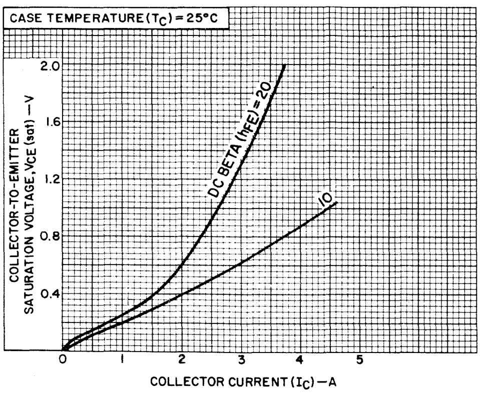


Fig. 22

TYPICAL SATURATION VOLTAGE CHARACTERISTICS FOR TYPE 2N5202

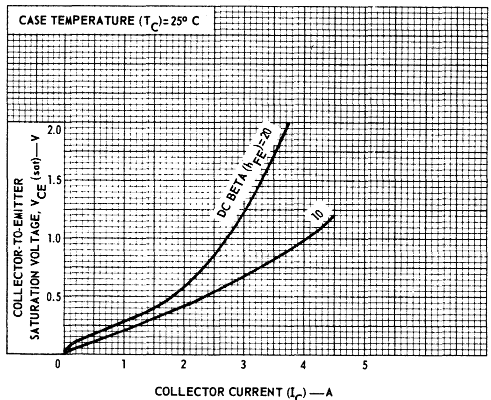
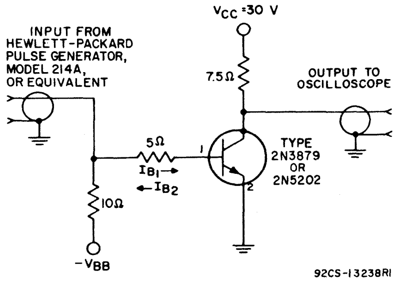


Fig. 23

CIRCUIT USED TO MEASURE SWITCHING TIMES FOR TYPES 2N3879 & 2N5202



INPUT PULSE:

Pulse rep. rate = 1,000 pulses/s
Pulse width = 20 μs

Fig. 24

OSCILLOSCOPE DISPLAY FOR MEASUREMENT OF SWITCHING TIMES (TEST CIRCUIT SHOWN IN FIG.24)

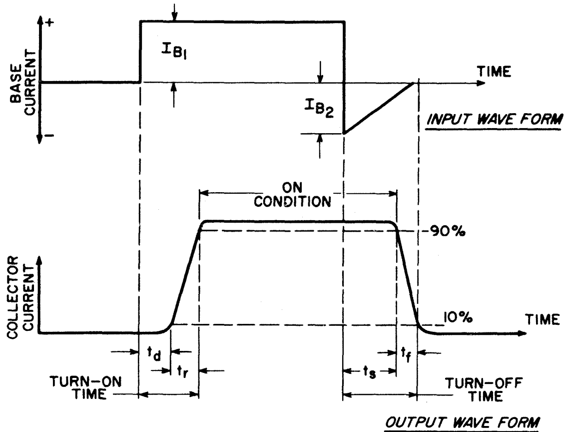


Fig. 25

92CS-12874

TYPICAL TURN-ON TIME FOR TYPES 2N3879 & 2N5202

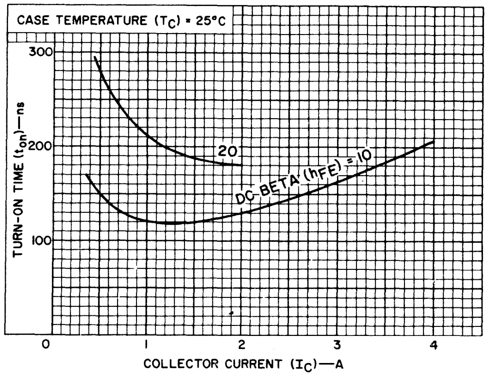


Fig. 26

TYPICAL STORAGE-TIME FOR TYPES 2N3879 & 2N5202

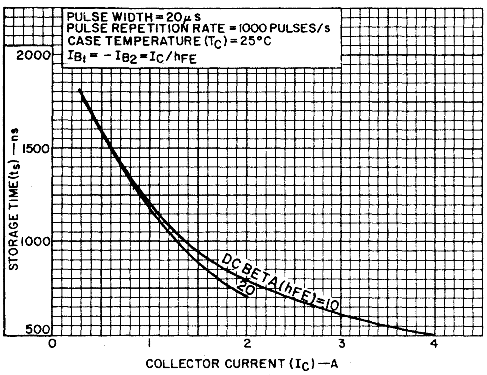


Fig. 27

92CS-13237

TYPICAL FALL-TIME FOR TYPES 2N3879 & 2N5202

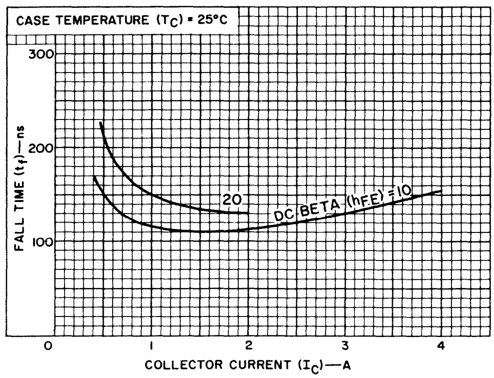
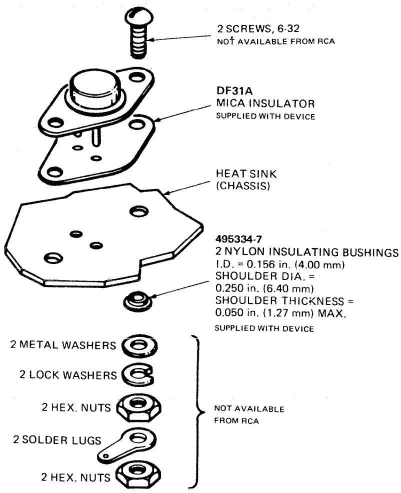


Fig. 28

92CS-13235

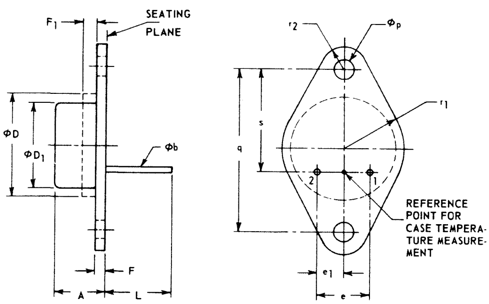


In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.24 – Suggested mounting hardware for types 2N3878, 2N3879, and 2N5202.

DIMENSIONAL OUTLINE FOR TYPES 2N3878, 2N3879, AND 2N5202

JEDEC TO-66



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	0.250	0.340	6.35	8.64	
ϕb	0.028	0.034	0.711	0.863	
ϕD	—	0.620	—	15.75	
ϕD_1	0.470	0.500	11.94	12.70	
e	0.190	0.210	4.83	5.33	
e_1	0.093	0.107	2.36	2.72	
F	0.050	0.075	1.27	1.91	2
F_1	—	0.050	—	1.27	1
L	0.360	—	9.14	—	
ϕp	0.142	0.152	3.61	3.86	
q	0.958	0.962	24.33	24.43	
r_1	—	0.350	—	8.89	
r_2	—	0.145	—	3.68	
s	0.570	0.590	14.48	14.99	

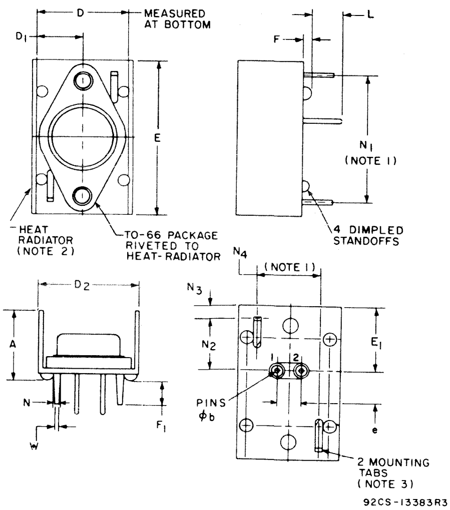
NOTES:
1. The outline contour is optional within zone defined by ϕD and F_1.
2. Dimension does not include sealing flange.

92SS 3738

TERMINAL CONNECTIONS FOR TYPES 2N3878, 2N3879, and 2N5202

Pin 1 - Base
Pin 2 - Emitter
Case, Mounting Flange - Collector

DIMENSIONAL OUTLINE FOR TYPE 40375 JEDEC TO-66 WITH HEAT RADIATOR



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A		0.616		15.64	
ϕb	0.028	0.034	0.711	0.864	
D	0.750	0.760	19.05	19.30	
D_1	0.375	0.380	9.52	9.65	
D_2	0.820	0.920	20.83	23.37	
E	1.297	1.327	32.94	33.70	
E_1	0.551	0.561	13.99	14.25	
e	0.190	0.210	4.83	5.33	
F	0.30	0.55	7.62	13.97	
F_1	0.175	0.210	4.44	5.33	
L	0.170		4.31		
N	0.052	0.065	1.32	1.65	
N_1	1.098	1.102	27.89	27.99	1
N_2	0.448	0.452	11.38	11.47	
N_3	0.099	0.113	0.25	0.29	
N_4	0.498	0.502	12.65	12.75	
W	0.048	0.060	1.22	1.52	

NOTES:
1. Measured at bottom of heat radiator.
2. 0.035 in. (0.889 mm) C.R.S., tin plated.
3. Recommended hole size for printed-circuit board is 0.070 in. (1.778 mm) dia.

TERMINAL CONNECTIONS FOR TYPE 40375

Pin 1 - Base
Pin 2 - Emitter
Heat-Radiator - Collector

Solid State Division

Power Transistors

2N6479 2N6481 2N6480 2N6482

(RADIAL)

H-1354

Radiation-Hardened Silicon N-P-N Power Transistors

Epitaxial-Planar Types for Aerospace and Military Applications

Rated for Operation in Radiation Environments with Cumulative Neutron Fluence Levels to 1 x 10^{14} Neutrons/cm^2 and Gamma Intensity to 1 x 10^8 Rad(Si)/s

RCA types 2N6479, 2N6480, 2N6481, and 2N6482● are epitaxial silicon n-p-n planar power-switching transistors. They are designed for aerospace applications in which they might be subjected to extreme neutron and gamma-ray exposure.

The 2N6479, 2N6480, 2N6481, and 2N6482 are intended for use in 5-to-10 ampere high-frequency power inverter service. Types 2N6479 and 2N6481 differ from types 2N6480 and 2N6482, respectively, in voltage and power ratings. In types 2N6479 and 2N6480, the collector is isolated from the case.

● Formerly RCA Dev. Nos. TA8007, TA8007B, TA8100, and TA8100B, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N6479 2N6481	2N6480 2N6482	
* COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	100	100	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:				
* With external base-to-emitter resistance (R_{BE}) ≤ 100 Ω	$V_{CER}(sus)$	80	100	V
With base open	$V_{CEO}(sus)$	60	80	V
* EMITTER-TO-BASE VOLTAGE	V_{EBO}	6	6	V
* CONTINUOUS COLLECTOR CURRENT	I_C	12	12	A
* PEAK COLLECTOR CURRENT		25	25	A
* CONTINUOUS BASE CURRENT	I_B	5	5	A
* TRANSISTOR DISSIPATION:	P_T			
At case temperatures up to 25°C		87	117	W
At case temperatures above 25°C		See Figs. 1,2, and 4		
* TEMPERATURE RANGE:				
Storage and Operating (Junction)		−65 to +200		°C
* TERMINAL TEMPERATURE (During Soldering):				
At distance ≥ 1/32 in. (0.8 mm) from seating plane for 10 s max.		230		°C

* In accordance with JEDEC registration data format JS-6 RDF-1.

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C*
PRE-RADIATION

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: VOLTAGE V dc: V_{CB}	V_{CE}	V_{EB}	CURRENT A dc: I_E	I_B	I_C	LIMITS 2N6479 2N6481 MIN.	MAX.	LIMITS 2N6480 2N6482 MIN.	MAX.	UNITS
Collector Cutoff Current: With emitter open	I_{CBO}	100						–	1	–	1	mA
With base shorted	I_{CES}		60					–	200	–	200	μA
* With base-emitter junction reverse-biased	I_{CEV}		100	0				–	1	–	1	mA
* At T_C = 100°C			60	0				–	1	–	1	
* Emitter Cutoff Current	I_{EBO}			6				–	2	–	2	mA
Emitter-to-Base Voltage	V_{EBO}				0.002			6	–	6	–	V
* Collector-to-Emitter Sustaining Voltage: With base open	$V_{CEO}(sus)^b$						0.2^a	60	–	80	–	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)^b$						0.2^b	80	–	100	–	
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					1.2	12^a	–	0.75	–	0.75	V
* Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$					1.2	12^a	–	1.5	–	1.5	V
* DC Forward Current Transfer Ratio	h_{FE}		2				12^a	20	300	20	300	
Second Breakdown Collector Current: With base forward-biased, t = 1 s	$I_{S/b}$▲		12					7.3	–	7.3	–	A
								2N6479 2N6481		2N6481 2N6482		
Second Breakdown Energy With base reverse-biased, R_{BE} = 100 Ω, L = 100 μH	$E_{S/b}$**						5	1.25	–	1.25	–	mJ
* Saturated Switching Time (See Figs. 15 and 16): Rise	t_r		V_{CC} = 30			1.2^c	12	–	400	–	400	ns
Storage	t_s					1.2^c	12	–	800	–	800	
Fall	t_f					1.2^c	12	–	200	–	200	
* Magnitude of Common Emitter Small-Signal Short Circuit Forward Current Transfer Ratio (f = 10 MHz)	$\|h_{fe}\|$		5				1	10	–	10	–	
Collector-to-Base Feedback Capacitance (f = 1 MHz)	C_{ob}	10			0			–	400	–	400	pF
								2N6479 2N6480		2N6481 2N6482		
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$		10				5	–	2	–	1.5	°C/W

* In accordance with JEDEC registration data format JS-6 RDF-1.
a Pulsed; pulse duration ≤ 350 μs, duty factor ≤ 2%.
b CAUTION: The sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$ MUST NOT be measured on a curve tracer. These sustaining voltages should be measured by means of the test circuit shown in Fig.13.
▲ $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage.
** $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse-bias conditions. $E_{S/b} = 1/2LI^2$, where L is a series load or leakage inductance and I is the collector current.
c $I_{B_1} = I_{B_2}$

POST-NEUTRON-RADIATION ELECTRICAL CHARACTERISTICS AFTER EXPOSURE TO 5 x 10^{13} NEUTRONS/cm^2 (1 MeV equiv.), *At Case Temperature (T_C) = 25°C*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS		UNITS
		VOLTAGE V dc			CURRENT A dc		For all Types		
		V_{CE}	V_{BE}	V_{EB}	I_C	I_B	MIN.	MAX.	
* Collector Cutoff Current: With base-emitter junction reverse-biased	I_{CEV}	100	0				–	1.2	mA
* Emitter Cutoff Current	I_{EBO}			5			–	2.2	mA
* Collector-to-Emitter Sustaining Voltage: With base open	$V_{CEO}(sus)$				0.2 0.2	0.05 0.05	80[b] 60[c]	– –	V
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				7[a]	1.4	–	1.5	V
* Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$				7[a]	1.4	–	1.5	V
* DC Forward Current Transfer Ratio	h_{FE}	5			7[a]		12	–	
Magnitude of Common Emitter, Small-Signal Short Circuit Forward Current Transfer Ratio (f = 10 MHz)	$\|h_{fe}\|$	5			1		10	–	
* Damage Constant	K▲						–	9×10^{-16}	

* In accordance with JEDEC registration data format JS-6 RDF-1.

a Pulsed; pulse duration ≤ 350 μs, duty factor ≤ 2%.

b For types 2N6480, 2N6482.

c For types 2N6479, 2N6481.

▲Damage constant $K = \dfrac{\dfrac{1}{h_{FE_2}} - \dfrac{1}{h_{FE_1}}}{\phi}$

Where h_{FE_1} = Beta prior to exposure

h_{FE_2} = Beta after exposure

ϕ = Neutron fluence (1 MeV equiv.)

Knowing K, h_{FE_2} may be calculated for other fluences using the relationship:

$$h_{FE_2} = \frac{1}{K\phi + \dfrac{1}{h_{FE_1}}}$$

TYPICAL CHARACTERISTIC DURING GAMMA EXPOSURE FOR DOSE RATES OF LESS THAN 1 x 10^8 RAD(Si)/sec

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS	UNITS
		VOLTAGE – V dc		For all Types	
		V_{CB}	V_{BE}	TYPICAL	
Collector-to-Base Charge Generation Constant	(C)	20	0	5×10^{-8}	Coulomb/Rad

The charge generated in the depletion region of a transistor is proportional to the volume of the depletion region, the total dose, and the energy of the gamma radiation.

The primary base-collector photo current $[I_{pp(base)}]$ = $(C)\dot{\gamma}$, where $\dot{\gamma}$ is the gamma dose rate in Rad(Si)/s.

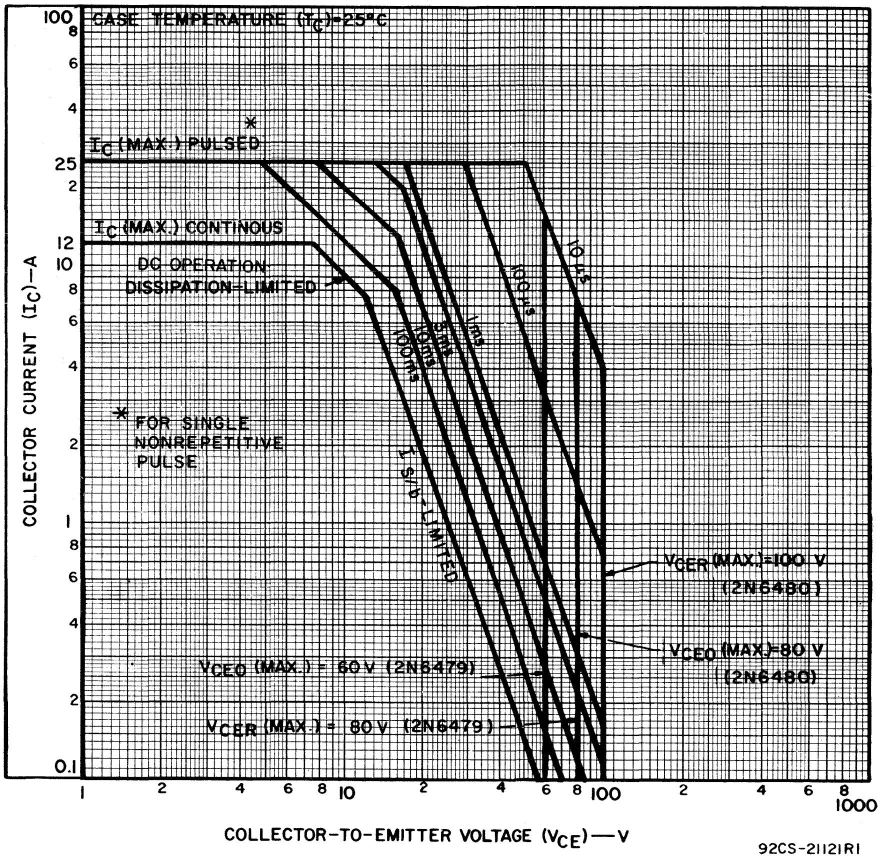


Fig. 1 — Maximum operating areas for 2N6479 and 2N6480.

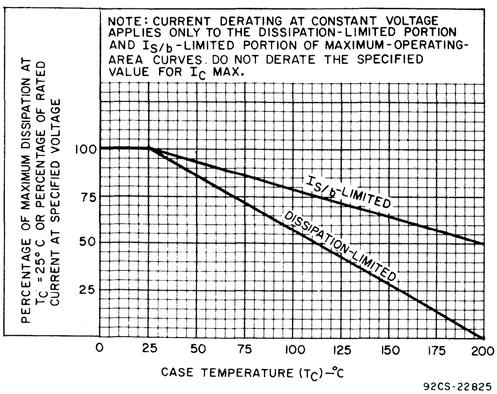


Fig.2 — Derating curves for all types.

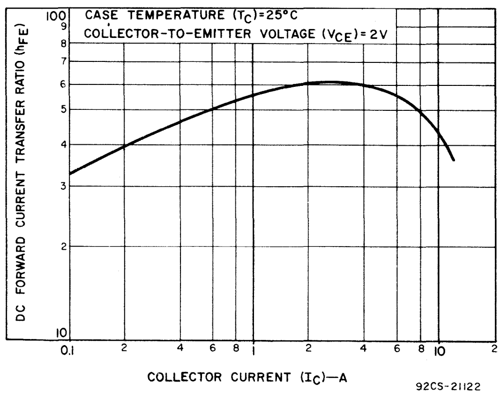


Fig.3 — Typical dc beta characteristic for all types.

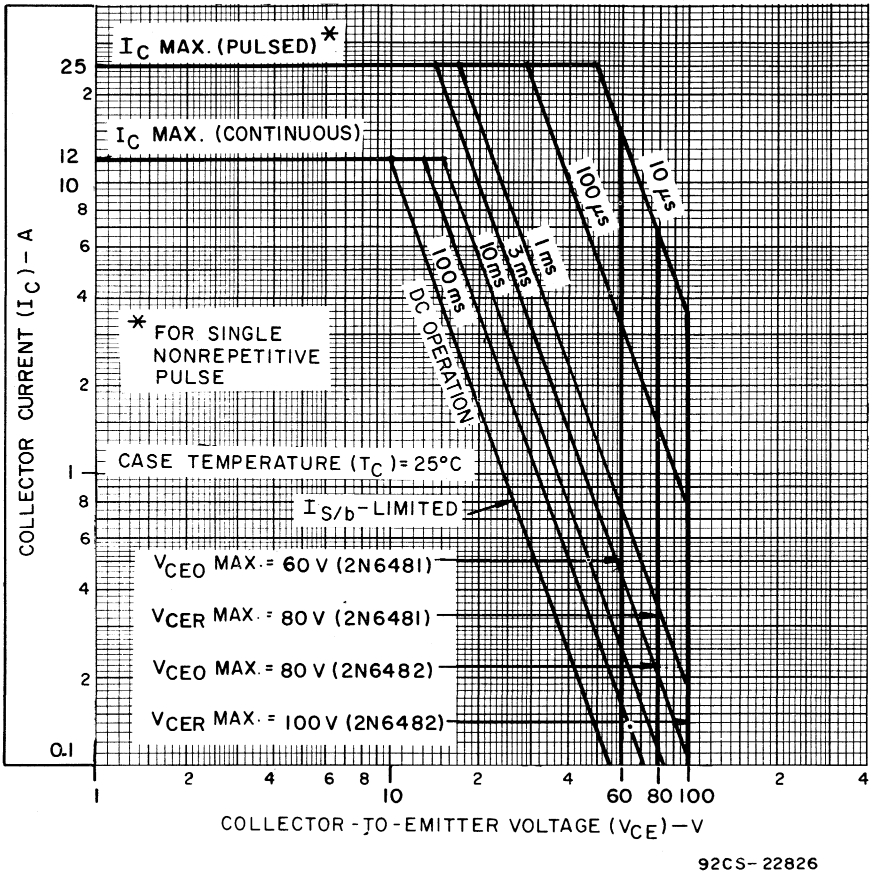


Fig.4 — Maximum operating areas for 2N6481 and 2N6482.

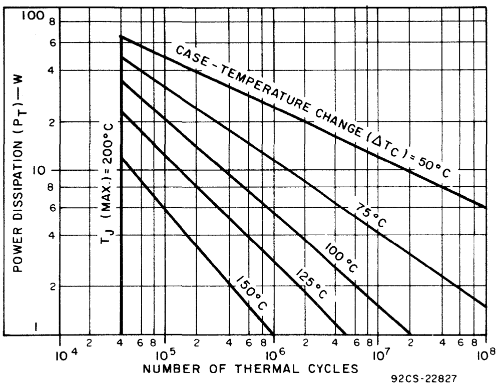


Fig.5 — Thermal-cycling rating chart for 2N6479 and 2N6480.

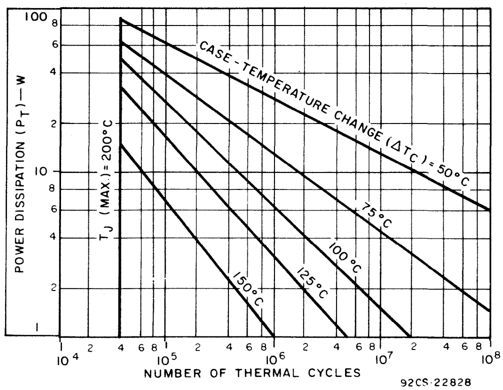


Fig.6 — Thermal-cycling rating chart for 2N6481 and 2N6482.

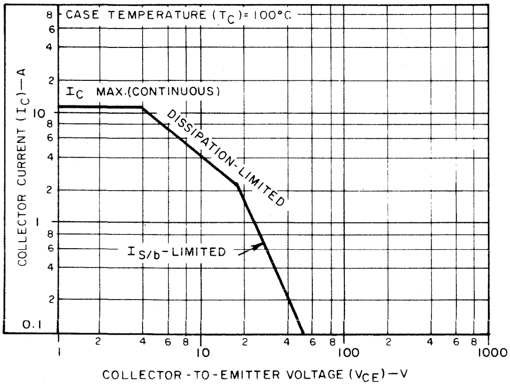


Fig.7 — Maximum operating area for 2N6479 and 2N6480 at 100°C case temperature.

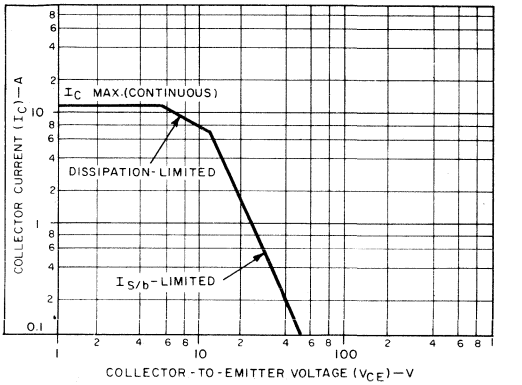


Fig.8 — Maximum operating area for 2N6481 and 2N6482 at 100°C case temperature.

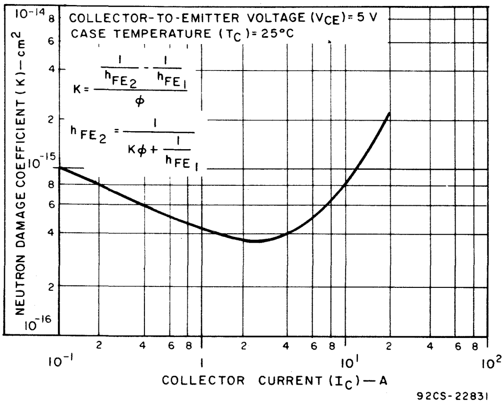


Fig.9 — Typical 1-MeV-equivalent neutron damage coefficient as a function of collector current for all types.

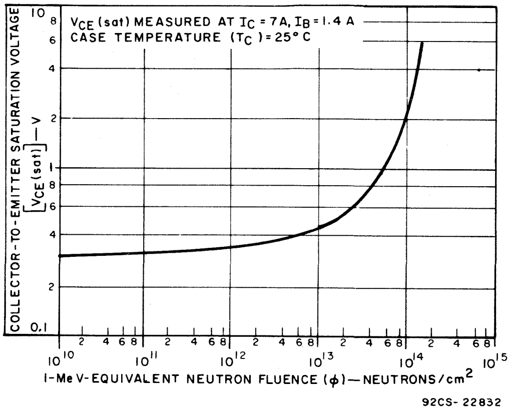


Fig.10 — Typical collector-to-emitter saturation voltage as a function of 1-MeV-equivalent neutron fluence for all types.

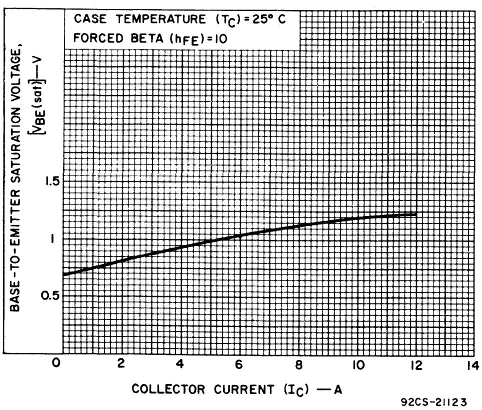


Fig.11 — Typical base-to-emitter saturation voltage characteristic for all types.

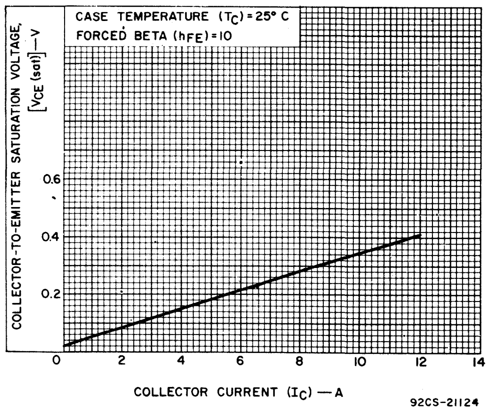


Fig.12 — Typical collector-to-emitter saturation voltage characteristic for all types.

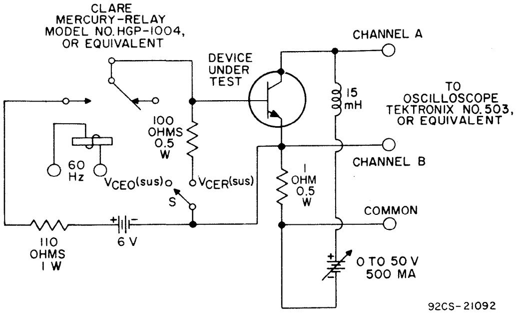
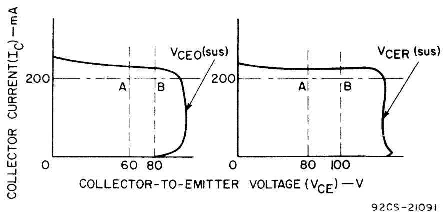


Fig.13 – Circuit used to measure sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$.



The sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$ are acceptable when the traces fall to the right of point "A" for types 2N6479 and 2N6481. The traces must fall to the right of point "B" for 2N6480 and 2N6482.

Fig.14 – Oscilloscope display for $V_{CEO}(sus)$ and $V_{CER}(sus)$ measurement. (Test circuit shown in Fig.13).

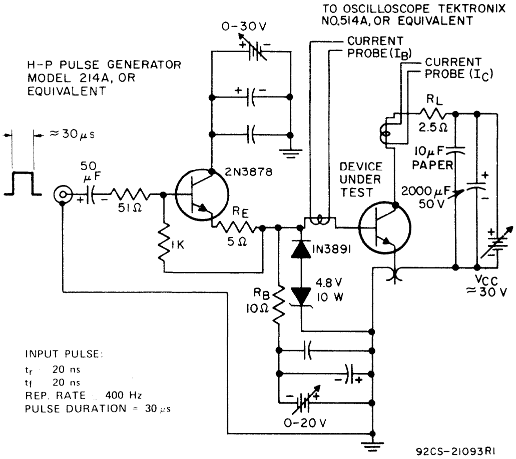


Fig.15 – Circuit used to measure saturated switching times.

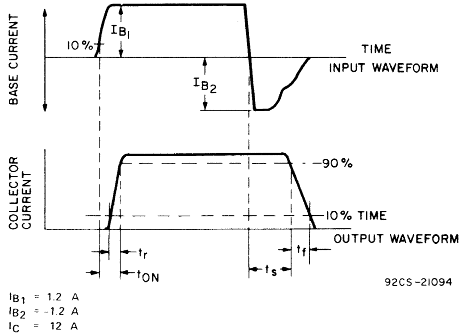
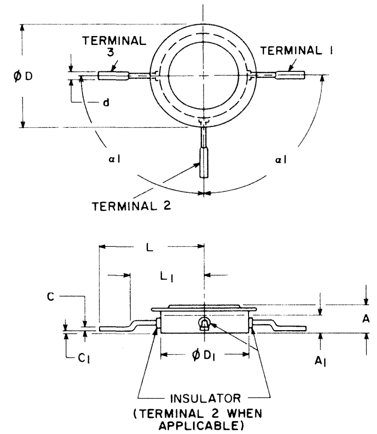


Fig.16 – Phase relationship between input and output currents showing reference points for specification of switching times. (Test circuit shown in Fig.15).

DIMENSIONAL OUTLINE (Radial Package)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	0.210	–	5.08	
A_1	–	0.125	–	3.17	1
C	0.015	0.019	0.38	0.48	
C_1	–	0.015	–	0.38	
ϕD	–	0.710	–	18.03	
$ϕD_1$	0.615	0.690	15.62	17.52	1
d	0.042	0.046	1.06	1.16	
L	–	0.705	–	17.90	
L_1	–	0.510	–	12.95	
α_1	90° ± 2°		90° ± 2°		

NOTE:
1. CONTROLLED AREA OF THE DIAMETER DOES NOT INCLUDE THE BRAZED AREA AROUND THE CERAMIC AND TERMINAL 2.

92CS-21090

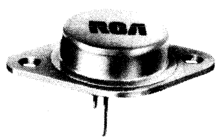
TERMINAL CONNECTIONS

	2N6479 2N6480	2N6481 2N6482
Terminal No. 1	– Base	Base
Terminal No. 2	– Collector	Collector, Case
Terminal No. 3	– Emitter	Emitter

RCA

Solid State Division

Power Transistors
2N5038
2N5039
2N6496



JEDEC TO-3 H-1570

High-Current, High-Power, High-Speed Silicon N-P-N Power Transistors

Devices for Switching and Amplifier Circuits in Industrial and Commercial Applications

Features:

- **Maximum operating area curves for dc and pulse operation**
- **$I_{S/b}$-limit line beginning at 28 V**
- **High collector current ratings**
- **High-dissipation capability**

RCA-2N5038, 2N5039, and 2N6496 are epitaxial silicon n-p-n power transistors. They differ in breakdown-voltage ratings, leakage-current, and dc-beta values.

The high current-handling capability of these transistors in conjunction with fast switching speeds make these devices especially suited for switching-control amplifiers, power gates, switching regulators, converters, and inverters. Other recommended applications include dc-rf amplifiers and power oscillators. These transistors are supplied in the JEDEC TO-3 package.

- **Switching Time:**

Switching Time	Measured at:
t_r = 0.5 μs max.	12 A (2N5038)
t_s = 1.5 μs max.	10 A (2N5039)
t_f = 0.5 μs max.	8 A (2N6496)

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N5038	2N5039	2N6496	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	150	120	150	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:					
With – 1.5 volts (V_{BE}) of reverse bias and external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CEX}(sus)	150	120	–	V
With $R_{BE} \leq 50$ Ω	V_{CER}(sus)	110	95	130	V
With base open	V_{CEO}(sus)	90	75	110	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	7	7	7	V
*CONTINUOUS COLLECTOR CURRENT	I_C	20	20	15	A
*PEAK COLLECTOR CURRENT		30	30	–	A
*CONTINUOUS BASE CURRENT	I_B	5	5	5	A
*TRANSISTOR DISSIPATION:	P_T				
At case temperatures up to 25°C and V_{CE} up to 28 V		140	140	140	W
At case temperature of 100°C and V_{CB} of 20 V		80	80	80	W
At case temperatures up to 25°C and V_{CE} above 28 V		← See Fig. 1. →			
At case temperatures above 25°C and V_{CE} above 28 V		← See Figs. 1 & 2. →			
*TEMPERATURE RANGE:					
Storage & Operating (Junction)		← –65 to 200 →			°C
PIN TEMPERATURE (During Soldering)					
At distances ≥ 1/32 in. (0.8 mm) from seating plane for 10 s max.		← 230 →			°C

*In accordance with JEDEC registration data format (JS-6, RDF-1)

11-73

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: VOLTAGE V dc				CURRENT A dc			LIMITS: 2N5038		2N5039		2N6496		UNITS
		V_{CB}	V_{CE}	V_{EB}	V_{BE}	I_C	I_E	I_B	Min.	Max.	Min.	Max.	Min.	Max.	
Collector Cutoff Current: With base open	I_{CEO}		55					0	–	–	–	20	–	–	mA
			70					0	–	20	–	–	–	–	
* With base-emitter junction reverse-biased	I_{CEV}		110		−1.5				–	–	–	50	–	–	
			140		−1.5				–	50	–	–	–	–	
			130		0				–	–	–	–	–	20	
* At T_C = 150°C			85		−1.5				–	–	–	10	–	–	
			100		−1.5				–	10	–	–	–	–	
			130		0				–	–	–	–	–	25	
* Emitter Cutoff Current	I_{EBO}			5		0			–	5	–	15	–	–	mA
				7		0			–	50	–	50	–	50	
DC Forward-Current Transfer Ratio	h_{FE}		5			2[a]			50	200	30	150	–	–	
*			5			10[a]			–	–	20	100	–	–	
*			5			12[a]			20	100	–	–	–	–	
*			2			8[a]			–	–	–	–	12	100	
* Magnitude of Small-Signal Forward-Current Transfer Ratio (At f = 5 MHz)	$\|h_{fe}\|$		10			2			12	–	12	–	12	–	
Collector-to-Emitter Sustaining Voltage: * With base open	$V_{CEO}(sus)$[b]					0.2		0	90	–	75	–	110	–	V
With base-emitter junction reverse biased and external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CEX}(sus)$[b]				−1.5	0.2		0	150	–	120	–	–	–	
With $R_{BE} \leqslant$ 50 Ω	$V_{CER}(sus)$[b]					0.2		0	110	–	95	–	130	–	
Emitter-to-Base Voltage	V_{EBO}					0	0.05		7	–	7	–	7	–	V
Base-to-Emitter Voltage	V_{BE}		5			10[a]			–	–	–	1.8	–	–	V
			5			12[a]			–	1.8	–	–	–	–	
			2			8[a]			–	–	–	–	–	1.6	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					10[a]		1.0	–	–	–	1.0	–	–	V
						12[a]		1.2	–	1.0	–	–	–	–	
*						20[a]		5	–	2.5	–	2.5	–	–	
*						8[a]		0.8	–	–	–	–	–	1.0	
* Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$					20[a]		5	–	3.3	–	3.3	–	–	V
						8[a]		0.8	–	–	–	–	–	2.0	
Output Capacitance	C_{ob}	10					0		–	300	–	300	–	300	pF
Second-Breakdown Collector Current[e] (With base forward biased)	$I_{S/b}$[d]		28						5.0	–	5.0	–	5.0	–	A
			45						0.9	–	0.9	–	0.9	–	
Second-Breakdown Energy (With base reverse biased, R_B = 20 Ω, L = 180 μH)	$E_{S/b}$[f]				−4	12			13	–	13	–	–	–	mJ
					−4	8			–	–	–	–	5.7	–	
* Sat. Switching Rise Time (See Figs. 24, 26, and 27.)	t_r	V_{CC} = 30 V				10		1.0[c]	–	–	–	0.5	–	–	μs
						12		1.2[c]	–	0.5	–	–	–	–	
						8		0.8[c]	–	–	–	–	–	0.5	
* Sat. Switching Storage Time (See Figs. 25, 26, and 27.)	t_s	V_{CC} = 30 V				10		1.0[c]	–	–	–	1.5	–	–	
						12		1.2[c]	–	1.5	–	–	–	–	
						8		0.8[c]	–	–	–	–	–	1.5	
* Sat. Switching Fall Time (See Figs. 24, 26, and 27.)	t_f	V_{CC} = 30 V				10		1.0[c]	–	–	–	0.5	–	–	
						12		1.2[c]	–	0.5	–	–	–	–	
						8		0.8[c]	–	–	–	–	–	0.5	
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$		10			10			–	1.25	–	1.25	–	1.25	°C/W

[a] Pulsed; pulse duration ≤350 μs, duty factor = 2%.

[b] CAUTION: The sustaining voltages $V_{CEO}(sus)$, $V_{CER}(sus)$, and $V_{CEX}(sus)$ MUST NOT be measured on a curve tracer. These sustaining voltages should be measured by means of the test circuit shown in Fig. 22.

[c] $I_{B1} = I_{B2}$ = value shown.

[d] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward-biased for transistor operation in the active region.

[e] Pulsed; 1-s non-repetitive pulse.

[f] $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse-bias conditions. $E_{S/b} = \frac{1}{2}LI^2$ where L is a series load or leakage inductance and I is the peak collector current.

*In accordance with JEDEC registration data format (JS-6, RDF-1)

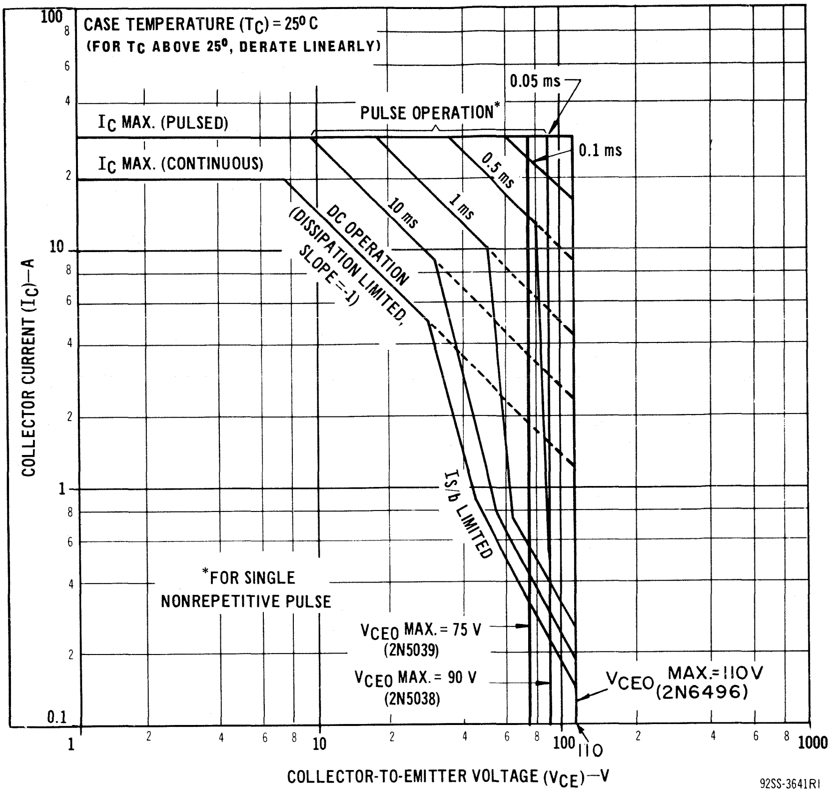


Fig. 1 — Maximum operating areas for all types.

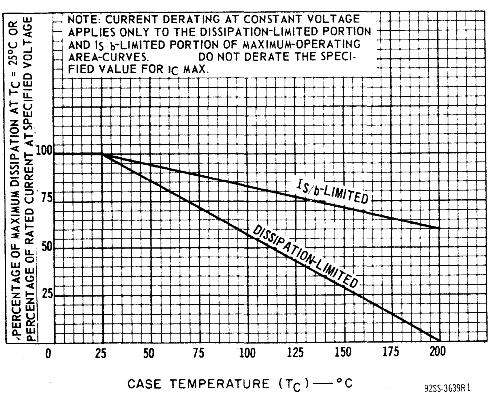


Fig. 2 — Dissipation derating curves for all types.

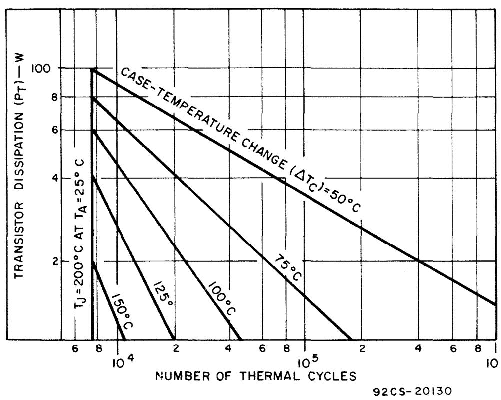


Fig. 3 — Thermal-cycling rating chart for all types.

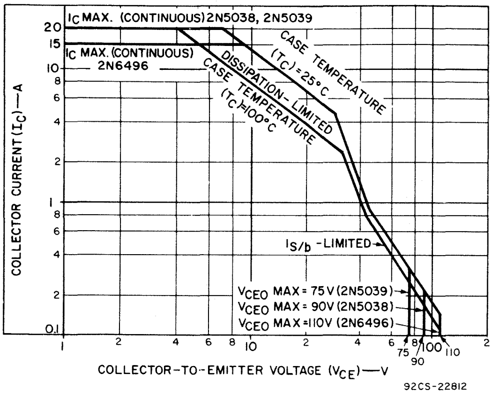


Fig. 4 — Maximum operating areas for all types.

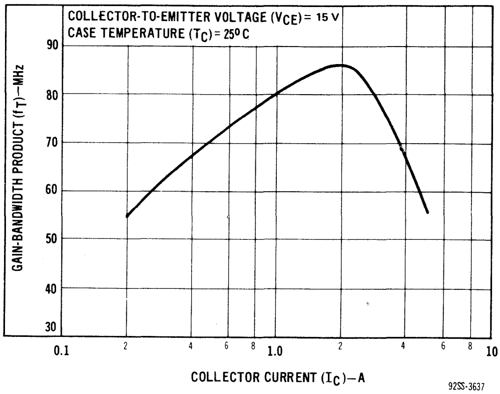


Fig. 5 — Typical gain-bandwidth product for all types.

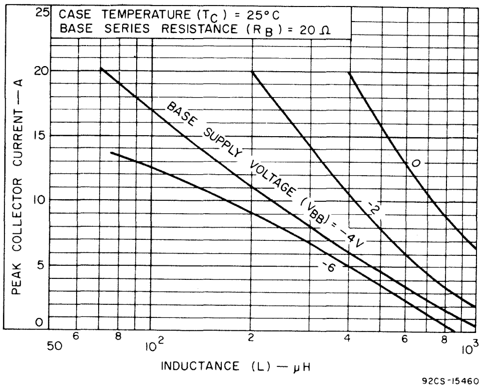


Fig. 6 — Maximum reverse-bias, second-breakdown characteristics for 2N5038 and 2N5039.

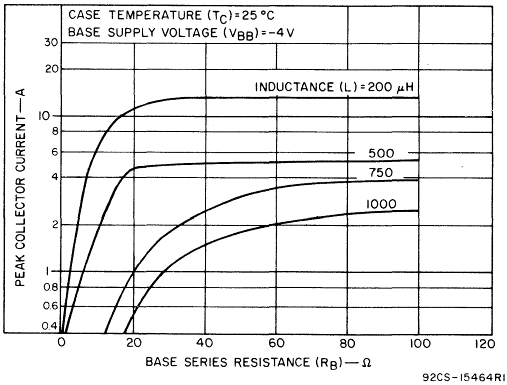


Fig. 7 — Maximum reverse-bias, second-breakdown characteristics for 2N5038 and 2N5039.

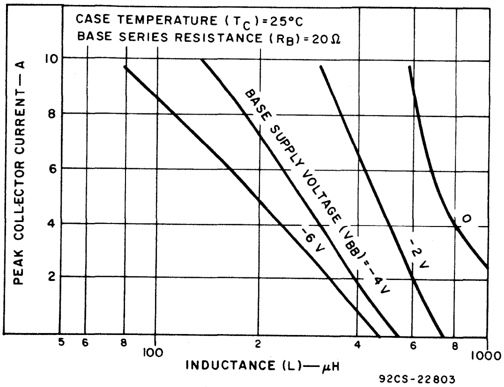


Fig. 8 — Maximum reverse-bias, second-breakdown characteristics for 2N6496.

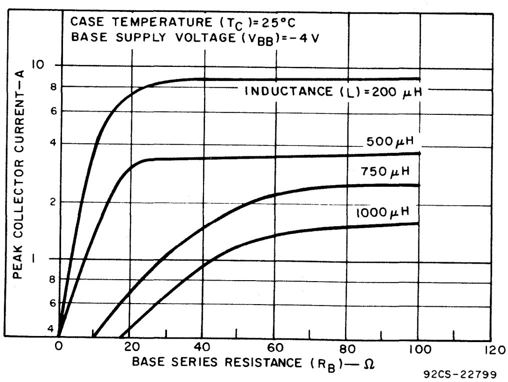


Fig. 9 — Maximum reverse-bias, second-breakdown characteristics for 2N6496.

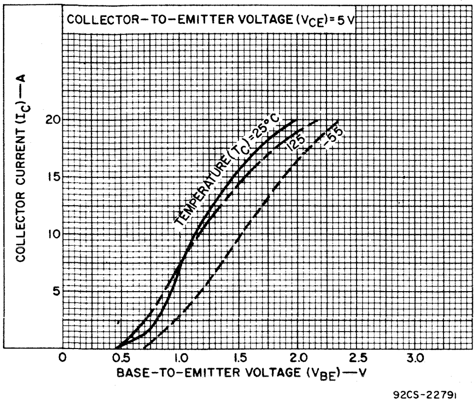


Fig. 10 — Typical transfer characteristics for 2N5038.

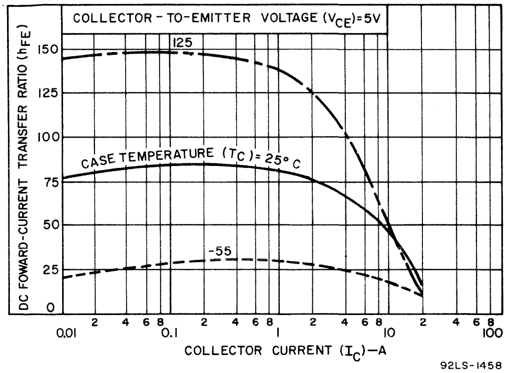


Fig. 11 — Typical dc beta characteristics for 2N5038.

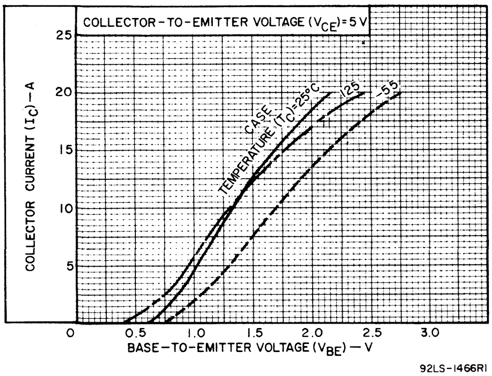


Fig. 12 — Typical transfer characteristics for 2N5039.

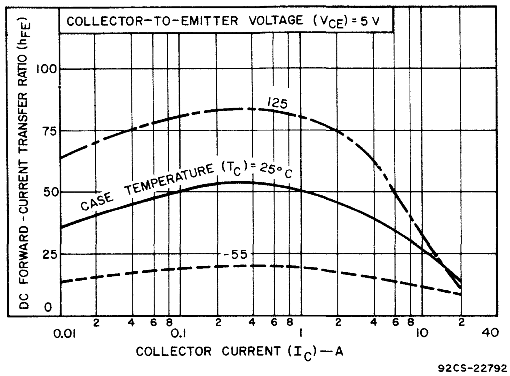


Fig. 13 — Typical dc beta characteristics for 2N5039.

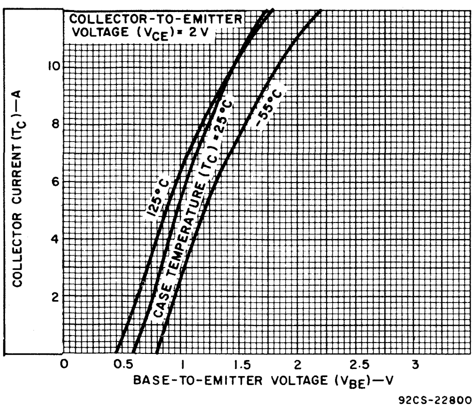


Fig. 14 — Typical transfer characteristics for 2N6496.

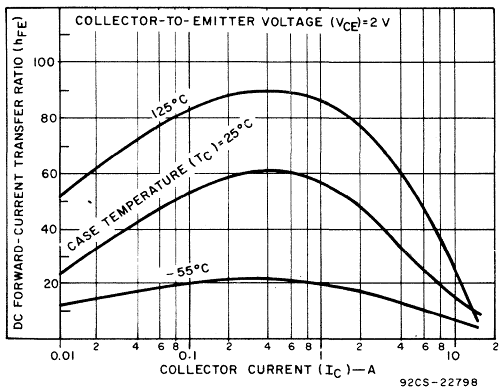


Fig. 15 — Typical dc beta characteristics for 2N6496.

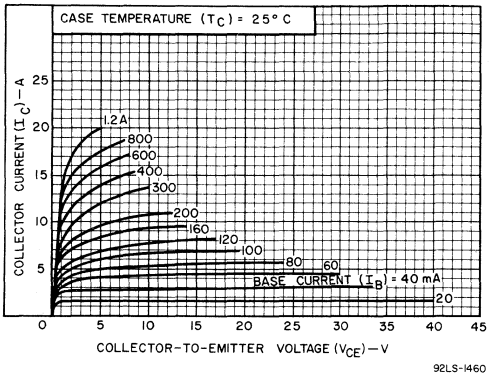


Fig. 16 — Typical output characteristics for 2N5038.

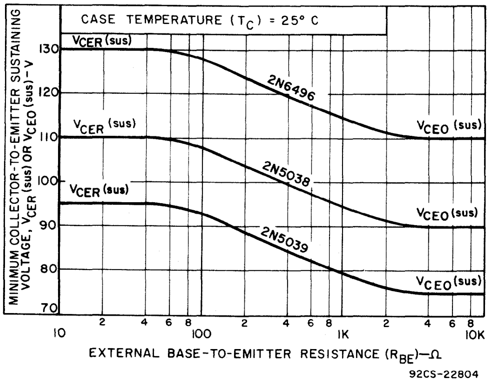


Fig. 17 — Collector-to-emitter sustaining voltage characteristic for all types.

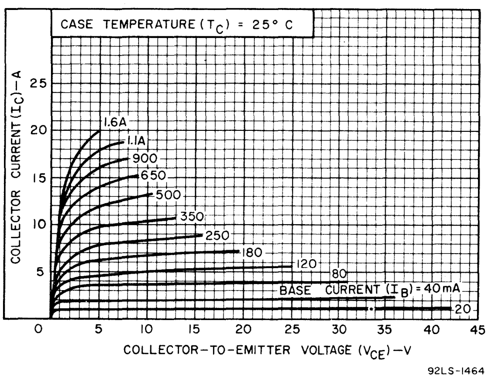


Fig. 18 — Typical output characteristics for 2N5039.

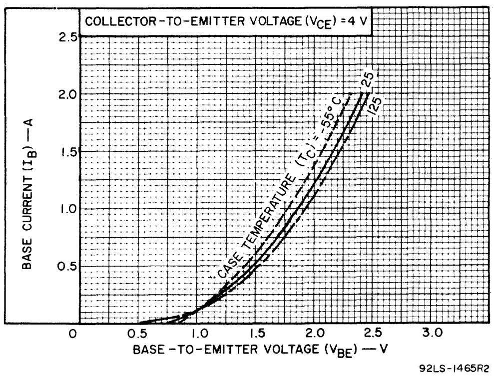


Fig. 19 — Typical input characteristics for 2N5038 and 2N5039.

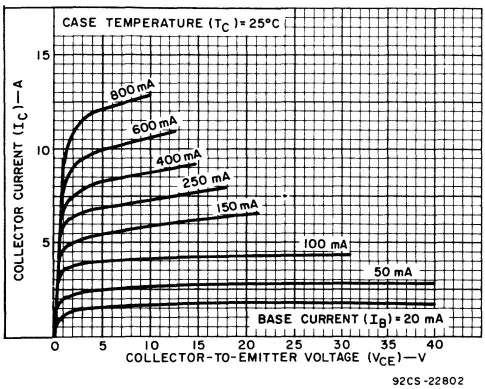


Fig. 20 — Typical output characteristics for 2N6496.

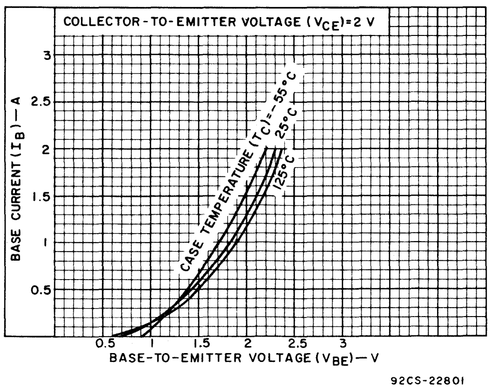
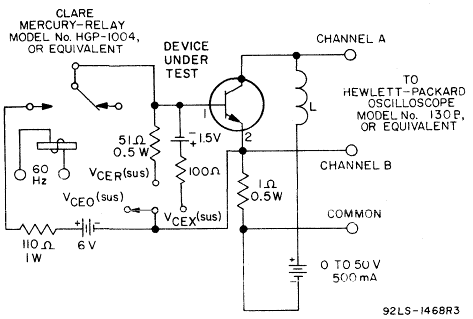
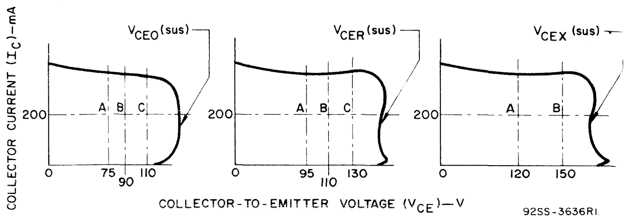


Fig. 21 — Typical input characteristics for 2N6496.



L = 15mH for $V_{CEO}(sus)$ and $V_{CER}(sus)$ measurements
L = 2mH for $V_{CEX}(sus)$ measurements

Fig. 22 — Circuit used to measure sustaining voltages $V_{CEO}(sus)$, $V_{CER}(sus)$, and $V_{CEX}(sus)$.



The sustaining voltages ($V_{CEO}(sus)$, $V_{CER}(sus)$, and $V_{CEX}(sus)$) are acceptable when the traces fall to the right of point "A" for type 2N5039, point "B" for type 2N5038 and point "C" for type 2N6496. (NOTE: 2N6496 is not tested for $V_{CEX}(sus)$.)

Fig. 23 — Oscilloscope display for measurement of sustaining voltages (Test circuit shown in Fig. 22).

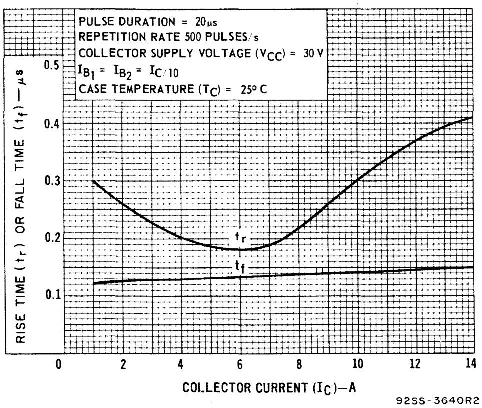


Fig. 24 — Typical rise-time and fall-time characteristics for all types.

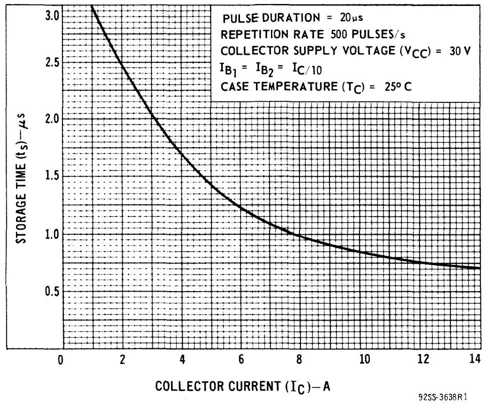


Fig. 25 — Typical storage time characteristic for all types.

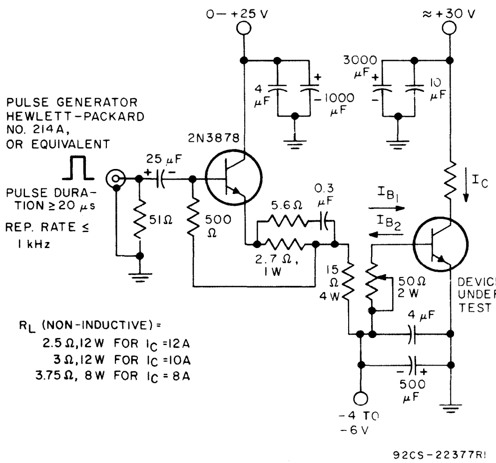


Fig. 26 — Circuit used to measure switching times for all types.

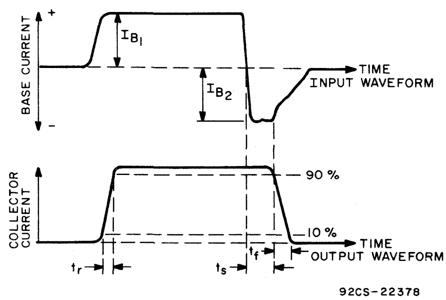
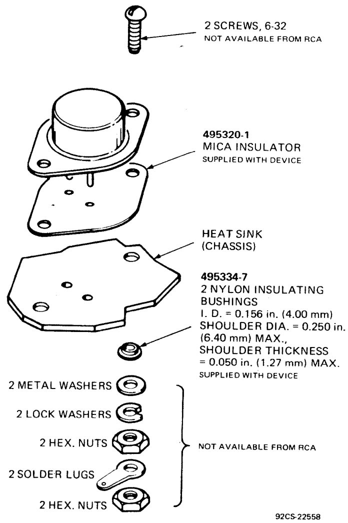


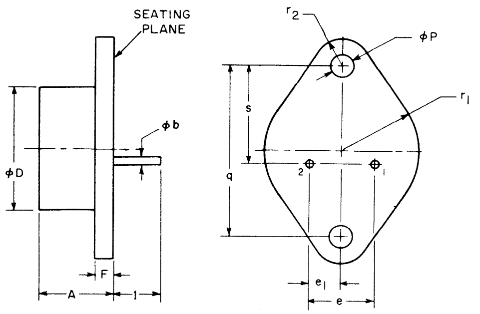
Fig. 27 — Phase relationship between input and output currents showing reference points for specification of switching times. (Test circuit shown in Fig. 26).



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 28 – Suggested mounting hardware.

DIMENSIONAL OUTLINE JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
ϕb	0.038	0.043	0.97	1.09	2
ϕD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e_1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
1	0.312		7.92		2
ϕP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r_1		0.525		13.34	
r_2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS–15222

TERMINAL CONNECTIONS

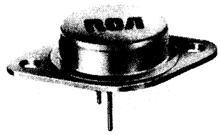
Pin 1 – Base
Pin 2 – Emitter
Case – Collector
Mounting Flange – Collector

RCA

Solid State
Division

Power Transistors

2N6354



JEDEC TO-3 H-1570

120-V, 10-A, 140-W Silicon N-P-N Transistor

For Switching Applications in
Military and Industrial Equipment

Features:

- **High V_{CEO}(sus): 120 V**
- **Maximum safe-area-of operation curves**
- **Low saturation voltage: V_{CE}(sat) $\leq$ 0.5 V**
- **Fast switching speeds at I_C = 5 A:**
  - $t_r \leq 0.3\ \mu s$
  - $t_s \leq 1\ \mu s$
  - $t_f \leq 0.2\ \mu s$
- **High dissipation rating: P_T = 80 W at 100°C**
  = 140 W at 25°C

RCA type 2N6354● is an epitaxial silicon n-p-n power transistor with a multiple-emitter-site structure. The device is supplied in the JEDEC TO-3 package.

Typical high-speed switching applications for the 2N6354 include switching-control amplifiers operated from a 48-V (nominal) power supply, power gates, switching regulators, dc-dc converters, and power oscillators.

● Formerly RCA Dev. No. TA7534.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	150	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With base open, sustaining	V_{CEO}(sus)	120	V
* With external base-to-emitter resistance (R_{BE}) = 500Ω	V_{CEX}	130	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	6.5	V
*COLLECTOR CURRENT (Continuous)	I_C	10	A
COLLECTOR CURRENT (Peak)		12	A
*BASE CURRENT (Continuous)	I_B	5	A
*TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25°C and V_{CE} up to 25 V		140	W
At case temperature of 100°C and V_{CB} of 20 V		80	W
At case temperatures up to 25°C and V_{CE} above 25 V		See Figs. 1 & 2	
At case temperatures above 25°C and V_{CE} above 25 V		See Figs. 1, 2, & 4	
*TEMPERATURE RANGE:			
Storage & Operating (Junction)		−65 to 200	°C
*PIN TEMPERATURE (During Soldering):			
At distance $\geq$ 1/32 in. (0.8 mm) from case for 10 s max.		230	°C

*In accordance with JEDEC registration data format JS-6 RDF-1.

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: DC VOLTAGE (V) V_{CE}	V_{CB}	V_{EB}	V_{BE}	DC CURRENT (A) I_C	I_B	LIMITS 2N6354 MIN.	MAX.	UNITS
* Collector-Cutoff Current: With emitter open	I_{CBO}		150					–	5	mA
With base open	I_{CEO}	100					0	–	20	mA
* With base-emitter junction reverse-biased	I_{CEV}	140			0			–	10	mA
* At T_C = 125°C	I_{CEV}	140			0			–	20	mA
* Emitter-Cutoff Current	I_{EBO}			6.5		0		–	5	mA
* Emitter-to-Base Voltage	V_{EBO}						0.005	6.5	–	V
* Collector-to-Emitter Voltage: At breakdown, with base open	$V_{(BR)CEO}$					0.2	0	120[b]	–	V
With external base-to emitter resistance (R_{BE}) ≤ 100 Ω	$V_{CER(sus)}$[f]					0.2	0	130[b]	–	V
* Saturation Voltage: Collector-to-Emitter	$V_{CE}(sat)$					5[a] 10[a]	0.5 1.0	– –	0.5 1	V
Base-to-Emitter	$V_{BE}(sat)$					5[a] 10[a]	0.5 1.0	– –	1.3 2	V
* DC Forward Current Transfer Ratio	h_{FE}	2 2				5[a] 10[a]		20 10	150 100	
Forward-Bias Second-Breakdown Collector Current[d]	$I_{S/b}$[c]	25 45						5.5 0.5	– –	A
Second-Breakdown Energy (With base reverse biased, R_{BE}=51 Ω, L = 25 µH)	$E_{S/b}$[g]			1		5		0.3	–	mJ
* Magnitude of Common Emitter, Small-Signal, Short-Circuit Forward Current Transfer Ratio (f = 10 MHz)	$\|h_{fe}\|$	10				1		8	–	
* Saturated Switching Time: (See Figs. 11 & 12) Rise Time	t_r	V_{CC} = 30				5 10	0.5[e] 1[e]	– –	0.3 1	µs
Storage Time	t_{s1}	V_{CC} = 30				5 10	0.5[e] 1[e]	– –	1 0.6	µs
Storage Time (No Load)	t_{s2}	V_{CC} = 30				0.5	0.5[e]	–	2	µs
Fall Time	t_f	V_{CC} = 30				5 10	0.5[e] 1[e]	– –	0.2 0.2	µs
Output Capacitance (f = 1 MHz)	C_{obo}		10					–	300	pF
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$	20				1		–	1.25	°C/W

*In accordance with JEDEC registration data format JS-6 RDF-1.

[a]Pulsed: pulse duration ≤ 350 µs, duty factor = 2%.

[b]CAUTION: The collector-to-emitter voltages, $V_{(BR)CEO}$ and $V_{CER}(sus)$, MUST NOT be measured on a curve tracer. These voltages should be measured by means of the test circuit shown in Fig.5.

[c]$I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward-biased for transistor operation in the active region.

[d]Pulsed; 1-s non-repetitive pulse.

[e]$I_{B_1} = I_{B_2}$ = value shown.

[f]L = 15 mH

[g]$E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse bias conditions. $E_{S/b} = \frac{1}{2}LI^2$ where L is a series load or leakage inductance and I is the peak collector current.

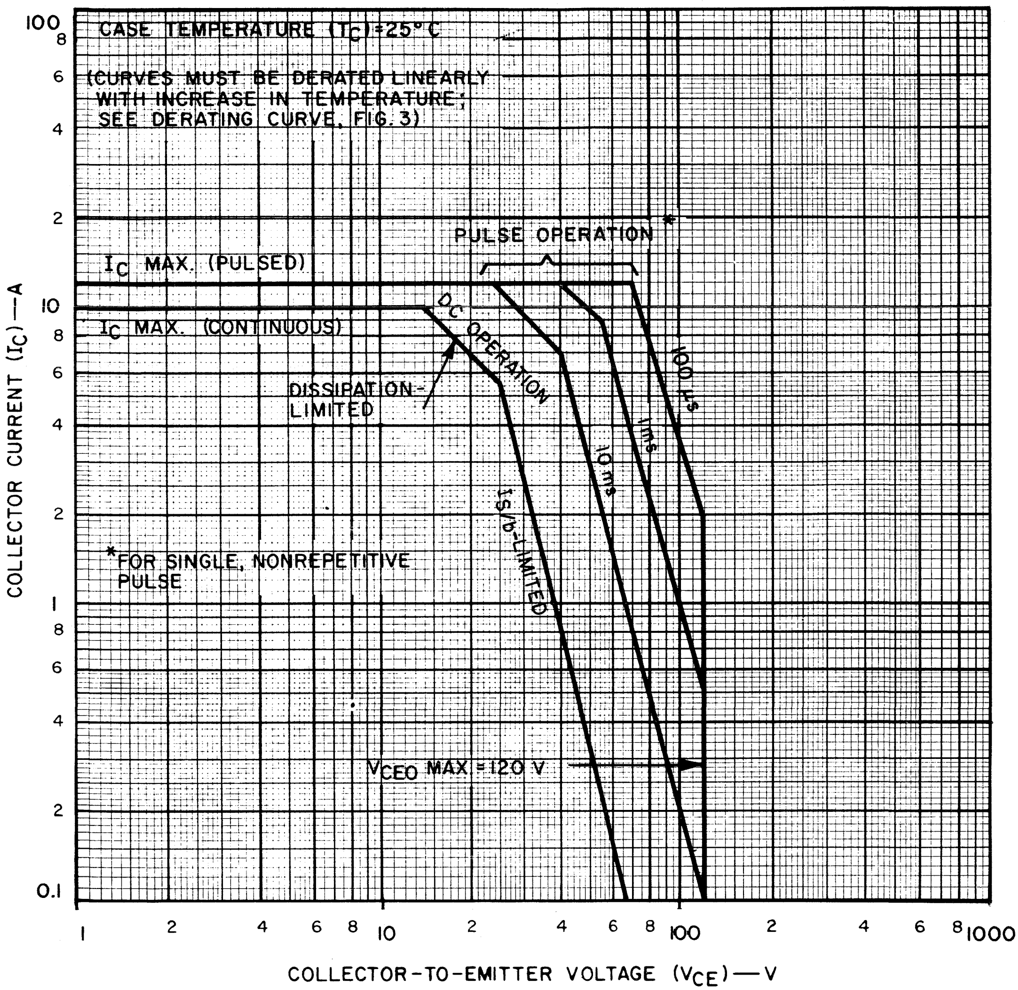


Fig.1 — Maximum operating areas.

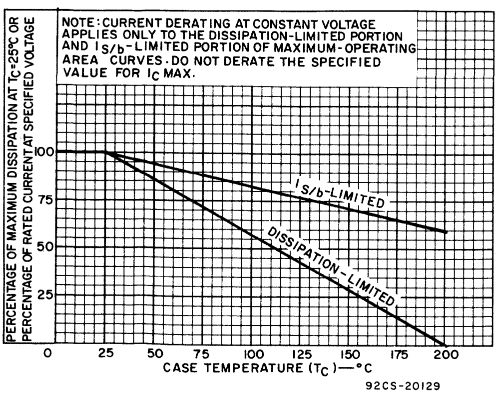


Fig.2 — Derating curves.

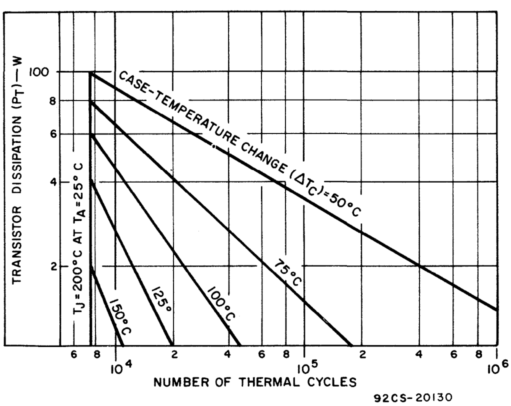


Fig.3 — Thermal-cycling rating chart.

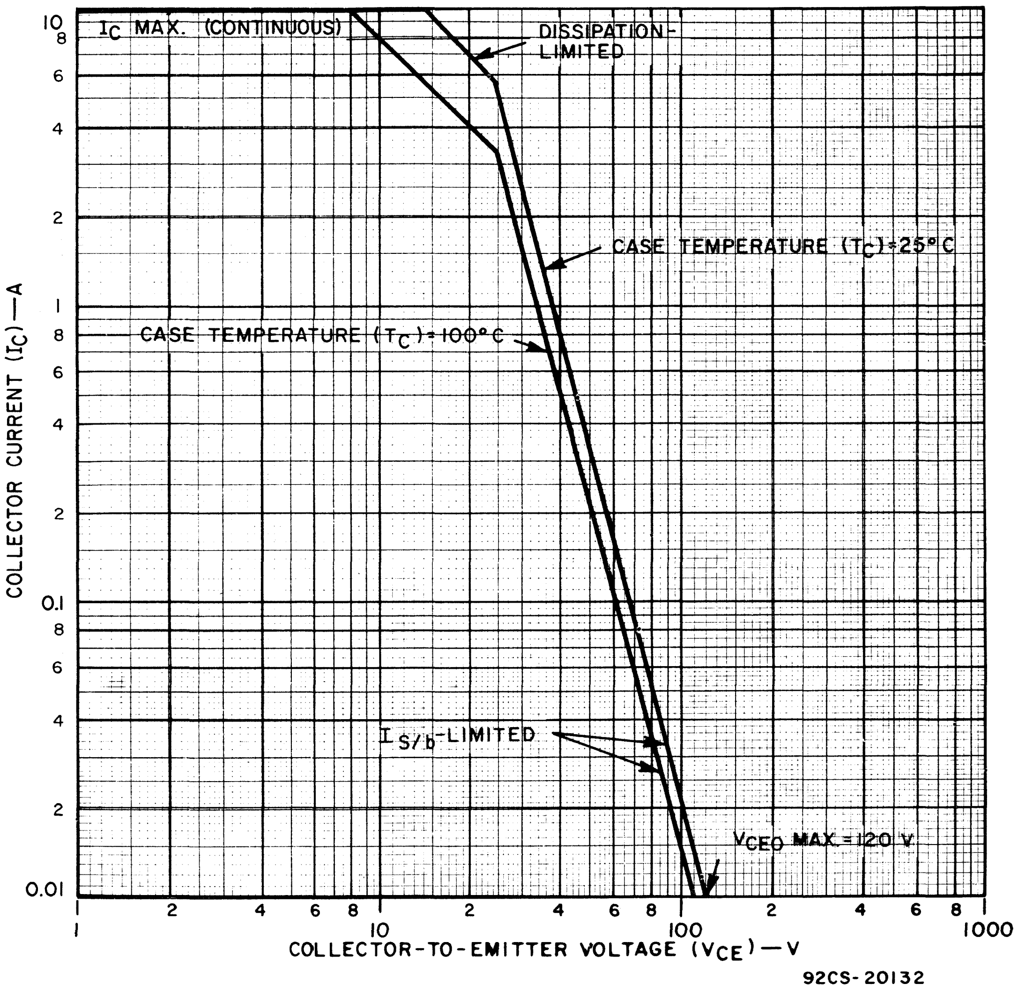


Fig.4 – Maximum operating areas.

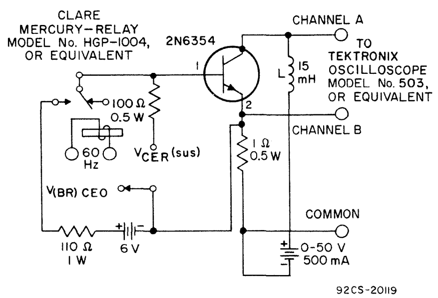
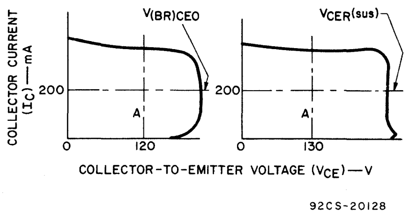


Fig.5—Circuit used to measure voltages $V_{(BR)CEO}$ and $V_{CER}(sus)$.



NOTE: The voltages, $V_{(BR)CEO}$ and V_{CER}(sus) are acceptable when the trace falls to the right of and above point "A".

Fig.6—Oscilloscope display for $V_{(BR)CEO}$ and $V_{CER}(sus)$ measurement (test circuit shown in Fig.5).

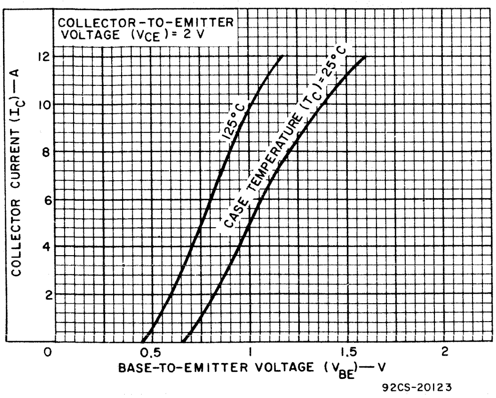


Fig.7—Typical transfer characteristics.

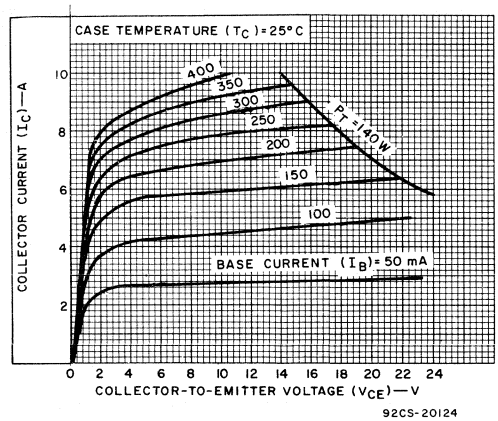


Fig.8—Typical output characteristics.

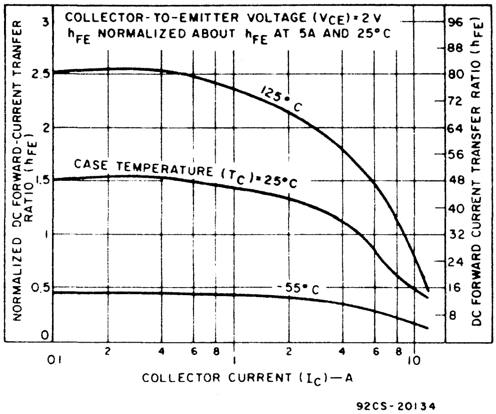


Fig.9—Typical normalized dc beta characteristics.

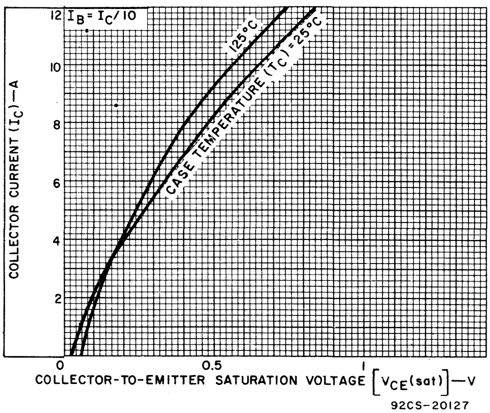


Fig. 10—Typical saturation voltage characteristics.

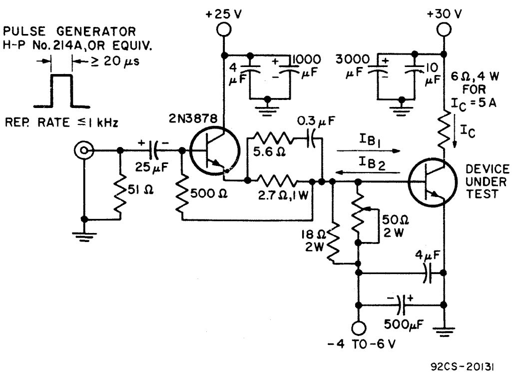


Fig. 11—Circuit used to measure switching times.

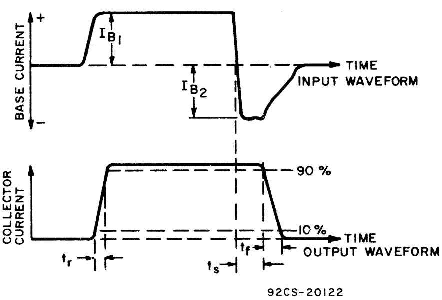


Fig. 12—Phase relationship between input and output currents showing reference points for specification of switching times (test circuit shown in Fig. 11).

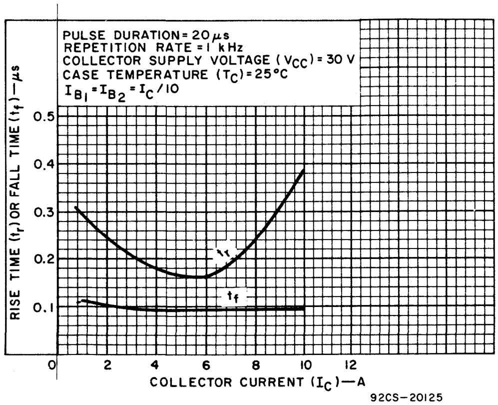


Fig. 13—Typical rise- and fall-time characteristics.

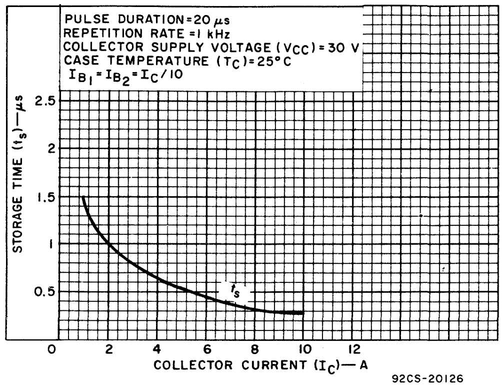


Fig. 14—Typical storage-time characteristics.

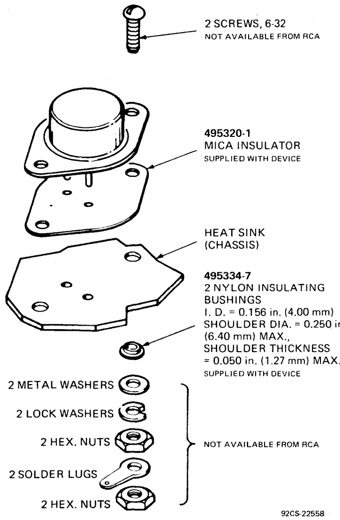


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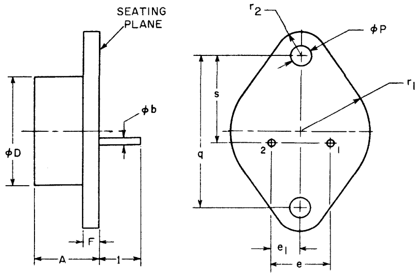
Fig. 15—Suggested mounting hardware.

DIMENSIONAL OUTLINE JEDEC TO-3



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	0.250	0.450	6.35	11.43	
φb	0.038	0.043	0.97	1.09	2
φD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e_1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
l	0.312		7.92		2
φP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r_1		0.525		13.34	
r_2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

* 92CS-15222

TERMINAL CONNECTIONS

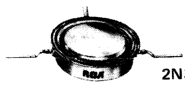
Pin 1 — Base
Pin 2 — Emitter
Mounting Flange, Case — Collector

RCA

Solid State
Division

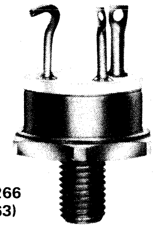
Power Transistors

2N3263 2N3264
2N3265 2N3266



H-1354

2N3263, 2N3264
(RADIAL)



H-1785

2N3265, 2N3266
(JEDEC TO-63)

High-Power, High-Speed, High-Current Silicon N-P-N Power Transistors

Epitaxial Types for Aerospace,
Military, and Industrial Applications

Features:

- **Low saturation voltages —**
  2N3263 and 2N3265
  $V_{CE}(sat)$ = 0.75 V (max.) at I_C = 15 A
  $V_{BE}(sat)$ = 1.60 V (max.) at I_C = 15 A
  2N3264 and 2N3266
  V_{CE} (sat) = 1.20 V (max.) at I_C = 15 A
  V_{BE} (sat) = 1.80 V (max.) at I_C = 15 A
- **High reliability and uniformity of characteristics**
- **High power dissipation**
- **Fast rise time at high collector current —**
  0.2 μs at 10 A (typical)

RCA-2N3263, 2N3264, 2N3265, and 2N3266• are n-p-n epitaxial silicon power transistors designed for high-reliability aerospace, military, and industrial equipment. Their high current-handling capability and fast switching speed make them desirable in applications where high circuit efficiency is required.

The 2N3263 and 2N3264 are sealed in flat 3/4-inch-diameter packages with radial leads. Types 2N3265 and 2N3266 utilize the JEDEC TO-63 package.

Typical high-speed switching applications for these transistors include switching-control amplifiers, power gates, switching regulators, dc-dc converters, and dc-ac inverters. Other recommended applications include dc-rf amplifiers and power oscillators.

• Formerly RCA Dev. Nos. TA2492, TA2493, TA2494, and TA2495, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N3264 2N3266	2N3263 2N3265	
* COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	120	150	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:				
With 1.5 volts (V_{BE}) of reverse bias	$V_{CEX}(sus)$	120	150	V
With external base-to-emitter resistance (R_{BE}) ≤ 50 Ω	$V_{CER}(sus)$	80	110	V
* With base open	V_{CEO} (sus)	60	90	V
* EMITTER-TO-BASE VOLTAGE	V_{EBO}	7	7	V
* COLLECTOR CURRENT	I_C	25	25	A
* BASE CURRENT	I_B	10	10	A
* TRANSISTOR DISSIPATION	P_T	*See Figs. 1 & 2*		
* TEMPERATURE RANGE:				
Storage and operating (Junction)		−65 to +200		°C
LEAD TEMPERATURE (During soldering):				
At distance ≥ 1/32 in. (0.8 mm) from seating plane for 10 s max.		230		°C

* In accordance with JEDEC registration data format.

6-72

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS						LIMITS				UNITS
		VOLTAGE V dc			CURRENT A dc			2N3264 2N3266		2N3263 2N3265		
		V_{CB}	V_{CE}	V_{EB}	I_E	I_B	I_C	MIN.	MAX.	MIN.	MAX.	
Collector Cutoff Current: With emitter open	I_{CBO}	60			0			–	10	–	–	mA
		80			0			–	–	–	4	
At T_C = 125°C		60			0			–	10	–	–	
		80			0			–	–	–	4	
* With base reverse-biased	I_{CEX}		120	1.5				–	20	–	–	
			150	1.5				–	–	–	20	
* Emitter Cutoff Current:	I_{EBO}			7			0	–	15	–	5	mA
* At T_C = 125°C				7			0	–	15	–	5	
Emitter-to-Base Voltage	V_{EBO}				0.02		0	7	–	7	–	V
Collector-to-Emitter Sustaining Voltage: * With base open	$V_{CEO}(sus)$●					0	0.2	60	–	90	–	V
With external base-to-emitter resistance (R_{BE}) ≤ 50 Ω	$V_{CER}(sus)$●					0	0.2	80	–	110	–	
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$●					2	20	–	1.6	–	1	V
						1.2	15	–	1.2	–	0.75	
* Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$●					2	20	–	2.2	–	1.8	V
						1.2	15	–	1.8	–	1.6	
* DC Forward Current * Transfer Ratio	h_{FE}●		3				5	35	–	40	–	
			3				15	20	80	25	75	
			2				15	–	–	20	55	
* Second-Breakdown Collector Current: (See Fig. 7) DC forward-biased	$I_{S/b}$▲	50						700	–	–	–	mA
		75						–	–	350	–	
* Pulsed, forward-biased, t_p = 250 μs		75						13.3	–	13.3	–	A
* Second-Breakdown Energy With base reverse-biased, and R_{BE} = 20Ω, L = 40μH	$E_{S/b}$**			6			10	2	–	2	–	mJ
* Saturated Switching Time: (See Figs. 3 & 4) Turn-on ($t_d + t_r$)	t_{ON}	V_{CC}= 30				1.2♠	15	–	0.5	–	0.5	μs
Storage	t_s					1.2♠	15	–	1.5	–	1.5	
Fall	t_f					1.2♠	15	–	0.5	–	0.5	
* Gain-Bandwidth Product (f = 1 MHz)	f_T		10				3	20	–	20	–	MHz
Collector-to-Base Feedback Capacitance (f = 1 MHz)	C_{ob}	10			0			–	500	–	500	pF
* Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$							2N3263 2N3264		2N3265 2N3266		°C/W
			10				10	–	1.5	–	1	

* In accordance with JEDEC registration data format.

● Pulsed; pulse duration ≤ 350 μs, duty factor ≤ 2%. CAUTION: The sustaining voltages $V_{CEO}(sus)$ and $V_{CER}(sus)$ MUST NOT be measured on a curve tracer. These sustaining voltages should be measured by means of the test circuit shown in Fig. 5.

▲ $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage.

** $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse bias conditions. $E_{S/b}$ = 1/2 LI^2, where L is a series load or leakage inductance and I is the collector current.

♠ $I_{B_1} = I_{B_2}$.

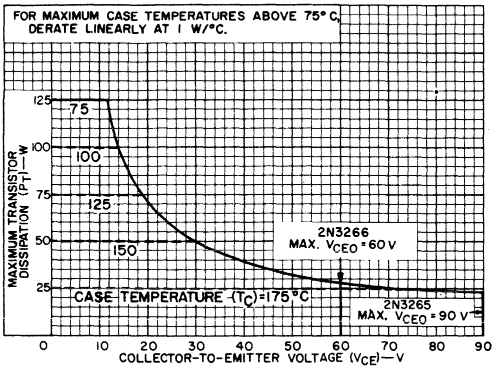


Fig.1—Rating chart for 2N3265 and 2N3266.

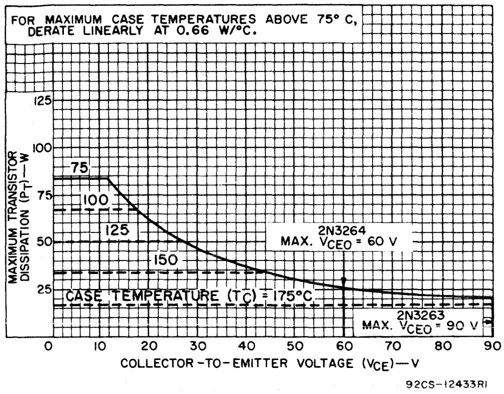


Fig.2—Rating chart for 2N3263 and 2N3264.

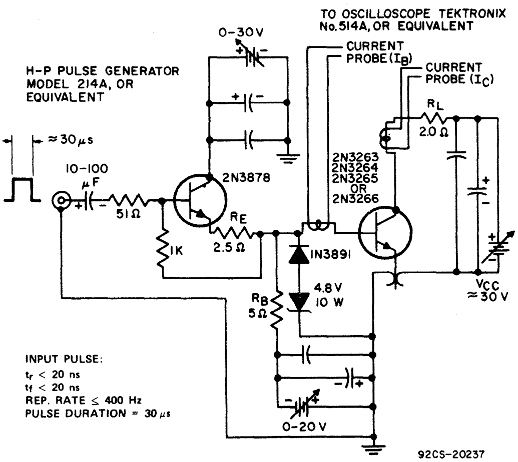


Fig.3—Circuit used to measure saturated switching times.

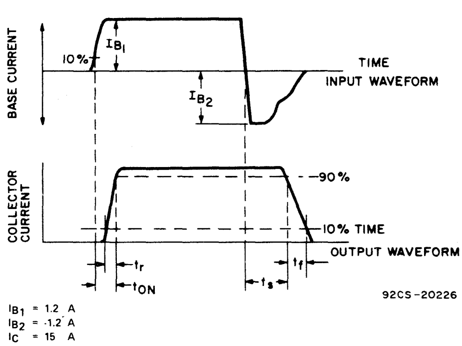


Fig.4—Phase relationship between input and output currents showing reference points for specification of switching times. (Test circuit shown in Fig. 3.)

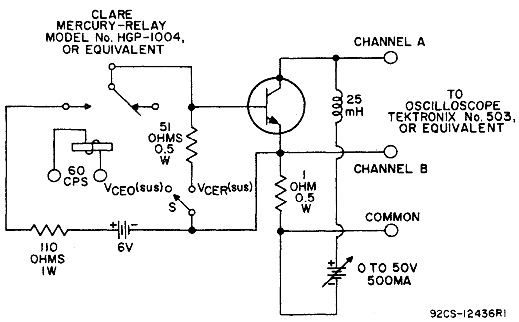
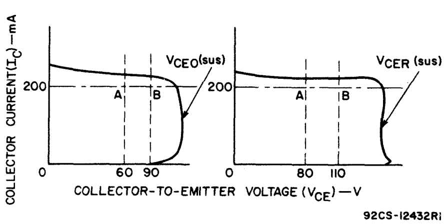


Fig.5—Circuit used to measure sustaining voltages V_{CEO}(sus) and V_{CER}(sus).



The sustaining voltages V_{CEO}(sus) and V_{CER}(sus) are acceptable when the traces fall to the right of point "A" for types 2N3264 and 2N3266. The traces must fall to the right of point "B" for types 2N3263 and 2N3265.

Fig.6—Oscilloscope display for V_{CEO}(sus) and V_{CER}(sus) measurement. (Test circuit shown in Fig. 5.)

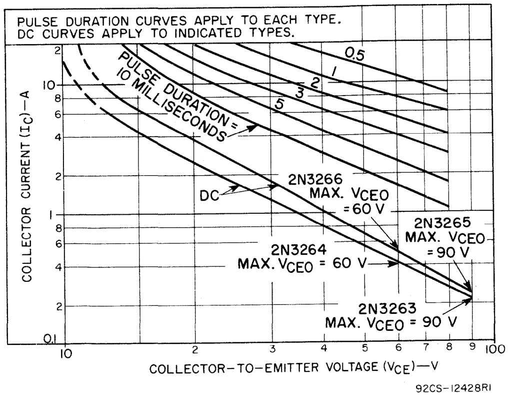


Fig.7—Safe-operating region as a function of pulse width.

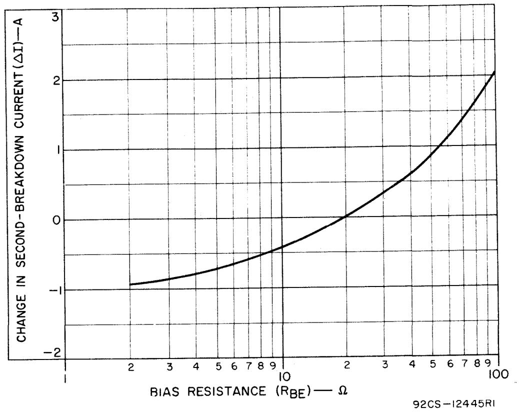


Fig.8—Typical change in $E_{S/b}$ as a function of base-to-emitter resistance.

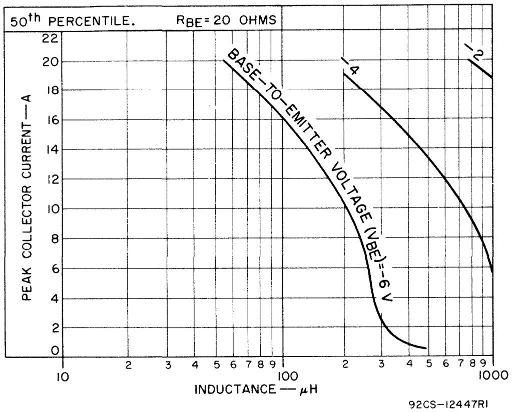


Fig.9—Collector current as a function of inductance (10th percentile).

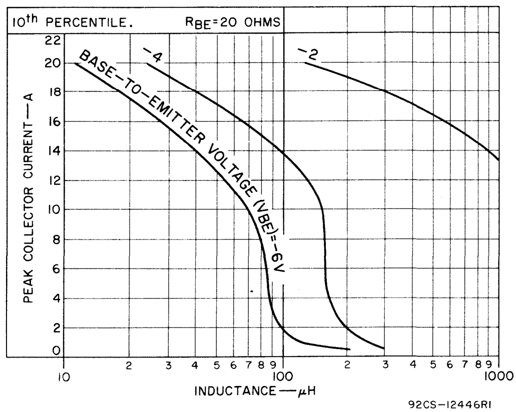


Fig.10—Collector current as a function of inductance (50th percentile).

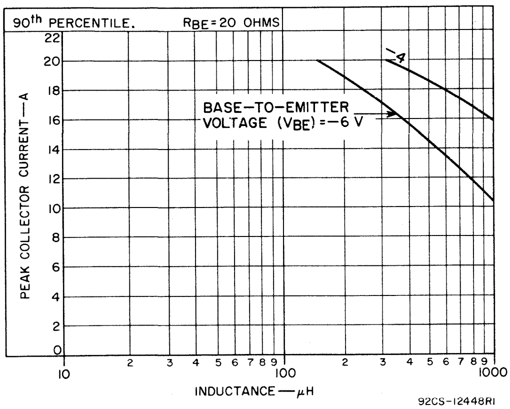


Fig.11—Collector current as a function of inductance (90th percentile).

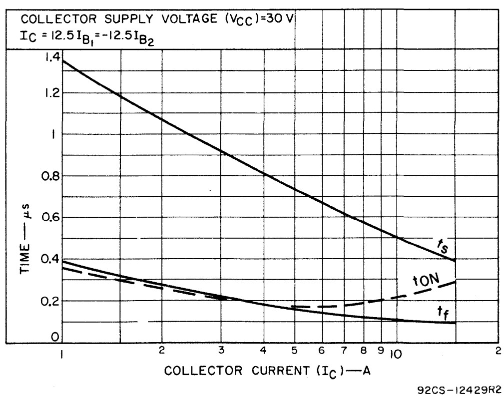


Fig.12—Typical saturated-switching characteristics.

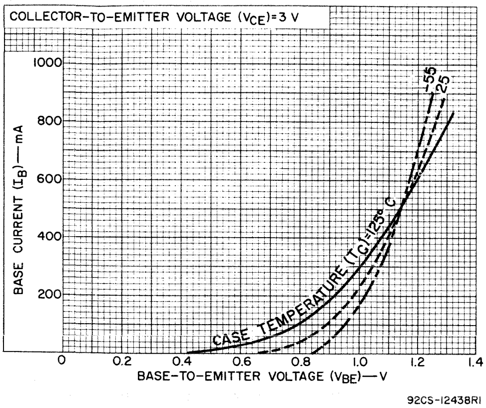


Fig. 13—Typical input characteristics.

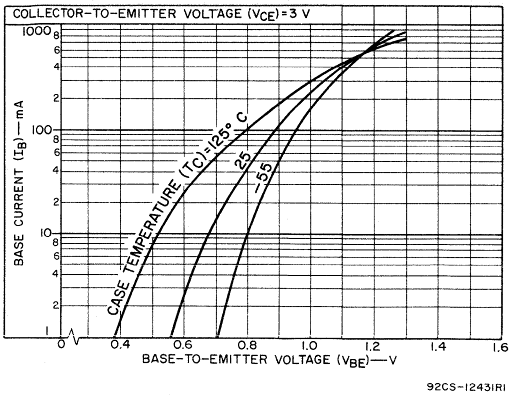


Fig. 14—Typical input characteristics.

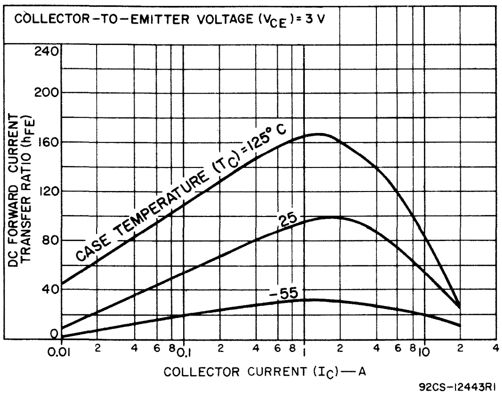


Fig. 15—Typical dc beta characteristics (median values).

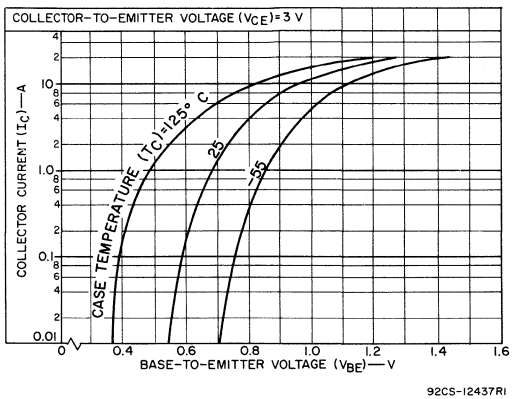


Fig. 16—Typical transfer characteristics.

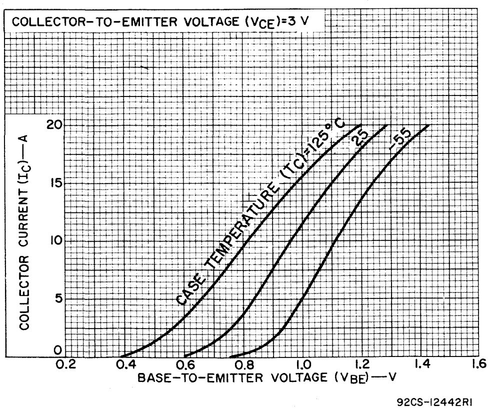


Fig. 17—Typical transfer characteristics.

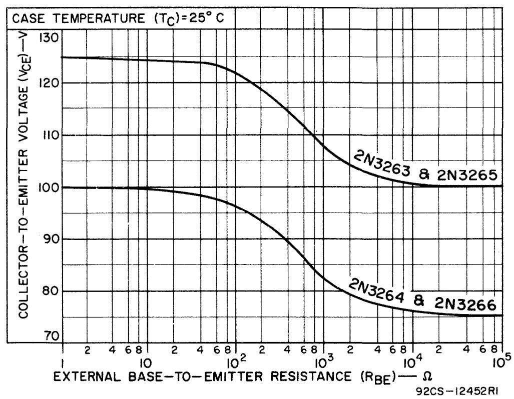
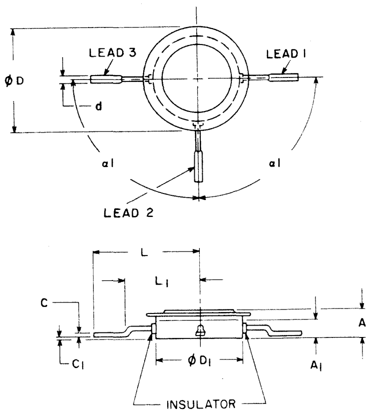


Fig. 18—Typical sustaining voltage vs. base-to-emitter resistance.

DIMENSIONAL OUTLINE
TYPES 2N3263 and 2N3264



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	0.200	–	5.08	
A_1	–	0.125	–	3.17	1
C	0.015	0.019	0.38	0.48	
C_1	–	0.015	–	0.38	
ϕD	–	0.710	–	18.03	
ϕD_1	0.615	0.690	15.62	17.52	1
d	0.042	0.046	1.06	1.16	
L	–	0.705	–	17.90	
L_1	–	0.510	–	12.95	
α_1	90° ± 2°		90° ± 2°		

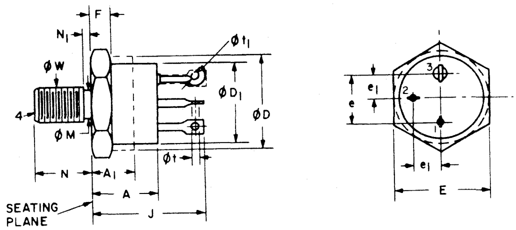
92CS- 20224

NOTE:
1. CONTROLLED AREA OF THE DIAMETER DOES NOT INCLUDE THE BRAZED AREA AROUND THE CERAMIC AND TERMINAL 2.

TERMINAL CONNECTIONS

Lead 1 – Base
Case, Lead 2 – Collector
Lead 3 – Emitter

DIMENSIONAL OUTLINE
TYPES 2N3265 and 2N3266
JEDEC TO-63



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.480	0.535	12.19	13.59	
A_1	–	0.300	–	7.62	2
ϕD	0.775	0.875	19.69	22.23	2
ϕD_1	0.745	0.775	18.92	19.69	
E	0.855	0.875	21.72	22.23	
e	0.485	0.515	12.32	13.08	5
e_1	0.240	0.260	6.10	6.60	5
F	0.090	0.167	2.29	4.24	1
J	0.937	1.030	23.80	26.16	
ϕM	0.278	0.312	7.06	7.92	
N	0.460	0.495	11.68	12.57	
N_1	–	0.105	–	2.67	
ϕt	0.060	0.105	1.52	2.67	
ϕt_1	0.060	0.105	1.52	2.67	4
ϕW	0.2806	0.2854	7.127	7.249	3

92CS-20225

NOTES:
1. DIMENSION DOES NOT INCLUDE SEALING FLANGES.
2. PACKAGE CONTOUR OPTIONAL WITHIN DIMENSIONS SPECIFIED.
3. PITCH DIAMETER · THREAD 5/16-24 UNF-2A (COATED). REFERENCE (SCREW THREAD STANDARDS FOR FEDERAL SERVICES · HANDBOOK H-28).
4. THIS TERMINAL CAN BE FLATTENED AND PIERCED OR HOOK TYPE.
5. POSITION OF LEADS IN RELATION TO THE HEXAGON IS NOT CONTROLLED.

TERMINAL CONNECTIONS

Pin 1 – Emitter
Pin 2 – Base
Case, Pin 3 – Collector

File No. 383

RCA

Solid State Division

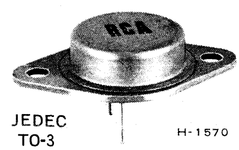
Power Transistors
2N5671
2N5672

RCA Types 2N5671 and 2N5672▲ are epitaxial silicon n-p-n transistors having high current and high power handling capability and fast switching speed. The 2N5672 is similar to the 2N5671 except that it has higher voltage ratings and lower leakage currents. These devices are especially suitable for switching-control amplifiers, power gates, switching regulators, power-switching circuits, converters, inverters, control circuits. Other recommended applications included DC-RF amplifiers and power oscillators.

▲Formerly Dev. Types TA7323 and TA7323A, respectively

SILICON N-P-N POWER TRANSISTORS

High-Current, High-Speed High-Power Types For Switching and Amplifier Applications in Military, Industrial, and Commercial Equipment



JEDEC TO-3 H-1570

MAXIMUM RATINGS, ***Absolute-Maximum Values:***

	2N5671	2N5672	
*COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	120	150	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:			
With base open, $V_{CEO}(sus)$	90	120	V
With external base-to-emitter resistance (R_{BE}) ≤ 50 Ω, $V_{CER}(sus)$	110	140	V
With external base-to-emitter resistance (R_{BE}) ≤ 50 Ω & V_{BE} = -1.5, $V_{CEX}(sus)$	120	150	V
*EMITTER-TO-BASE VOLTAGE, V_{EBO}	7	7	V
*COLLECTOR CURRENT, I_C	30	30	A
*BASE CURRENT, I_B	10	10	A
*TRANSISTOR DISSIPATION, P_T:			
At case temperatures up to 25° C and V_{CE} up to 24 V	140	140	W
At case temperatures up to 25° C and V_{CE} above 24 V	See Fig. 2.		
At case temperatures above 25° C and V_{CE} above 24 V	See Figs.1&2.		
*TEMPERATURE RANGE:			
Storage & Operating (Junction)	−65 to +200		°C
*PIN TEMPERATURE (During Soldering)			
At distances ≥ 1/32 in. from seating plane for 10 s max	230		°C

*In accordance with JEDEC registration data format (JS-6, RFD-1)

Features

- **Maximum Safe-Area-of-Operation Curves . . .** $I_{S/b}$ **limit line beginning at 24 V**
- **Fast Turn-On Time . . .** t_{on} **= 0.5µs max. at** I_C **= 15 A**
- **High-Current Capability . . .** h_{FE}, $V_{CE}(sat)$, $V_{BE}(sat)$, **&** V_{BE} **measured at** I_C **= 15 A**
- **Low** $V_{CE}(sat)$ **= 0.75 V max.**
- **High** P_T **= 140 W max. at** T_C **= 25° C**

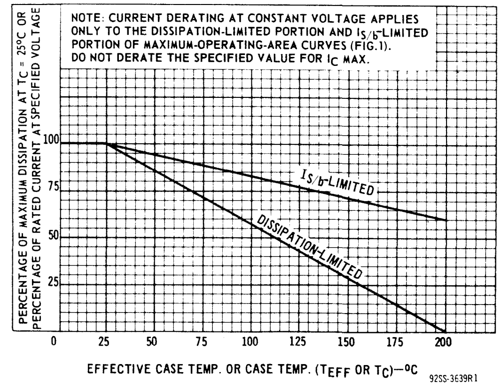


Fig. 1 - Dissipation derating curves for types 2N5671 & 2N5672

11-73

ELECTRICAL CHARACTERISTICS, *Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: DC Collector Voltage (V) V_{CB}	V_{CE}	DC Emitter or Base Voltage (V) V_{EB}	V_{BE}	DC Current (A) I_C	I_E	I_B	LIMITS Type 2N5671 Min.	Max.	Type 2N5672 Min.	Max.	UNITS
Collector-Cutoff Current	I_{CEO}	–	80	–	–	–	–	0	–	10	–	10	mA
*	I_{CEV}	–	110	–	-1.5	–	–	–	–	12	–	–	mA
			135	–	-1.5	–	–	–	–	–	–	10	mA
*	I_{CEV} (T_C=150° C)	–	100	–	-1.5	–	–	–	–	15	–	10	mA
* Emitter-Cutoff Current	I_{EBO}	–	–	7	–	0	–	–	–	10	–	10	mA
Collector-to-Emitter Sustaining Voltage: (See Figs. 3,4, & 5) With base open	$V_{CEO}(sus)$	–	–	–	–	0.2	–	0	90[a]	–	120[a]	–	V
With external base-to-emitter resistance (R_{BE}) ≤50 Ω	$V_{CER}(sus)$	–	–	–	–	0.2	–	0	110[a]	–	140[a]	–	V
With base-emitter junction reverse biased & R_{BE} ≤ 50 Ω	$V_{CEX}(sus)$	–	–	–	-1.5	0.2	–	–	120[a]	–	150[a]	–	V
* Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$	–	–	–	–	15	–	1.2	–	1.5	–	1.5	V
Base-to-Emitter Voltage	V_{BE}	–	5	–	–	15	–	–	–	1.6	–	1.6	V
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	–	–	–	–	15	–	1.2	–	0.75	–	0.75	V
* DC Forward-Current Transfer Ratio	h_{FE}	– –	2 5	– –	– –	15 20	– –	– –	20 20	[illegible] –	20 20	100 –	
Second-Breakdown Collector Current[c] With base forward biased	$I_{S/b}$[b]	– –	24 45	– –	– –	– –	– –	– –	5.8[c] 0.9[c]	– –	5.8[c] 0.9[c]	– –	A A
Second-Breakdown Energy With base reverse biased R_{BE} = 20 Ω, L = 180 μH	$E_{S/b}$[d]	–	–	–	-4	15	–	–	20	–	20	–	mJ
Gain-Bandwidth Product	f_T	–	10	–	–	2	–	–	50	–	50	–	MHz
Output Capacitance (At 1 MHz)	C_{ob}	10	–	–	–	–	0	–	–	900	–	900	pF
* Saturated Switching Turn-On Time (Delay Time + Rise Time)	t_{on}	V_{CC}= 30 V	–	–	–	15	–	I_{B1}= I_{B2}= 1.2	–	0.5	–	0.5	μs
* Saturated Switching Storage Time	t_s	V_{CC}= 30 V	–	–	–	15	–	I_{B1}= I_{B2}= 1.2	–	1.5	–	1.5	μs
* Saturated Switching Fall Time	t_f	V_{CC}= 30 V	–	–	–	15	–	I_{B1}= I_{B2}= 1.2	–	0.5	–	0.5	μs
Thermal Resistance (Junction-to-Case)	θ_{J-C}	–	40	–	–	0.5	–	–	–	1.25	–	1.25	°C/W

[a] CAUTION: The sustaining voltages $V_{CEO}(sus)$, $V_{CER}(sus)$, and $V_{CEX}(sus)$ MUST NOT be measured on a curve tracer. These sustaining voltages should be measured by means of the test circuit shown in Fig. 3.

[b] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward biased for transistor operation in the active region.

[c] Pulsed; 1-s, non-repetitive pulse.

[d] $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse bias conditions. $E_{S/b} = \frac{1}{2} LI^2$, where L is a series load or leakage inductance and I is the peak collector current.

* In accordance with JEDEC registration data format (JS-6, RFD-1)

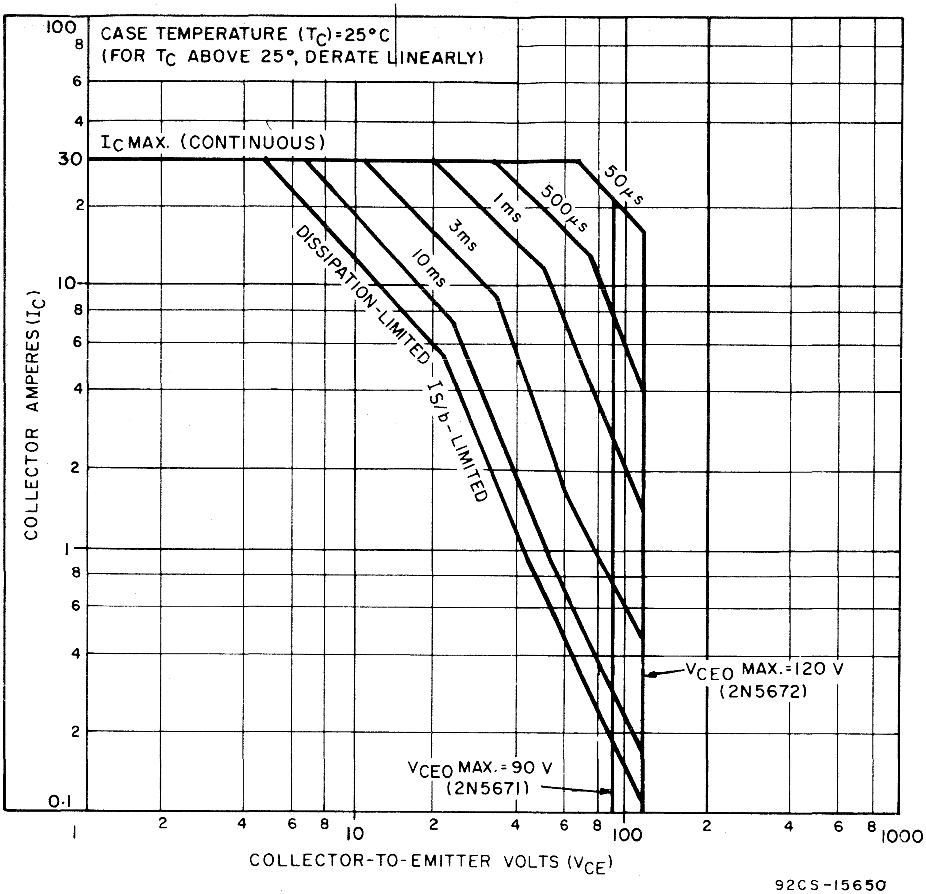


Fig.2 - Maximum operating areas for types 2N5671 & 2N5672

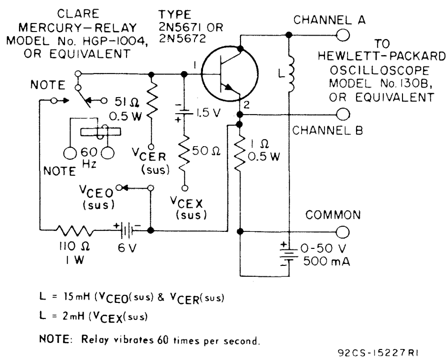
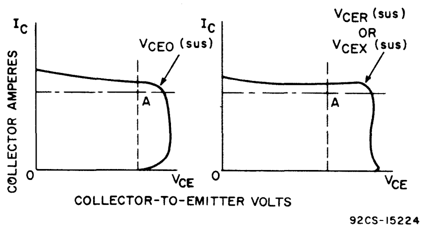


Fig. 3 - Circuit used to measure sustaining voltages $V_{CEO}(sus)$, $V_{CER}(sus)$, & $V_{CEX}(sus)$ for types 2N5671 & 2N5672



NOTE: The sustaining Voltages $V_{CEO}(sus)$, $V_{CER}(sus)$ or, $V_{CEX}(sus)$ are acceptable when the trace falls to the right and above point "A". (For values of current and voltage, see Electrical Characteristics.)

Fig. 4 - Oscilloscope display for measurement of sustaining voltages for types 2N5671 & 2N5672 (Test circuit shown in Fig. 3.)

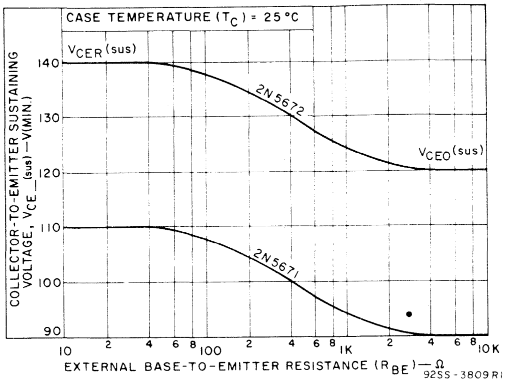


Fig. 5 - Collector-to-emitter sustaining voltage characteristics for types 2N5671 & 2N5672

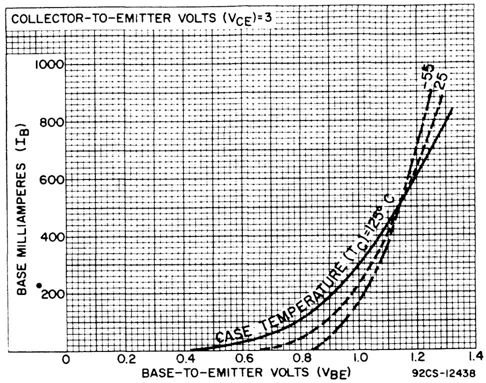


Fig. 6 - Typical input characteristics for types 2N5671 & 2N5672

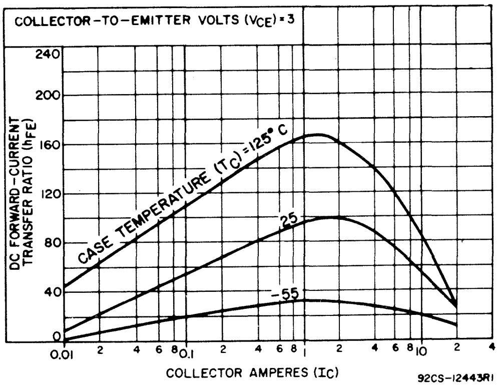


Fig. 7 - Typical DC beta characteristics for types 2N5671 & 2N5672

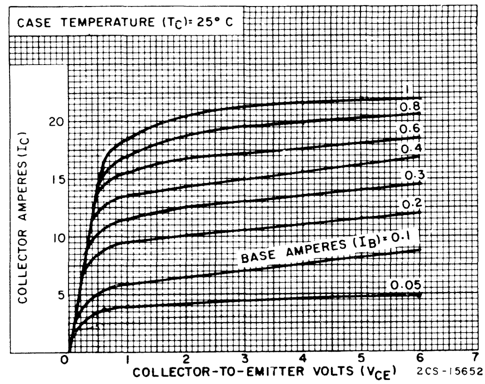


Fig. 8 - Typical output characteristics for types 2N5671 & 2N5672

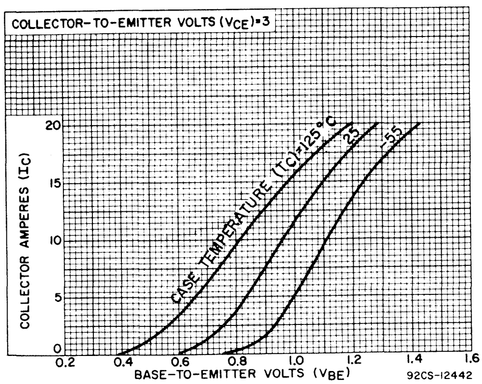


Fig. - 9 Typical transfer characteristics for types 2N5671 & 2N5672

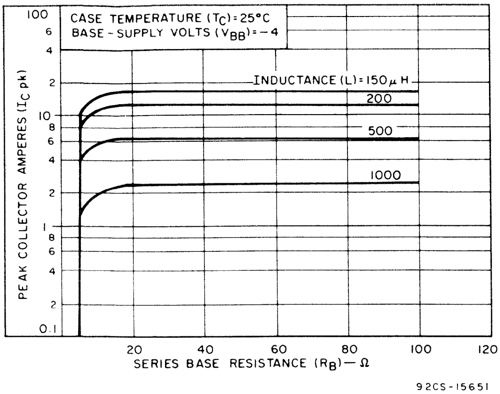


Fig. 10 - Maximum reverse-bias, second-breakdown characteristics for types 2N5671 & 2N5672

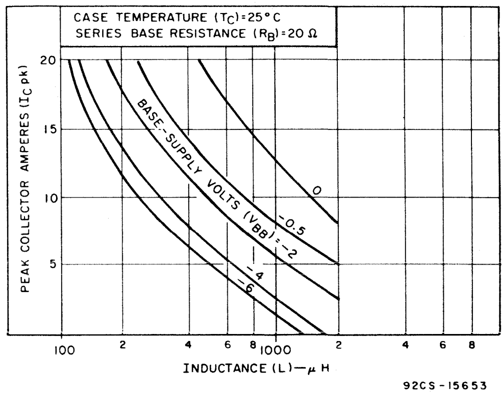


Fig. 11 - Maximum reverse-bias, second-breakdown characteristics for types 2N5671 & 2N5672

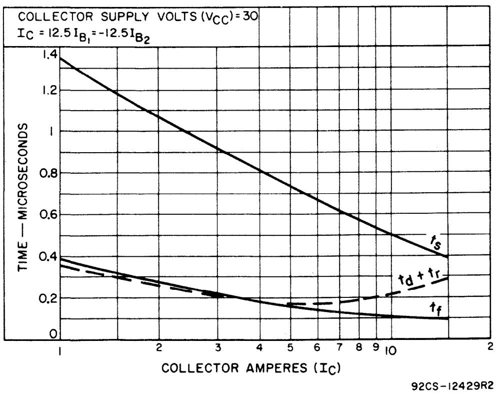
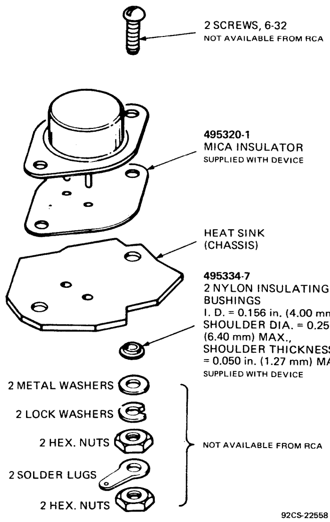


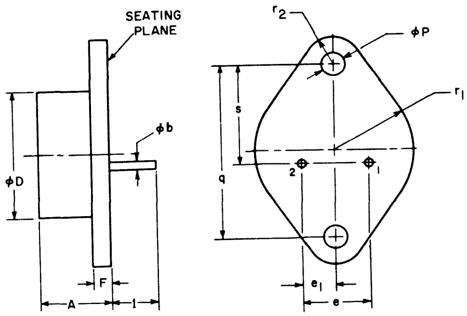
Fig. 12 - Typical saturated switching characteristics for types 2N5671 & 2N5672



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 13 - Suggested hardware for mounting types 2N5671 & 2N5672

DIMENSIONAL OUTLINE
for Types 2N5671 & 2N5672
JEDEC TO-3



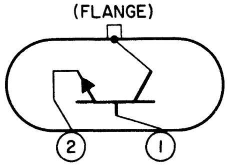
SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	.250	.450	6.35	11.43	
φb	.038	.043	.97	1.09	2
φD		.875		22.23	
e	.420	.440	10.67	11.18	
e_1	.205	.225	5.21	5.72	
F		.135		3.43	
l	.312		7.92		2
φP	.151	.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r_1		.525		13.34	
r_2		.188		4.78	
s	.655	.675	16.64	17.15	1

92CS-15222

NOTES:

1. These dimensions should be measured at points .050 in. (1.27 mm) to .055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

TERMINAL DIAGRAM

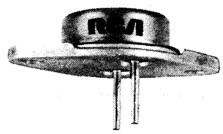


Pin 1 – Base
Pin 2 – Emitter
Mounting Flange, Case – Collector

RCA
Solid State
Division

Power Transistors

2N6032
2N6033



Modified JEDEC TO-3
(0.060-In. – Dia. Pins)

H 1627

High-Current, High-Speed, High-Power Transistors

Silicon N-P-N Types

For Switching and Amplifier Applications in Military, Industrial, and Commercial Equipment

Features:

- **Low V_{CE}(sat) = 1.0 V max. at 40 A, 1.3 V max. at 50 A**
- **Maximum Safe-Area-of-Operation Curve. . . $I_{S/b}$ limit line beginning at 24 V**
- **Fast Storage Time . . . t_s = 1.5 μs max at I_C = 40 A (2N6033) 50A (2N6032)**
- **High-Current Capability . . . V_{CE}(sat) & V_{BE} measured at I_C = 40 A (2N6033) = 50 A (2N6032)**
- **High P_T (140 W max. at T_C = 25°C)**

RCA Types 2N6032 and 2N6033* are epitaxial silicon n-p-n transistors having high-current and high-power handling capability and fast switching speed. The 2N6033 is similar to the 2N6032; they differ in maximum values for continuous collector current and sustaining voltage.

*Formerly RCA Dev. Types TA7337 and TA7337A, respectively.

MAXIMUM RATINGS, *Absolute Maximum Values:*

		2N6032	2N6033	
* COLLECTOR-TO-BASE VOLTAGE . . .	V_{CBO}	120	150	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:				
With base open	V_{CEO}(sus)	90	120	V
With external base-to-emitter resistance (R_{BE}) ≤ 50 Ω	V_{CER}(sus)	110	140	V
* With external base-to-emitter resistance (R_{BE}) ≤ 50 Ω & V_{BE} = -1.5 V	V_{CEX}(sus)	120	150	V
* EMITTER-TO-BASE VOLTAGE	V_{EBO}	7	7	V
* CONTINUOUS COLLECTOR CURRENT	I_C	50	40	A
* BASE CURRENT	I_B	10	10	A
* EMITTER CURRENT	I_E	50	40	A
* TRANSISTOR DISSIPATION:	P_T			
At case temperatures up to 25°C and V_{CE} up to 24 V		140	140	W
At case temperatures up to 25°C and V_{CE} above 24 V		See Fig. 2.		
At case temperatures above 25°C and V_{CE} above 24 V		See Figs. 2 & 5		
* TEMPERATURE RANGE:				
Storage & Operating (Junction)		-65 to +200		°C
* PIN TEMPERATURE (During Soldering):				
At distances ≥ 1/32 in. (0.8 mm) from seating plane for 10 s max		230		°C

*In accordance with JEDEC registration data format JS-6 RDF-1.

Applications:

- **Switching-control amplifiers**
- **Power gates**
- **Switching regulators**
- **Power-switching circuits**
- **Power oscillators**
- **DC-RF amplifiers**
- **Converters**
- **Inverters**
- **Control circuits**

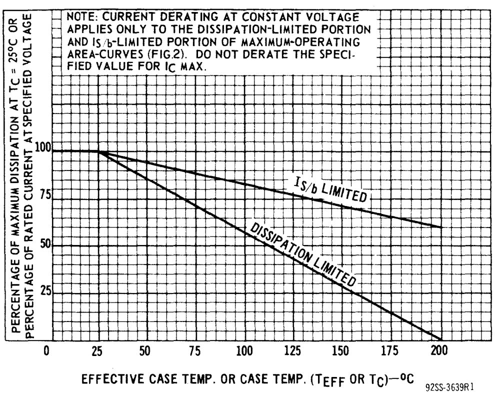


Fig. 1 – Derating curves for both types.

ELECTRICAL CHARACTERISTICS, Case Temperature (T_C) = 25°C Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: DC Collector Voltage (V) V_{CB}	V_{CE}	DC Emitter or Base Voltage (V) V_{EB}	V_{BE}	DC Current (A) I_C	I_E	I_B	LIMITS: Type 2N6032 Min.	Max.	Type 2N6033 Min.	Max.	UNITS
Collector-Cutoff Current: With base open	I_{CEO}	–	80	–	–	–	–	0	–	10	–	10	mA
* With base-emitter junction reverse biased	I_{CEV}	–	110	–	-1.5	–	–	–	–	12	–	–	mA
		–	135	–	-1.5	–	–	–	–	–	–	10	
(T_C = 150°C)		–	100	–	-1.5	–	–	–	–	15	–	10	mA
* Emitter-Cutoff Current	I_{EBO}	–	–	7	–	0	–	–	–	10	–	10	mA
Collector-to-Emitter Sustaining Voltage: *(See Figs. 12 & 13)* * With base open	V_{CEO}(sus)	–	–	–	–	0.2	–	0	90[a]	–	120[a]	–	V
With external base to emitter resistance (R_{BE}) ≤ 50 Ω	V_{CER}(sus)	–	–	–	–	0.2	–	0	110[a]	–	140[a]	–	V
With base-emitter junction reverse biased & R_{BE} ≤ 50 Ω	V_{CEX}(sus)	–	–	–	-1.5	0.2	–	0	120[a]	–	150[a]	–	V
* Base-to-Emitter Saturation Voltage[c]	V_{BE}(sat)	–	–	–	–	50	–	5	–	2	–	–	V
		–	–	–	–	40	–	4	–	–	–	2	
Base-to-Emitter Voltage	V_{BE}	–	2	–	–	50	–	–	–	2	–	–	V
		–	2	–	–	40	–	–	–	–	–	2	
* Collector-to-Emitter Saturation Voltage[c]	V_{CE}(sat)	–	–	–	–	50	–	5	–	1.3	–	–	V
		–	–	–	–	40	–	4	–	–	–	1	
* DC Forward-Current Transfer Ratio[c]	h_{FE}	–	2.6	–	–	50	–	–	10	50	–	–	
		–	2	–	–	40	–	–	–	–	10	50	
Second-Breakdown Collector Current With base forward biased	$I_{S/b}$[b]	–	24	–	–	–	–	–	5.8[c]	–	5.8[c]	–	A
		–	40	–	–	–	–	–	0.9[c]	–	0.9[c]	–	
Second-Breakdown Energy With base reverse biased (L = 310 µH, R_{BE} = 5 Ω)	$E_{S/b}$[d]	–	–	–	-4	20	–	–	62	–	62	–	mJ
* Magnitude of common-emitter small-signal, short-circuit, forward-current transfer ratio (at 5 MHz)	$\|h_{fe}\|$		10			2			10	–	10	–	
Gain-Bandwidth Product	f_T	–	10	–	–	2	–	–	50	–	50	–	MHz
Output Capacitance (at 1 MHz)	C_{obo}	10	–	–	–	–	0	–	–	800	–	800	pF
Saturated Switching Time: Turn-On (Delay Time + Rise Time)	t_{on}	V_{CC}= 30V	–	–	–	50		5[e]	–	1	–	–	µs
			–	–	–	40	–	4[e]	–	–	–	1	
* Rise	t_r	V_{CC}= 30V	–	–	–	50	–	5[e]	–	1	–	–	µs
			–	–	–	40	–	4[e]	–	–	–	1	
* Storage	t_s	V_{CC}= 30V	–	–	–	50	–	5[e]	–	1.5	–	–	µs
			–	–	–	40	–	4[e]	–	–	–	1.5	
* Fall	t_f	V_{CC}= 30V	–	–	–	50	–	5[e]	–	0.5	–	–	µs
			–	–	–	40	–	4[e]	–	–	–	0.5	
Thermal Resistance (Junction-to-Case)	$\theta_{J\text{-}C}$	–	20	–	–	2.5	–	–	–	1.25	–	1.25	°C/W

[a] CAUTION: The sustaining voltages V_{CEO}(sus), V_{CER}(sus), and V_{CEX}(sus) MUST NOT be measured on a curve tracer. These sustaining voltages should be measured by means of the test circuit shown in Fig. 12.

[b] $I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward biased for transistor operation in the active region.

[c] Pulsed; 1-s, non-repetitive pulse.

[d] $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse-bias conditions. $E_{S/b} = \frac{1}{2}LI^2$, where L is a series load or leakage inductance and I is the peak collector current.

[e] $I_{B_1} = I_{B_2}$ *In accordance with JEDEC registration format JS-6 RDF-1.

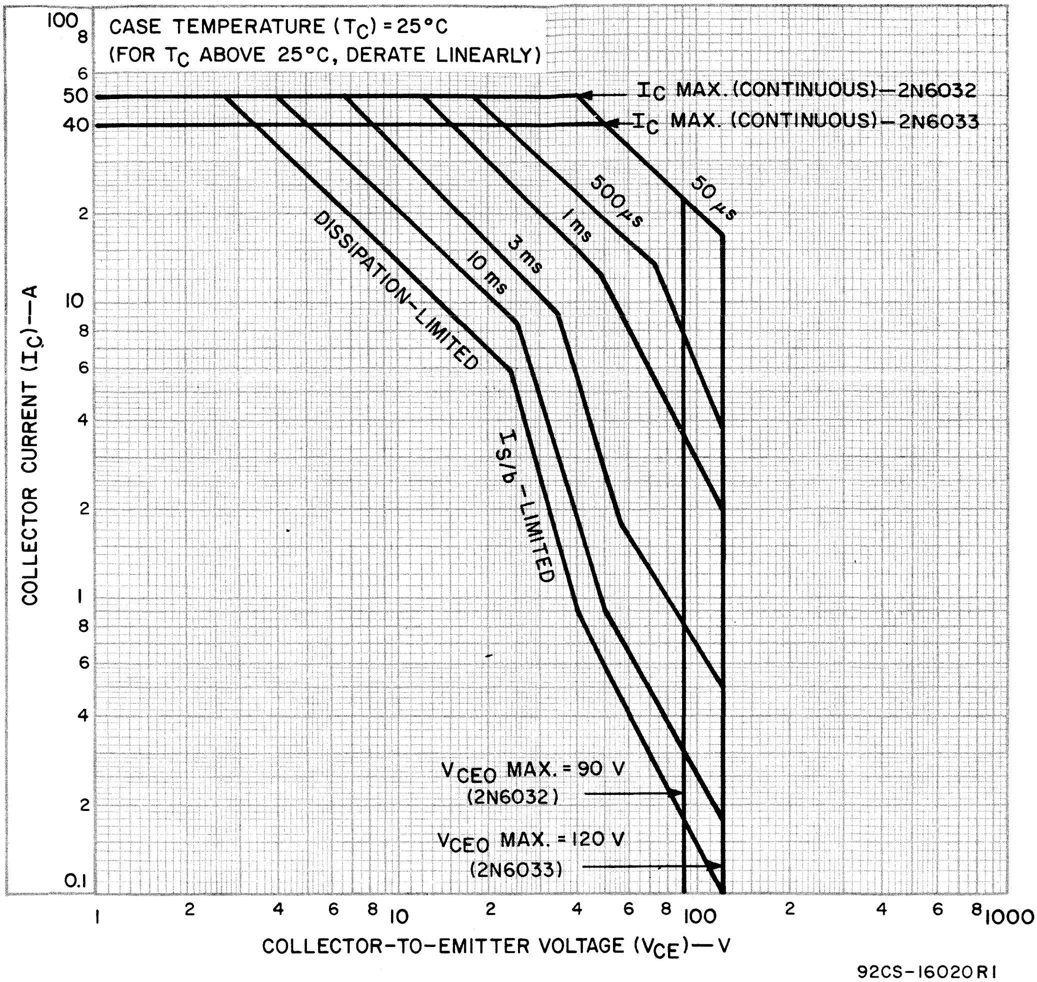


Fig. 2 — Maximum operating areas for both types.

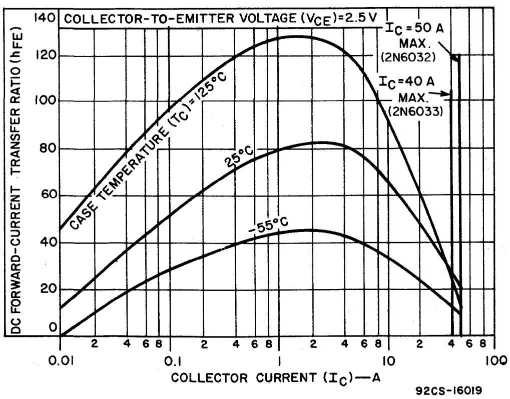


Fig. 3 – Typical dc-beta characteristic for both types.

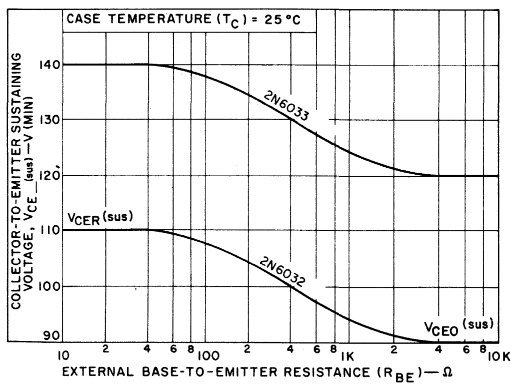


Fig. 4 – Collector-to-emitter sustaining voltage characteristics for both types.

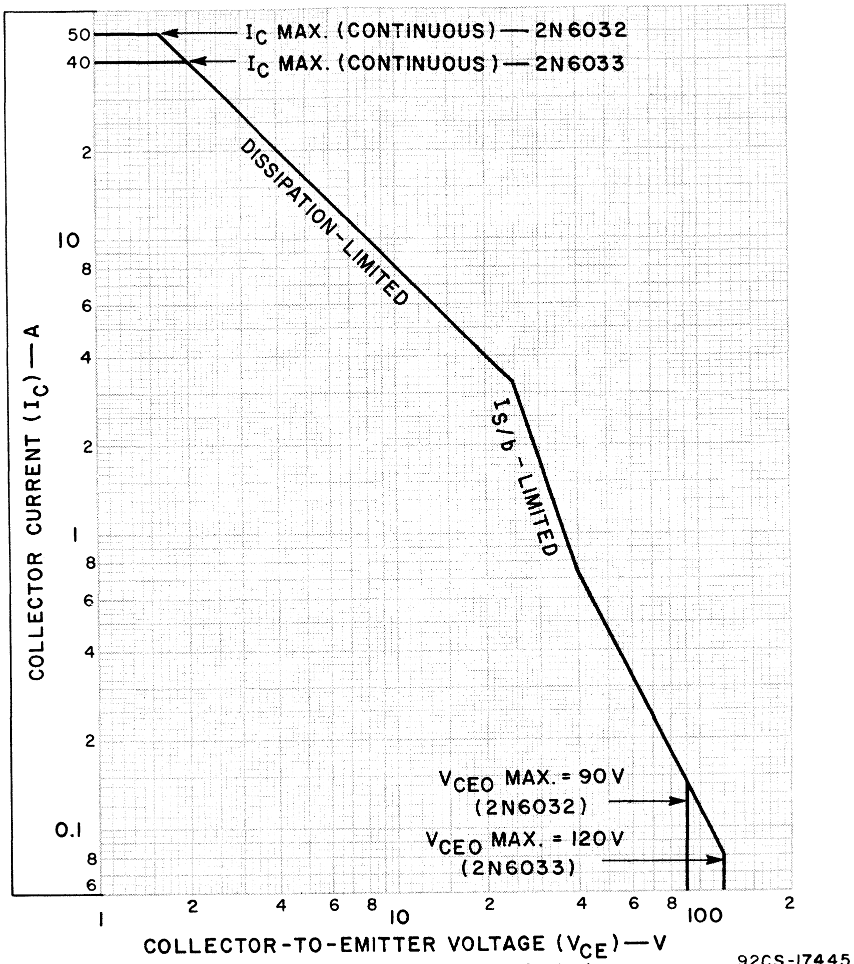


Fig. 5 — Maximum operating areas for both types at case temperature (T_C) = 100°C.

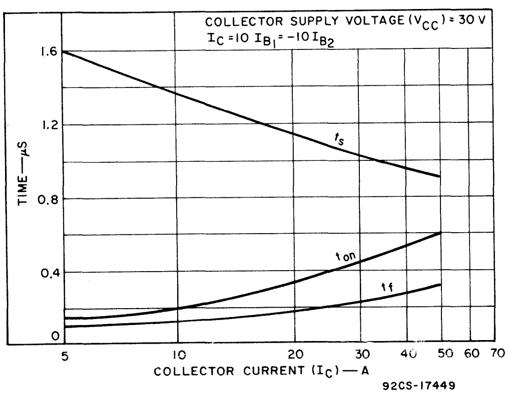


Fig. 6 — Typical saturated switching characteristics for both types.

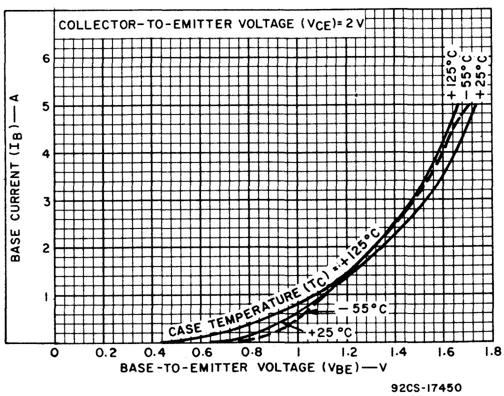


Fig. 7 — Typical input characteristics for both types.

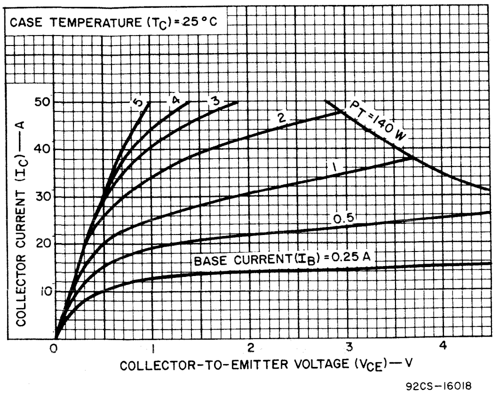


Fig. 8 — Typical collector characteristics for both types.

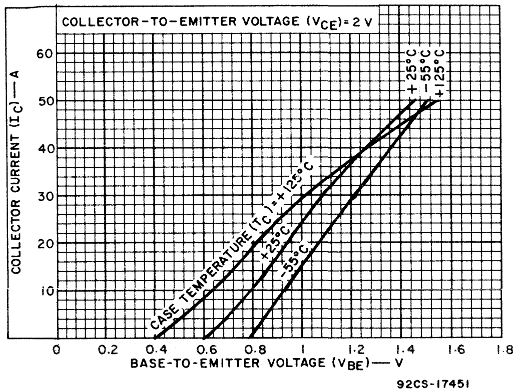


Fig. 9 — Typical transfer characteristics for both types.

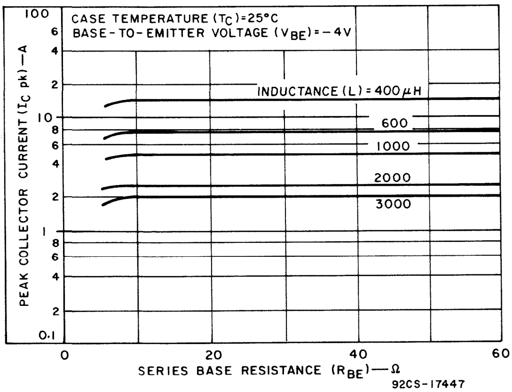


Fig. 10 — Maximum reverse-bias second-breakdown characteristics for both types.

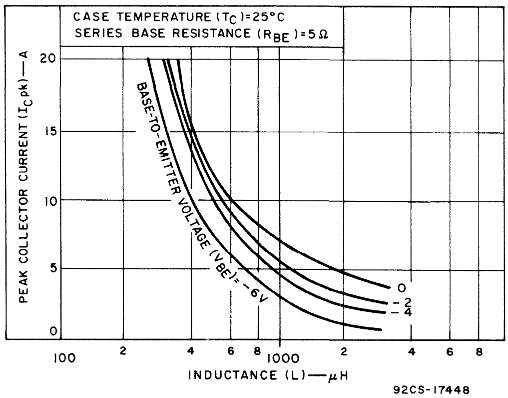


Fig. 11 — Maximum reverse-bias second-breakdown characteristics for both types.

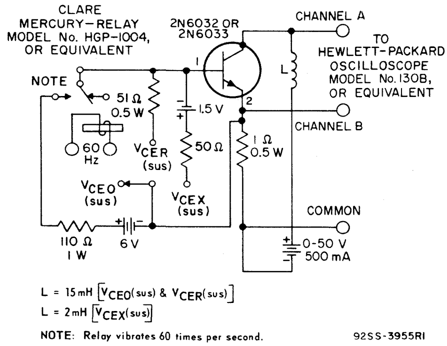


Fig. 12 — Circuit used to measure sustaining voltages $V_{CEO}(sus)$, $V_{CER}(sus)$, & $V_{CEX}(sus)$ for both types.

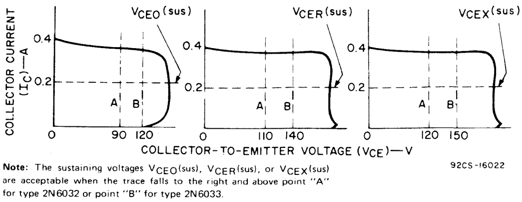


Fig. 13 — Oscilloscope display for measurement of sustaining voltages for both types. (Test circuit shown in Fig. 5).

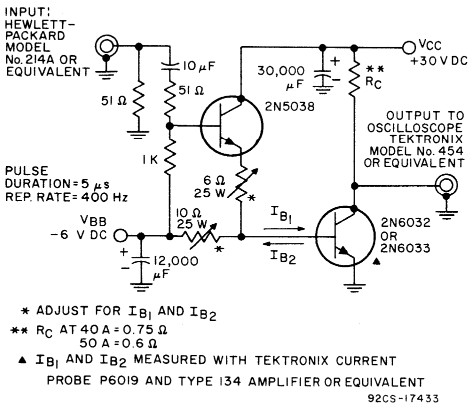
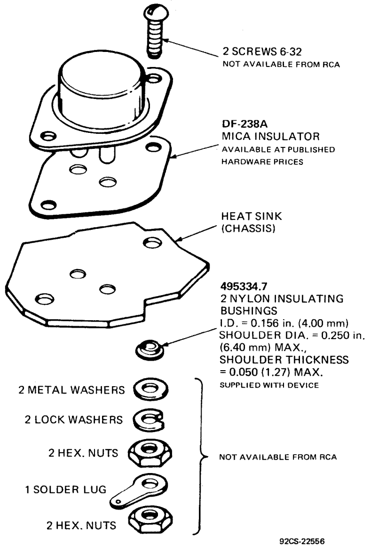


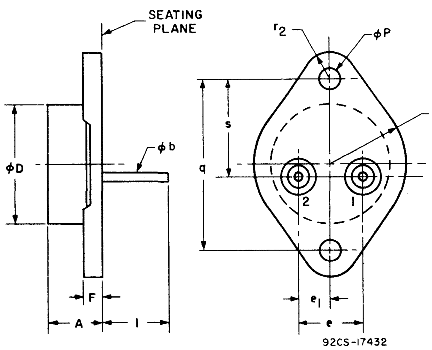
Fig. 14 — Switching-time test set.



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 15 — Suggested mounting hardware for modified TO-3 with 0.060-inch pins.

DIMENSIONAL OUTLINE
MODIFIED JEDEC TO-3 (0.060-Inch, Dia., Pins)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.300	0.350	7.62	8.89	
φb	0.059	0.061	1.50	1.55	2
φD		0.800		20.32	
e	0.420	0.440	10.67	11.18	
e1	0.205	0.225	5.21	5.72	
F		0.114		2.90	
l	0.440	0.470	11.18	11.94	2
φp	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r1		0.525		13.34	
r2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:
1. THESE DIMENSIONS SHOULD BE MEASURED AT POINTS 0.050" (1.27 mm) TO 0.055" (1.40 mm) BELOW SEATING PLANE. WHEN GAGE IS NOT USED, MEASUREMENT WILL BE MADE AT SEATING PLANE.
2. TWO LEADS.

TERMINAL CONNECTIONS
Pin 1 — Base
Pin 2 — Emitter
Case — Collector
Mounting Flange — Collector

RCA

Solid State
Division

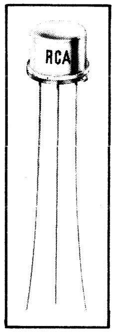
Power Transistors

2N697

RCA-2N697 is a silicon n-p-n transistor designed for use in high-speed-switching applications in military and industrial data-processing equipment.

This transistor is especially designed and processed to assure stability of characteristics and reliable performance under conditions of severe thermal and mechanical stress, and other environmental hazards.

For High-Speed Switching Service In Electronic Data-Processing Systems



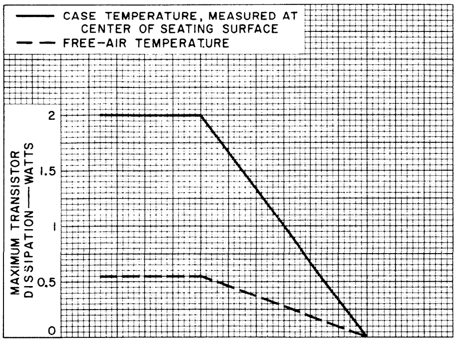
JEDEC TO-5

- tested in accordance with military specification MIL-S-19500B
- exceptional reliability
- exceptional stability of characteristics—stabilized by prolonged baking at 300°C
- typical pulse beta = 75
- low saturation voltages:
  $V_{CE}(sat)$ = 1.5 volts max. at I_C = 150 ma
  $V_{BE}(sat)$ = 1.3 volts max. at I_C = 150 ma

Maximum Ratings, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE With emitter open	60 max.	volts
EMITTER-TO-BASE VOLTAGE With collector open	5 max.	volts
COLLECTOR-TO-EMITTER VOLTAGE With external $R_{BE} \leq$ 10 ohms	40 max.	volts
COLLECTOR CURRENT	500 max.	ma
TRANSISTOR DISSIPATION:		
At case temperatures up to 25° C.	2 max.	watts
At case temperatures above 25° C.	See *Rating Chart*	
At free-air temperatures up to 25° C.	0.6 max.	watt
At free-air temperatures above 25° C.	See *Rating Chart*	
OPERATING TEMPERATURE RANGE: (Case or free-air)	-65 to +175	°C
LEAD TEMPERATURE: 1/16" ± 1/32" from case, for immersion for 10 seconds max.	255 max.	°C

R_{BE} = Base-to-emitter resistance.



Rating Chart for Type 2N697.

ELECTRICAL CHARACTERISTICS

At a free-air temperature of 25° C unless otherwise indicated

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: DC COLLECTOR-TO-BASE VOLTAGE V_{CB} volts	DC COLLECTOR-TO-EMITTER VOLTAGE V_{CE} volts	DC COLLECTOR CURRENT I_C ma	DC EMITTER CURRENT I_E ma	DC BASE CURRENT I_B ma	LIMITS min.	LIMITS typ.	LIMITS max.	UNITS
Collector-to-Base Breakdown Voltage	BV_{CBO}			0.1	0		60	75	-	volts
Emitter-to-Base Breakdown Voltage	BV_{EBO}			0	0.1		5	7.5	-	volts
Collector-to-Emitter Voltage (R_{BE} = 10 ohms)	V_{CER}			100[a]			40	50	-	volts
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$			150		15	-	0.8	1.5	volts
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$			150		15	-	1	1.3	volts
Collector-Cutoff Current:	I_{CBO}									
At T_{FA} = 25° C		30			0		-	0.01	1	μa
At T_{FA} = 150° C		30			0		-	1	100	μa
DC-Pulse Forward-Current Transfer Ratio[b]	h_{FE}		10	150			40	75	120	
Small-Signal Forward-Current Transfer Ratio	h_{fe} at 20 Mc		10	50			2.5	5	-	
Output Capacitance	C_{ob}	10			0		-	20	35	μμf
Gain-Bandwidth Product[c]	f_T						-	100	-	Mc

[a] Pulsed to prevent excessive heating of collector junction.

[b] Pulse width ≤ 12 msec, duty cycle ≤ 2%.

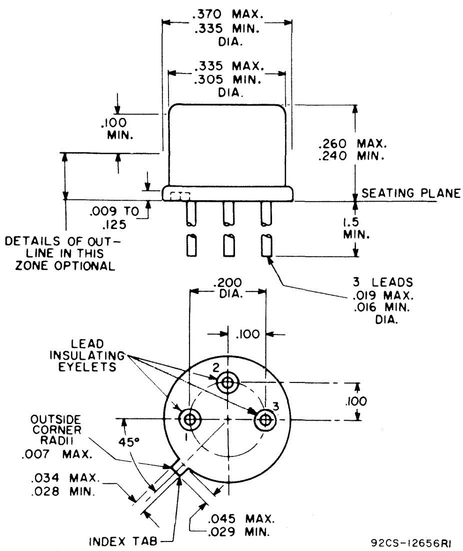
R_{BE} = External base-to-emitter resistance.

[c] Frequency at which h_{fe} = 1.

T_{FA} = Free-air temperature.

DIMENSIONAL OUTLINE FOR TYPE 2N697

JEDEC TO-5



TERMINAL CONNECTIONS

Lead No.1 - Emitter

Lead No.2 - Base

Lead No.3 - Collector

RCA

Solid State Division

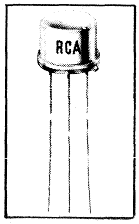
Power Transistors

2N699

RCA-2N699 is a silicon n-p-n planar transistor intended for a wide variety of small-signal and medium-power applications in military and industrial equipment. The 2N699 features a minimum gain-bandwidth product of 50 MHz making it well suited for vhf and video applications.

The junction design of the 2N699 makes possible higher breakdown voltage ratings, lower saturation voltages, higher sustaining voltages, and lower output capacitance.

For Small-Signal and Medium-Power Applications



JEDEC TO-5

- minimum gain-bandwidth product = 50 Mc
- planar construction — insures low noise and low leakage characteristics
- low output capacitance
- high breakdown voltage (BV_{CBO}) = 120 volts minimum at I_C = 0.1 ma
- low saturation voltage

Maximum Ratings, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE:		
With emitter open.	120 max.	volts
COLLECTOR-TO-EMITTER VOLTAGE:		
With external $R_{BE} \leq$ 10 ohms. .	80 max.	volts
EMITTER-TO-BASE VOLTAGE:		
With collector open.	5 max.	volts
TRANSISTOR DISSIPATION:		
At case temperatures up to 25° C . .	2 max.	watts
At case temperatures above 25° C . . .	See *Rating Chart*	
At free-air temperatures up to 25° C . .	0.6 max.	watt
At free-air temperatures above 25° C . . .	See *Rating Chart*	
TEMPERATURE RANGE:		
Storage.	-65 to +300	°C
Operating (Junction)	175	°C

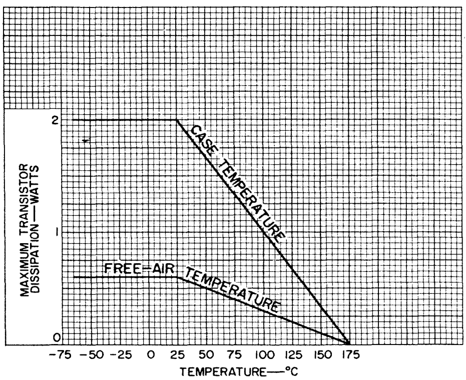


Fig. 1 – Rating Chart for Type 2N699.

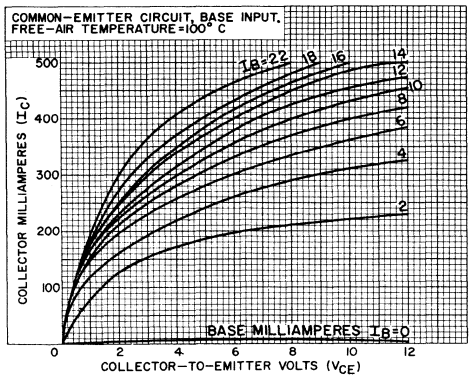


Fig. 2 – Typical Collector Characteristics at 100° C for Type 2N699.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	TEST CONDITIONS: Case Temperature °C	Frequency Kc	DC Collector-to-Base Voltage (volts) V_{CB}	DC Collector-to-Emitter Voltage (volts) V_{CE}	DC Emitter-to-Base Voltage (volts) V_{EB}	DC Collector Current (ma) I_C	DC Emitter Current (ma) I_E	DC Base Current (ma) I_B	LIMITS Min.	LIMITS Max.	Units
Collector-Cutoff Current	I_{CBO}	25		60				0		-	2	µa
Emitter-Cutoff Current	I_{EBO}	25				2	0			-	100	µa
Collector-to-Base Breakdown Voltage	BV_{CBO}	25					0.1	0		120	-	volts
DC-Pulse Forward-Current Transfer Ratio *	h_{FE}	25			10		150			40	120	
Collector-to-Emitter Sustaining Voltage with External Base-to-Emitter Resistance = 10 ohms*	$V_{CER}(sus)$	25					100			80	-	volts
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	25					150		15	-	5	volts
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$	25					150		15	-	1.3	volts
Small-Signal Forward-Current Transfer Ratio	h_{fe}	25 25 25	1 1 20 Mc		5 10 10		1 5 50			35 45 2.5	100 - -	
Output Capacitance	C_{ob}	25		10				0		-	20	pf
Input Resistance	h_{ib}	25 25	1 1		5 10		1 5			20 -	30 10	ohms ohms
Voltage-Feedback Ratio	h_{rb}	25 25	1 1		5 10		1 5			- -	2.5×10^{-4} 3×10^{-4}	
Output Conductance	h_{ob}	25 25	1 1		5 10		1 5			0.1 -	0.5 1	µmho µmho
Thermal Resistance: Junction-to-case Junction-to-free air	θ_{J-C} θ_{J-FA}	- -								- -	75 250	°C/watt °C/watt

* Pulse width ≤ 300 µsec, duty factor ≤ 2%.

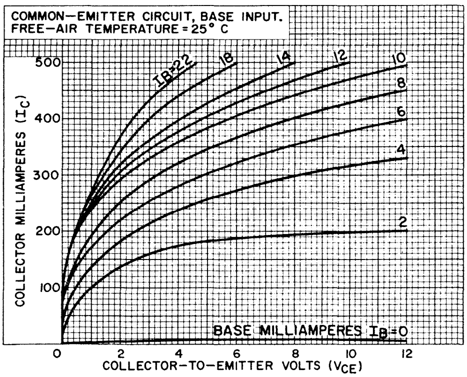


Fig.3 – Typical Collector Characteristics at 25° C for Type 2N699.

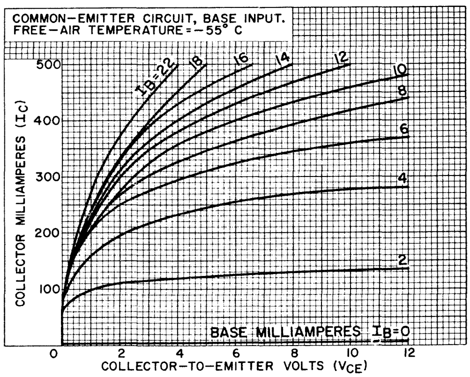


Fig.4 – Typical Collector Characteristics at -55° C for Type 2N699.

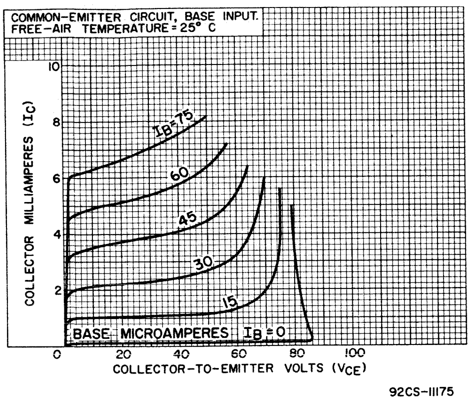


Fig.5 – Typical Collector Characteristics at 25° C for Type 2N699.

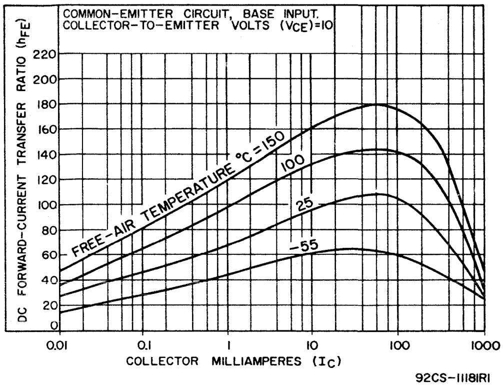


Fig.6 – Typical DC-Forward-Current Transfer-Ratio Characteristics for Type 2N699.

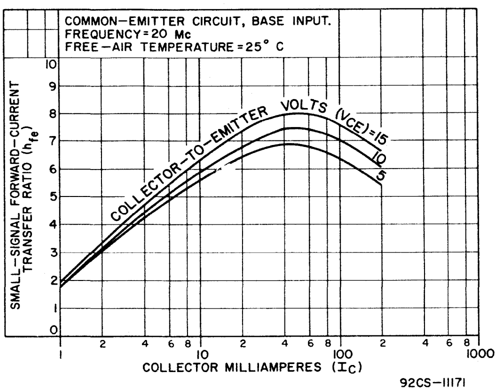


Fig.7 – Typical Small-Signal Forward-Current Transfer-Ratio Characteristics for Type 2N699.

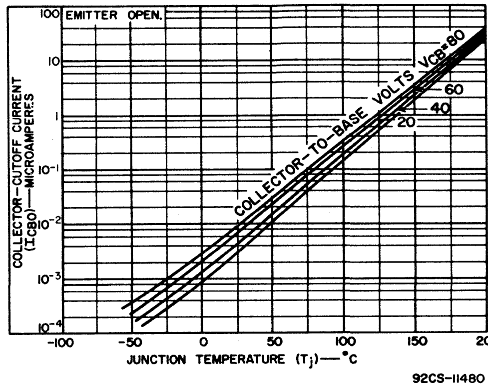
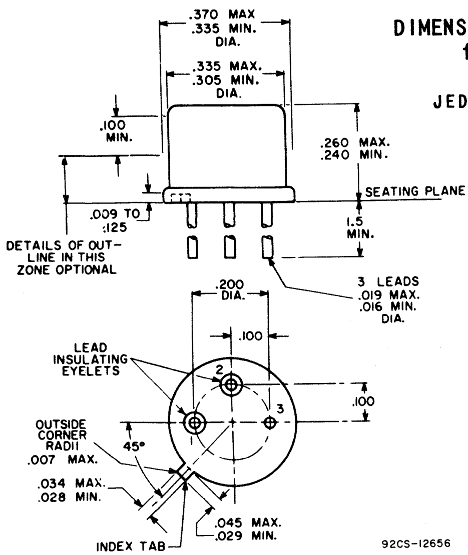


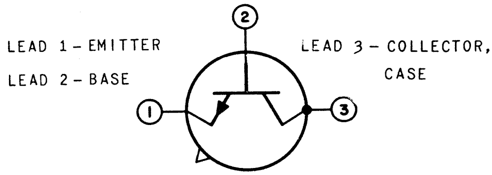
Fig.8 – Typical Collector-Cutoff-Current Characteristics for Type 2N699.

DIMENSIONAL OUTLINE for Type 2N699

JEDEC No. TO-5



TERMINAL DIAGRAM

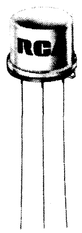


RCA

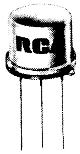
Solid State
Division

Power Transistors

2N2102
2N1613



2N2102L
2N1613L
JEDEC TO-5
H-1380



2N2102S
2N1613S
JEDEC TO-39
H-1381

Medium-Power Silicon N-P-N Planar Transistors

For Small-Signal Applications
In Industrial and Commercial Equipment

Features:

- **For operation at junction temperature up to 200°C**
- **Planar construction for low noise and low leakage**
- **Low output capacitance**

These devices are generally available with ½-inch leads (TO-39 package). They are also available in the U.S.A., Canada, Latin America, and Far East with 1½-inch leads (TO-5 package); the shorter-lead versions are specified by a suffix letter "S" after the type number, and the longer-lead versions by a suffix letter "L".

RCA-2N2102 and 2N1613 are silicon n-p-n planar transistors intended for a wide variety of small-signal and medium-power applications in military and industrial equipment. They feature exceptionally low noise, low leakage, high switching speed, and high pulsed beta.

RCA-2N2102 is a direct replacement for the 2N1613. In addition, because of its junction design, the 2N2102 has higher breakdown-voltage ratings, higher dissipation ratings, lower saturation voltages, higher sustaining voltages, and lower output capacitance.

RCA-2N2102 Features:

- **Minimum gain bandwidth product (f_T) of 120 MHz; useful in applications from dc to 20 MHz**
- **High breakdown voltage:**
  $V_{(BR)CBO}$ = 120 V min. at I_C = 0.1 mA
- **Low saturation voltages:**
  $V_{CE}(sat)$ = 0.5 V max. at I_C = 150 mA
  $V_{BE}(sat)$ = 1.1 V max. at I_C = 150 mA
- **Beta (h_{FE}) controlled over 5 decades of I_C**

MAXIMUM RATINGS, *Absolute-Maximum Values:*		**2N2102**	**2N1613**	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	120	75	V
*COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:				
With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$	80	50	V
With base open	$V_{CEO}(sus)$	65	–	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	7	7	V
COLLECTOR CURRENT	I_C	1*	1	A
*TRANSISTOR DISSIPATION:	P_T			
At case temperatures up to 25° C		5	3	W
At free-air temperatures up to 25° C		1	0.8	W
At temperatures above 25° C		See Figs. 1 and 2		
*TEMPERATURE RANGE:				
Storage and operating (Junction)		← -65 to + 200 →		°C
*LEAD TEMPERATURE (During soldering):				
At distance ⩾ 1/16 in. (1.58 mm) from seating plane for 10 s max.		← 300 →		°C

*In accordance with JEDEC registration data format

11-73

ELECTRICAL CHARACTERISTICS, *at Case Temperature (T_C) = 25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS						LIMITS				UNITS
		VOLTAGE V dc			CURRENT mA dc			2N2102		2N1613		
		V_{CB}	V_{CE}	V_{EB}	I_E	I_B	I_C	MIN.	MAX.	MIN.	MAX.	
* Collector Cutoff Current:	I_{CBO}	60			0			–	0.002	–	0.01	μA
At T_C = 150°C	I_{CBO}	60			0			–	2	–	10	μA
* Emitter Cutoff Current	I_{EBO}			5			0	–	0.002	–	0.01	μA
* Collector-to-Emitter Reachthrough Voltage	V_{RT}			-1.5	0			120	–	–	–	V
* Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$				0		0.1	120	–	75	–	V
* Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$				0.1		0	7	–	7	–	V
* Collector-to-Emitter Sustaining Voltage: With external R_{BE} = 10 Ω	$V_{CER}(sus)$						100•	80	–	50	–	V
With base open	$V_{CEO}(sus)$					0	100•	65	–	–	–	V
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					15	150•	–	0.5	–	1.5	V
* Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$					15	150•	–	1.1	–	1.3	V
* DC Forward-Current Transfer Ratio:	h_{FE}		10 10 10 10 10 10				0.01 0.1 10• 150• 500• 1000•	10 20 35 40 25 10	– – – 120 – –	– 20 35 40 20 –	– – – 120 – –	
At T_C = -55°C	h_{FE}		10				10•	20	–	20	–	
* Small-Signal Forward-Current Transfer Ratio: At f = 1 kHz 1 kHz 20 MHz	h_{fe}		5 10 10				1 5 50	30 35 3	100 150 –	30 35 3	100 150 –	
* Input Resistance (At f = 1 kHz)	h_{ib}	5 10					1 5	24 4	34 8	24 4	34 8	Ω
* Small-Signal Reverse Voltage Transfer (Feedback) Ratio (At f = 1 kHz)	h_{rb}	5 10 10					1 1 5	– – –	3×10^{-4} – 3×10^{-4}	– – –	3×10^{-4} 3×10^{-4} –	
* Output Conductance (At f = 1 kHz)	h_{ob}	5 10					1 5	0.08 0.08	0.5 1	0.05 0.1	0.5 1	μmho
* Output Capacitance	C_{ob}	10			0			–	15	–	25	pF
* Input Capacitance	C_{ib}			0.5			0	–	80	–	80	pF
* Noise Figure: Circuit Bandwidth (BW) = 1 Hz; Reference signal freq. = 1 kHz; Generator resistance (R_G) = 510 Ω (2N1613); (Z_G) = 1000 Ω (2N2102)	NF		10				0.3	–	6	–	12	dB
* Switching Time (See Fig. 14)	$t_d+t_r+t_f$							–	30	–	30	ns
Thermal Resistance: Junction-to-case Junction-to-free air	$R_{\theta JC}$ $R_{\theta JA}$							– –	35 175	– –	58.3 219	°C/W

*In accordance with JEDEC registration data format

•Pulsed. Pulse duration = 300 μsec; duty factor = 1.8% (2N2102), ≤2% (2N1613)

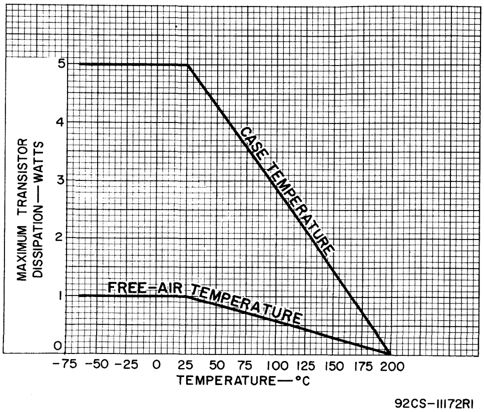


Fig.1 — Rating chart for 2N2102.

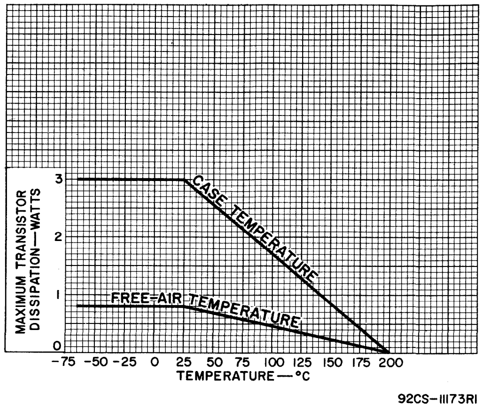


Fig.2 — Rating chart for 2N1613.

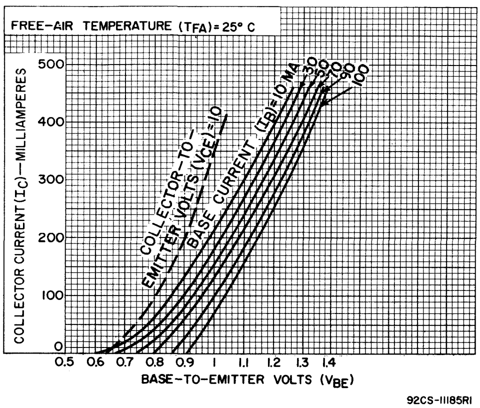


Fig.3 — Typical transfer characteristics for both types.

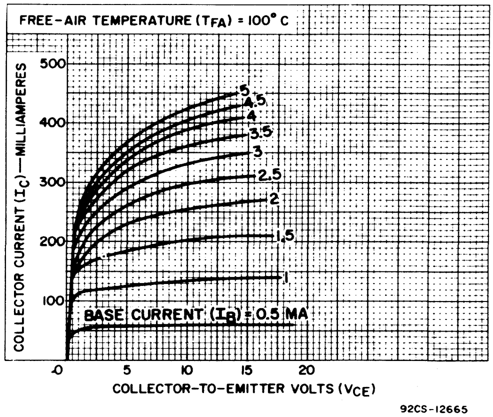


Fig.4 — Typical output characteristics for both types.

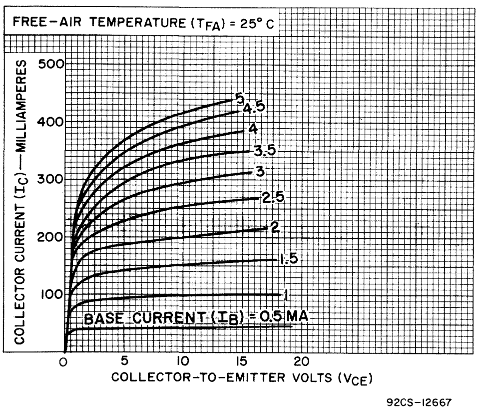


Fig.5 — Typical output characteristics for both types.

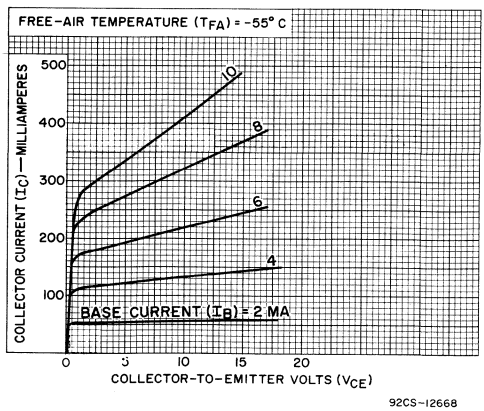


Fig.6 — Typical output characteristics for both types.

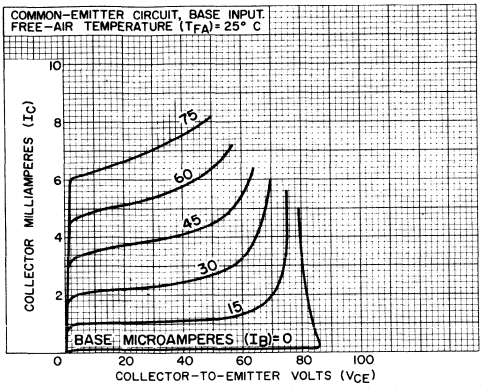


Fig.7 — Typical output characteristics for both types.

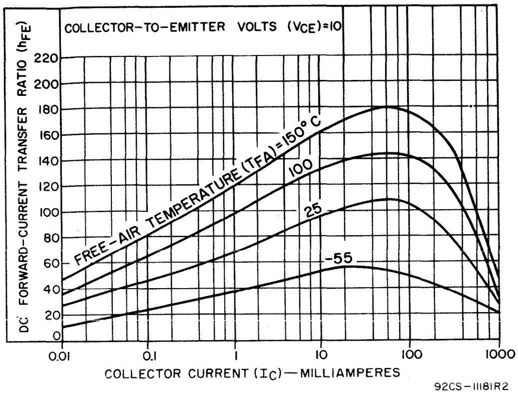


Fig.8 — Typical dc beta characteristics for both types.

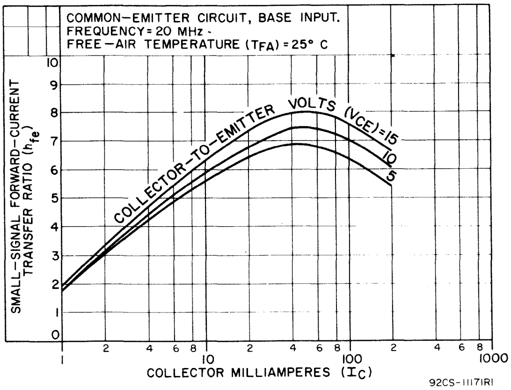


Fig.9 — Typical dc beta characteristics for both types.

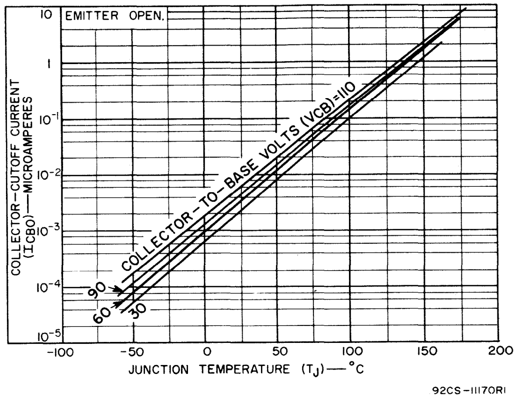


Fig.10 — Typical leakage characteristics for both types.

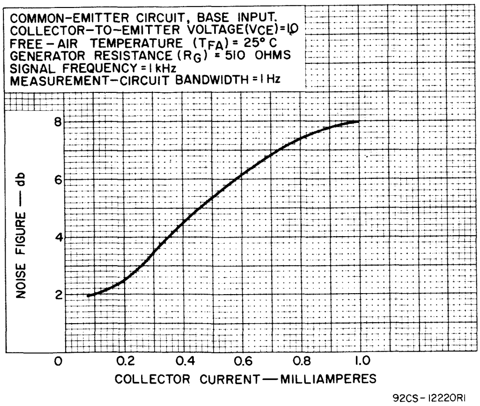


Fig.11 — Typical noise figure characteristics for both types.

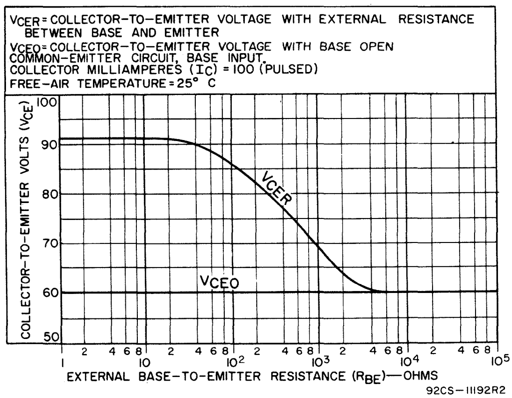


Fig.12 — Sustaining voltage vs. base-to-emitter resistance for 2N1613.

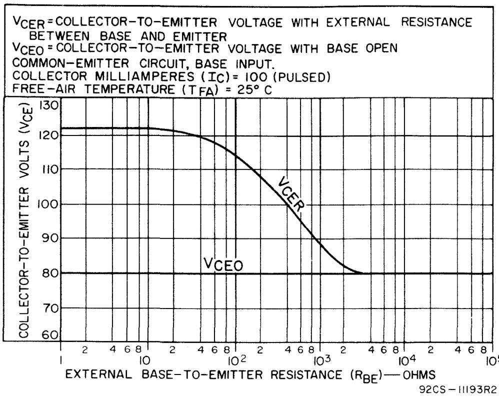
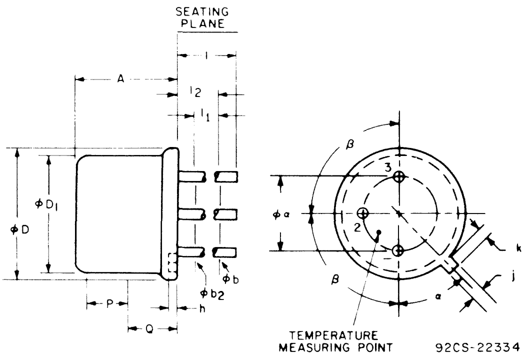


Fig.13 — Sustaining voltage vs. base-to-emitter resistance for 2N2102.

DIMENSIONAL OUTLINE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
φa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
φb	0.016	0.021	0.406	0.533	2
φb2	0.016	0.019	0.406	0.483	2
φD	0.350	0.370	8.89	9.40	
φD1	0.305	0.335	8.00	8.51	
h	0.009	0.041	0.229	1.04	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
L long lead	1.500		38.10		2
L short lead	0.500		12.70		2
l1		0.050		1.27	2
l2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and l. Diameter is uncontrolled in l_1.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

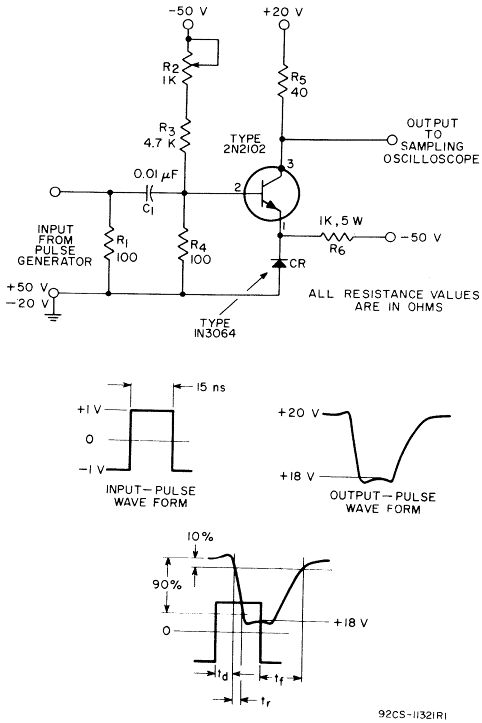


Fig.14 — Circuit for measurement of switching time, and associated waveforms.

TERMINAL CONNECTIONS

Lead 1 - Emitter
Lead 2 - Base
Case, Lead 3 - Collector

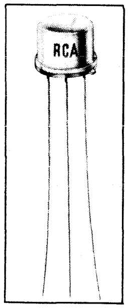
RCA Solid State Division

Power Transistors

2N1711

RCA-2N1711 is a silicon n-p-n planar transistor intended for a wide variety of small-signal and medium-power applications in military and industrial equipment. It features exceptionally low noise and low leakage characteristics, high pulse beta (h_{FE}), high breakdown voltage ratings, low saturation voltages, high sustaining voltages, and low output capacitance.

For Small-Signal and Medium-Power Applications



JEDEC TO-5

- minimum gain-bandwidth product = 70 Mc, useful in applications from dc to 25 Mc
- operation at high junction temperatures— up to 200° C
- planar construction—insures low noise and low leakage characteristics
- low saturation voltages:
  $V_{CE}(sat) = 0.5$ volt typical at $I_C = 150$ ma
  $V_{BE}(sat) = 1.1$ volts typical at $I_C = 150$ ma
- low output capacitance

Maximum Ratings, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	75 max.	volts
COLLECTOR-TO-EMITTER VOLTAGE, V_{CER}		
With external $R_{BE} \leq$ 10 ohms.	50 max.	volts
EMITTER-TO-BASE VOLTAGE, V_{EBO}	7 max.	volts
COLLECTOR CURRENT, I_C	1 max.	amp
TRANSISTOR DISSIPATION:		
At case temperatures } up to 25° C.	3 max.	watts
At case temperatures } above 25° C.	See *Fig.1*	
At free-air temperatures } up to 25° C.	0.8 max.	watt
At free-air temperatures } above 25° C.	See *Fig.1*	
TEMPERATURE RANGE:		
Storage.	-65 to +300	°C
Operating (Junction) . . .	-65 to +200	°C

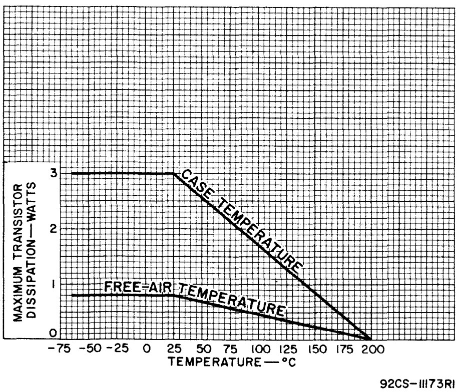


Fig. 1 - Rating Chart for Type 2N1711.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	TEST CONDITIONS								LIMITS		Units
		Case Temperature °C	Frequency kc	DC Collector-to-Base Voltage (volts) V_{CB}	DC Collector-to-Emitter Voltage (volts) V_{CE}	DC Emitter-to-Base Voltage (volts) V_{EB}	DC Collector Current (ma) I_C	DC Emitter Current (ma) I_E	DC Base Current (ma) I_B	Min.	Max.	
Collector-Cutoff Current	I_{CBO}	25 150		60 60				0 0		- -	0.01 10	μa μa
Emitter-Cutoff Current	I_{EBO}	25				5	0			-	0.005	μa
DC-Pulse Forward-Current Transfer Ratio[a]	h_{FE}	25 25 25			10 10 10		10 150 500			75 100 40	- 300 -	
DC Forward-Current Transfer Ratio	h_{FE}	25 25 -55			10 10 10		0.01 0.1 10			20 35 35	- - -	
Collector-to-Base Breakdown Voltage	BV_{CBO}	25					0.1	0		75	-	volts
Emitter-to-Base Breakdown Voltage	BV_{EBO}	25					0	0.1		7	-	volts
Collector-to-Emitter Reach-Through Voltage	V_{RT}	25				1.5[b]	0.1			75	-	volts
Collector-to-Emitter Sustaining Voltage with External Base-to-Emitter Resistance = 10 ohms	$V_{CER}(sus)$	25					100 (pulsed)			50	-	volts
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	25					150		15	-	1.5	volts
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$	25					150		15	-	1.3	volts
Small-Signal Forward-Current Transfer Ratio	h_{fe}	25 25 25	1 1 20 Mc		5 10 10		1 5 50			50 70 3.5	200 300 -	
Noise Figure: Generator resistance (R_G) = 510 ohms, circuit bandwidth (BW) = 1 cycle	NF	25	1	10			0.3			-	8	db
Output Capacitance	C_{ob}	25		10				0		-	25	pf
Input Capacitance	C_{ib}	25				0.5	0			-	80	pf
Input Resistance	h_{ib}	25 25	1 1	5 10			1 5			24 4	34 8	ohms ohms
Voltage-Feedback Ratio	h_{rb}	25 25	1 1	5 10			1 5			- -	5×10^{-4} 5×10^{-4}	
Output Conductance	h_{ob}	25 25	1 1	5 10			1 5			0.1 0.1	0.5 1	μmho μmho
Thermal Resistance: Junction-to-case Junction-to-free air	θ_{J-C} θ_{J-FA}	- -								- -	58.3 219	°C/watt °C/watt

[a] Pulse duration, 300 μsec; duty factor, 1.8%.

[b] V_{EBF} = Emitter-to-base floating potential.

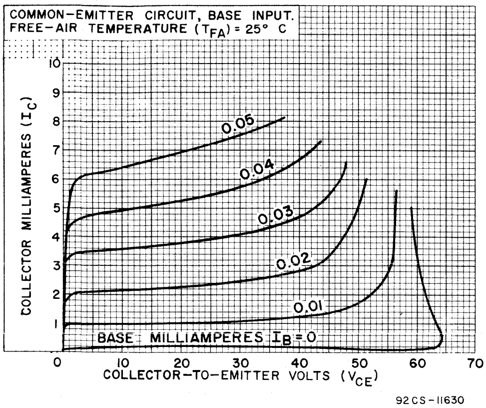


Fig. 2 - Typical Collector Characteristics at 25^{o} C for Type 2N1711.

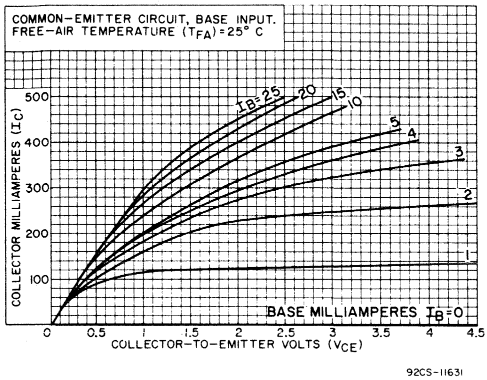


Fig. 5 - Typical Collector Characteristics at 25^{o} C for Type 2N1711.

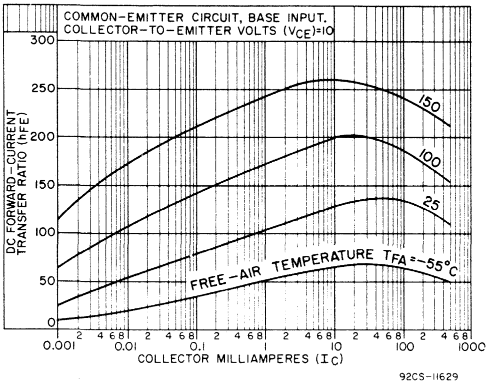


Fig. 3 - Typical DC - Forward - Current Transfer - Ratio Characteristics for Type 2N1711.

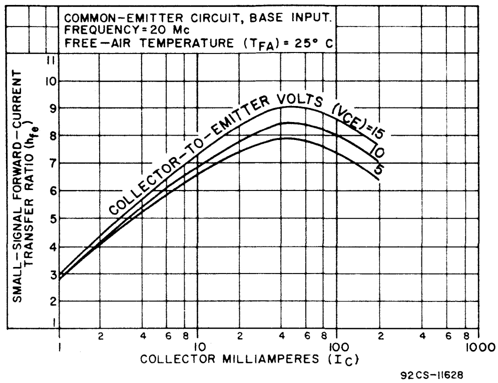


Fig. 6 - Typical Small - Signal Forward-Current Transfer - Ratio Characteristics for Type 2N1711.

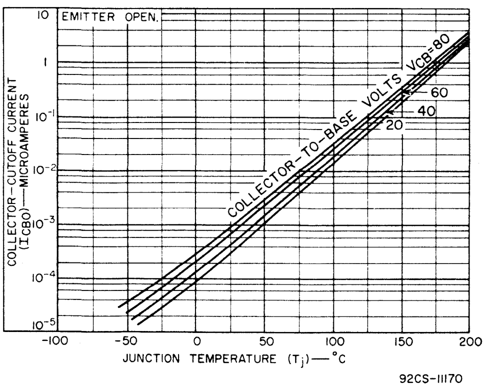


Fig. 4 - Typical Collector - Cutoff - Current Characteristics for Type 2N1711.

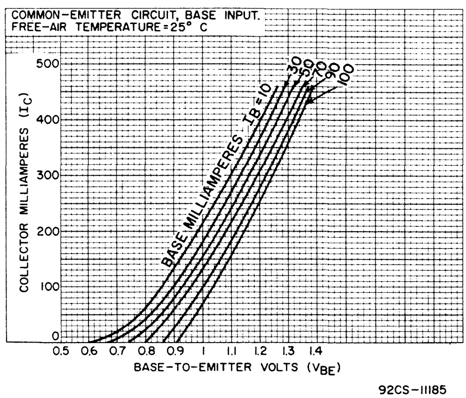


Fig. 7 - Typical Transfer Characteristics for Type 2N1711.

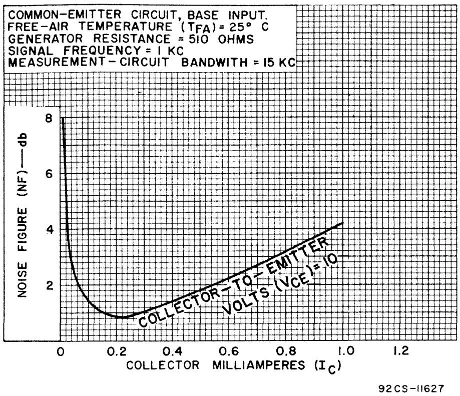
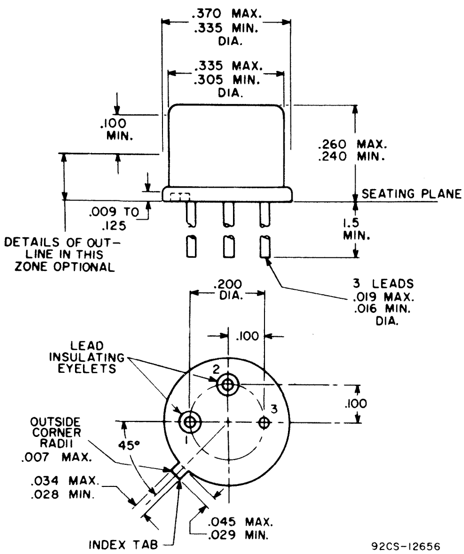
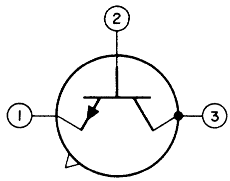


Fig. 8 - Typical AF-Noise-Figure Characteristic for Type 2N1711.

DIMENSIONAL OUTLINE
JEDEC No. TO-5



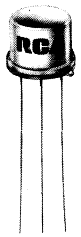
TERMINAL DIAGRAM



LEAD 1 – EMITTER
LEAD 2 – BASE
LEAD 3 – COLLECTOR, CASE

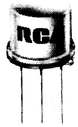
RCA
Solid State Division

Power Transistors
2N2405
2N1893



2N1893L
2N2405L
JEDEC TO-5

H-1380



2N1893S
2N2405S
JEDEC TO-39

H-1381

Medium-Power Silicon N-P-N Planar Transistors

For Small-Signal Applications
In Industrial and Commercial Equipment

Features:

- **For operation at junction temperature up to 200°C**
- **Planar construction for low noise and low leakage**
- **Low output capacitance**

These devices are generally available with ½-inch leads (TO-39 package). They are also available in the U.S.A., Canada, Latin America, and Far East with 1½-inch leads (TO-5 package); the shorter-lead versions are specified by a suffix letter "S" after the type number, and the longer-lead versions by a suffix letter "L".

RCA-2N2405▲ and 2N1893 are silicon n-p-n planar transistors intended for a variety of small-signal and medium-power applications. They feature exceptionally high collector-to-emitter sustaining voltage, low leakage characteristics, high switching speeds, and high pulse beta (h_{FE}).

RCA-2N2405 is a direct replacement for type 2N1893 for most applications. In addition, the 2N2405 has higher voltage ratings, lower saturation voltages, and higher sustaining voltages than the 2N1893.

▲ Formerly Dev. Type TA2235A.

RCA-2N2405 Features:

- **Minimum gain-bandwidth product (f_T) of 120 MHz; useful in applications from dc to 50 MHz**
- **High sustaining voltage:**
  $V_{CEO}(sus)$ = 90 V min.
- **Low saturation voltages:**
  $V_{CE}(sat)$ = 0.5 V max. at I_C = 150 mA
  $V_{BE}(sat)$ = 1.1 V max. at I_C = 150 mA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N2405	2N1893	
*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	120	120	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:				
With external base-to-emitter resistance (R_{BE}) ≤ 10 Ω	$V_{CER}(sus)$	140	100	V
With base-emitter junction reverse-biased	$V_{CEX}(sus)$	120●	120	V
* With base open	$V_{CEO}(sus)$	90	80	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	7	7	V
*COLLECTOR CURRENT	I_C	1	0.5	A
*TRANSISTOR DISSIPATION:	P_T			
At case temperatures up to 25°C		5	3	W
At free-air temperatures up to 25°C		1	0.8	W
At temperatures above 25°C		See Figs. 1 and 2		
*TEMPERATURE RANGE:				
Storage and operating (Junction)		← −65 to +200 →		°C
*LEAD TEMPERATURE (During soldering):				
At distance from seating plane for 10 s max. ≥ 1/16 in. (1.58 mm) for 2N1893 and ≥ 1/32 in. (0.8 mm) for 2N2405		← 255 →		°C

* In accordance with JEDEC registration data format (JS-9 RDF-2)

● R_{BE} = 500 Ω (2N2405)

ELECTRICAL CHARACTERISTICS, *Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: DC Collector Voltage (V) V_{CB}	DC Collector Voltage (V) V_{CE}	DC Emitter Voltage (V) V_{EB}	DC Current (mA) I_C	DC Current (mA) I_E	DC Current (mA) I_B	LIMITS Type 2N2405 Min.	Type 2N2405 Max.	Type 2N1893 Min.	Type 2N1893 Max.	UNITS
* Collector-Cutoff Current:	I_{CBO}	90				0		-	0.01	-	0.01	μA
T_C = 150°C		90				0		-	10	-	15	
* Emitter-Cutoff Current	I_{EBO}			5	0			-	0.01	-	0.01	μA
Collector-to-Emitter Sustaining Voltage: * With base open	$V_{CEO}(sus)$				100ᵃ		0	90	-	-	-	V
					30ᵃ		0	90	-	80	-	
* With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{CER}(sus)$				100ᵃ			140	-	100	-	V
(R_{BE}) = 500 Ω					100ᵃ			120	-	-	-	
* Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$				0.1	0		120	-	120	-	V
* Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$				0	0.1		7	-	7	-	V
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				150ᵃ		15	-	0.5	-	5	V
					50ᵃ		5	-	0.2	-	1.2	
* Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$				150ᵃ		15	-	1.1	-	1.3	V
					50ᵃ		5	-	0.9	-	0.9	
* DC Forward-Current Transfer Ratio	h_{FE}		10		150ᵃ			60	200	40	120	
*			10		10ᵃ			35	-	35	-	
*			10		0.1			-	-	20	-	
* T_C = -55°C	h_{FE}		10		10			20	-	-	-	
			10		10			-	-	20	-	
Small-Signal Forward-Current Transfer Ratio: * f = 1 kHz	h_{fe}		5		1			-	-	30	100	
* 1 kHz			5		5			50	275	-	-	
* 1 kHz			10		5			-	-	45	-	
* 20 MHz			10		50			-	-	2.5	-	
20 MHz			10		50			6	-	-	-	
* Input Resistance (at f = 1 kHz)	h_{ib}	5			1			24	34	20	30	Ω
		10			5			4	8	4	8	
* Voltage-Feedback Ratio (at f = 1 kHz)	h_{rb}	5			1			-	3×10^{-4}	-	1.25×10^{-4}	
		10			5			-	3×10^{-4}	-	1.5×10^{-4}	
* Output Conductance (at f = 1 kHz)	h_{ob}	5			1			-	0.5	-	0.5	μmho
		10			5			-	0.5	-	0.5	
* Output Capacitance	C_{obo}	10				0		-	15	-	15	pF
* Input Capacitance	C_{ibo}			0.5	0			-	80	-	85	pF
Noise Figure (Wide-Band) Generator resistance (R_G) = 500 Ω Circuit Bandwidth (BW) = 15 kHz Reference signal frequency = 1 kHz	NF	10			0.3			-	6	-	-	dB
* Thermal Resistance: Junction-to-case	$\theta_{J\text{-}C}$							-	35	-	58.3	°C/W
Junction-to-ambient	$\theta_{J\text{-}A}$							-	175	-	219	

ᵃ Pulsed. Pulse duration = 300 μsec max.; duty factor ≤ 2%.

* In accordance with JEDEC registration data format (JS-9 RDF-2).

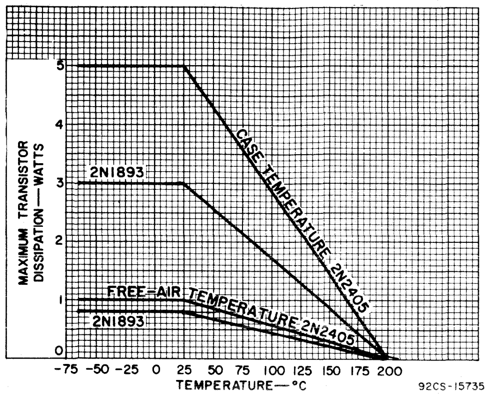


Fig.1 — Dissipation derating curves for types 2N2405 and 2N1893.

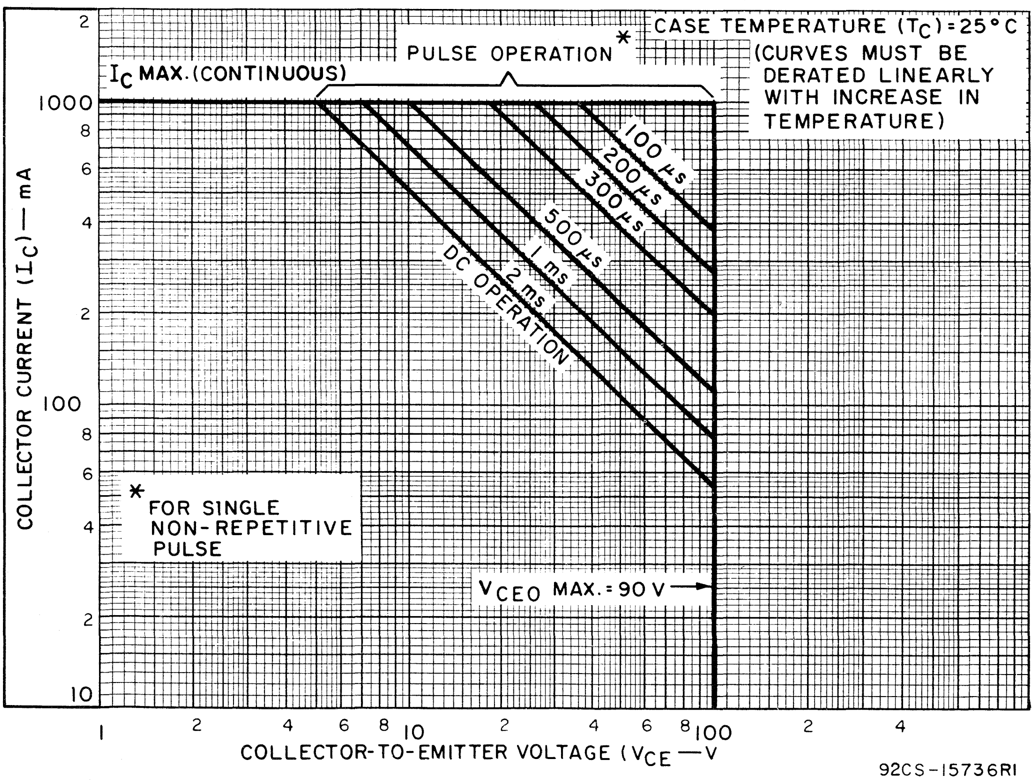


Fig.2 — Maximum operating areas for type 2N2405.

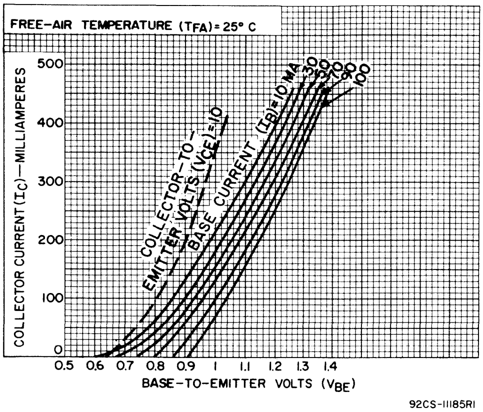


Fig.3 - Typical transfer characteristics for types 2N2405 and 2N1893.

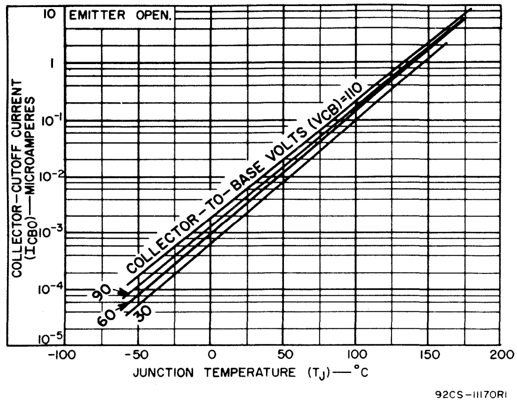


Fig.4 - Typical cutoff characteristics for types 2N2405 and 2N1893.

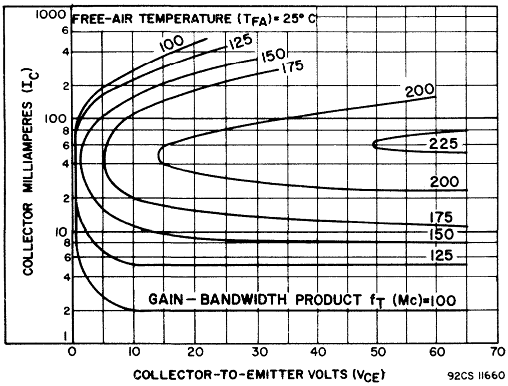


Fig.5 - Typical gain bandwidth product characteristics for types 2N2405 and 2N1893.

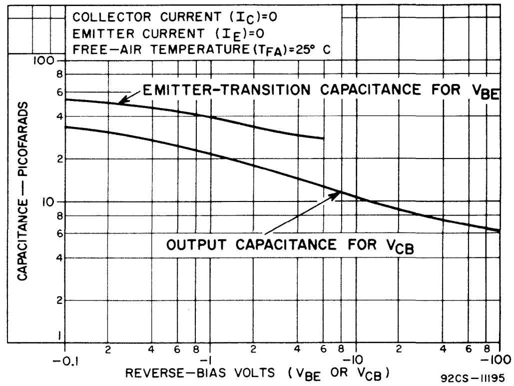


Fig.6 - Typical capacitance characteristics for types 2N2405 and 2N1893.

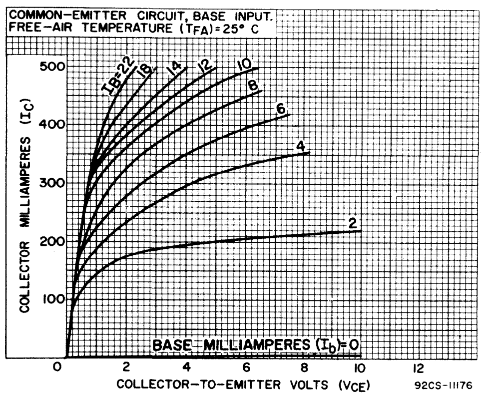


Fig.7 - Typical collector characteristics at 25°C for type 2N2405.

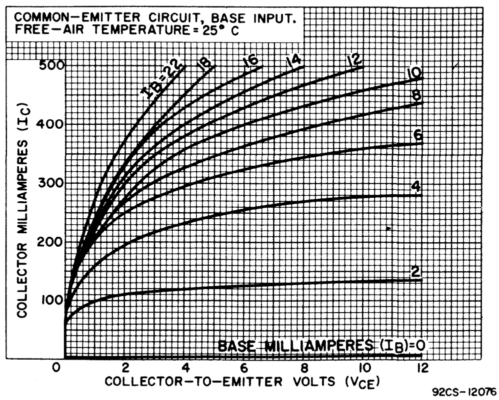


Fig.8 - Typical collector characteristics at 25°C for type 2N1893.

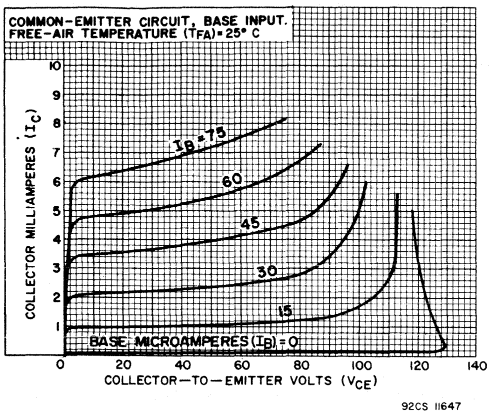


Fig.9 - Typical collector characteristics at 25°C for type 2N2405.

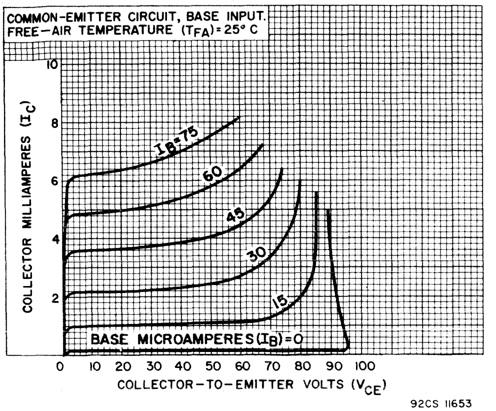


Fig.10 - Typical collector characteristics at 25°C for type 2N1893.

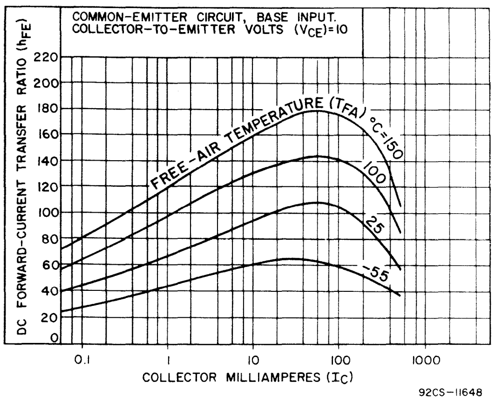


Fig.11 - Typical dc-beta characteristics for types 2N2405 and 2N1893.

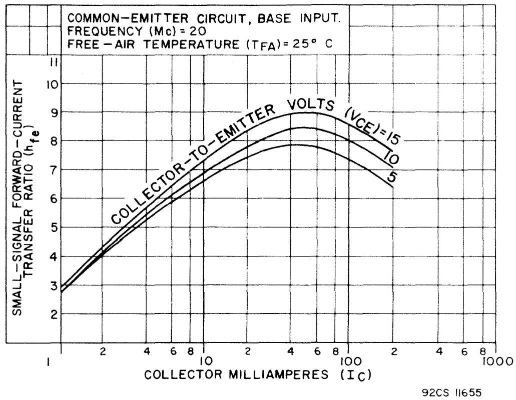


Fig.12 - Typical small-signal beta characteristics for types 2N2405 and 2N1893.

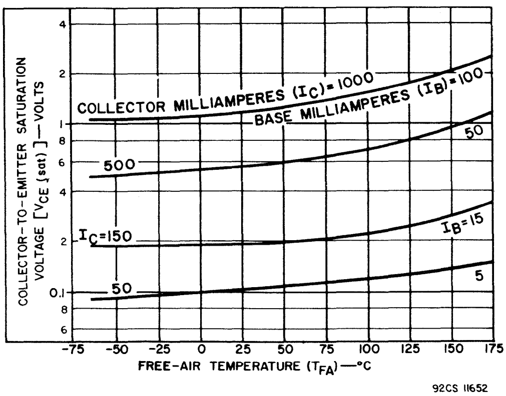


Fig.13 - Typical saturation characteristics for types 2N2405 and 2N1893.

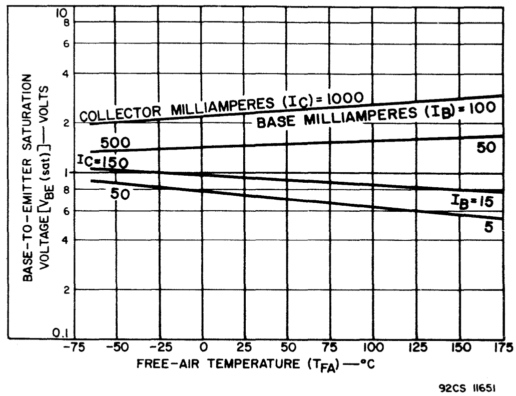


Fig.14 - Typical saturation characteristics for types 2N2405 and 2N1893.

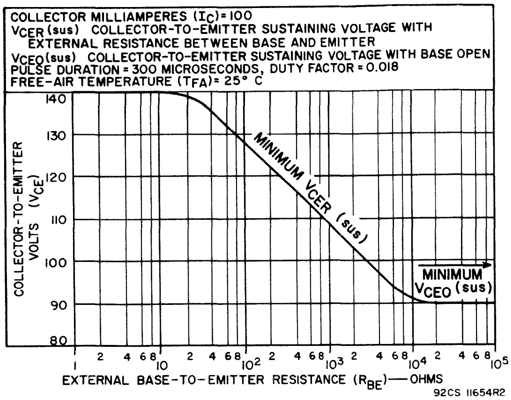


Fig.15 - Sustaining voltage characteristic for type 2N2405.

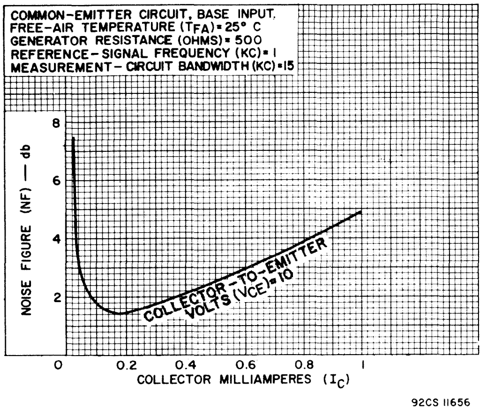


Fig.16 - Typical wide-band noise characteristic for type 2N2405.

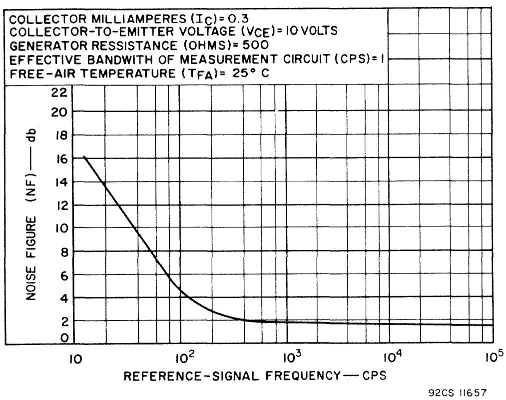
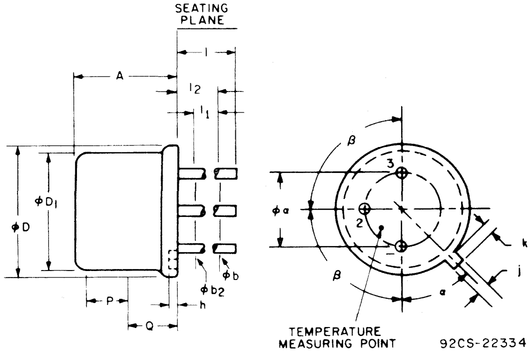


Fig.17 - Typical narrow-band noise characteristic for type 2N2405.

DIMENSIONAL OUTLINE



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
ϕa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
ϕb	0.016	0.021	0.406	0.533	2
ϕb_2	0.016	0.019	0.406	0.483	2
ϕD	0.350	0.370	8.89	9.40	
ϕD_1	0.305	0.335	8.00	8.51	
h	0.009	0.041	0.229	1.04	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
L long lead	1.500		38.10		2
L short lead	0.500		12.70		2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and l. Diameter is uncontrolled in l_1.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

TERMINAL DESIGNATIONS

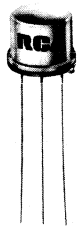
Lead 1 - Emitter
Lead 2 - Base
Lead 3 - Collector, Case

RCA

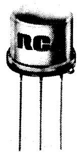
Solid State Division

Power Transistors

2N2270



2N2270L
JEDEC TO-5
H-1380



2N2270S
JEDEC TO-39
H-1381

Silicon N-P-N Planar Transistor

General-Purpose Type for Small-Signal, Medium-Power Applications

Features:

- **Minimum gain-bandwidth product = 100 MHz; useful in applications from dc to 20 MHz**
- **Operation at high junction temperatures**
- **Planar construction for low-noise and low-leakage characteristics**
- **Very low output capacitance**

These devices are generally available with ½-inch leads (TO-39 package). They are also available in the U.S.A., Canada, Latin America, and Far East with 1½-inch leads (TO-5 package); the shorter-lead versions are specified by a suffix letter "S" after the type number, and the longer-lead versions by a suffix letter "L".

RCA-2N2270 is a silicon n-p-n planar transistor intended for a wide variety of small-signal and medium-power applications in military and industrial equipment. It features exceptionally low noise and leakage characteristics, and very low output capacitance.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

* COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	60	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter resistance (R_{BE}) ≤ 10 Ω	V_{CER}	60	V
* With base open	V_{CEO}	45	V
* EMITTER-TO-BASE VOLTAGE	V_{EBO}	7	V
* COLLECTOR CURRENT	I_C	1	A
* TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25°C		5	W
At case temperatures above 25°C		See Fig. 1	
At free-air temperatures up to 25°C		1	W
At free-air temperatures above 25°C		See Fig. 1	
* TEMPERATURE RANGE:			
Storage and operating (Junction)		-65 to +200	°C
* LEAD TEMPERATURE (During soldering):			
At distance ≥ 1/16 in. (1.58 mm) from seating plane for 10 s max		230	°C

* In accordance with JEDEC registration data format (JS-6 RDF-1)

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ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	VOLTAGE V V_{CB}	VOLTAGE V V_{CE}	VOLTAGE V V_{EB}	CURRENT mA I_C	CURRENT mA I_E	CURRENT mA I_B	LIMITS MIN.	LIMITS MAX.	UNITS
* Collector Cutoff Current: With emitter open	I_{CBO}	60				0		–	0.05	µA
At T_C = 150°C		60				0		–	50	
* Emitter Cutoff Current	I_{EBO}			5	0			–	0.1	µA
* Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$				0.05 µA	0		60	–	V
* Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$				0	0.1		7	–	V
* Collector-to-Emitter Sustaining Voltage: With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{CER}(sus)$				100[a]			60	–	V
With base open	$V_{CEO}(sus)$				100[a]		0	45	–	
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				150[a]		15	–	0.9	V
* Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$				150[a]		15	–	1.2	V
* DC Forward Current Transfer Ratio	h_{FE}		10		150[a]			50	200	
			10		1			30	–	
* Small-Signal Forward Current Transfer Ratio: f = 1 kHz	h_{fe}		10		5			50	275	
f = 20 MHz			10		50			5	–	
* Gain-Bandwidth Product	f_T		10		50			100	–	MHz
* Noise Figure: Generator resistance (R_G) = 1 kΩ Circuit bandwidth (BW) = 1 Hz f = 1 kHz	NF		10 (V_{cc})		0.3			–	10	dB
* Output Capacitance	C_{ob}	10				0		–	15	pF
* Input Capacitance	C_{ib}			0.5	0			–	80	pF
* Saturated Switching Time (See Fig. 8)	$t_d+t_r+t_s+t_f$							–	30	ns
* Thermal Resistance: Junction-to-case	$R_{\theta JC}$							–	35	°C/W
Junction-to-free air	$R_{\theta FA}$							–	175	

* In accordance with JEDEC registration data format (JS-6 RDF-1)

[a] Pulsed: Pulse duration = 300 µs; duty factor = 1.8%

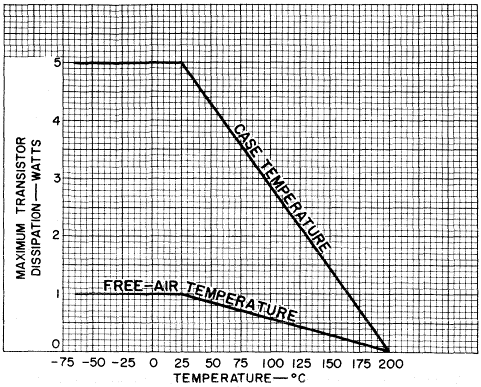


Fig. 1—Rating chart.

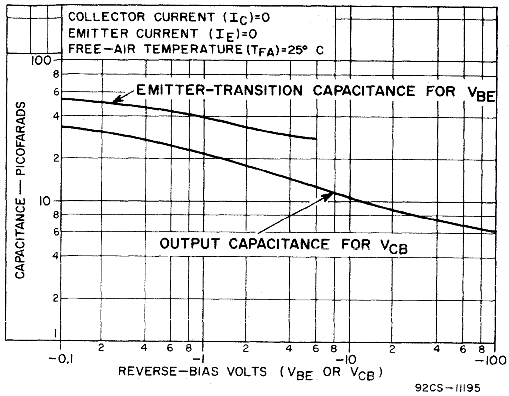


Fig. 2—Typical emitter-transition-capacitance and output-capacitance characteristics.

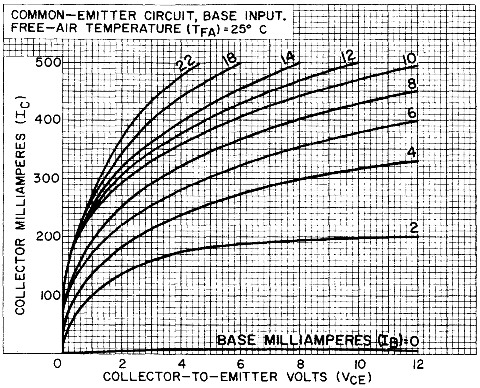


Fig. 3—Typical collector characteristics.

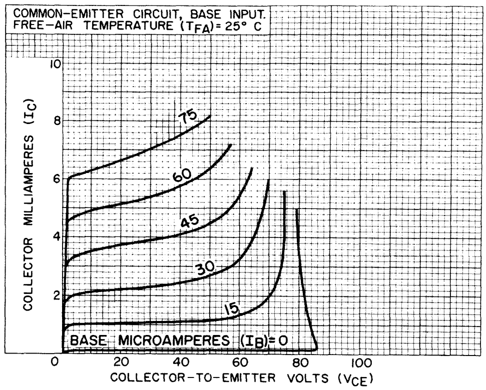


Fig. 4—Typical collector characteristics.

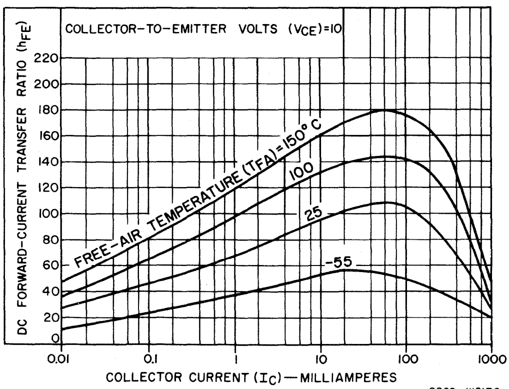


Fig. 5—Typical dc forward-current transfer ratio characteristics.

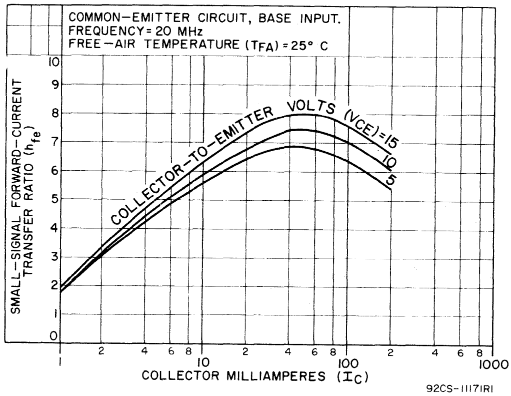


Fig. 6—Typical small-signal forward-current transfer ratio characteristics.

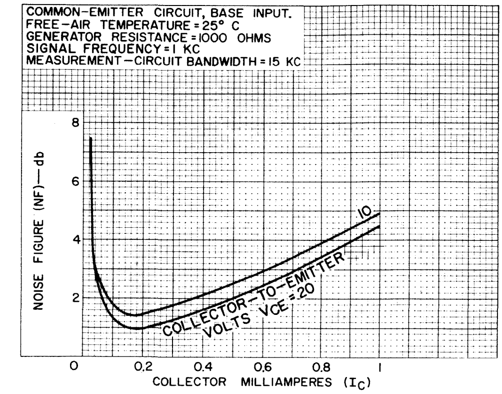


Fig. 7—Typical af noise-figure characteristics.

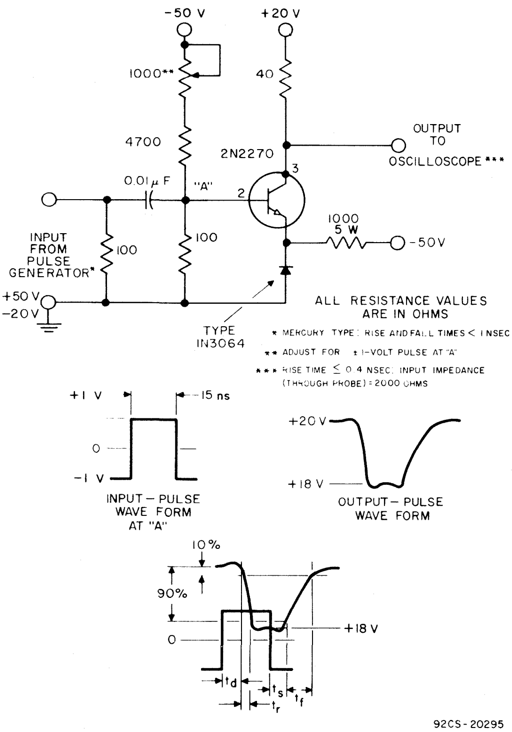
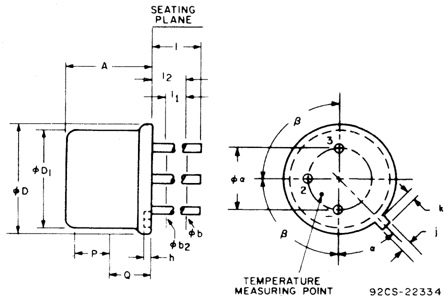


Fig. 8—Test circuit for measurement of saturated switching time and associated waveforms.

DIMENSIONAL OUTLINE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
φa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
φb	0.016	0.021	0.406	0.533	2
φb2	0.016	0.019	0.406	0.483	2
φD	0.350	0.370	8.89	9.40	
φD1	0.305	0.335	8.00	8.51	
h	0.009	0.041	0.229	1.04	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
L long lead	1.500		38.10		2
L short lead	0.500		12.70		2
l1		0.050		1.27	2
l2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and l. Diameter is uncontrolled in l_1.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

TERMINAL CONNECTIONS

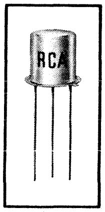
Lead 1 — Emitter
Lead 2 — Base
Lead 3 — Collector, Case

For basic transistor theory, circuits, and application information, refer to "RCA Solid State Power Circuits Designer's Handbook", SP-52, or "RCA Transistor, Thyristor, & Diode Manual", SC-15.

RCA Solid State Division

Power Transistors
2N2895 2N2896 2N2897

For Small-Signal and Low-to-Medium-Power Applications



JEDEC TO-18

RCA-2N2895, 2N2896, and 2N2897 are silicon n-p-n planar transistors intended for a wide variety of small-signal and low-to-medium-power applications in military and industrial equipment.

These transistors are TO-18 versions of RCA's versatile 2N2102 family of n-p-n triple-diffused silicon transistors for small-signal and medium-power military and industrial applications.

Like the 2N2102, the 2N2895 offers five levels of beta control from 0.1 ma to 0.5 ampere.

High-voltage type 2N2896 offers a BV_{CEO} of 90 volts min. and V_{CER} (sus) of 140 volts min., controlled for values of R_{BE} from 0 to 100,000 ohms.

RCA-2N2897 is an economy version offering many of the advantages of the 2N2896.

These transistors feature extremely low leakage characteristics, high pulse dc beta, high small-signal beta, very low output capacitance, and large gain-bandwidth products. Type 2N2895 also has an exceptionally low noise figure of 8 db max.

FEATURES:

- high mimimum gain-bandwidth products –
  120 Mc for 2N2895, 2N2896
  100 Mc for 2N2897
  useful in applications from dc to 40 Mc
- planar construction – for low noise and low leakage characteristics
- operation at high junction temperatures – up to 200° C
- very low output capacitance – 15 pf max.
- high switching-speed capabilities (non-sat)

Maximum Ratings, *Absolute-Maximum Values:*

	2N2895	2N2896	2N2897	
COLLECTOR-TO-BASE VOLTAGE, V_{CBO} . .	120	140	60 max.	volts
COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO}	65	90	45 max.	volts
COLLECTOR-TO-EMITTER VOLTAGE, V_{CER} (With $R_{BE} \leq$ 10 ohms)	80	140	60 max.	volts
EMITTER-TO-BASE VOLTAGE, V_{EBO} . .	7	7	7 max.	volts
COLLECTOR CURRENT, I_C	1	1	1 max.	amp
TRANSISTOR DISSIPATION, P_T:				
For case temperatures up to 25° C. .	1.8	1.8	1.8 max.	watts
above 25° C. .	See Rating Chart (Fig. 1)			
TRANSISTOR DISSIPATION, P_T (Cont'd):				
For free-air temperatures up to 25° C. .	0.5	0.5	0.5 max.	watt
above 25° C. .	See Rating Chart (Fig. 1)			
TEMPERATURE RANGE:				
Storage and Operating (Junction) . . .	-65 to +200			°C
LEAD TEMPERATURE (During Soldering): At distances $\geq$ 1/32 inch from lead seals for 10 seconds max. .	255	255	255 max.	°C

2N2895, formerly Dev. No. TA2275
2N2896, formerly Dev. No. TA2276
2N2897, formerly Dev. No. TA2277

ELECTRICAL CHARACTERISTICS

Characteristics	Symbols	TEST CONDITIONS: Case Temperature T_C	Frequency f	DC Collector-to-Base Voltage V_{CB}	DC Collector-to-Emitter Voltage V_{CE}	DC Emitter-to-Base Voltage V_{EB}	DC Collector Current I_C	DC Emitter Current I_E	DC Base Current I_B	LIMITS: Type 2N2895 Min.	Type 2N2895 Max.	Type 2N2896 Min.	Type 2N2896 Max.	Type 2N2897 Min.	Type 2N2897 Max.	Units
		°C	kc	volts	volts	volts	ma	ma	ma							
Collector-Cutoff Current	I_{CBO}	25		90				0		-	-	-	0.01	-	-	µa
		150		90				0		-	-	-	10	-	-	µa
		25		60				0		-	0.002	-	-	-	0.05	µa
		150		60				0		-	2	-	-	-	50	µa
Emitter-Cutoff Current	I_{EBO}	25				5	0			-	0.002	-	0.01	-	0.05	µa
DC Forward-Current Transfer Ratio	h_{FE}	25			10		150[b]			40	120	60	200	50	200	
		25			10		500[b]			25	-	-	-	-	-	
		25			10		0.1			20	-	-	-	-	-	
		25			10		1			-	-	35	-	35	-	
		25			10		10			35	-	-	-	-	-	
		-55			10		10			20	-	20	-	-	-	
Collector-to-Base Breakdown Voltage	BV_{CBO}	25					0.1	0		120	-	140	-	60	-	volts
Emitter-to-Base Breakdown Voltage	BV_{EBO}	25					0	0.1		7	-	7	-	7	-	volts
Collector-to-Emitter Sustaining Voltage	$V_{CEO}(sus)$	25					100[b]		0	65	-	90	-	45	-	volts
Collector-to-Emitter Sustaining Voltage with R_{BE} = 10 ohms	$V_{CER}(sus)$	25					100[b]			80	-	140	-	60	-	volts
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	25					150[b]		15	-	0.6	-	0.6	-	1	volt
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$	25					150[b]		15	-	1.2	-	1.2	-	1.3	volts
Small-Signal Forward-Current Transfer Ratio	h_{fe}	25	1		5		5			50	200	50	275	50	275	
		25	20 Mc		10		50			6	-	6	-	5	-	
Noise Figure: Generator resistance = 510 ohms, circuit bandwidth = 1 cps	NF	25	1		10		0.3			-	8	-	-	-	-	db
Output Capacitance	C_{ob}	25	140	10				0		-	15	-	15	-	15	pf
Input Capacitance	C_{ib}	25	140			0.5	0			-	80	-	80	-	80	pf
Thermal Resistance: Junction-to-Base	θ_{J-C}	-								-	97	-	97	-	97	°C/watt
Junction-to-Free Air	θ_{J-FA}	-								-	350	-	350	-	350	°C/watt

b Pulse test: Pulse duration = 300 µsec; duty factor = 1.8%.

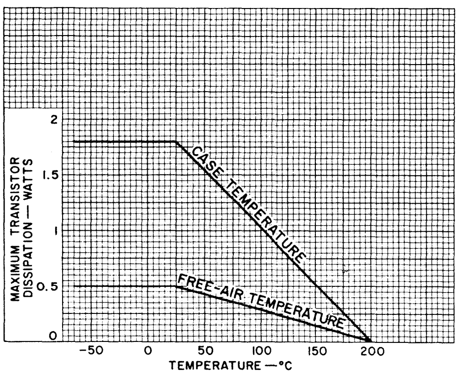


Fig. 1 - Rating Chart for Types 2N2895 2N2896, and 2N2897

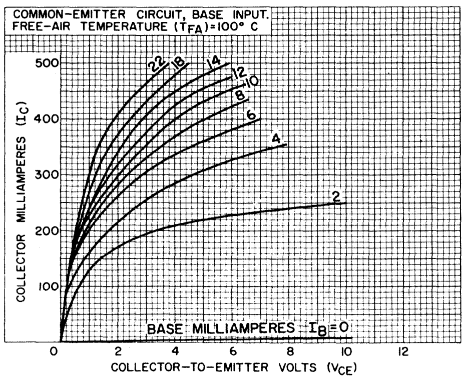


Fig. 2 - Typical Collector Characteristics at 100° C for Type 2N2895

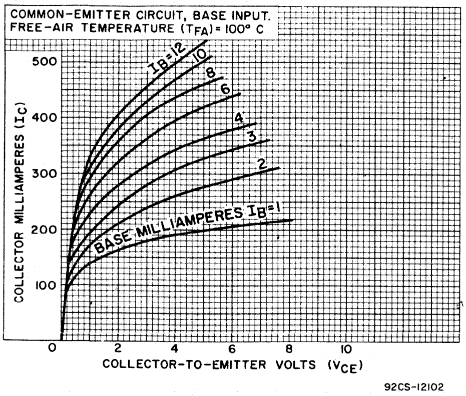


Fig. 3 - Typical Collector Characteristics at 100° C for Types 2N2896 and 2N2897.

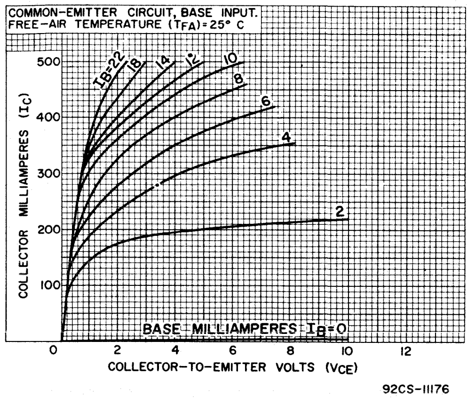


Fig. 4 - Typical Collector Characteristics at 25° C for Type 2N2895.

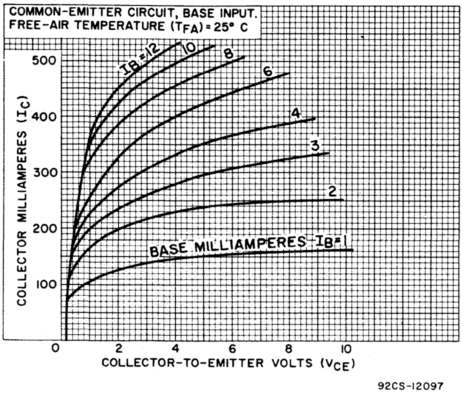


Fig. 5 - Typical Collector Characteristics at 25° C for Types 2N2896 and 2N2897.

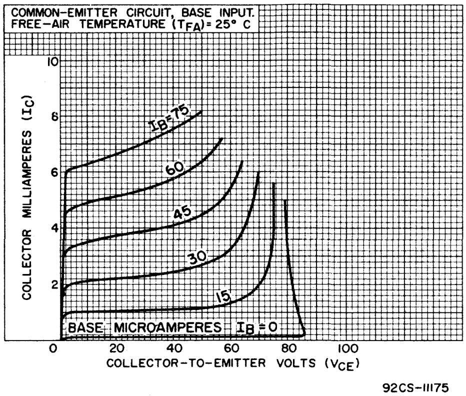


Fig. 6 - Typical Collector Characteristics at 25° C for Type 2N2895.

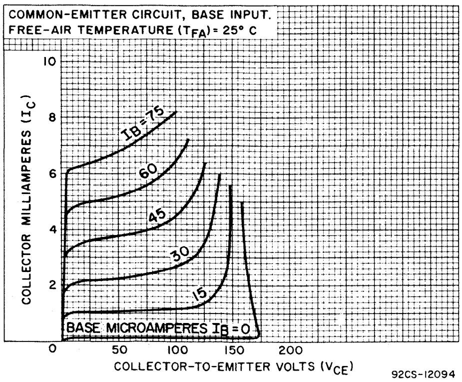


Fig. 7 - Typical Collector Characteristics at 25° C for Type 2N2896.

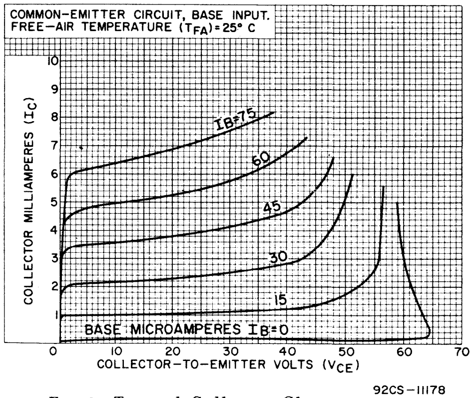


Fig. 8 - Typical Collector Characteristics at 25° C for Type 2N2897.

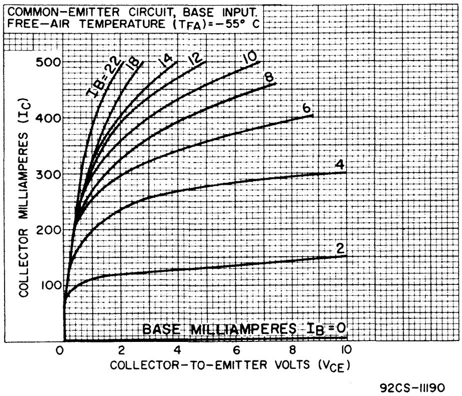


Fig. 9 - Typical Collector Characteristics at -55° C for Type 2N2895.

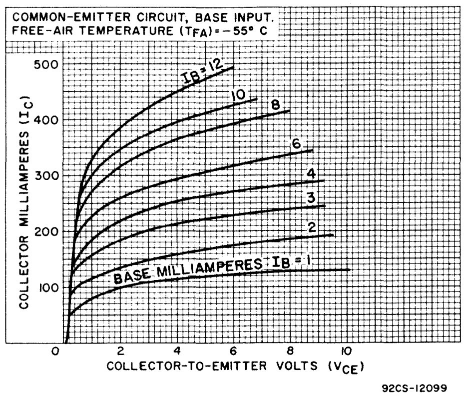


Fig. 10 - Typical Collector Characteristics at -55° C for Types 2N2896 and 2N2897.

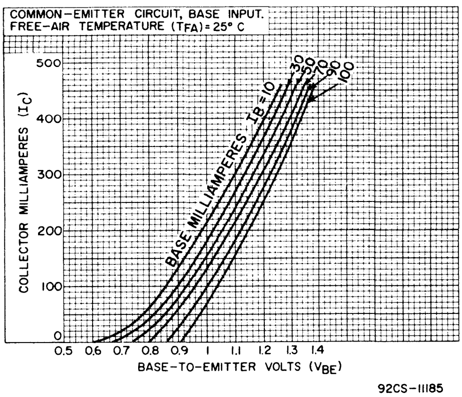


Fig. 11 - Typical Transfer Characteristics for Types 2N2895 and 2N2896.

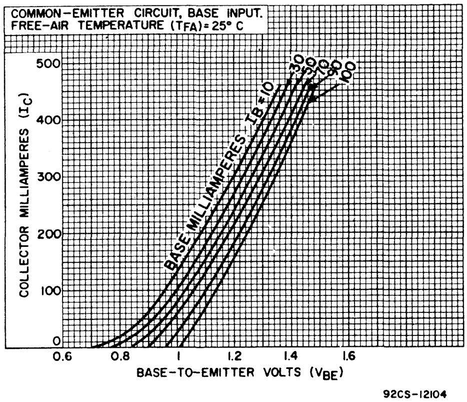


Fig. 12 - Typical Transfer Characteristics for Type 2N2897.

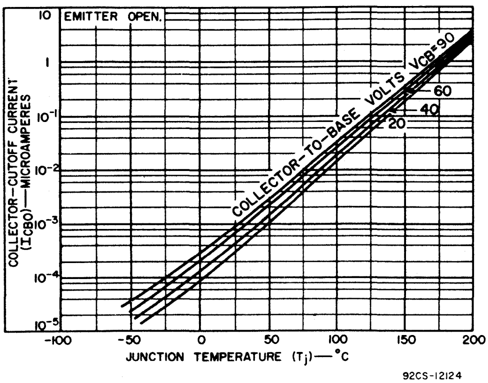


Fig. 13 - Typical Collector-Cutoff-Current Characteristics for Types 2N2895 and 2N2896.

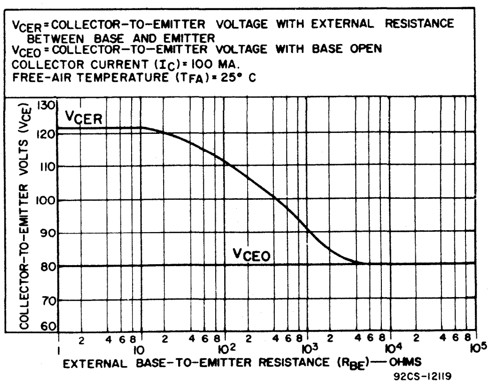


Fig. 14 - Typical Collector-to-Emitter-Voltage Characteristic for Type 2N2895.

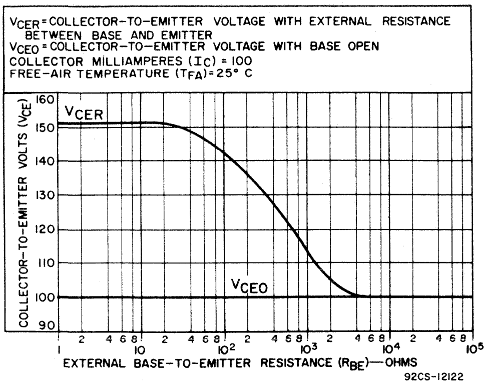


Fig. 15 - Typical Collector-to-Emitter-Voltage Characteristic for Type 2N2896.

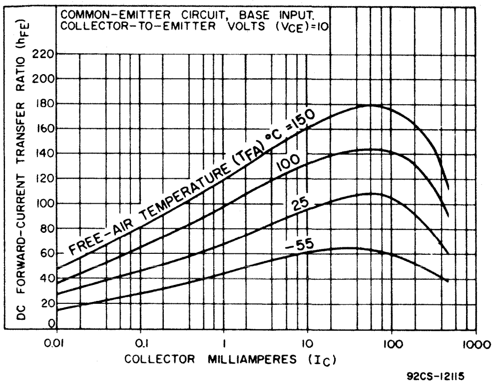


Fig. 16 - Typical DC-Forward-Current Transfer-Ratio Characteristics for Type 2N2895.

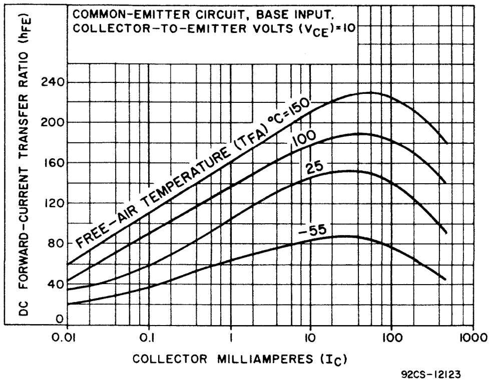


Fig. 17 - Typical DC-Forward-Current Transfer-Ratio Characteristics for Types 2N2896 and 2N2897.

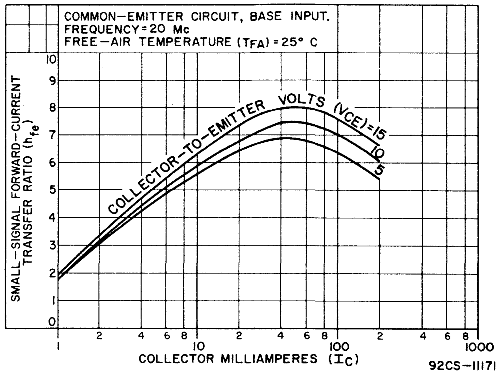


Fig. 18 - Typical Small-Signal Forward-Current Transfer-Ratio Characteristics for Types 2N2895, 2N2896 and 2N2897 .

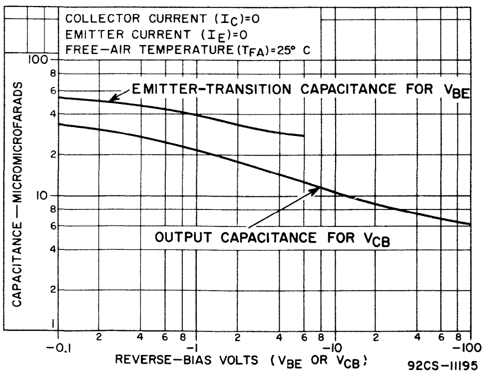


Fig. 19 - Typical Emitter-Transition-Capacitance and Output-Capacitance Characteristics for Types 2N2895, 2N2896 and 2N2897.

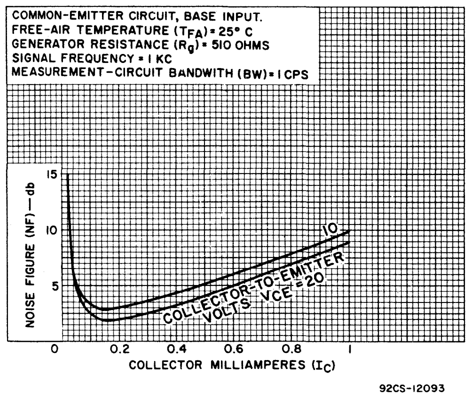
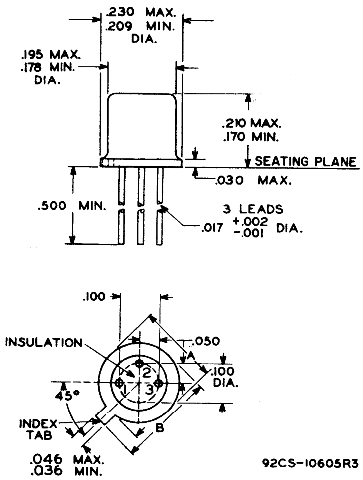
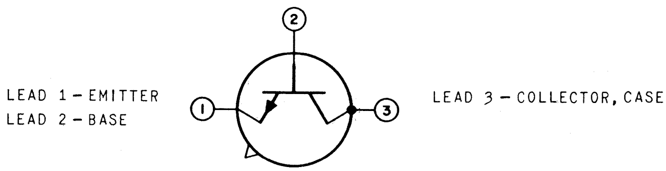


Fig. 20 - Typical AF-Noise-Figure Characteristics for Type 2N2895.

2N2895, 2N2896, and 2N2897
DIMENSIONAL OUTLINE
JEDEC No. TO-18



TERMINAL DIAGRAM
(Bottom View)
For All Types

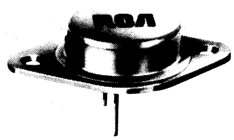


Monolithic Darlington Power Transistors

RCA
Solid State
Division

Power Transistors
RCA1000
RCA 1001

8-Ampere Silicon N-P-N Darlington Power Transistors



H-1570 JEDEC TO-3

For Use as Output Devices in General-Purpose Switching and Amplifier Applications

Features:

- **High dc current gain:** **h_{FE} = 1000 min. at I_C = 3 A**
- **Monolithic construction with built-in base-emitter shunt resistors**

RCA-1000 and 1001 are monolithic silicon n-p-n Darlington transistors intended for medium-power applications as output devices. The double epitaxial construction of these units provides good forward and reverse second-breakdown capability. Their high gain makes it possible for them to be driven directly from integrated circuits.

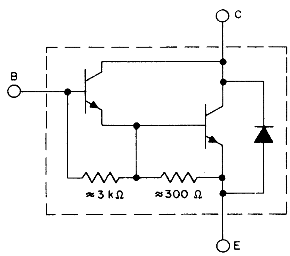


Fig. 1—Schematic diagram of RCA 1000 and RCA 1001 Darlington power transistors.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		RCA-1000	RCA-1001	
COLLECTOR-TO-BASE VOLTAGE:				
With emitter open	V_{CBO}	60	80	V
COLLECTOR-TO-EMITTER VOLTAGE:				
With base open	V_{CEO}	60	80	V
EMITTER-TO-BASE VOLTAGE:				
With collector open	V_{EBO}	5	5	V
COLLECTOR CURRENT:	I_C			
Continuous		8	8	A
Pulsed		15	15	A
BASE CURRENT (Continuous)	I_B	0.1	0.1	A
TRANSISTOR DISSIPATION:	P_T			
At case temperatures up to 25°C		90	90	W
At case temperatures above 25°C, derate linearly at		0.515		W/°C
TEMPERATURE RANGE:				
Storage & Operating (Junction)		−55 to +200		°C
LEAD TEMPERATURE (During Soldering):				
At distance ≥ 1/8 in. (3.17 mm) from case to 10 s max.		235		°C

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ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: DC VOLTAGE (V) V_{CB}	V_{CE}	V_{BE}	DC CURRENT (A) I_C	I_B	LIMITS: RCA-1000 MIN.	MAX.	RCA-1001 MIN.	MAX.	UNITS
Collector Cutoff Current: With base open	I_{CEO}		30			0	–	500	–	–	μA
			40			0	–	–	–	500	
With external base-to-emitter resistance (R_{BE}) = 1 kΩ	I_{CER}	60					–	1	–	–	mA
		80					–	–	–	1	
At T_C = 150°C		60					–	5	–	–	
		80					–	–	–	5	
Emitter Cutoff Current	I_{EBO}			5	0		–	2	–	2	mA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$				0.1[a]	0	60	–	–	–	V
					0.1[a]	0	–	–	80	–	
DC Forward Current Transfer Ratio	h_{FE}		3		3		1000	–	1000	–	
			3		4		750	–	750	–	
Base-to-Emitter Voltage	V_{BE}		3		3[a]		–	2.5	–	2.5	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				3[a]	0.012	–	2	–	2	V
					8[a]	0.04	–	4	–	4	
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$						–	1.94	–	1.94	°C/W

[a] Pulsed: Pulse duration ≤ 300 μs, duty factor ≤ 2%.

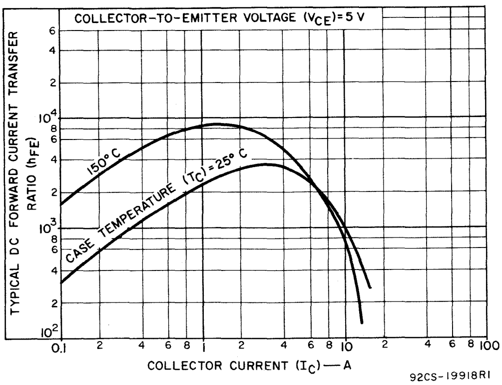


Fig.2—Typical dc beta characteristics for both types.

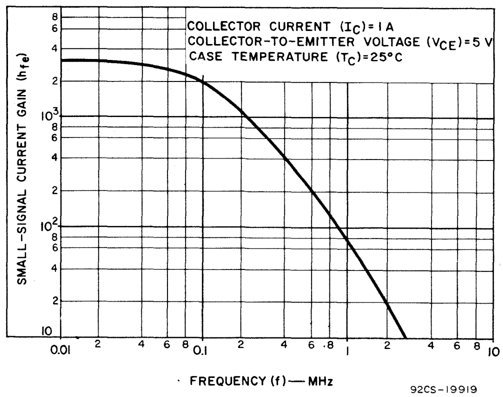


Fig.3—Typical small-signal gain for both types.

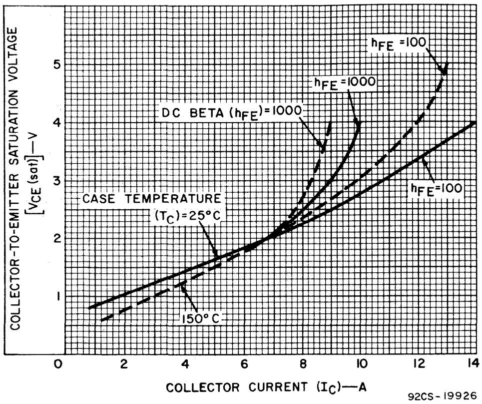


Fig.4—Typical saturation characteristics for both types.

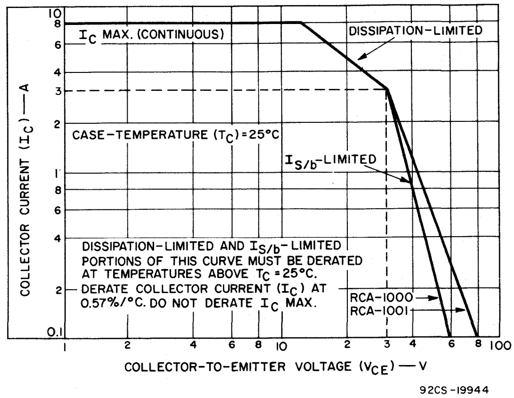


Fig.5—DC safe-area-of-operation for both types.

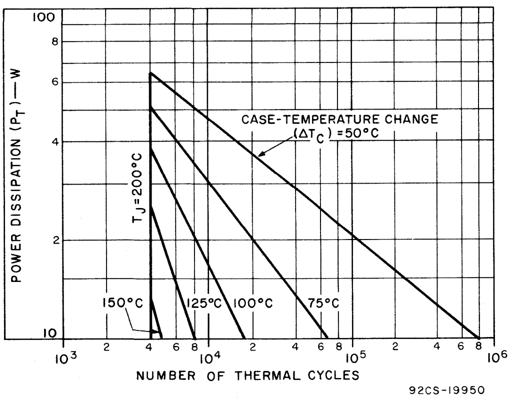
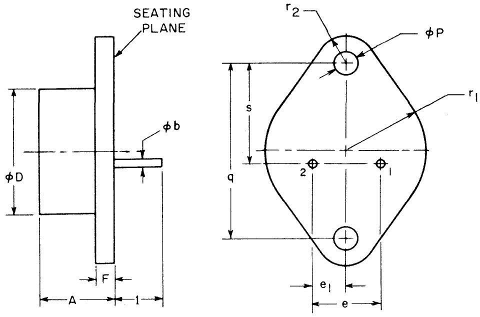


Fig.6—Thermal-cycling rating chart for both types.

DIMENSIONAL OUTLINE—JEDEC TO-3



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	0.250	0.450	6.35	11.43	
φb	0.038	0.043	0.97	1.09	2
φD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
l	0.312		7.92		2
φP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r1		0.525		13.34	
r2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS–15222

TERMINAL CONNECTIONS

Pin 1 — Base
Pin 2 — Emitter
Case — Collector
Mounting Flange — Collector

RCA

Solid State
Division

Power Transistors

2N6055
2N6056

JEDEC TO-3

H-1570

8-Ampere Silicon N-P-N Darlington Power Transistors

60- and 80-Volt, 100-Watt Types
With Gain of 750 at 4 Amperes

Features:

- Operation from IC without predriver
- Low leakage at high temperature
- High reverse-second-breakdown capability

Applications:

- Power switching
- Hammer drivers
- Audio amplifiers
- Series and shunt regulators

RCA-2N6055 and 2N6056 are monolithic n-p-n silicon Darlington transistors designed for low- and medium-frequency power applications. The double epitaxial construction of these devices provides good forward and reverse second-breakdown capability. Their high gain makes it possible for them to be driven directly from integrated circuits.

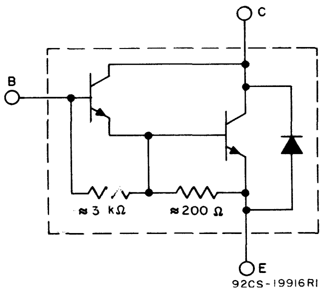


Fig. 1– Schematic diagram of 2N6055 and 2N6056 Darlington power transistors.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N6055	2N6056	
* COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	60	80	V
COLLECTOR-TO-EMITTER VOLTAGE:				
With base reverse-biased, V_{BE} = −1.5 V, sustaining	V_{CEV} (sus)	60	80	V
With external base-to-emitter resistance (R_{BE}) = 100Ω, sustaining	V_{CER} (sus)	60	80	V
* With base open	V_{CEO}	60	80	V
* EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	5	V
COLLECTOR CURRENT:	I_C			
* Continuous		8	8	A
Peak		16	16	A
* CONTINUOUS BASE CURRENT	I_B	120	120	mA
* TRANSISTOR DISSIPATION:	P_T			
At case temperatures up to 25°C		100	100	W
At case temperatures above 25°C		See Figs. 2 and 3		
* TEMPERATURE RANGE:				
Storage & Operating (Junction)		−65 to +200		°C
* PIN TEMPERATURE (During Soldering):				
At distances ⩾ 1/16 in. (1.58 mm) from seating plane for 10 s max		235		°C

* In accordance with JEDEC registration data format JS-6 RDF-2

ELECTRICAL CHARACTERISTICS, *at Case Temperature (T_C) = 25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS DC VOLTAGE V			TEST CONDITIONS DC CURRENT A			LIMITS 2N6055		LIMITS 2N6056		UNITS
		V_{CE}	V_{EB}	V_{BE}	I_C	I_E	I_B	MIN.	MAX.	MIN.	MAX.	
* Collector Cutoff Current: With base open	I_{CEO}	30					0	–	0.5	–	–	mA
		40					0	–	–	–	0.5	mA
With base-emitter junction reverse-biased	I_{CEX}	60		−1.5				–	0.5	–	–	mA
		80		−1.5				–	–	–	0.5	mA
At T_C = 150°C	I_{CEX}	60		−1.5				–	5	–	–	mA
		80		−1.5				–	–	–	5	mA
* Emitter Cutoff Current	I_{EBO}		5		0			–	2	–	2	mA
* DC Forward Current Transfer Ratio	h_{FE}	3			8[a]			100	–	100	–	
		3			4[a]			750	18,000	750	18,000	
Collector-to-Emitter Sustaining Voltage: With base open	$V_{CEO}(sus)$				0.1[a]			60[a]	–	80[a]	–	V
With external base-to-emitter resistance (R_{BE}) = 100Ω	$V_{CER}(sus)$				0.1[a]			60[a]	–	80[a]	–	V
With base-emitter junction reverse-biased	$V_{CEX}(sus)$			−1.5	0.1[a]			60[a]	–	80[a]	–	V
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				4[a]		0.016	–	2	–	2	V
					8[a]		0.08	–	3	–	3	V
* Base-to-Emitter Voltage	V_{BE}	3			4[a]			–	2.8	–	2.8	V
At saturation	$V_{BE}(sat)$				8[a]		0.08	–	4	–	4	V
* Magnitude of Common-Emitter, Small-Signal Short-Circuit, Forward Current Transfer Ratio (f = 1 MHz)	$\|h_{fe}\|$	3			3			4	–	4	–	
* Common-Base Output Capacitance (f = 0.1 MHz), V_{CB} = 10V	C_{obo}					0		–	200	–	200	pF
* Common-Emitter, Small-Signal, Short-Circuit Forward Current Transfer Ratio (f = 1 kHz)	h_{fe}	3			3			300	–	300	–	–
Second Breakdown Energy With base reverse-biased and L = 12 mH, R_{BE} = 100Ω	$E_{S/b}$[b]			−1.5	5			150	–	150	–	mJ
Forward-Bias Second Breakdown Collector Current (1-s non-repetitive pulse)	$I_{S/b}$	33.3						3	–	3	–	A
		40						–	–	2	–	A
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$							–	1.75	–	1.75	°C/W

* In accordance with JEDEC registration data format JS-6 RDF-2.

[a] Pulsed: Pulse duration = 300 μs, duty factor = 2%.

[b] $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse bias conditions. $E_{S/b} = \frac{1}{2}LI^2$, where L is a series load or leakage inductance and I is the peak collector current.

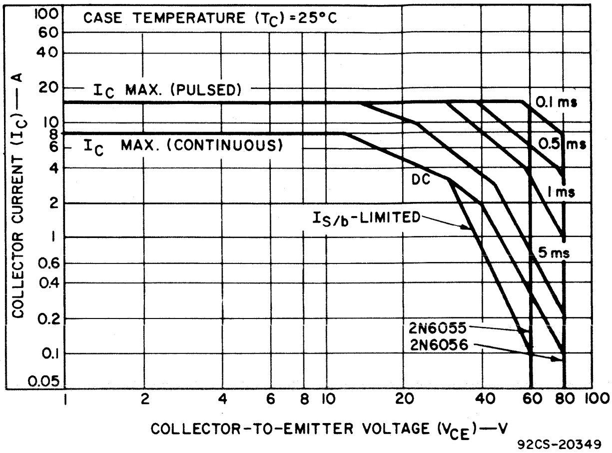


Fig. 2— Maximum operating areas for types 2N6055 and 2N6056.

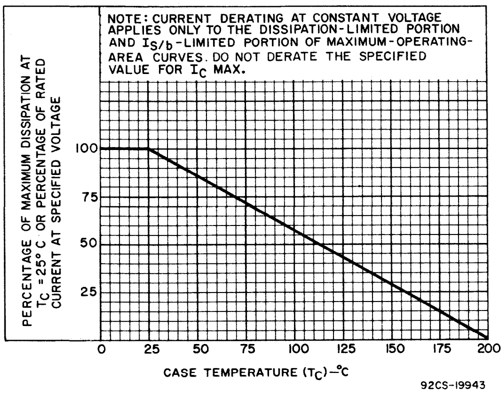


Fig. 3— Derating curve for both types.

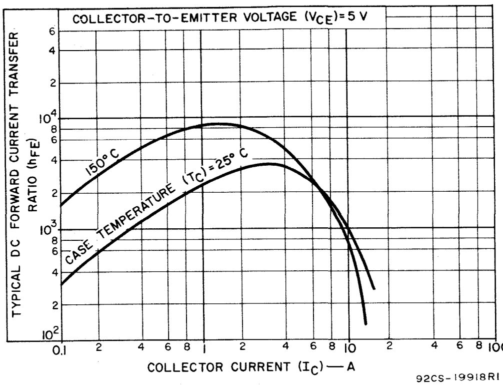


Fig. 4— Typical dc beta characteristics for both types.

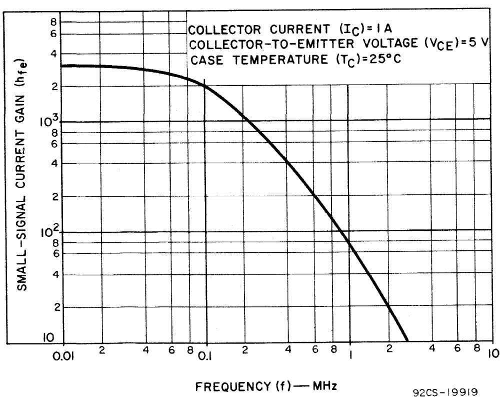


Fig. 5— Typical small-signal gain for both types.

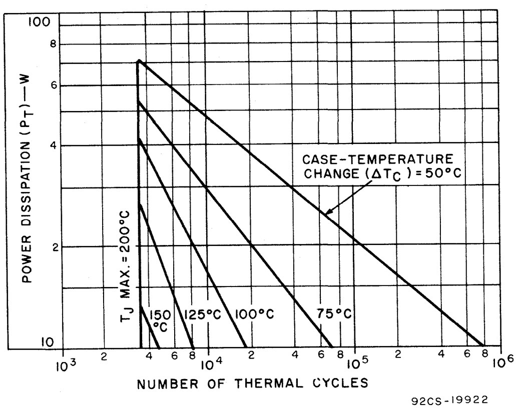


Fig. 6— Thermal-cycling rating chart for both types.

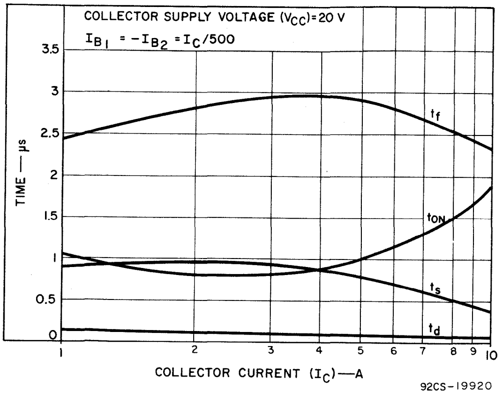


Fig. 7— Typical saturated switching-time characteristics for both types.

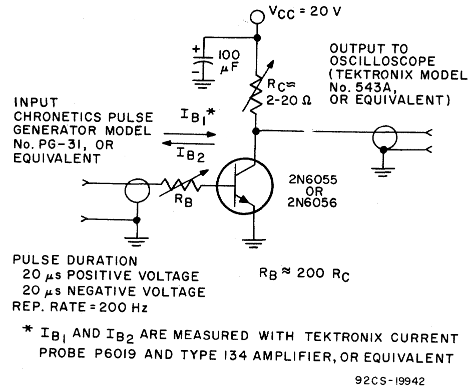


Fig. 8— Circuit used to measure saturated switching times.

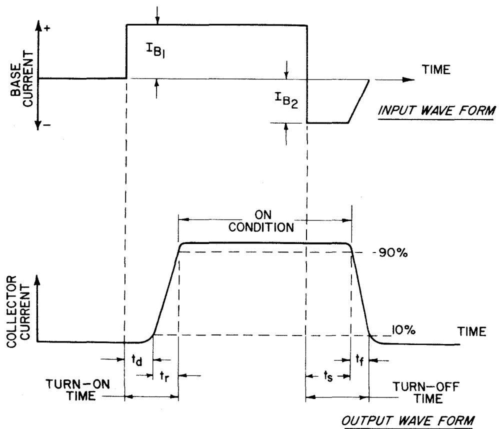


Fig. 9— Phase relationship between input current and output current showing reference points for specification of switching times (test circuit shown in Fig. 8).

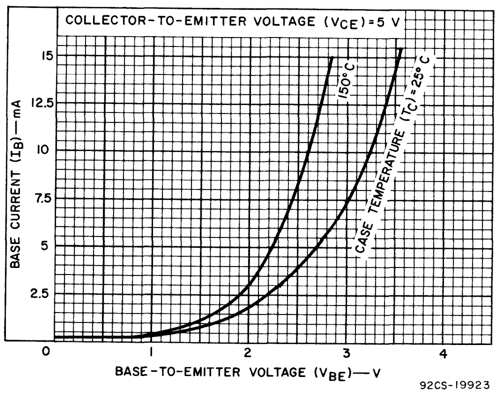


Fig. 10—Typical input characteristics for both types.

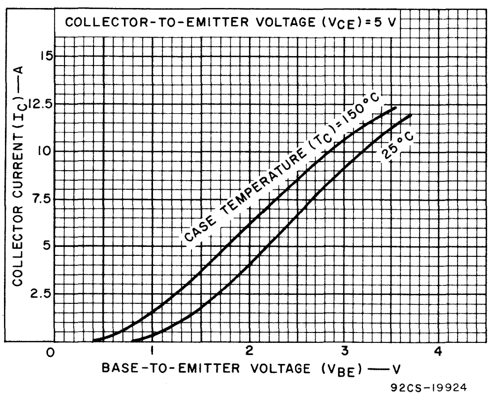


Fig. 11—Typical transfer characteristics for both types.

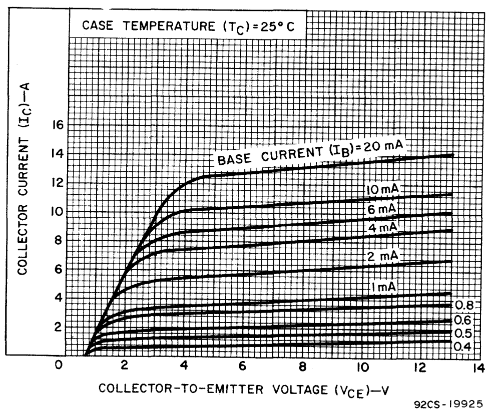


Fig. 12—Typical output characteristics for both types.

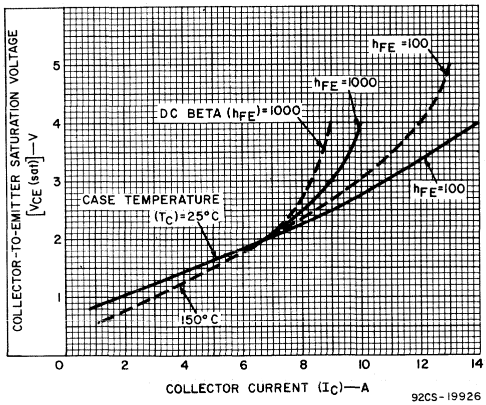
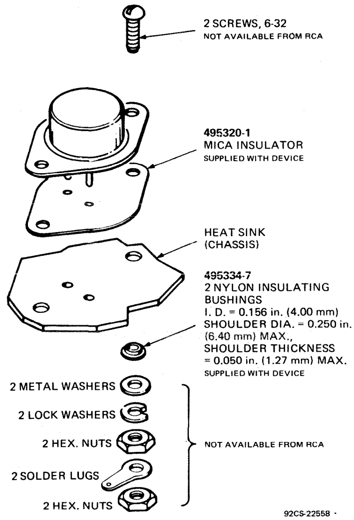


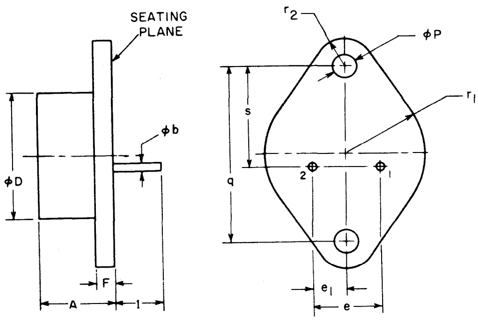
Fig. 13—Typical saturation-voltage characteristics for both types.



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 14—Suggested mounting hardware.

DIMENSIONAL OUTLINE JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
φb	0.038	0.043	0.97	1.09	2
φD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
l	0.312		7.92		2
φP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r1		0.525		13.34	
r2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS–15222

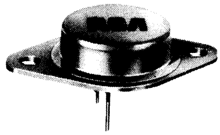
TERMINAL CONNECTIONS

Pin 1 — Base
Pin 2 — Emitter
Case — Collector
Mounting Flange — Collector

RCA
Solid State
Division

Power Transistors

2N6383 2N6384 2N6385



JEDEC TO-3

H-1570

10-Ampere, N-P-N Darlington Power Transistors

40-60-80 Volts, 100 Watts
Gain of 1000 at 5 A

Features:

- Operates from IC without predriver
- Low leakage at high temperature
- High reverse second-breakdown capability

Applications:

- Power switching
- Audio amplifiers
- Hammer drivers
- Series and shunt regulators

The 2N6383, 2N6384, and 2N6385● are monolithic n-p-n silicon Darlington transistors designed for low- and medium-frequency power applications. The double epitaxial construction of these devices provides good forward and reverse second-breakdown capability; their high gain makes it possible for them to be driven directly from integrated circuits.

●Formerly RCA Dev. Nos. TA8349, TA8486, and TA8348.

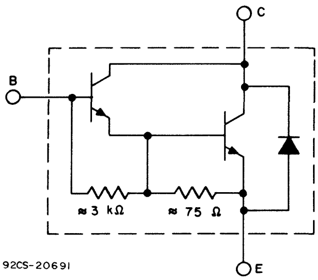


Fig. 1—Schematic diagram for all types.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N6385	2N6384	2N6383	
* COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	80	60	40	V
COLLECTOR-TO-EMITTER VOLTAGE:					
With external base-to-emitter resistance (R_{BE}) = 100Ω, sustaining	$V_{CER}(sus)$	80	60	40	V
With base open, sustaining	$V_{CEO}(sus)$	80	60	40	V
* With base reverse-biased V_{BE} = −1.5 V, R_{BB} = 100Ω	V_{CEX}	80	60	40	V
* EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	5	5	V
COLLECTOR CURRENT:	I_C				
* Continuous		10	10	10	A
Peak		15	15	15	A
* CONTINUOUS BASE CURRENT	I_B	0.25	0.25	0.25	A
* TRANSISTOR DISSIPATION:	P_T				
At case temperatures up to 25°C		100	100	100	W
At case temperatures above 25°C		← See Fig. 3 →			
* TEMPERATURE RANGE:					
Storage and Operating (Junction)		← −65 to +200 →			°C
* PIN TEMPERATURE (During Soldering):					
At distances ≥ 1/32 in. 0.8 mm from seating plane for 10 s max.		← 235 →			°C

*In accordance with JEDEC registration data format JS-6 RDF-2.

11-72

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS					LIMITS						UNITS
		VOLTAGE V dc			CURRENT A dc		2N6385		2N6384		2N6383		
		V_{CE}	V_{EB}	V_{BE}	I_C	I_B	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
* Collector-Cutoff Current: With base open	I_{CEO}	80 60 40				0 0 0	– – –	1 – –	– – –	– 1 –	– – –	– – 1	mA
With base open and T_C = 150°C	I_{CEO}	80 60 40				0 0 0	– – –	10 – –	– – –	– 10 –	– – –	– – 10	mA
* With base reverse-biased	I_{CEV}	80 60 40		−1.5 −1.5 −1.5			– – –	0.3 – –	– – –	– 0.3 –	– – –	– – 0.3	mA
* With base reverse-biased and T_C = 150°C	I_{CEV}	80 60 40		−1.5 −1.5 −1.5			– – –	3 – –	– – –	– 3 –	– – –	– – 3	mA
* Emitter-Cutoff Current	I_{EBO}		5		0		–	5	–	5	–	5	mA
* Collector-to-Emitter Sustaining Voltage: With base open	V_{CEO}(sus)				0.2[a]	0	80	–	60	–	40	–	V
With external base-to-emitter resistance (R_{BE}) = 100Ω	V_{CER}(sus)				0.2[a]		80	–	60	–	40	–	V
With base-emitter junction reverse-biased	V_{CEV}(sus)			−1.5	0.2[a]		80	–	60	–	40	–	V
* DC Forward Current Transfer Ratio	h_{FE}	3 3			5[a] 10[a]		1000 100	20,000 –	1000 100	20,000 –	1000 100	20,000 –	
* Base-to-Emitter Voltage	V_{BE}	3 3			5[a] 10[a]		– –	2.8 4.5	– –	2.8 4.5	– –	2.8 4.5	V
* Collector-to-Emitter Saturation Voltage	V_{CE}(sat)				5[a] 10[a]	0.01[a] 0.1[a]	– –	2 3	– –	2 3	– –	2 3	V
Parallel Diode Forward Voltage Drop	V_F				−10		–	4	–	4	–	4	V
* Common-Emitter, Small-Signal, Short-Circuit Forward Current Transfer Ratio (f = 1 kHz)	h_{fe}	5			1		1000	–	1000	–	1000	–	
* Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 1.0 MHz)	$\|h_{fe}\|$	5			1		20	–	20	–	20	–	
* Common Base Output Capacitance (f = 1 MHz)	C_{ob}	V_{CB} = 10				I_E = 0	–	200	–	200	–	200	pF
Second Breakdown Energy With base reverse-biased and L = 12 mH, R_{BE} = 100Ω	$E_{S/b}$[b]			−1.5	4.5		120	–	120	–	120	–	mJ
Forward-Bias Second Break-down Collector Current (1-s non-repetitive pulse)	$I_{S/b}$	75 55 35					0.22 – –	– – –	– 0.62 –	– – –	– – 2.85	– – –	A
Thermal Resistance Junction-to-Case	$R_{\theta JC}$						–	1.75	–	1.75	–	1.75	°C/W

[a] Pulsed: Pulse duration = 300 μs, duty factor = 1.8%.

[b] $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse bias conditions. $E_{S/b} = \frac{1}{2}LI^2$ where L is a series load or leakage inductance, and I is the peak collector current.

* In accordance with JEDEC registration data format JS-6 RDF-2.

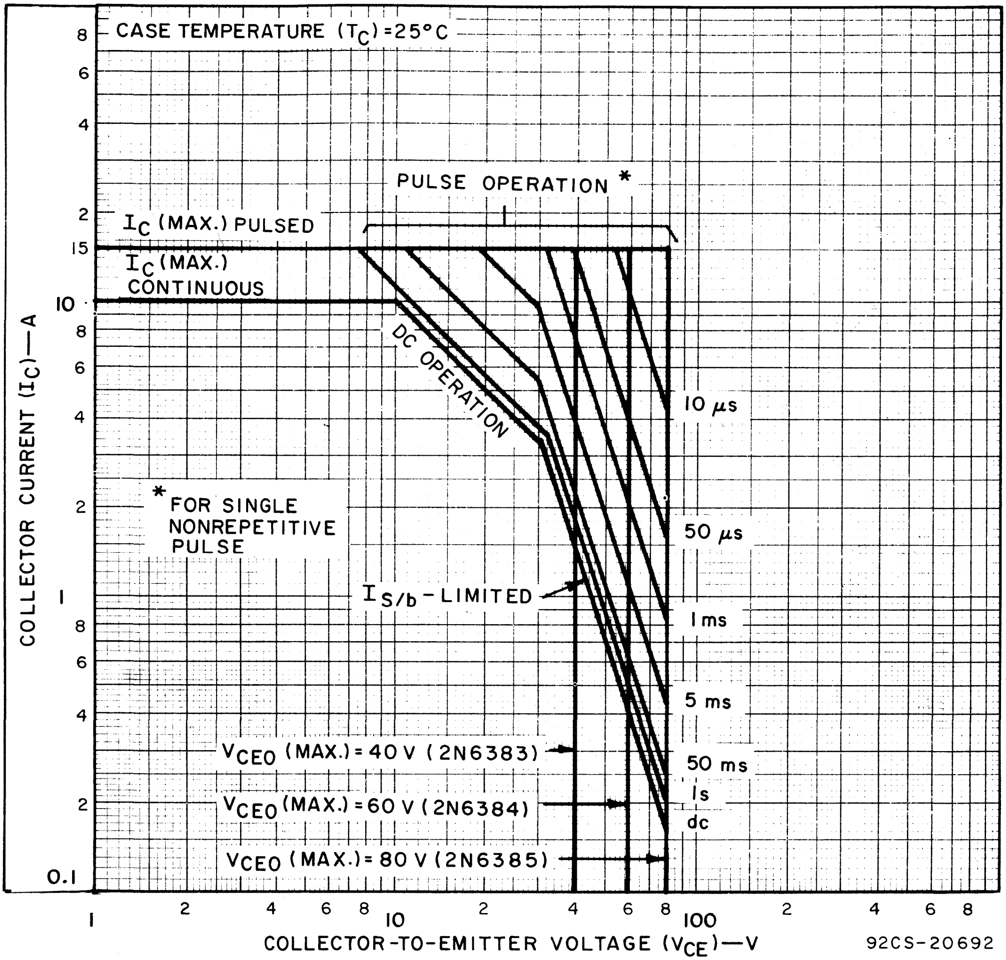


Fig. 2—Maximum operating area for all types.

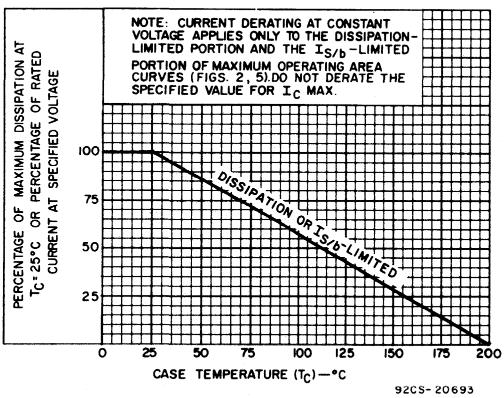


Fig. 3—Derating curves for all types.

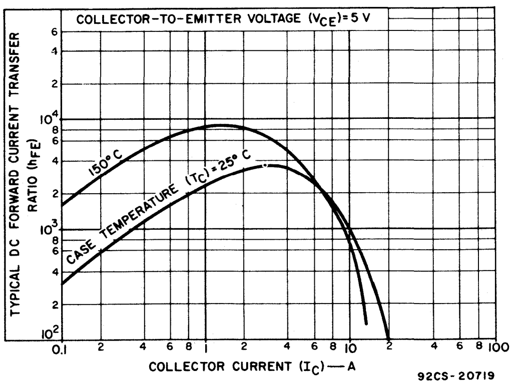


Fig. 4—Typical dc-beta characteristics for all types.

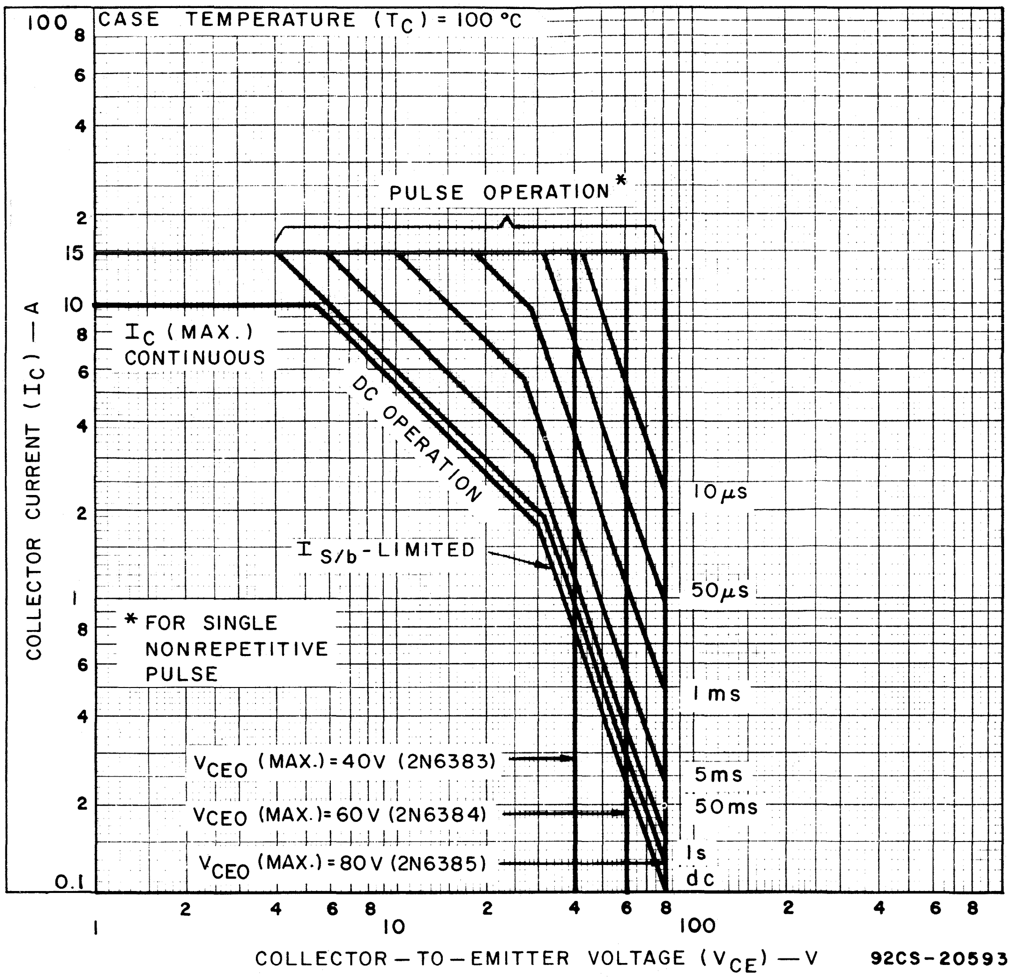


Fig. 5—Maximum operating area for all types.

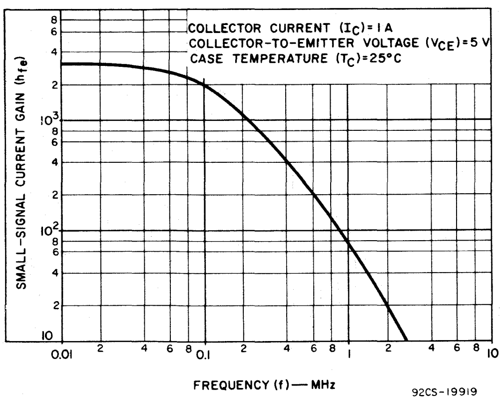


Fig. 6—Typical small-signal gain for all types.

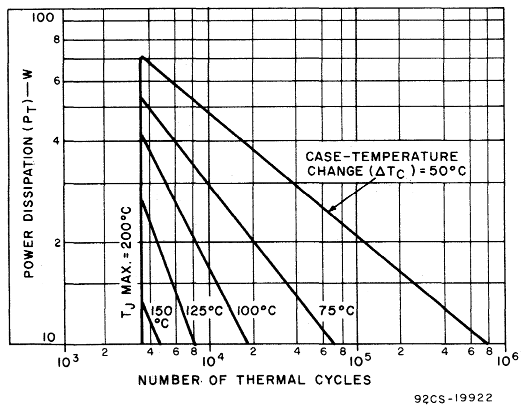


Fig. 7—Thermal-cycling rating chart for all types.

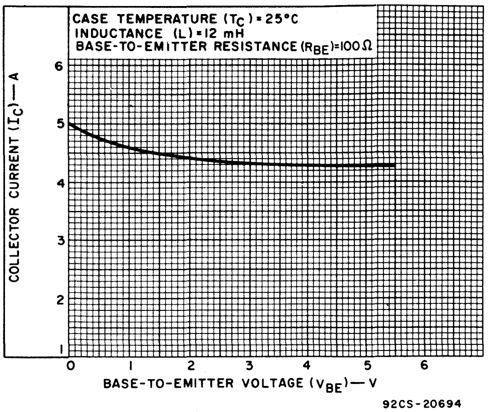


Fig. 8—Minimum values of reverse-bias second breakdown characteristic ($E_{S/b}$) for all types.

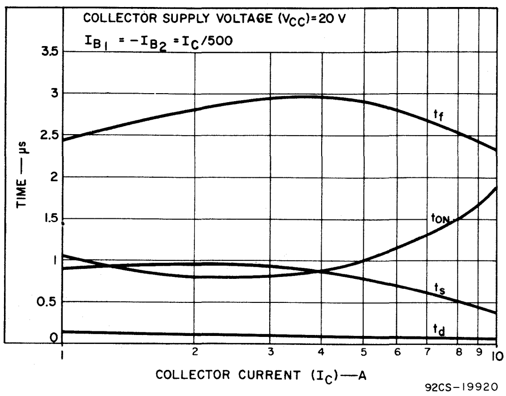


Fig. 9—Typical saturated switching-time characteristics for all types.

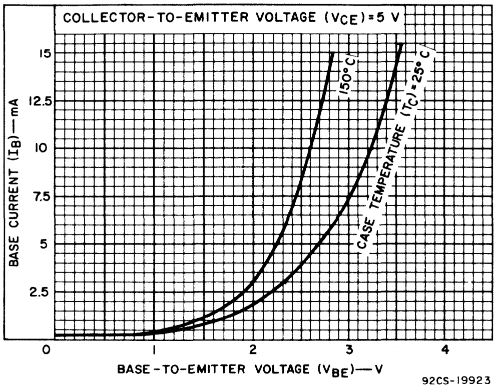


Fig. 10—Typical input characteristics for all types.

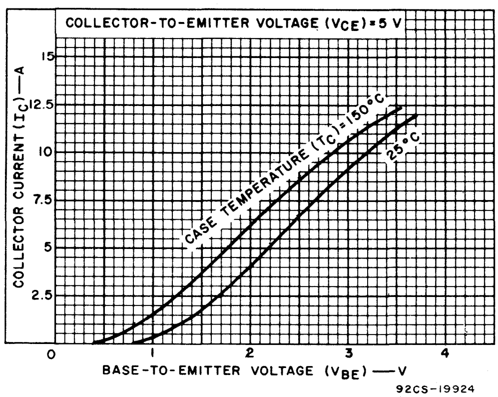


Fig. 11—Typical transfer characteristics for all types.

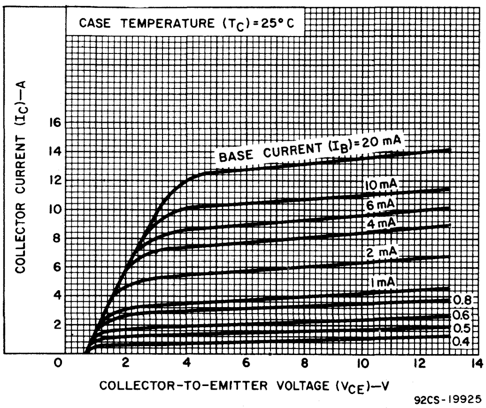


Fig. 12—Typical output characteristics for all types.

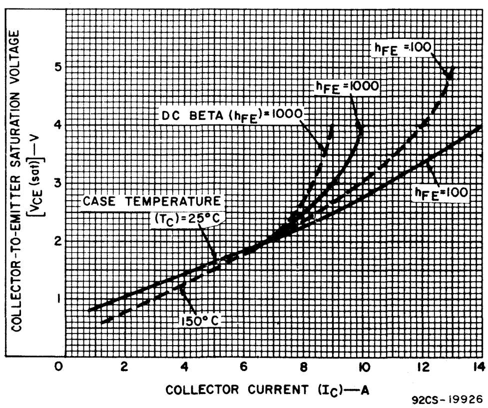


Fig. 13—Typical saturation characteristics for all types.

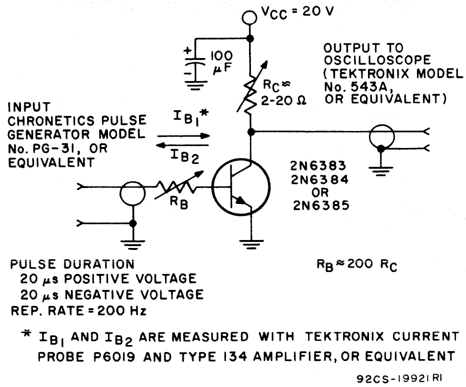


Fig. 14—Circuit used to measure saturated switching times.

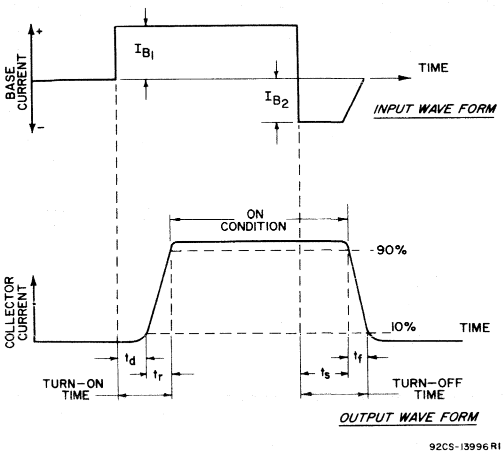
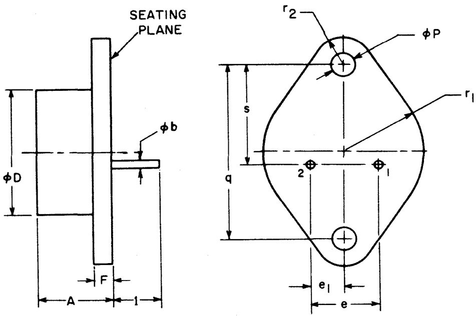


Fig. 15—Phase relationship between input current and output current showing reference points for specification of switching times (test circuit shown in Fig. 14).

DIMENSIONAL OUTLINE - JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
φb	0.038	0.043	0.97	1.09	2
φD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
l	0.312		7.92		2
φP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r1		0.525		13.34	
r2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS–15222

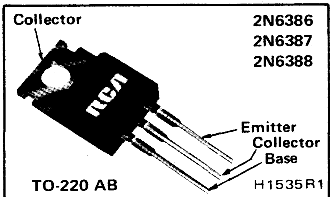
TERMINAL CONNECTIONS

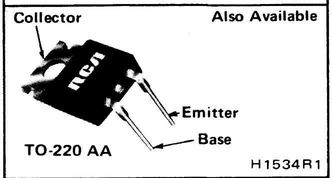
Pin 1 - Base
Pin 2 - Emitter
Case - Collector
Mounting Flange - Collector

Solid State Division

Power Transistors

2N6386 2N6387 2N6388





10-Ampere, N-P-N Darlington Power Transistors

40-60-80 Volts, 40 Watts
Gain of 1000 at 5 A (2N6387, 2N6388)
Gain of 1000 at 3 A (2N6386)

Features:

- Operates from IC without predriver
- Low leakage at high temperature
- High reverse second-breakdown capability

Applications:

- Power switching
- Audio amplifiers
- Hammer drivers
- Series and shunt regulators

The 2N6386, 2N6387, and 2N6388● are monolithic n-p-n silicon Darlington transistors designed for low- and medium-frequency power applications. The double epitaxial construction of these devices provides good forward and reverse second-breakdown capability; their high gain makes it possible for them to be driven directly from integrated circuits.

● Formerly RCA Dev. Nos. TA8202, TA8485, and TA8201, respectively.

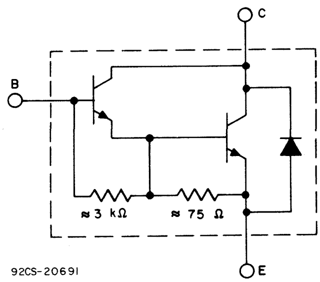


Fig. 1—Schematic diagram for all types.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		2N6388	2N6387	2N6386	
* COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	80	60	40	V
COLLECTOR-TO-EMITTER VOLTAGE:					
With external base-to-emitter resistance (R_{BE}) = 100Ω, sustaining	$V_{CER}(sus)$	80	60	40	V
With base open, sustaining	$V_{CEO}(sus)$	80	60	40	V
* With base reverse-biased V_{BE} = −1.5 V	V_{CEX}	80	60	40	V
* EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	5	5	V
COLLECTOR CURRENT:	I_C				
* Continuous		10	10	8	A
Peak		15	15	15	A
* CONTINUOUS BASE CURRENT	I_B	0.25	0.25	0.25	A
* TRANSISTOR DISSIPATION:	P_T				
At case temperatures up to 25°C		40	40	40	W
At case temperatures above 25°C		← See Fig. 3 →			
TEMPERATURE RANGE:					
Storage and Operating (Junction)		← −65 to +150 →			°C
* LEAD TEMPERATURE (During Soldering):					
At distances ≥ 1/8 in. (3.17 mm) from case for 10 s max.		← 235 →			°C

*In accordance with JEDEC registration data format JS-6 RDF-2.

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: VOLTAGE V dc V_{CE}	V_{EB}	V_{BE}	CURRENT A dc I_C	I_B	LIMITS 2N6388 MIN.	2N6388 MAX.	2N6387 MIN.	2N6387 MAX.	2N6386 MIN.	2N6386 MAX.	UNITS
* Collector-Cutoff Current: With base open	I_{CEO}	80 60 40				0 0 0	– – –	1 – –	– – –	– 1 –	– – –	– – 1	mA
With base open and T_C = 150°C	I_{CEO}	80 60 40				0 0 0	– – –	10 – –	– – –	– 10 –	– – –	– – 10	mA
* With base reverse-biased	I_{CEV}	80 60 40		−1.5 −1.5 −1.5			– – –	0.3 – –	– – –	– 0.3 –	– – –	– – 0.3	mA
* With base reverse-biased and T_C = 150°C	I_{CEV}	80 60 40		−1.5 −1.5 −1.5			– – –	3 – –	– – –	– 3 –	– – –	– – 3	mA
* Emitter-Cutoff Current	I_{EBO}		5		0		–	5	–	5	–	5	mA
* Collector-to-Emitter Sustaining Voltage: With base open	$V_{CEO}(sus)$				0.2[a]	0	80	–	60	–	40	–	V
With external base-to-emitter resistance (R_{BE}) = 100Ω	$V_{CER}(sus)$				0.2[a]		80	–	60	–	40	–	V
With base-emitter junction reverse-biased	$V_{CEV}(sus)$			1.5	0.2[a]		80	–	60	–	40	–	V
* DC Forward Current Transfer Ratio	h_{FE}	3 3 3 3			3[a] 5[a] 8[a] 10[a]		– 1000 – 100	– 20,000 – –	– 1000 – 100	– 20,000 – –	1000 – 100 –	20,000 – – –	
* Base-to-Emitter Voltage	V_{BE}	3 3 3 3			3[a] 5[a] 8[a] 10[a]		– – – –	– 2.8 – 4.5	– – – –	– 2.8 – 4.5	– – – –	2.8 – 4.5 –	V
* Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				3[a] 5[a] 8[a] 10[a]	0.006[a] 0.01[a] 0.08[a] 0.1[a]	– – – –	– 2 – 3	– – – –	– 2 – 3	– – – –	2 – 3 –	V
Parallel Diode Forward Voltage Drop	V_F				−8 −10		– –	– 4	– –	– 4	– –	4 –	V
* Common-Emitter, Small-Signal, Short-Circuit Forward Current Transfer Ratio (f = 1 kHz)	h_{fe}	5			1		1000	–	1000	–	1000	–	
* Magnitude of Common-Emitter, Small-Signal, Short-Circuit, Forward Current Transfer Ratio (f = 1.0 MHz)	$\|h_{fe}\|$	5			1		20	–	20	–	20	–	
* Common Base Output Capacitance (f = 1 MHz)	C_{ob}	V_{CB} = 10				I_E = 0	–	200	–	200	–	200	pF
Second Breakdown Energy With base reverse-biased and L = 12 mH, R_{BE} = 100Ω	$E_{S/b}$[b]			−1.5	4.5		120	–	120	–	120	–	mJ
Forward-Bias Second Breakdown Collector Current (0.5-s non-repetitive pulse)	$I_{S/b}$	35					1.2	–	1.2	–	1.2	–	A
Thermal Resistance Junction-to-Case	$R_{\theta JC}$						–	3.12	–	3.12	–	3.12	°C/W

[a] Pulsed: Pulse duration = 300 μs, duty factor = 1.8%.

[b] $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse bias conditions. $E_{S/b} = \frac{1}{2}LI^2$ where L is a series load or leakage inductance, and I is the peak collector current.

* In accordance with JEDEC registration data format JS-6 RDF-2.

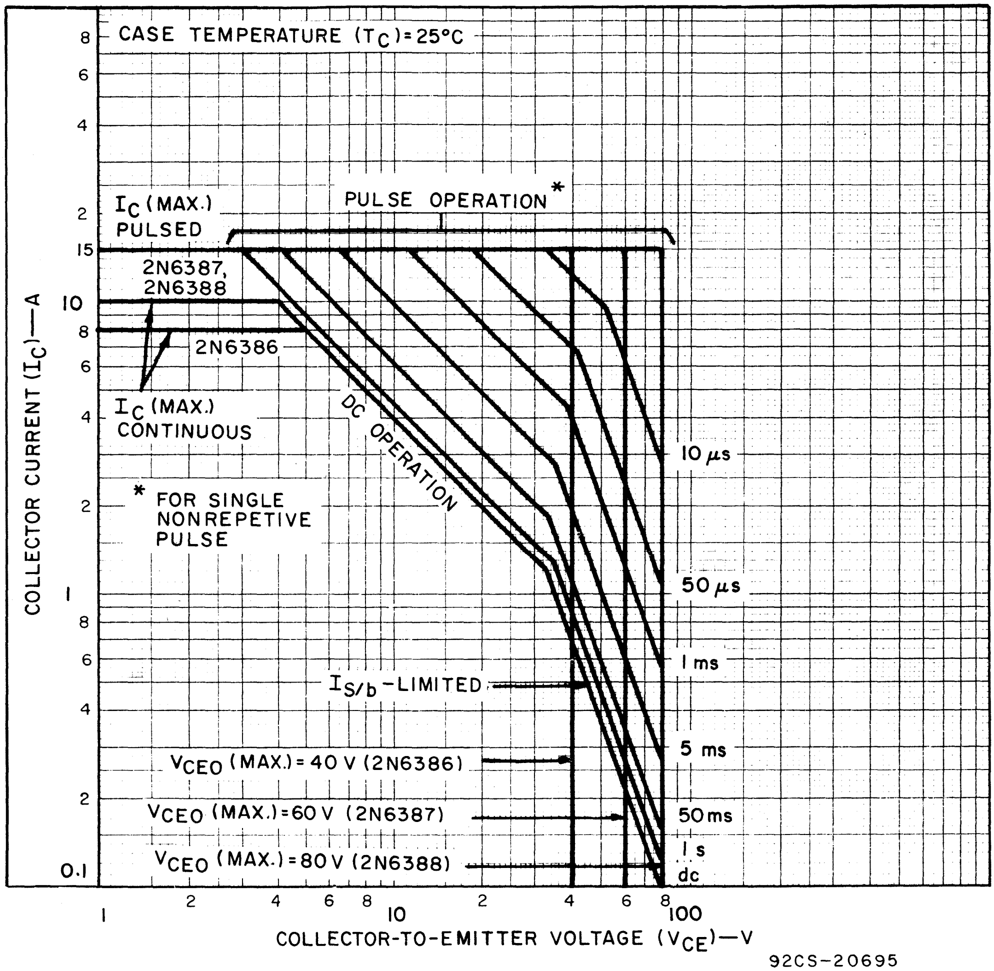


Fig. 2—Maximum operating area for all types.

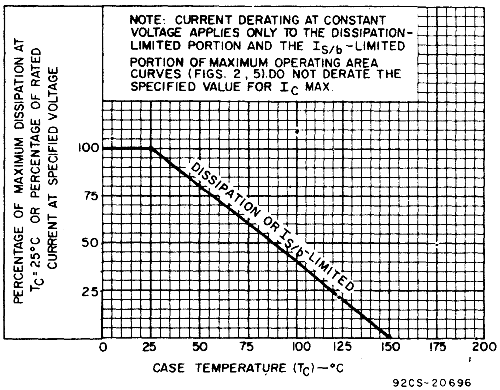


Fig. 3—Derating curves for all types.

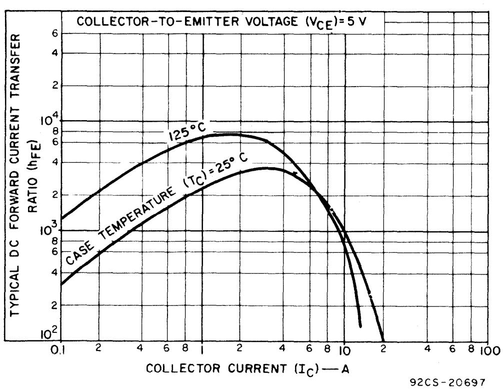


Fig. 4—Typical dc-beta characteristics for all types.

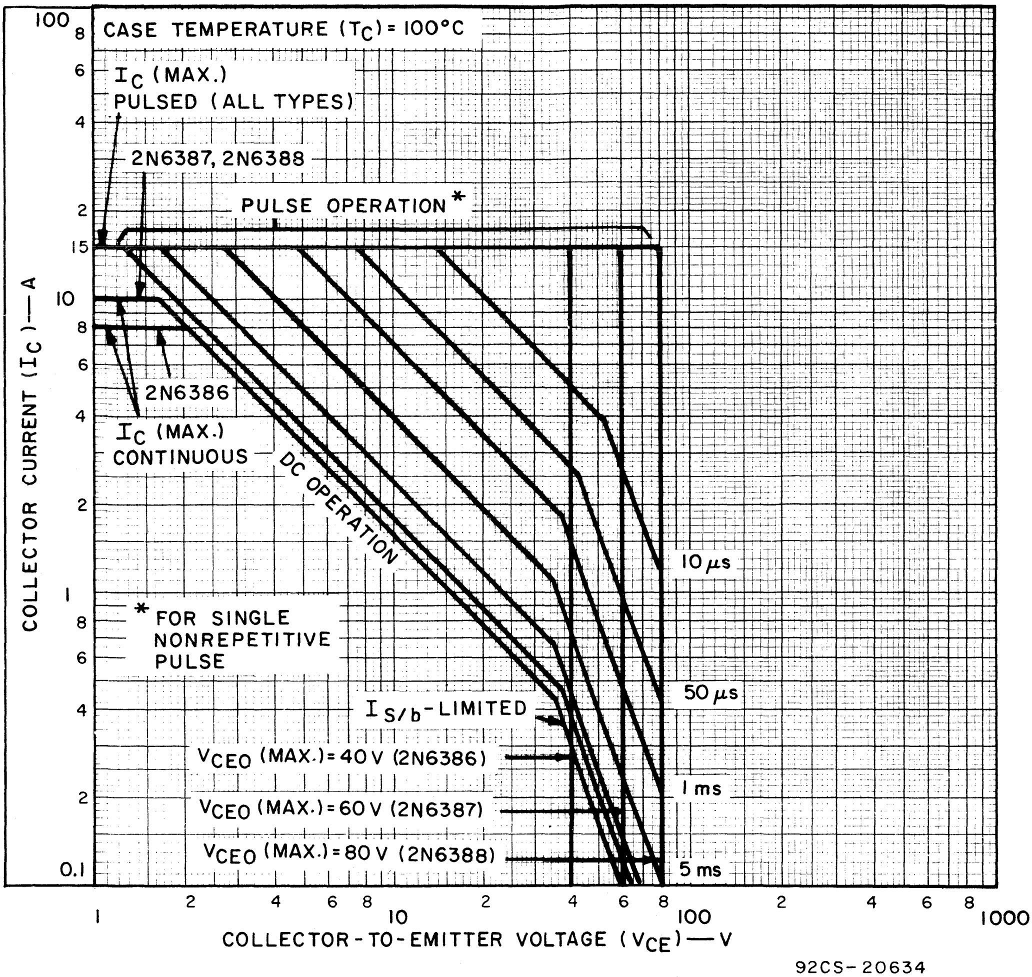


Fig. 5—Maximum operating area for all types.

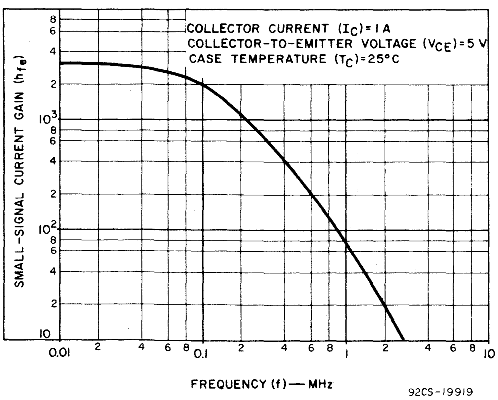


Fig. 6—Typical small-signal gain for all types.

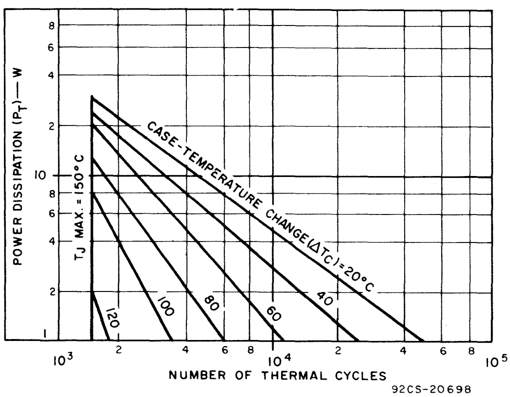


Fig. 7—Thermal-cycling rating chart for all types.

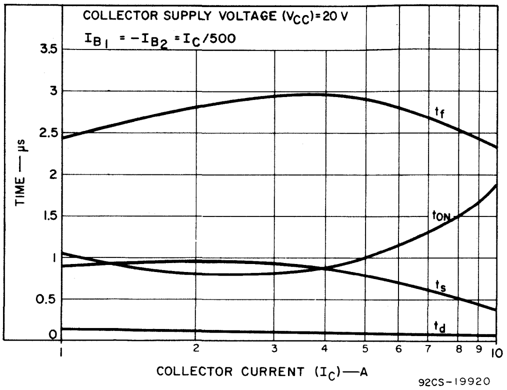


Fig. 8—Typical saturated switching-time characteristics for all types.

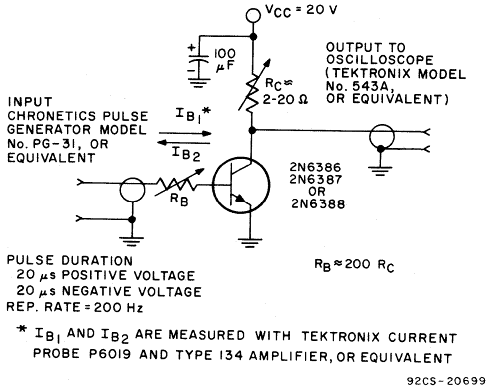


Fig. 9—Circuit used to measure saturated switching times.

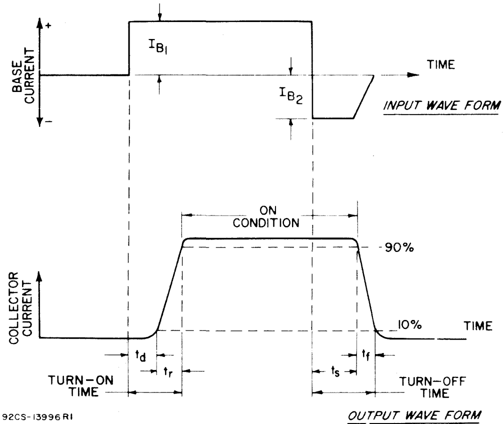


Fig. 10—Phase relationship between input current and output current showing reference points for specification of switching times (test circuit shown in Fig. 9).

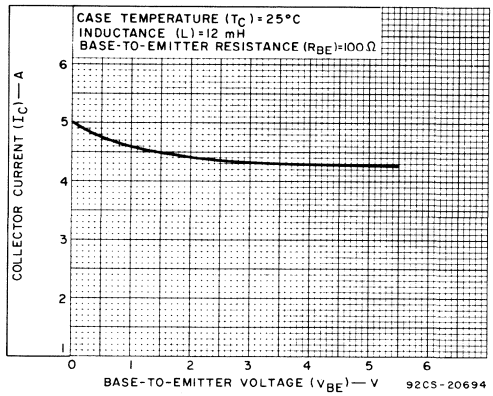


Fig. 11—Minimum values of reverse-bias second breakdown characteristic ($E_{S/b}$) for all types.

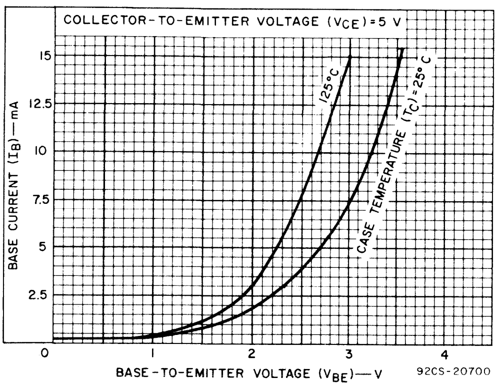


Fig. 12—Typical input characteristics for all types.

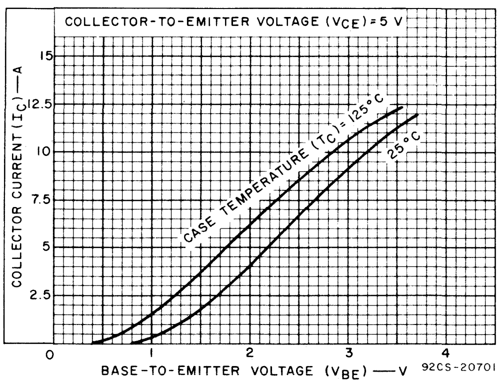


Fig. 13—Typical transfer characteristics for all types.

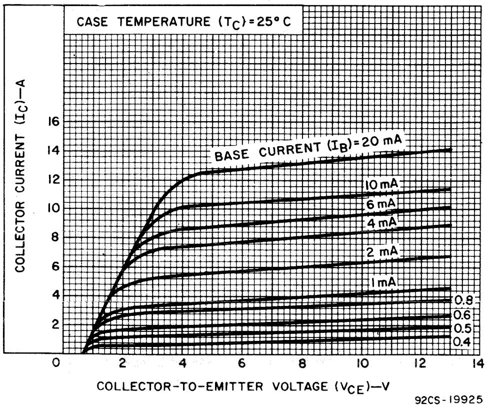


Fig. 14—Typical output characteristics for all types.

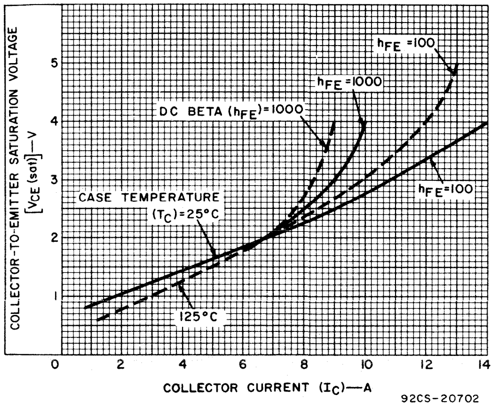
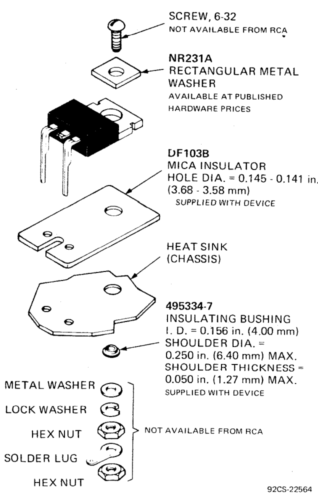
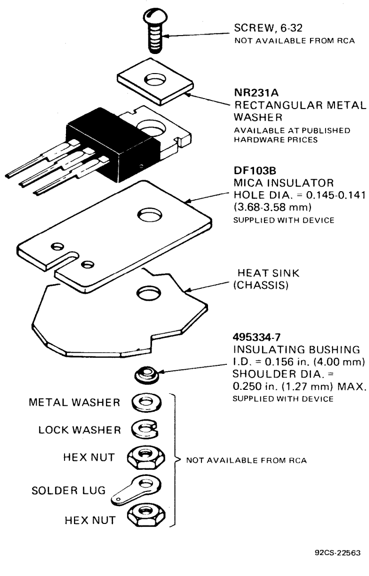


Fig. 15—Typical saturation characteristics for all types.





In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 16—Suggested mounting hardware for use with JEDEC TO-220 AA package.

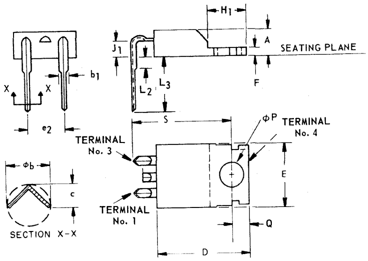
Fig. 17—Suggested mounting hardware for use with JEDEC TO-220 AB package.

VERSAWATT PACKAGE MOUNTING

For complete discussion on handling and mounting of RCA molded-plastic power devices, refer to RCA Application Note AN-4124.

For basic transistor theory, circuits, and application information, refer to "RCA Solid State Power Circuits Designer's Handbook", SP-52 or "RCA Transistor, Thyristor, & Diode" manual, SC-15.

DIMENSIONAL OUTLINE FOR OPTIONAL LEAD CONFIGURATION (JEDEC TO-220 AA)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.02	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e_2	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L_2	–	0.050	–	1.27	–
L_3	0.360	0.422	9.15	10.71	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–
S	0.580	0.610	14.74	15.49	–

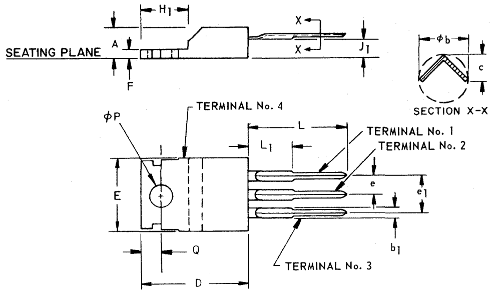
92CS-17990R1

NOTES:
1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.050 – 0.055 (1.27 – 1.40 mm) below seating plane.

TERMINAL CONNECTIONS

Lead No. 1 – Base
Stub – Do not use stub as tie point.
Lead No. 3 – Emitter
Mounting Flange – Collector

STANDARD DIMENSIONAL OUTLINE FOR 2N6386, 2N6387, and 2N6388 (JEDEC TO-220 AB)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

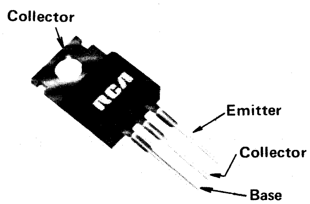
NOTES:
1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS

Lead No. 1 – Base
Lead No. 2 – Collector
Lead No. 3 – Emitter
Mounting Flange – Collector

RCA
Solid State Division

Power Transistors
Preliminary Data
BDX33 BDX33A
BDX33B BDX33C



JEDEC TO-220AB H1535R1

10-Ampere N-P-N Darlington Power Transistors

45-60-80-100 Volts, 70 Watts

Gain of 750 at 4 A (BDX33, BDX33A)
Gain of 750 at 3 A (BDX33B, BDX33C)

Features:

- Operates from IC without predriver
- Low leakage at high temperature
- High reverse second-breakdown capability

Applications:

- Power switching
- Audio amplifiers
- Hammer drivers
- Series and shunt regulators

The BDX33, BDX33A, BDX33B, and BDX33C are monolithic silicon Darlington transistors designed for low- and medium-frequency power applications. The high gain of these devices makes it possible for them to be driven directly from integrated circuits. They are complementary to the BDX34, BDX34A, BDX34B, and BDX34C, described in File 694.

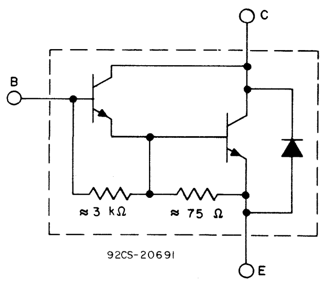


Fig. 1—Schematic diagram for all types.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		BDX33	BDX33A	BDX33B	BDX33C	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	45	60	80	100	V
COLLECTOR-TO-EMITTER VOLTAGE:						
With external base-to-emitter resistance (R_{BE}) = 100Ω, sustaining	$V_{CER}(sus)$	45	60	80	100	V
With base open, sustaining	$V_{CEO}(sus)$	45	60	80	100	V
With base reverse-biased V_{BE} = −1.5 V	$V_{CEX}(sus)$	45	60	80	100	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	5	5	5	V
CONTINUOUS COLLECTOR CURRENT	I_C	10	10	10	10	A
CONTINUOUS BASE CURRENT	I_B	0.25	0.25	0.25	0.25	A
TRANSISTOR DISSIPATION:	P_T					
At case temperatures up to 25°C		70	70	70	70	W
At case temperatures above 25°C		Derate linearly 0.56				W/°C
TEMPERATURE RANGE:						
Storage and Operating (Junction)		← −65 to +150 →				°C
LEAD TEMPERATURE (During Soldering):						
At distances ≥ 1/8 in. (3.17 mm) from case for 10 s max.		← 235 →				°C

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ELECTRICAL CHARACTERISTICS, *At Case Temperature (TC) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: VOLTAGE V dc				CURRENT A dc		LIMITS: BDX33C		BDX33B		BDX33A		BDX33		UNITS
		V_{CB}	V_{CE}	V_{EB}	V_{BE}	I_C	I_B	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Collector Cutoff Current With base open	I_{CEO}		50				0	–	0.5	–	–	–	–	–	–	mA
			40				0	–	–	–	0.5	–	–	–	–	
			30				0	–	–	–	–	–	0.5	–	–	
			20				0	–	–	–	–	–	–	–	0.5	
With base open and T_C = 100°C			50				0	–	10	–	–	–	–	–	–	
			40				0	–	–	–	10	–	–	–	–	
			30				0	–	–	–	–	–	10	–	–	
			20				0	–	–	–	–	–	–	–	10	
With emitter open	I_{CBO}	100						–	1	–	–	–	–	–	–	
		80						–	–	–	1	–	–	–	–	
		60						–	–	–	–	–	1	–	–	
		45						–	–	–	–	–	–	–	1	
With emitter open and T_C = 100°C		100						–	5	–	–	–	–	–	–	
		80						–	–	–	5	–	–	–	–	
		60						–	–	–	–	–	5	–	–	
		45						–	–	–	–	–	–	–	5	
Emitter-Cutoff Current	I_{EBO}			5		0		–	10	–	10	–	10	–	10	mA
Collector-to-Emitter Sustaining Voltage: With base open	$V_{CEO}(sus)$					0.1[a]	0	100	–	80	–	60	–	45	–	V
With external-base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$					0.1[a]		100	–	80	–	60	–	45	–	
With base-emitter junction reverse-biased	$V_{CEV}(sus)$				–1.5	0.1[a]		100	–	80	–	60	–	45	–	
DC Forward-Current Transfer Ratio	h_{FE}		3			3[a]		750	–	750	–	–	–	–	–	
			3			4[a]		–	–	–	–	750	–	750	–	
Base-to-Emitter Voltage	V_{BE}		3			3[a]		–	2.5	–	2.5	–	–	–	–	V
			3			4[a]		–	–	–	–	–	2.5	–	2.5	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$					3[a]	0.006	–	2.5	–	2.5	–	–	–	–	V
						4[a]	0.008	–	–	–	–	–	2.5	–	2.5	
Parallel-Diode Forward Voltage Drop	V_F					8		–	4	–	4	–	4	–	4	V
Common-Emitter, Small-Signal, Short-Circuit Forward-Current Transfer Ratio: (f = 1 kHz)	h_{fe}		5			1		1000	–	1000	–	1000	–	1000	–	
Magnitude of Common Emitter, Small-Signal, Short-Circuit, Forward-Current Transfer Ratio (f = 1.0 MHz)	$\|h_{fe}\|$		5			1		20	–	20	–	20	–	20	–	
Second-Breakdown Energy With base reverse-biased and L = 12 mH, R_{BE} = 100Ω	$E_{S/b}$[b]				–1.5	4.5		120	–	120	–	120	–	120	–	mJ
Forward-Bias Second-Breakdown Collector Current (0.5-s non-repetitive pulse)	$I_{S/b}$		25					2.8	–	2.8	–	2.8	–	2.8	–	A
			36					1	–	1	–	1	–	1	–	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$							–	1.78	–	1.78	–	1.78	–	1.78	°C/W

[a] Pulsed: Pulse duration = 300 μs, duty factor = 1.8%.

[b] $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse bias conditions.
$E_{S/b} = 1/2LI^2$ where L is a series load or leakage inductance and I is the peak collector current.

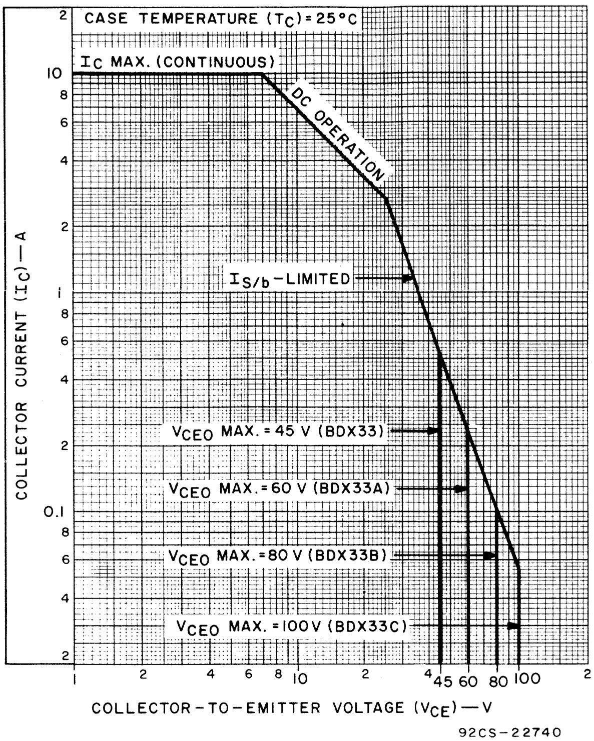


Fig. 2 — Maximum operating areas for all types.

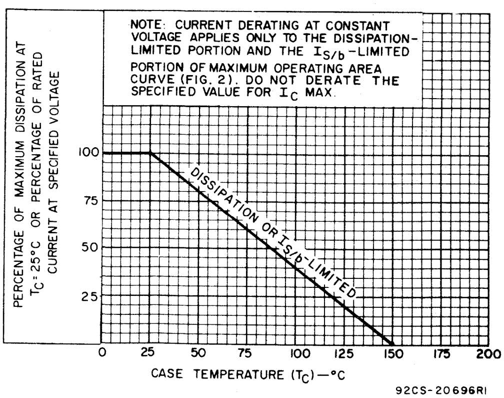


Fig. 3 — Current derating curve for all types.

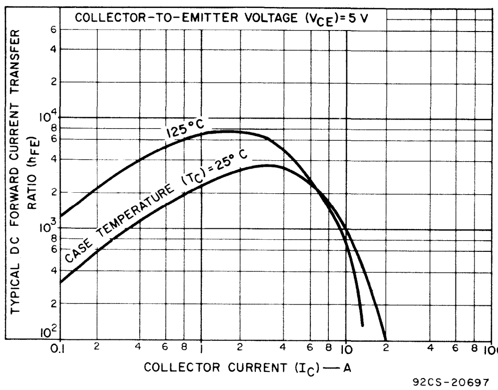


Fig. 4 — Typical dc-beta characteristics for all types.

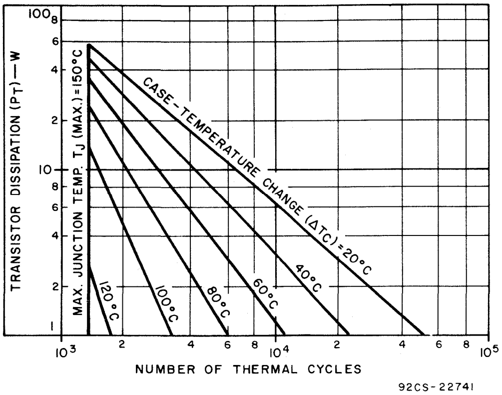


Fig. 5 — Thermal-cycling rating chart for all types.

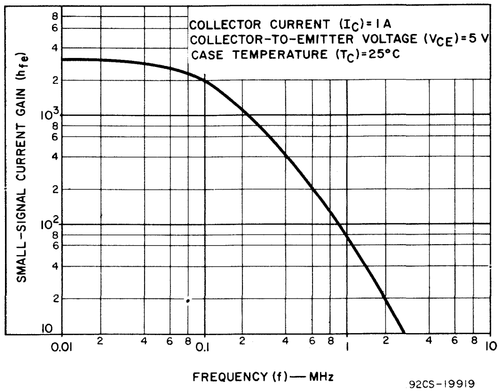


Fig. 6 — Typical small-signal gain for all types.

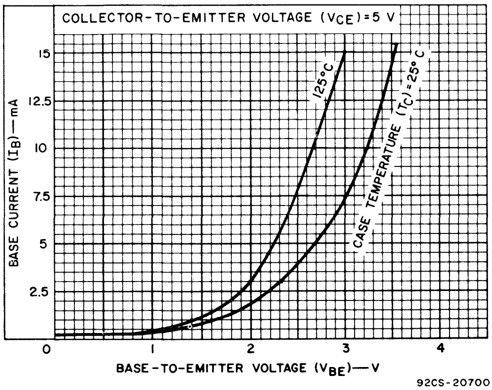


Fig. 7 — Typical input characteristics for all types.

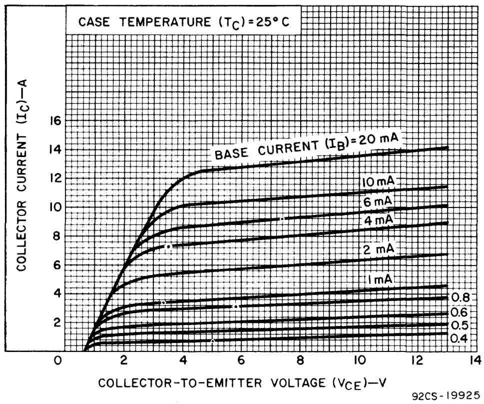


Fig. 8 — Typical output characteristics for all types.

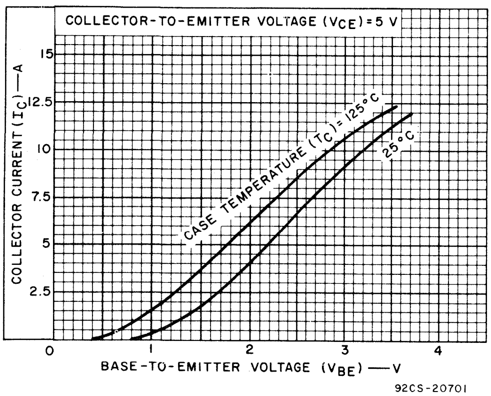


Fig. 9 — Typical transfer characteristics for all types.

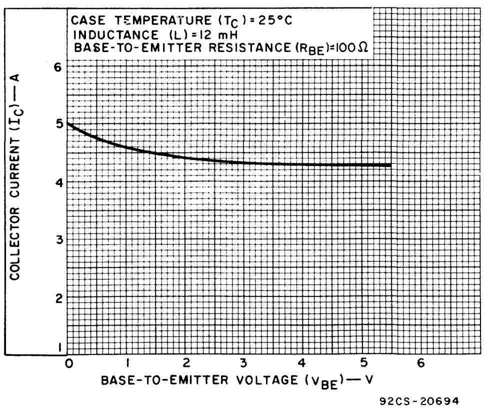


Fig. 10 — Minimum values of reverse-bias second breakdown characteristic ($E_{S/b}$) for all types.

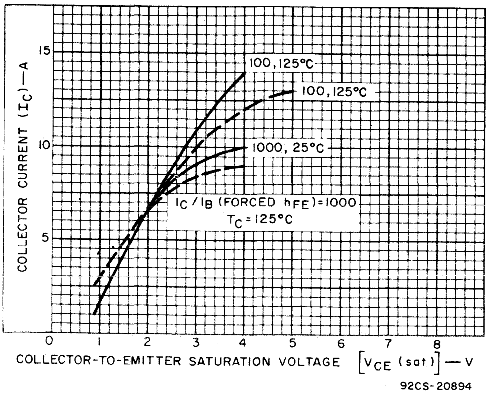


Fig. 11 — Typical saturation characteristics for all types.

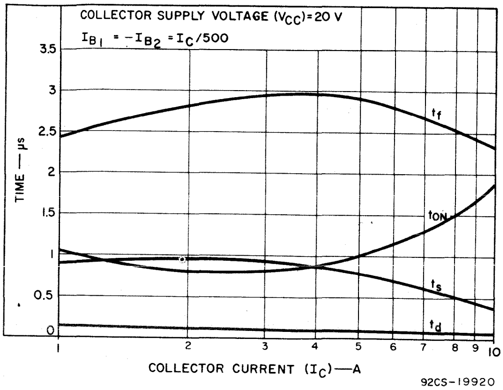


Fig. 12 — Typical saturated switching-time characteristics for all types.

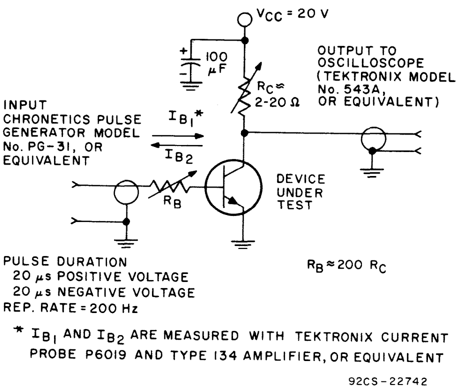


Fig. 13 — Circuit used to measure saturated switching times.

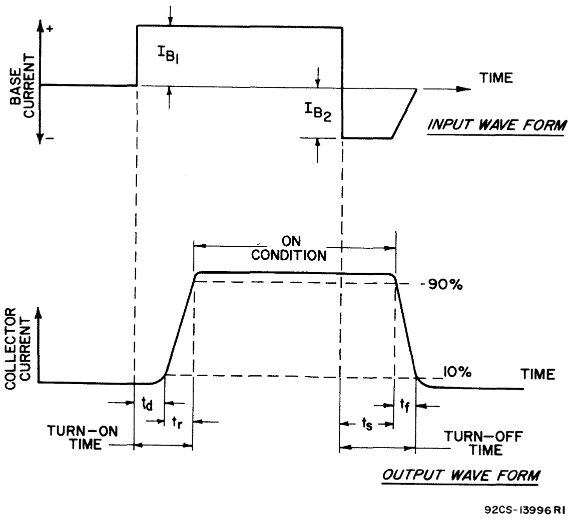


Fig. 14 — Phase relationship between input current and output current showing reference points for specification of switching times (test circuit shown in Fig. 13).

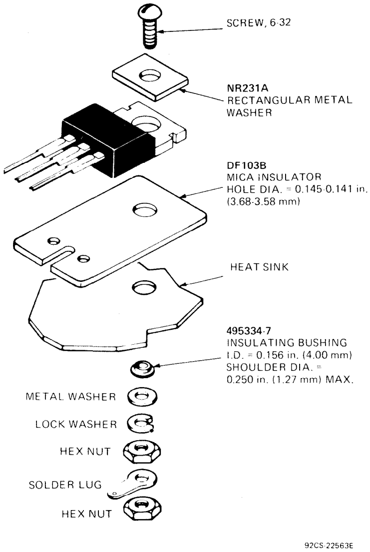
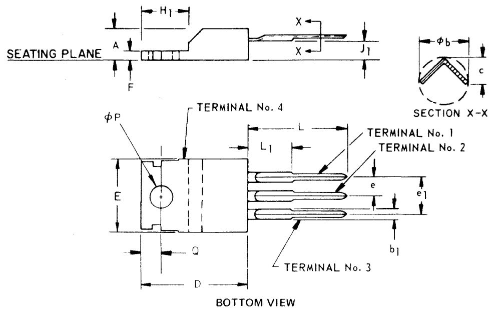


Fig. 15 — Suggested mounting hardware for use with JEDEC TO-220 AB package.

DIMENSIONAL OUTLINE JEDEC TO-220 AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
ϕb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
ϕP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

VERSAWATT PACKAGE MOUNTING

For complete discussion on handling and mounting of RCA molded-plastic power devices, refer to RCA Application Note AN-4124.

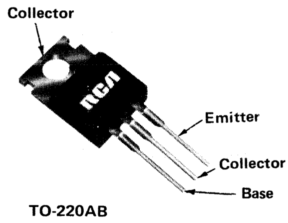
For basic transistor theory, circuits, and application information, refer to "RCA Solid State Power Circuits Designer's Handbook", SP-52, or "RCA Transistor, Thyristor, & Diode Manual", SC-15.

TERMINAL CONNECTIONS

Lead No. 1 – Base
Lead No. 2 – Collector
Lead No. 3 – Emitter
Mounting Flange – Collector

RCA Solid State Division

Power Transistors Preliminary Data
BDX34 BDX34A BDX34B BDX34C



10-Ampere P-N-P Darlington Power Transistors

45-60-80-100 Volts, 70 Watts
Gain of 750 at 4 A (BDX34, BDX34A)
Gain of 750 at 3 A (BDX34B, BDX34C)

Features:
- **Operates from IC without predriver**
- **Low leakage at high temperature**
- **High reverse second-breakdown capability**

Applications:
- **Power switching**
- **Audio amplifiers**
- **Hammer drivers**
- **Series and shunt regulators**

The BDX34, BDX34A, BDX34B, and BDX34C are monolithic p-n-p silicon Darlington transistors designed for low- and medium-frequency power applications. The high gain of these devices makes it possible for them to be driven directly from integrated circuits. They are complementary to the BDX33, BDX33A, BDX33B, and BDX33C, described in File 693.

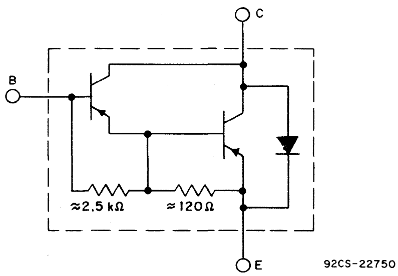


Fig.1 — Schematic diagram for all types.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		BDX34	BDX34A	BDX34B	BDX34C	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	−45	−60	−80	−100	V
COLLECTOR-TO-EMITTER VOLTAGE:						
With external base-to-emitter resistance (R_{BE}) = 100 Ω, sustaining	$V_{CER}(sus)$	−45	−60	−80	−100	V
With base open, sustaining	$V_{CEO}(sus)$	−45	−60	−80	−100	V
With base reverse-biased V_{BE} = −1.5 V	$V_{CEX}(sus)$	−45	−60	−80	−100	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	−5	−5	−5	−5	V
CONTINUOUS COLLECTOR CURRENT	I_C	−10	−10	−10	−10	A
CONTINUOUS BASE CURRENT	I_B	−0.25	−0.25	−0.25	−0.25	A
TRANSISTOR DISSIPATION:						
At case temperatures up to 25°C		70	70	70	70	W
At case temperatures above 25°C		Derate linearly 0.56				W/°C
TEMPERATURE RANGE:						
Storage and Operating (Junction)		← −65 to + 150 →				°C
LEAD TEMPERATURE (During Soldering):						
At distances ≥ 1/8 in. (3.17 mm) from case for 10 s max.		← 235 →				°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS						LIMITS								UNITS
		VOLTAGE V dc				CURRENT A dc		BDX34C		BDX34B		BDX34A		BDX34		
		V_{CB}	V_{CE}	V_{EB}	V_{BE}	I_C	I_B	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Collector Cutoff Current With base open	I_{CEO}		–50				0	–	–0.5	–	–	–	–	–	–	mA
			–40				0	–	–	–	–0.5	–	–	–	–	
			–30				0	–	–	–	–	–	–0.5	–	–	
			–20				0	–	–	–	–	–	–	–	–0.5	
With base open and T_C = 100°C			–50				0	–	–10	–	–	–	–	–	–	
			–40				0	–	–	–	–10	–	–	–	–	
			–30				0	–	–	–	–	–	–10	–	–	
			–20				0	–	–	–	–	–	–	–	–10	
With emitter open	I_{CBO}	–100						–	–1	–	–	–	–	–	–	
		–80						–	–	–	–1	–	–	–	–	
		–60						–	–	–	–	–	–1	–	–	
		–45						–	–	–	–	–	–	–	–1	
With emitter open and T_C = 100°C		–100						–	–5	–	–	–	–	–	–	
		–80						–	–	–	–5	–	–	–	–	
		–60						–	–	–	–	–	–5	–	–	
		–45						–	–	–	–	–	–	–	–5	
Emitter-Cutoff Current	I_{EBO}			–5		0		–	–10	–	–10	–	–10	–	–10	mA
Collector-to-Emitter Sustaining Voltage: With base open	V_{CEO}(sus)					–0.1[a]	0	–100	–	–80	–	–60	–	–45	–	
With external-base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}(sus)					–0.1[a]		–100	–	–80	–	–60	–	–45	–	V
With base-emitter junction reverse-biased	V_{CEV}(sus)				1.5	–0.1[a]		–100	–	–80	–	–60	–	–45	–	
DC Forward-Current Transfer Ratio	h_{FE}		–3			–3[a]		750	–	750	–	–	–	–	–	
			–3			–4[a]		–	–	–	–	750	–	750	–	
Base-to-Emitter Voltage	V_{BE}		–3			–3[a]		–	–2.5	–	–2.5	–	–	–	–	V
			–3			–4[a]		–	–	–	–	–	–2.5	–	–2.5	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)					–3[a]	–0.006	–	–2.5	–	–2.5	–	–	–	–	V
						–4[a]	–0.008	–	–	–	–	–	–2.5	–	–2.5	
Parallel-Diode Forward Voltage Drop	V_F					–8		–	–4	–	–4	–	–4	–	–4	V
Common-Emitter, Small-Signal, Short-Circuit Forward-Current Transfer Ratio: (f = 1 kHz)	h_{fe}		–5			–1		1000	–	1000	–	1000	–	1000	–	
Magnitude of Common Emitter, Small-Signal, Short-Circuit, Forward-Current Transfer Ratio (f = 1.0 MHz)	$\|h_{fe}\|$		–5			–1		20	–	20	–	20	–	20	–	
Second-Breakdown Energy With base reverse-biased and L = 3 mH, R_{BE} = 100 Ω	$E_{S/b}$[b]				+1.5	–4.5		30	–	30	–	30	–	30	–	mJ
Forward-Bias Second-Breakdown Collector Current (0.5-s non-repetitive pulse)	$I_{S/b}$		–20					–3.5	–	–3.5	–	–3.5	–	–3.5		A
			–33					–1	–	–1	–	–1	–	–1	–	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$							–	1.78	–	1.78	–	1.78	–	1.78	°C/W

[a] Pulsed: Pulse duration = 300 μs, duty factor = 1.8%.
[b] $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse bias conditions.
$E_{S/b}$ = 1/2LI^2 where L is a series load or leakage inductance and I is the peak collector current.

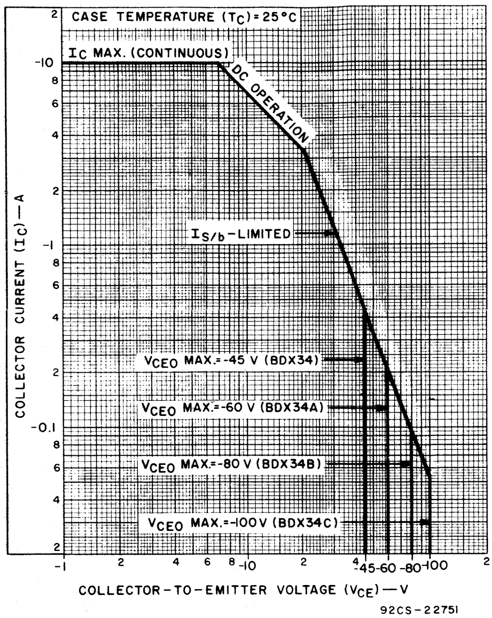


Fig.2 — Maximum operating areas for all types.

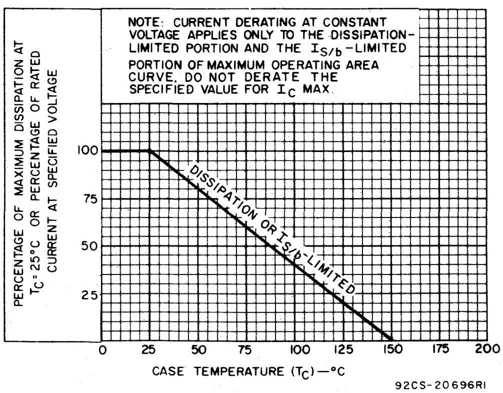


Fig.3 — Current derating curve for all types.

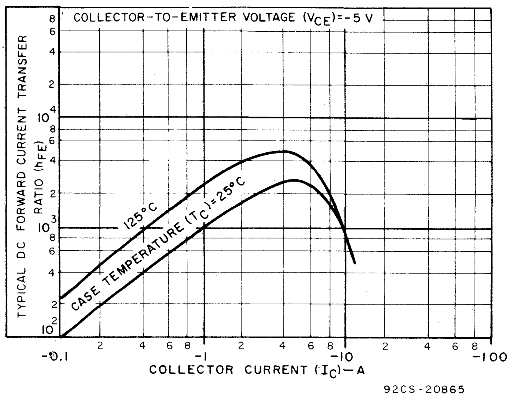


Fig.4 — Typical dc beta characteristics for all types.

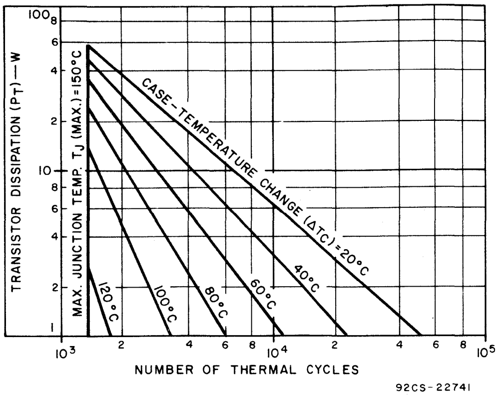


Fig.5 — Thermal-cycling rating chart for all types.

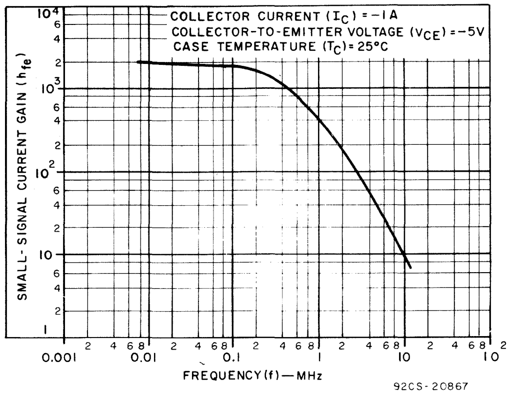


Fig.6 — Typical small-signal gain for all types.

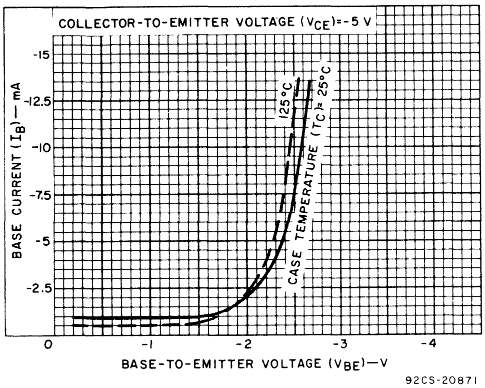


Fig.7 — Typical input characteristics for all types.

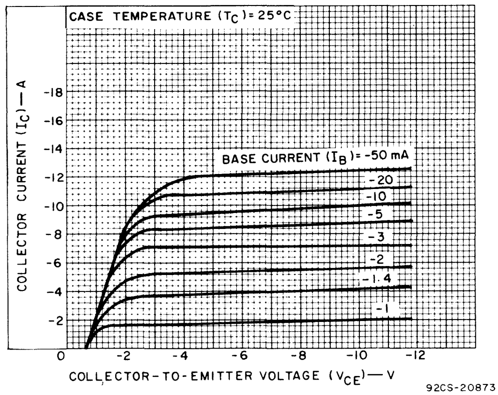


Fig.8 — Typical output characteristics for all types.

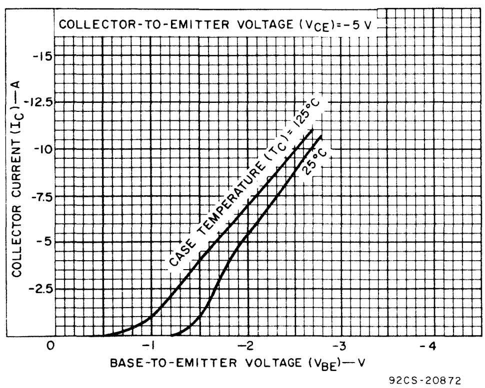


Fig.9 — Typical transfer characteristics for all types.

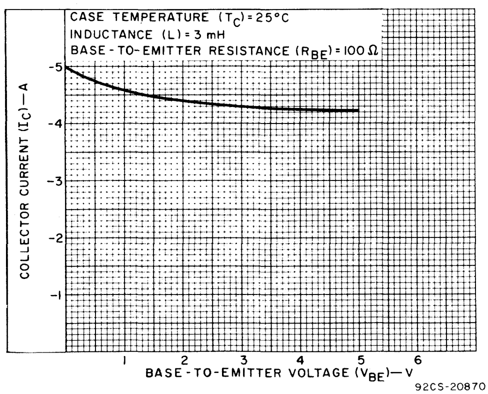


Fig.10 — Minimum values of reverse-bias second breakdown characteristic ($E_{S/b}$) for all types.

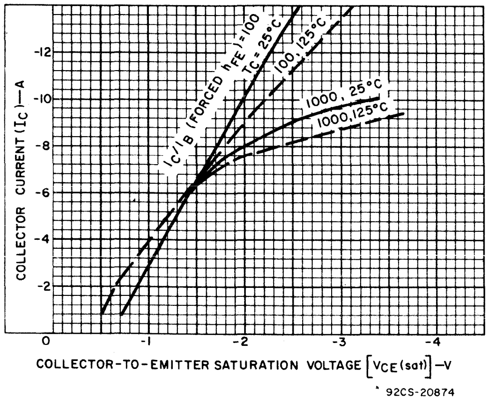


Fig. 11 — Typical saturation characteristics for all types.

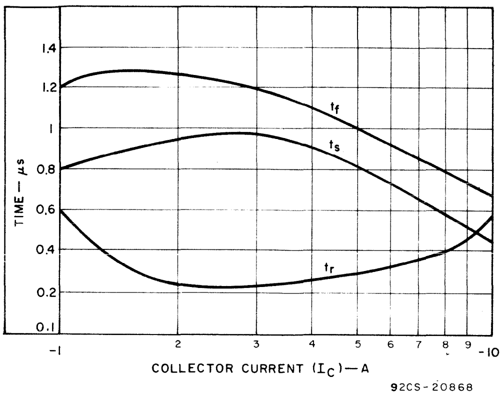


Fig. 12 — Typical saturated switching-time characteristics for all types.

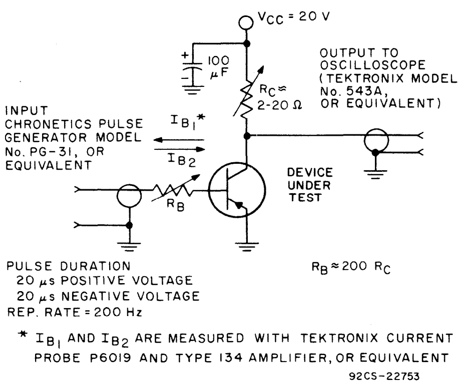


Fig. 13 — Circuit used to measure saturated switching times.

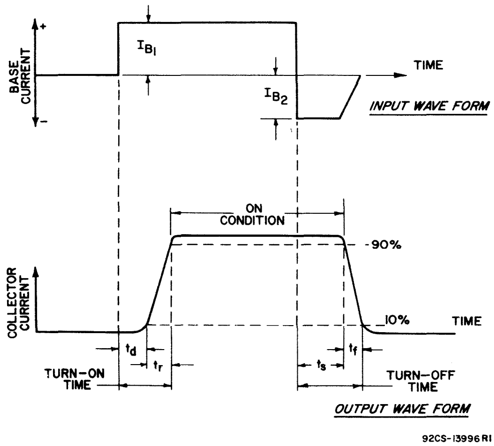


Fig. 14 — Phase relationship between input current and output current showing reference points for specification of switching times (test circuit shown in Fig. 13).

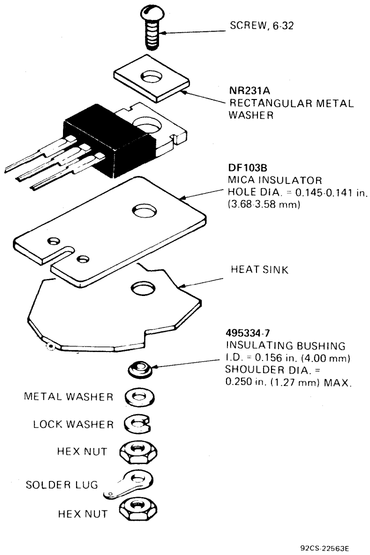


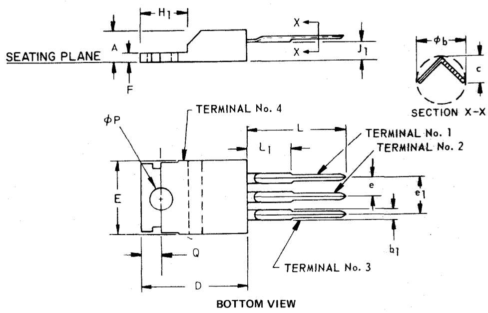
Fig. 15 — Suggested mounting hardware for use with JEDEC TO-220AB package.

VERSAWATT PACKAGE MOUNTING

For complete discussion on handling and mounting of RCA molded-plastic power devices, refer to RCA Application Note AN-4124.

For basic transistor theory, circuits, and application information, refer to "RCA Solid State Power Circuits Designer's Handbook", SP-52, or "RCA Transistor, Thyristor, & Diode Manual", SC-15.

DIMENSIONAL OUTLINE
JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:
1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

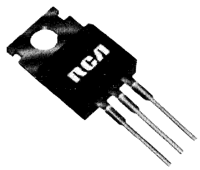
TERMINAL CONNECTIONS

Lead No. 1 — Base
Lead No. 2 — Collector
Lead No. 3 — Emitter
Mounting Flange — Collector

Special Audio Power Transistors

Solid State Division

Power Transistors
RCA1C10
RCA1C11



RCA1C10
RCA1C11

JEDEC TO-220AB H-1535R1

Silicon Transistors for 12-Watt True-Complementary-Symmetry Audio Amplifiers

RCA1C10 and RCA1C11 are n-p-n and p-n-p epitaxial-base silicon power transistors, respectively, especially characterized for audio-output service. To enhance circuit economics, they are provided in the JEDEC TO-220AB version of the VERSAWATT plastic package.

The 12-watt audio-amplifier circuit shown in Figs. 1 and 7 uses RCA1C10 and RCA1C11 as output devices in conjunction with three discrete transistors, two diodes, and a single 36-volt power supply; the amplifier output is capacitively coupled to an 8-ohm speaker. The choice of a true-complementary-symmetry output stage provides excellent fidelity for a low-cost system.

The 12-watt amplifier circuit shown in Figs. 2 and 10 uses RCA1C10 and RCA1C11 discrete transistors, an integrated circuit, one diode, and a 36-volt split power supply; the amplifier output is directly coupled to an 8-ohm speaker. The integrated circuit-true-complementary-symmetry combination provides a high-quality, low-cost amplifier.

The RCA CA3094AT integrated circuit provides sufficient drive current for the complementary-symmetry output stage. Tone controls, bass and treble, with functions of "boost" and "cut" are incorporated into the feedback loop of the amplifier, resulting in excellent signal-to-noise ratio and freedom from distortion. Ratings and characteristics of type CA3094AT are given in RCA data bulletin File 598.

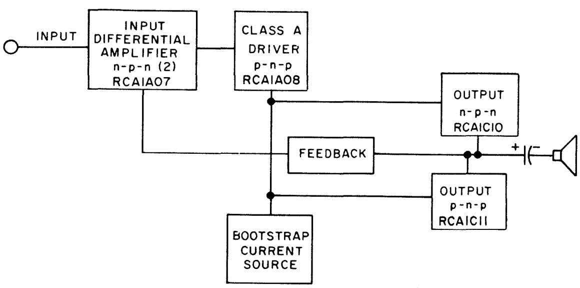


Fig. 1— Block diagram and transistor complement for 12-watt true-complementary-symmetry audio amplifier.

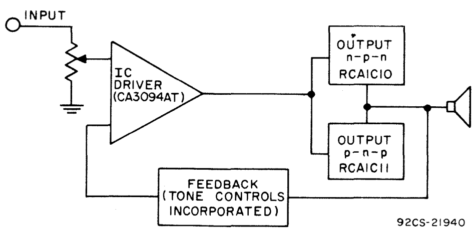


Fig.2— Block diagram and transistor complement for 12-watt true-complementary-symmetry audio amplifier with integrated-circuit driver.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		RCA1C10	RCA1C11	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	40	–40	V
COLLECTOR-TO-EMITTER VOLTAGE:				
With base open	V_{CEO}	40	–40	V
With external base-to-emitter resistance (R_{BE}) = 100Ω	V_{CER}	50	–50	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	–5	V
COLLECTOR CURRENT	I_C	7	–7	A
BASE CURRENT	I_B	3	–3	A
TRANSISTOR DISSIPATION:	P_T			
At case temperatures up to 25°C		40	40	W
At case temperatures above 25°C		← See Fig. 3 →		
TEMPERATURE RANGE:				
Storage & Operating (Junction)		← –65 to 150 →		°C
PIN TEMPERATURE (During Soldering):				
At distances ≥1/32 in. (0.8 mm) from case for 10 s max.		← 230 →		°C

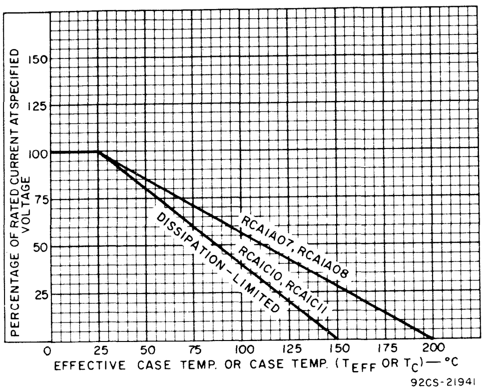


Fig.3 – Derating curves for all types.

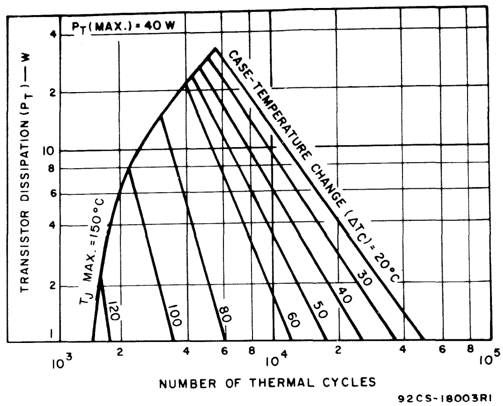


Fig.4 – Thermal-cycling ratings for RCA1C10 and RCA1C11.

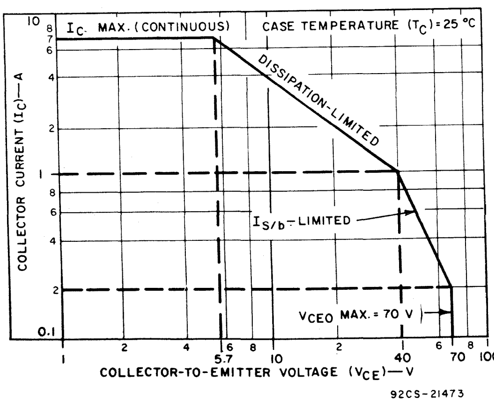


Fig.5 – Maximum operating areas for RCA1C10.

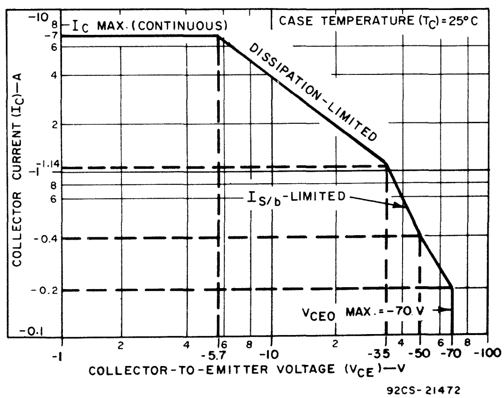


Fig.6 – Maximum operating areas for RCA1C11.

Type RCA1C10
Package: JEDEC TO-220AB
Construction: Silicon n-p-n, epitaxial-base

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 35 V, R_{BE} = 100Ω	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 5 V	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 0.1 A, I_B = 0	40	–	V
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = 0.1 A, R_{BE} = 100Ω	50	–	V
Gain Bandwidth Product	f_T	V_{CE} = 4 V, I_C = 0.5 A	4	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 1.5 A, V_{CE} = 4 V	50	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 1.5 A, I_B = 0.075 A	–	1	V
Base-to-Emitter Voltage	V_{BE}	I_C = 1.5 A, V_{CE} = 4 V	–	1.5	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 20 V, t = 0.4 s	2	–	A

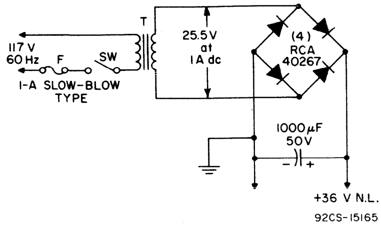
For characteristics curves and test conditions, refer to published data for prototype 2N6292 (File 542).

Type RCA1C11
Package: JEDEC TO-220AB
Construction: Silicon p-n-p, epitaxial base

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = –35 V, R_{BE} = 100Ω	–	–10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –5 V	–	–1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = –0.1 A, I_B = 0	–40	–	V
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = –0.1 A, R_{BE} = 100Ω	–50	–	V
Gain Bandwidth Product	f_T	V_{CE} = –4 V, I_C = –0.5 A	10	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –1.5 A, V_{CE} = –4 V	50	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = –1.5 A, I_B = –0.075 A	–	–1	V
Base-to-Emitter Voltage	V_{BE}	I_C = –1.5 A, V_{CE} = –4 V	–	–1.5	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = –20 V, t = 0.4 s	–2	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N6107 (File 488).



NOTES:
1. T: Thordarson 23V118, Stancor TP4, Triad F-93X, or equivalent (for Stereo Amplifiers).
2. Resistors are 1/2-watt unless otherwise specified; values are in ohms.
3. Capacitances are in µF unless otherwise specified.
4. Non-inductive resistors.

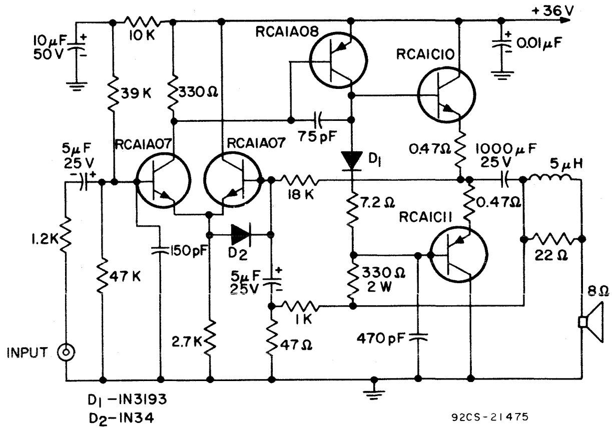


Fig.7— 12-watt amplifier circuit featuring complementary-symmetry output.

TYPICAL PERFORMANCE DATA
For 12-Watt Audio Amplifier Circuit

Measured at a line voltage of 120 V, T_A = 25°C, and a frequency of 1 kHz, unless otherwise specified.

Power:	
Rated power (8-Ω load, at rated distortion)	12 W
Typical power (4-Ω load)	12 W
Typical power (16-Ω load)	6.5 W
Music power (8-Ω load, at 5% THD with regulated supply)	15 W
Dynamic power (8-Ω load, at 1% THD with regulated supply)	13 W
Total Harmonic Distortion:	
Rated distortion	1.0%
IM Distortion:	
10 dB below continuous power output at 60 Hz and 7 kHz (4:1)	1.5%
Sensitivity:	
At continuous power-output rating	600 mV
Hum and Noise:	
Below continuous power output:	
Input shorted	90 dB
Input open	70 dB
Input Resistance	23 kΩ

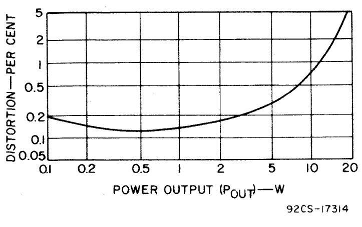


Fig.8—Distortion vs. power output.

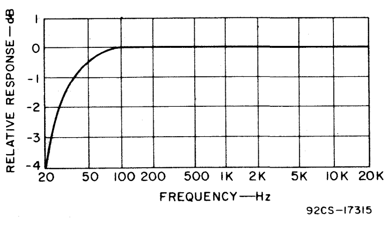
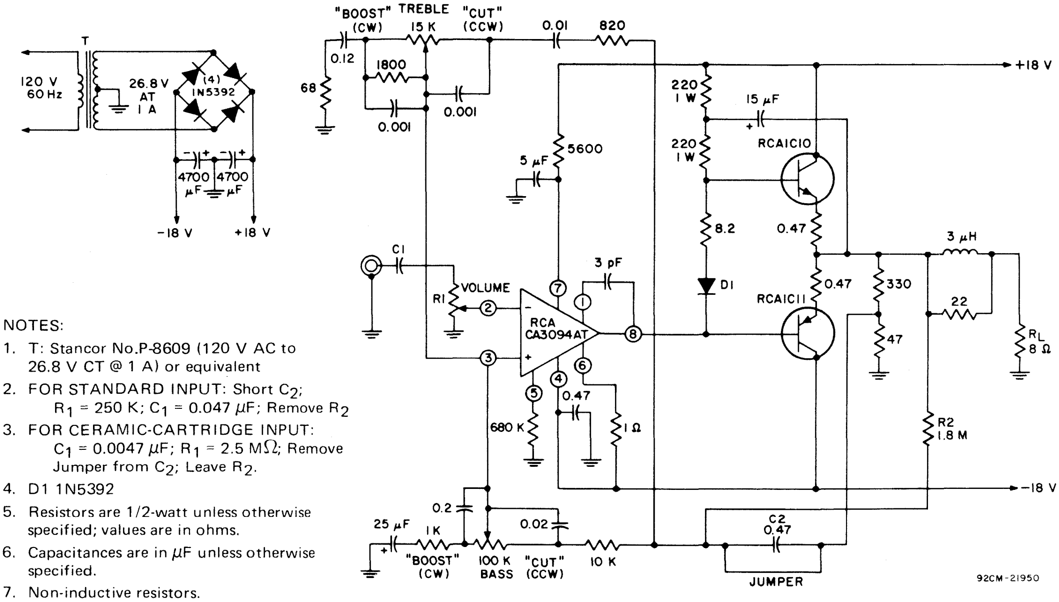


Fig.9—Response curve.



NOTES:

1. T: Stancor No.P-8609 (120 V AC to 26.8 V CT @ 1 A) or equivalent
2. FOR STANDARD INPUT: Short C_2; R_1 = 250 K; C_1 = 0.047 μF; Remove R_2
3. FOR CERAMIC-CARTRIDGE INPUT: C_1 = 0.0047 μF; R_1 = 2.5 MΩ; Remove Jumper from C_2; Leave R_2.
4. D1 1N5392
5. Resistors are 1/2-watt unless otherwise specified; values are in ohms.
6. Capacitances are in μF unless otherwise specified.
7. Non-inductive resistors.

Fig. 10—12-watt amplifier circuit featuring an integrated-circuit driver and a true-complementary-symmetry output stage.

TYPICAL PERFORMANCE DATA

For 12-Watt Audio Amplifier Circuit

Measured at a line voltage of 120 V, T_A = 25°C, and a frequency of 1 kHz, unless otherwise specified.

Power:

Rated power (8-Ω load, at rated distortion)	12 W
Typical power (4-Ω load)	9 W
Typical power (16-Ω load)	6.5 W
Music power (8-Ω load, at 5% THD with regulated supply)	15 W

Total Harmonic Distortion:

Rated distortion	1.0%
Typical at 1 W	0.05%

IM Distortion:

10 dB below continuous power output at 60 Hz and 2 kHz (4:1)	0.2%

Sensitivity:

At continuous power-output rating (tone controls flat)	100 mV

Hum and Noise:

Below continuous power output: Input open	83 dB
Input resistance	250 kΩ
Voltage Gain	40 dB
Tone Control Range	See Fig.12

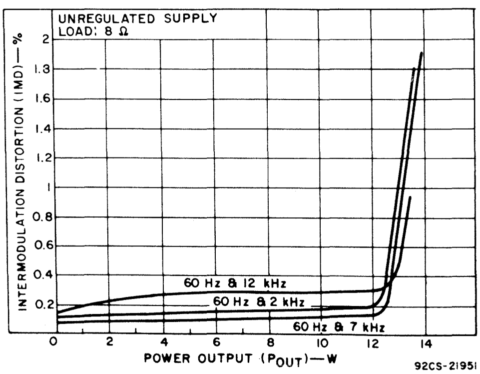


Fig. 11—Intermodulation distortion vs. power output.

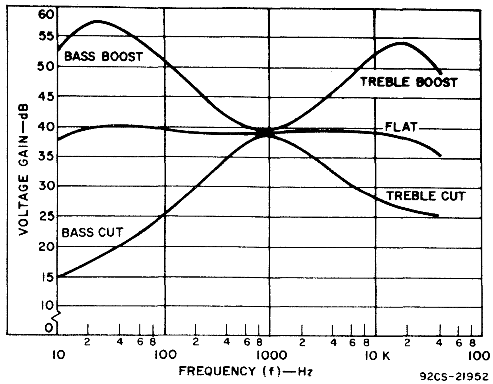


Fig. 12—Voltage gain vs. frequency.

		RCA1A07	RCA1A08	
MAXIMUM RATINGS, *Absolute-Maximum Values:*				
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	50	−50	V
COLLECTOR-TO-EMITTER VOLTAGE:				
With base open	V_{CEO}	40	−40	V
With external base-to-emitter resistance (R_{BE}) = 10Ω	V_{CER}	50	–	V
With external base-to-emitter resistance (R_{BE}) = 300Ω	V_{CER}	–	−50	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	3	−5	V
COLLECTOR CURRENT	I_C	1	−1	A
BASE CURRENT	I_B	0.05	−0.05	A
TRANSISTOR DISSIPATION:	P_T			
At case temperatures up to 25°C		5	7	W
At case temperatures above 25°C		← *See Fig. 3* →		
TEMPERATURE RANGE:				
Storage & Operating (Junction)		← −65 to +200 →		°C
PIN TEMPERATURE (During Soldering):				
At distances ≥1/32 in. (0.8 mm) from case for 10 s max.		← 230 →		°C

For ratings and characteristics of Integrated Circuit Type CA3094T, refer to published data in File 598.

Type RCA1A07
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 40 V	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 3 V, I_C = 0	–	0.1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 100 mA	40	–	V
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = 100 mA, R_{BE} = 10Ω	50	–	V
Gain Bandwidth Product	f_T	V_{CE} = 10 V, I_C = 50 mA	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 3 mA, V_{CE} = 10 V	50	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 20 mA, I_B = 1 mA	–	1	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$	I_C = 20 mA, I_B = 1 mA	–	1.3	V

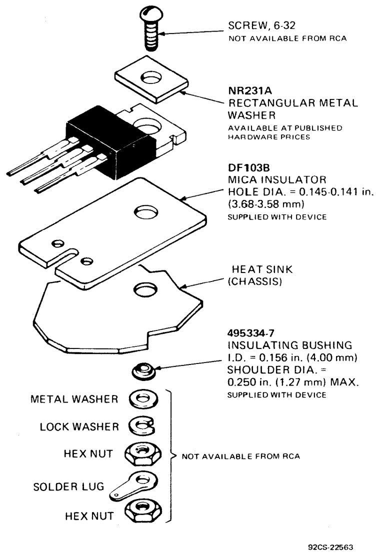
For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

Type RCA1A08
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter-resistance	I_{CER}	V_{CE} = −40 V, R_{BE} = 330Ω	–	−10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = −5 V	–	−0.1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = −100 mA, I_B = 0	−40	–	V
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = −100 mA, R_{BE} = 330Ω	−50	–	V
Gain Bandwidth Product	f_T	V_{CE} = −10 V, I_C = −50 mA	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = −50 mA, V_{CE} = −1.5 V	70	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = −100 mA, I_B = −5 mA	–	−1.4	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$	I_C = −100 mA, I_B = −5 mA	–	−1.4	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = −35 V, t = 0.05 s	−0.12	–	A

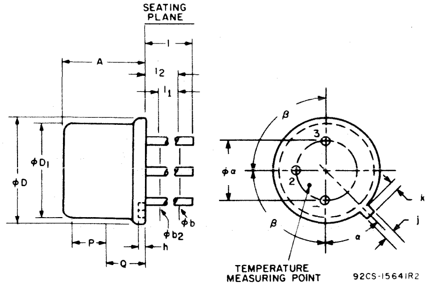
For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.13–Suggested mounting hardware for JEDEC TO-220AB

DIMENSIONAL OUTLINE FOR TYPES RCA1A07, RCA1A08 JEDEC TO-39



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
φa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
φb	0.016	0.021	0.406	0.533	2
φb2	0.016	0.019	0.406	0.483	2
φD	0.350	0.370	8.89	9.40	
φD1	0.315	0.335	8.00	8.51	
h	0.009	0.041	0.229	1.04	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
l	0.500		12.70		2
l1		0.050		1.27	2
l2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

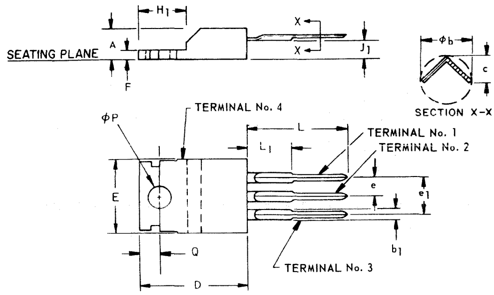
Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads) φb2 applies between l1 and l2. φb applies between l2 and 0.5 in. (12.70 mm) from seating plane. Diameter is uncontrolled in l1 and beyond 0.5 in. (12.70 mm) from seating plane.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

DIMENSIONAL OUTLINE FOR TYPES RCA1C10, RCA1C11 JEDEC TO-220AB



BOTTOM VIEW

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H1	0.230	0.270	5.85	6.85	1
J1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

1. Tab contour optional within H1 and E.
2. Position of lead to be measured 0.250 – 0.255 (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS FOR TYPES RCA1A07, RCA1A08

Lead 1 – Emitter
Lead 2 – Base
Case, Lead 3 – Collector

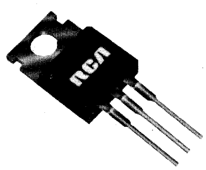
TERMINAL CONNECTIONS FOR TYPES RCA1C10, RCA 1C11

Lead 1 – Base
Lead 2 – Collector
Lead 3 – Emitter
Mounting Flange – Collector

RCA
Solid State
Division

Power Transistors

RCA1C14



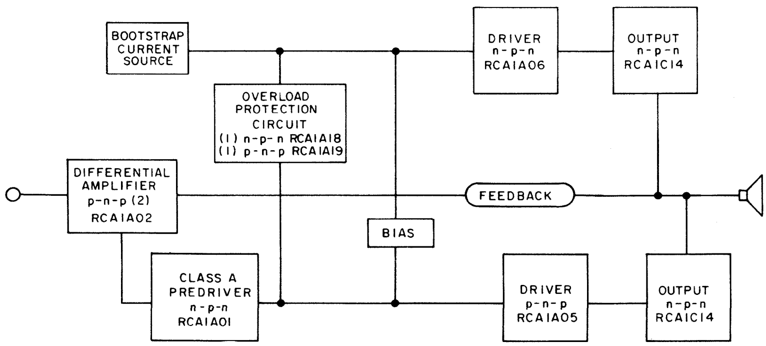
RCA1C14

JEDEC TO-220AB H-1535R1

Silicon Transistor for 25-Watt Quasi-Complementary-Symmetry Audio Amplifiers

RCA1C14 is an n-p-n hometaxial-base silicon power transistor provided in the JEDEC TO-220AB package. This device is ideally suited for use in the output stage of quasi-complementary-symmetry audio amplifiers

The 25-watt audio-amplifier circuit shown in Figs. 1 and 5 uses two RCA1C14 transistors in conjunction with seven TO-39 low-level audio transistors, 11 diodes, and a 52-volt split supply. The amplifier output is directly coupled to an 8-ohm speaker. Ruggedness and economy are features of this high fidelity amplifier.



92CS-21956

Fig.1— Block diagram and transistor complement for 25-watt quasi-complementary-symmetry audio amplifier.

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MAXIMUM RATINGS, *Absolute-Maximum Values:*

		RCA1C14	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	60	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With base open	V_{CEO}	40	V
With external base-to-emitter resistance (R_{BE}) = 100Ω	V_{CER}	60	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	V
COLLECTOR CURRENT	I_C	7	A
BASE CURRENT	I_B	3	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25°C		50	W
At case temperatures above 25°C		*See Fig. 2*	
TEMPERATURE RANGE:			
Storage & Operating (Junction)		−65 to 150	°C
PIN TEMPERATURE (During Soldering):			
At distances ≥1/32 in. (0.8 mm) from case for 10 s max.		230	°C

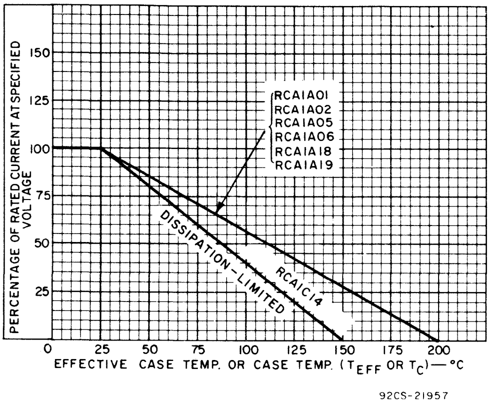


Fig.2— Derating curves for all types.

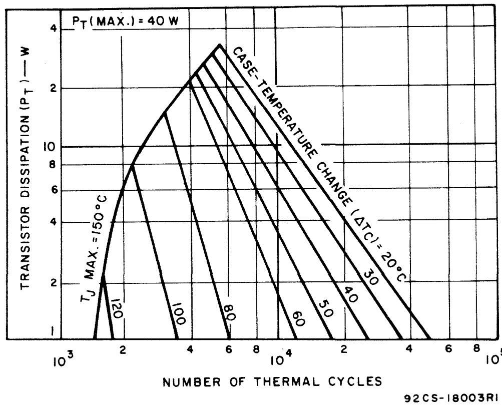


Fig.3— Thermal-cycling ratings for RCA1C14.

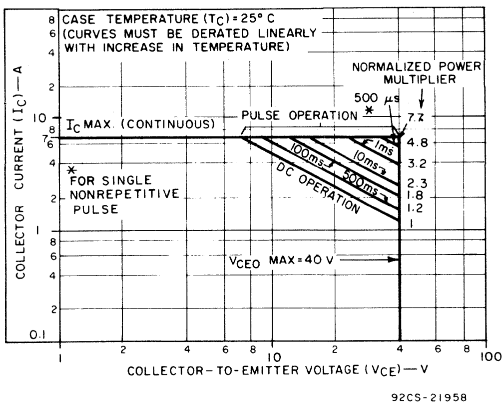
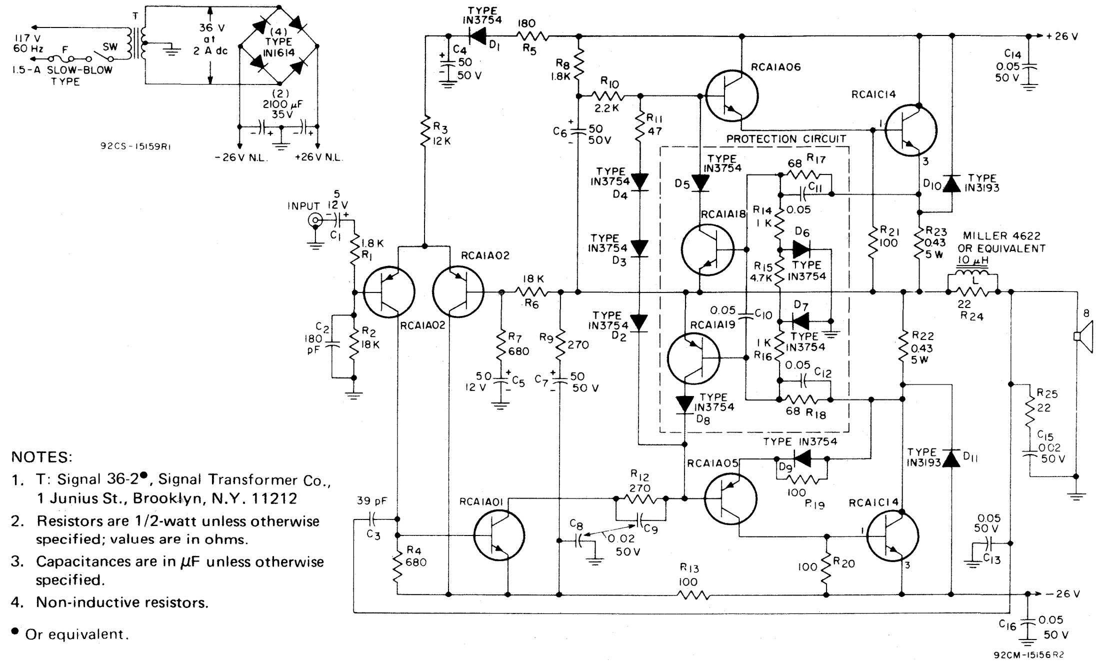


Fig.4— Maximum operating areas for RCA1C14.



NOTES:
1. T: Signal 36-2•, Signal Transformer Co., 1 Junius St., Brooklyn, N.Y. 11212
2. Resistors are 1/2-watt unless otherwise specified; values are in ohms.
3. Capacitances are in µF unless otherwise specified.
4. Non-inductive resistors.

• Or equivalent.

Fig.5— 25-watt amplifier circuit featuring quasi-complementary- symmetry output.

TYPICAL PERFORMANCE DATA
For 25-Watt Audio Amplifier

Measured at a line voltage of 120 V, T_A = 25°C, and a frequency of 1 kHz, unless otherwise specified

Power:
- Rated power (8-Ω load, at rated distortion) ..... 25 W
- Typical power (4-Ω load) ..... 45 W
- Typical power (16-Ω load) ..... 16 W
- Music power (8-Ω load, at 5% THD with regulated supply) ..... 38 W
- Dynamic power (8-Ω load, at 1% THD with regulated supply) ..... 33 W

Total Harmonic Distortion:
- Rated distortion 1.0%

IM Distortion:
- 10 dB below continuous power output at 60 Hz and 7 kHz (4:1) 0.1%

Sensitivity:
- At continuous power-output rating ..... 600 mV

Hum and Noise:
- Below continuous power output:
  - Input shorted ..... 80 dB
  - Input open ..... 75 dB

Input Resistance ..... 20 kΩ

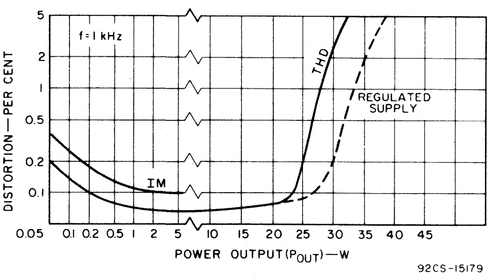


Fig.6— Distortion vs. power output.

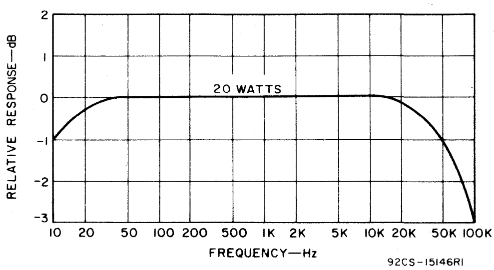


Fig.7— Response curve.

Type RCA1C14
Package: JEDEC TO-220AB
Construction: Silicon n-p-n, hometaxial base

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 50 V, R_{BE} = 100Ω	–	0.5	mA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 5 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 1 A, I_B = 0	40	–	V
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = 0.1 A, R_{BE} = 100Ω	60	–	V
Gain Bandwidth Product	f_T	I_C = 0.5 A, V_{CE} = 4 V	0.8	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 3 A, V_{CE} = 4 V	20	70	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 3 A, I_B = 0.3A	–	1	V
Base-to-Emitter Voltage	V_{BE}	I_C = 3 A, V_{CE} = 4 V	–	1.4	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 40 V, t=0.5 s	1.25	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N5495 (File 353).

MAXIMUM RATINGS, *Absolute Maximum Values:*

		RCA1A01	RCA1A02	RCA1A05	RCA1A06	RCA1A18	RCA1A19	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	–	–	–75	75	–	–	V
COLLECTOR-TO-EMITTER VOLTAGE: With base open	V_{CEO}	70	–50	–	–	10	–10	V
With external base-to-emitter resistance (R_{BE}) = 100Ω	V_{CER}	–	–	–75	75	–	–	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4	–4	–4	4	4	–4	V
COLLECTOR CURRENT	I_C	1	–1	–1	1	1	–1	A
BASE CURRENT	I_B	0.5	–0.5	–0.5	0.5	0.5	–0.5	A
TRANSISTOR DISSIPATION: At case temperatures up to 25°C	P_T	5	7	5	5	7	7	W
At case temperatures above 25°C		← See Fig. 2 →						
TEMPERATURE RANGE: Storage & Operating (Junction)		← –65 to 200 →						°C
PIN TEMPERATURE (During Soldering): At distance ≥1/32 in. (0.8 mm) from case for 10 s max.		← 230 →						°C

Type RCA1A01
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 60 V, I_B = 0	–	1	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 100 mA	70	–	V
Gain Bandwidth Product	f_T	V_{CE} = 4 V, I_C = 50 mA	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 mA, V_{CE} = 4 V	40	200	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 150 mA, I_B = 15 mA	–	1.4	V
Base-to-Emitter Voltage	V_{BE}	I_C = 10 mA, V_{CE} = 4 V	–	1	V

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

Type RCA1A02
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = –40 V, I_B = 0	–	–1	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –4 V, I_C = 0	–	–1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = –0.1 A	–50	–	V
Gain Bandwidth Product	f_T	V_{CE} = –4 V, I_C = –50 mA	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –0.1 mA, V_{CE} = –10 V	30	200	
Base-to-Emitter Voltage	V_{BE}	I_C = –0.1 mA, V_{CE} = –10 V	–	–0.8	V

For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).

Type RCA1A05
Package: JEDEC TO-39
Construction: Silicon p-n-p epitaxial planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = −65 V, R_{BE} = 100Ω	–	−10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = −4 V, I_C = 0	–	−0.1	mA
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = −0.1 A, R_{BE} = 100Ω	−75	–	V
Gain Bandwidth Product	f_T	I_C = −50 mA, V_{CE} = −4 V	60		MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = −150 mA, V_{CE} = −4 V	50	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = −150 mA, I_B = −15 mA	–	−0.8	V
Base-to-Emitter Voltage	V_{BE}	I_C = −150 mA, V_{CE} = −4 V	–	−1.4	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = −65 V, t = 0.4 s	−0.1	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).

Type RCA1A06
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 65 V, R_{BE} = 100Ω	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	0.1	mA
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = 100 mA, R_{BE} = 100Ω	75	–	V
Gain Bandwidth Product	f_T	I_C = 50 mA, V_{CE} = 4 V	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 150 mA, V_{CE} = 4 V	50	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 150 mA, I_B = 15 mA	–	0.8	V
Base-to-Emitter Voltage	V_{BE}	I_C = 150 mA, V_{CE} = 4 V	–	1.4	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 65 V, t = 0.4 s	0.077	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

Type RCA1A18
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With base open	I_{CEO}	$V_{CE} = 5$ V, $I_B = 0$	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	$V_{EB} = 4$ V, $I_C = 0$	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	$I_C = 10$ mA, $I_B = 0$	10	–	V
Gain Bandwidth Product	f_T	$I_C = 50$ mA, $V_{CE} = 4$ V	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	$I_C = 10$ mA, $V_{CE} = 4$V	40	250	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	$I_C = 10$ mA, $I_B = 0.5$ mA	–	1	V
Base-to-Emitter Voltage	V_{BE}	$I_C = 10$ mA, $V_{CE} = 4$ V	–	0.78	V

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

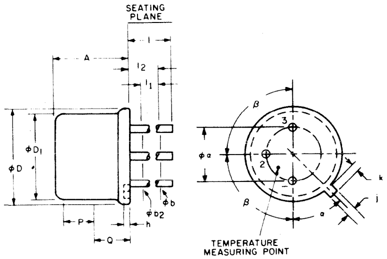
Type RCA1A19
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With base open	I_{CEO}	$V_{CE} = -5$ V, $I_B = 0$	–	−10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	$V_{EB} = -4$V, $I_C = 0$	–	−1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	$I_C = -10$ mA, $I_B = 0$	−10	–	V
Gain Bandwidth Product	f_T	$I_C = -50$ mA, $V_{CE} = -4$ V	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	$I_C = -10$mA, $V_{CE} = -4$V	40	250	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	$I_C = -10$mA, $I_B = -0.5$mA	–	−1	V
Base-to-Emitter Voltage	V_{BE}	$I_C = -10$ mA, $V_{CE} = -4$ V	–	−0.78	V

For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).

DIMENSIONAL OUTLINE FOR TYPES RCA1A01, RCA1A02, RCA1A05, RCA1A06, RCA1A18, RCA1A19 JEDEC TO-39



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
ϕa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
ϕb	0.016	0.021	0.406	0.533	2
ϕb2	0.016	0.019	0.406	0.483	2
ϕD	0.350	0.370	8.89	9.40	
ϕD1	0.315	0.335	8.00	8.51	
h	0.009	0.041	0.229	1.04	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
l	0.500		12.70		2
l1		0.050		1.27	2
l2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

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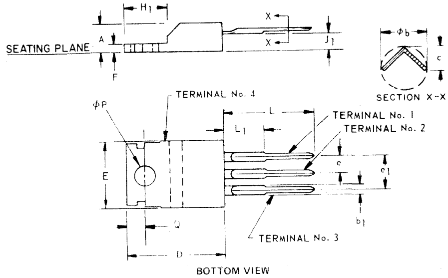
Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads) ϕb2 applies between l1 and l2. ϕb applies between l2 and 0.5 in. (12.70 mm) from seating plane. Diameter is uncontrolled in l1 and beyond 0.5 in. (12.70 mm) from seating plane.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

DIMENSIONAL OUTLINE FOR TYPE RCA1C14 JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
ϕb	0.020	0.045	0.51	1.14	–
b1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H1	0.230	0.270	5.85	6.85	1
J1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L1	–	0.250	–	6.35	–
ϕP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

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NOTES:

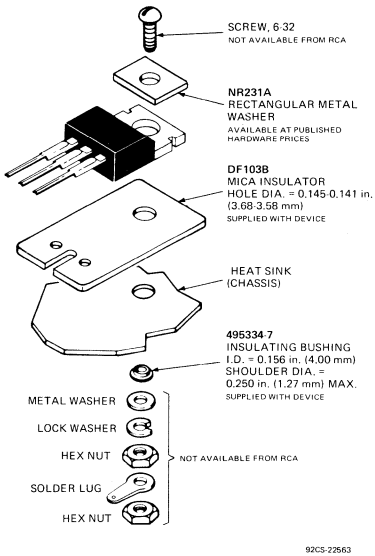
1. Tab contour optional within H1 and E.
2. Position of lead to be measured 0.250 – 0.255 (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS FOR TYPES RCA1A01, RCA1A02, RCA1A05, RCA1A06, RCA1A18, RCA1A19

Lead 1 – Emitter
Lead 2 – Base
Case, Lead 3 – Collector

TERMINAL CONNECTIONS FOR TYPE RCA1C14

Lead 1 – Base
Lead 2 – Collector
Lead 3 – Emitter
Lead 4 – Collector



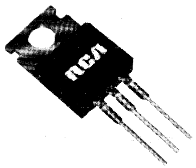
In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Suggested mounting hardware for JEDEC TO-220AB.

Solid State
Division

Power Transistors

RCA1C05
RCA1C06



RCA1C05
RCA1C06

JEDEC TO-220AB H-1535R1

Silicon Transistors for 25-Watt Full-Complementary-Symmetry Audio Amplifiers

RCA1C05 and RCA1C06 are n-p-n and p-n-p epitaxial-base silicon power transistors, respectively. These complementary output devices for audio applications are provided in the JEDEC TO-220AB plastic package.

The 25-watt audio-amplifier circuit shown in Figs. 1 and 2 uses RCA1C05 and RCA1C06 as output devices in conjunction with seven TO-39 discrete transistors, ten diodes, and a 52-volt split power supply. The amplifier output is directly coupled to an 8-ohm speaker. The full-complementary-symmetry output stage provides excellent high-frequency performance at moderate cost.

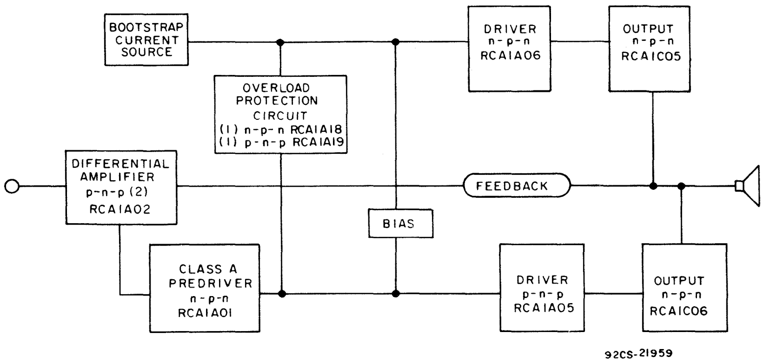


Fig.1— Block diagram and transistor complement for 25-watt full-complementary-symmetry audio amplifier.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		RCA1C05	RCA1C06	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	60	−60	V
COLLECTOR-TO- EMITTER VOLTAGE:				
With base open	V_{CEO}	50	−50	V
With external base-to-emitter resistance (R_{BE}) = 100Ω	V_{CER}	60	−60	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	−5	V
COLLECTOR CURRENT	I_C	7	−7	A
BASE CURRENT	I_B	3	−3	A
TRANSISTOR DISSIPATION:	P_T			
At case temperatures up to 25°C		40	40	W
At case temperatures above 25°C		← See Fig. 5 →		
TEMPERATURE RANGE:				
Storage & Operating (Junction)		← −65 to +150 →		°C
PIN TEMPERATURE (During Soldering):				
At distances ≥1/32 in. (0.8 mm) from case of 10 s max.		← 230 →		°C

Type RCA1C05
Package: JEDEC TO-220AB
Construction: Silicon n-p-n, epitaxial base

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 50 V, R_{BE} = 100Ω	–	1	mA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{BE} = 5 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = 0.1 A, R_{BE} = 100Ω	60	–	V
Gain Bandwidth Product	f_T	I_C = 0.1 A, V_{CE} = 4 V	4	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 3 A, V_{CE} = 4 V	20	120	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C = 3 A, I_B = 0.3 A	–	1	V
Base-to-Emitter Voltage	V_{BE}	I_C = 3 A, V_{CE} = 4 V	–	1.5	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 20 V, t = 0.5 s	2	–	A

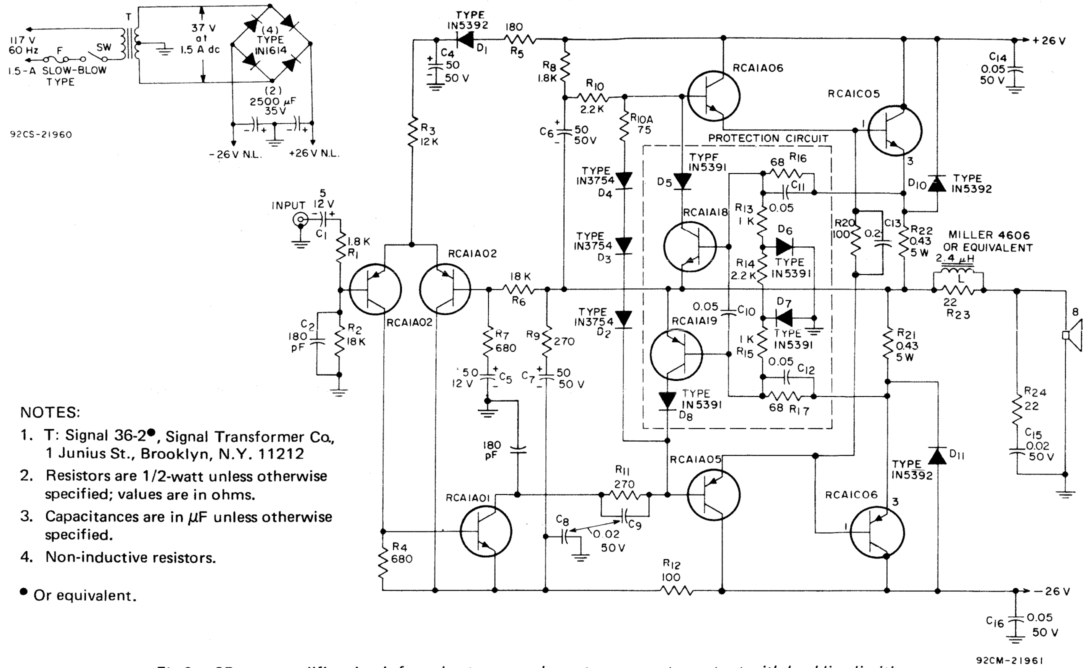
For characteristics curves and test conditions, refer to published data for prototype 2N6292 (File 542).

Type RCA1C06
Package: JEDEC TO-220AB
Construction: Silicon p-n-p, epitaxial base

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = −50 V, R_{BE} = 100Ω	–	−1	mA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = −5 V, I_C = 0	–	−1	mA
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = −0.1 A, R_{BE} = 100Ω	−60	–	V
Gain Bandwidth Product	f_T	I_C = −0.1 A, V_{CE} = −4 V	10	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = −3 A, V_{CE} = −4 V	20	120	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C = −3 A, I_B = −0.3 A	–	−1	V
Base-to-Emitter Voltage	V_{BE}	I_C = −3 A, V_{CE} = −4 V	–	−1.5	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = −20 V, t = 0.5 s	−2	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N6107 (File 488).



NOTES:

1. T: Signal 36-2•, Signal Transformer Co., 1 Junius St., Brooklyn, N.Y. 11212
2. Resistors are 1/2-watt unless otherwise specified; values are in ohms.
3. Capacitances are in µF unless otherwise specified.
4. Non-inductive resistors.

• Or equivalent.

Fig.2 — 25-watt amplifier circuit featuring true-complementary-symmetry output with load line limiting.

TYPICAL PERFORMANCE DATA
For 25-Watt Audio Amplifier

Measured at a line voltage of 120 V, T_A = 25°C, and a frequency of 1 kHz, unless otherwise specified.

Power:	
Rated power (8-Ω load, at rated distortion)	25 W
Typical power (4-Ω load)	45 W
Typical power (16-Ω load)	16 W
Total Harmonic Distortion:	
Rated distortion	1.0%
Typical at 20 W	0.05%
IM Distortion:	
10 dB below continuous power output at 60 Hz and 7 kHz (4:1)	0.1%
IHF Power Bandwidth:	
3 dB below rated continuous power at rated distortion	80 kHz
Sensitivity:	
At continuous power-output rating	600 mV
Hum and Noise:	
Below continuous power output:	
Input shorted	80 dB
Input open	75 dB
Input Resistance	20 kΩ

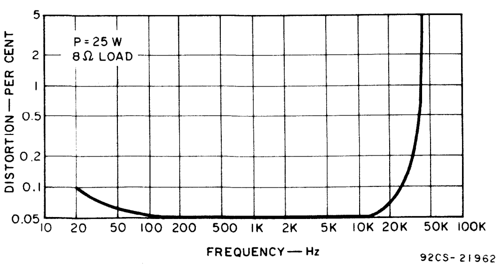


Fig.3— Typical distortion vs. frequency.

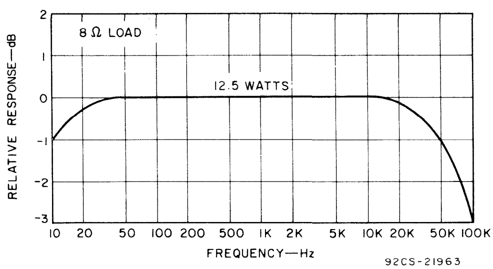


Fig.4— Response curve.

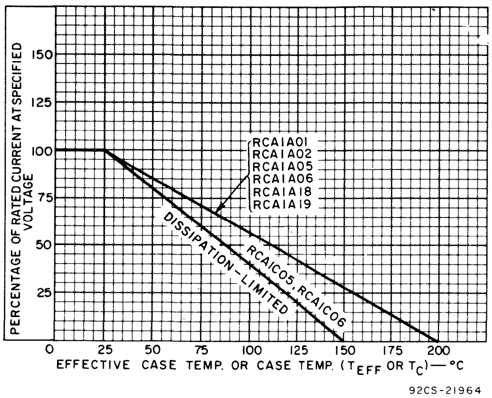


Fig.5 — Derating curve for all types.

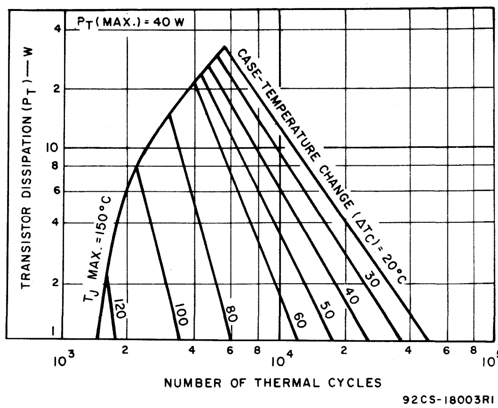


Fig.6 — Thermal-cycling ratings for RCA1C05 and RCA1C06.

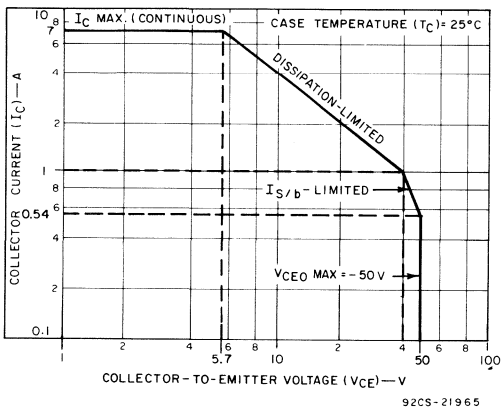


Fig.7 — Maximum operating areas for RCA1C05.

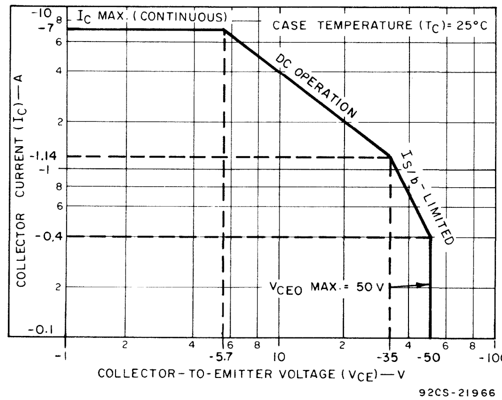


Fig.8 — Maximum operating areas for RCA1C06.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		RCA1A01	RCA1A02	RCA1A05	RCA1A06	RCA1A18	RCA1A19	
COLLECTOR-TO-BASE VOLTAGE ...	V_{CBO}	–	–	–75	75	–	–	V
COLLECTOR-TO-EMITTER VOLTAGE:								
With base open	V_{CEO}	70	–50	–	–	10	–10	V
With external base-to-emitter resistance (R_{BE}) = 100Ω	V_{CER}	–	–	–75	75	–	–	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4	–4	–4	4	4	–4	V
COLLECTOR CURRENT	I_C	1	–1	–1	1	1	–1	A
BASE CURRENT	I_B	0.5	–0.5	–0.5	0.5	0.5	–0.5	A
TRANSISTOR DISSIPATION:	P_T							
At case temperatures up to 25°C ...		5	7	5	5	7	7	W
At case temperatures above 25°C ...		← See Fig.5 →						
TEMPERATURE RANGE:								
Storage & Operating (Junction)		← –65 to 200 →						°C
PIN TEMPERATURE (During Soldering):								
At distances ≥1/32 in. (0.8 mm) from case for 10 s max.		← 230 →						°C

Type RCA1A01
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 60 V, I_B = 0	–	1	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 100 mA	70	–	V
Gain Bandwidth Product	f_T	V_{CE} = 4 V, I_C = 50 mA	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 mA, V_{CE} = 4 V	40	200	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 150 mA, I_B = 15 mA	–	1.4	V
Base-to-Emitter Voltage	V_{BE}	I_C = 10 mA, V_{CE} = 4 V	–	1	V

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

Type RCA1A02
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = –40 V, I_B = 0	–	–1	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –4 V, I_C = 0	–	–1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = –0.1 A	–50	–	V
Gain Bandwidth Product	f_T	V_{CE} = –4 V, I_C = – 50 mA	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –0.1 mA, V_{CE} = –10 V	30	200	
Base-to-Emitter Voltage	V_{BE}	I_C = –0.1 mA, V_{CE} = –10 V	–	–0.8	V

For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).

Type RCA1A05
Package: JEDEC TO-39
Construction: Silicon p-n-p, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = –65 V, R_{BE} = 100Ω	–	–10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –4 V, I_C = 0	–	–1.0	mA
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = –0.1 A, R_{BE} = 100Ω	–75	–	V
Gain Bandwidth Product	f_T	I_C = –50 mA, V_{CE} = –4 V	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –150 mA, V_{CE} = –4 V	50	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = –150 mA, I_B = –15 mA	–	–0.8	V
Base-to-Emitter Voltage	V_{BE}	I_C = –150 mA, V_{CE} = –4 V	–	–1.4	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = –65 V, t = 0.4 s	–0.1	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).

Type RCA1A06
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 65 V, R_{BE} = 100Ω	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	0.1	mA
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = 100 mA, R_{BE} = 100Ω	75	–	V
Gain Bandwidth Product	f_T	I_C = 50 mA, V_{CE} = 4 V	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 150 mA, V_{CE} = 4 V	50	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 150 mA, I_B = 15 mA	–	0.8	V
Base-to-Emitter Voltage	V_{BE}	I_C = 150 mA, V_{CE} = 4 V	–	1.4	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 65 V, t = 0.4 s	0.077	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

Type RCA1A18
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	$V_{CE} = 5$ V, $I_B = 0$	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	$V_{EB} = 4$ V, $I_C = 0$	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	$I_C = 10$ mA, $I_B = 0$	10	–	V
Gain Bandwidth Product	f_T	$I_C = 50$ mA, $V_{CE} = 4$ V	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	$I_C = 10$ mA, $V_{CE} = 4$ V	40	250	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	$I_C = 10$ mA, $I_B = 0.5$ mA	–	1	V
Base-to-Emitter Voltage	V_{BE}	$I_C = 10$ mA, $V_{CE} = 4$ V	–	0.78	V

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

Type RCA1A19
Package: JEDEC TO-39
Construction: Silicon p-n-p, planar

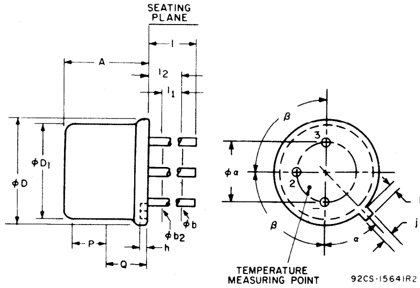
ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	$V_{CE} = -5$ V, $I_B = 0$	–	–10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	$V_{EB} = -4$ V, $I_C = 0$	–	–1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	$I_C = -10$ mA, $I_B = 0$	–10	–	V
Gain Bandwidth Product	f_T	$I_C = -50$ mA, $V_{CE} = -4$ V	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	$I_C = -10$ mA, $V_{CE} = -4$ V	40	250	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	$I_C = -10$ mA, $I_B = -0.5$ mA	–	–1	V
Base-to-Emitter Voltage	V_{BE}	$I_C = -10$ mA, $V_{CE} = -4$ V	–	–0.78	V

For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).

DIMENSIONAL OUTLINE FOR TYPES RCA1A01, RCA1A02, RCA1A05, RCA1A06, RCA1A18, RCA1A19

JEDEC TO-39



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
φa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
φb	0.016	0.021	0.406	0.533	2
φb2	0.016	0.019	0.406	0.483	2
φD	0.350	0.370	8.89	9.40	
φD1	0.315	0.335	8.00	8.51	
h	0.009	0.041	0.229	1.04	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
l	0.500		12.70		2
l1		0.050		1.27	2
l2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

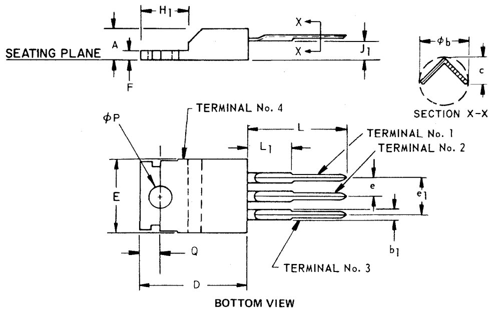
Note 2: (Three leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and 0.5 in. (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond 0.5 in. (12.70 mm) from seating plane.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

DIMENSIONAL OUTLINE FOR TYPES RCA1C05, RCA1C06

JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H1	0.230	0.270	5.85	6.85	1
J1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS FOR TYPES RCA1A01, RCA1A02, RCA1A05, RCA1A06, RCA1A18, RCA1A19

Lead 1 – Emitter
Lead 2 – Base
Case, Lead 3 – Collector

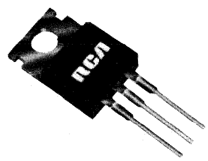
TERMINAL CONNECTIONS FOR TYPES RCA1C05, RCA1C06

Lead 1 – Base
Lead 2 – Collector
Lead 3 – Emitter
Lead 4 – Collector

Solid State Division

Power Transistors

RCA1C09


RCA1C09

JEDEC TO-220AB H-1535R1

Silicon Transistor for 40-Watt Quasi-Complementary-Symmetry Audio Amplifiers

RCA1C09 is an n-p-n hometaxial-base silicon power transistor packaged in the JEDEC TO-220AB (VERSAWATT) case. Two of these devices, driven in the class-B mode by the RCA1A06 and RCA1A05 silicon n-p-n and p-n-p transistors, can be used as output devices in audio-amplifier applications.

The 40-watt amplifier shown in Figs. 1 and 5 uses two RCA1C09 transistors as output units in conjunction with seven TO-39 transistors, 11 diodes, and a 64-volt split power supply. The amplifier output is directly coupled to an 8-ohm speaker. This 40-watt amplifier features ruggedness and economy in the mid-power range.

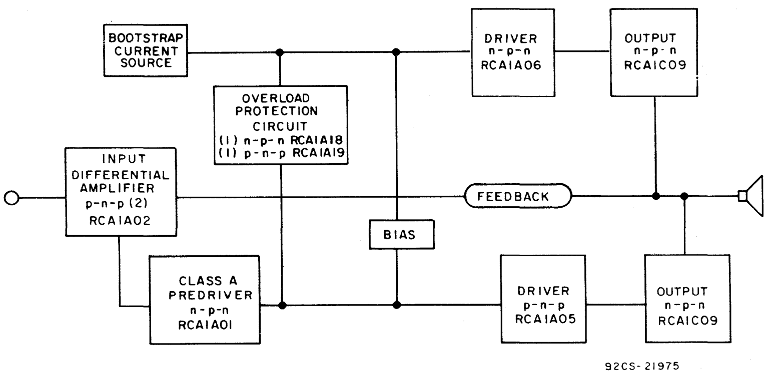


Fig.1— Block diagram and transistor complement for 40-watt quasi-complementary-symmetry audio amplifier.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		RCA1C09	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	75	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With base open	V_{CEO}	65	V
With external base-to-emitter resistance (R_{BE}) = 100Ω	V_{CER}	75	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	V
COLLECTOR CURRENT	I_C	10	A
BASE CURRENT	I_B	4	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25°C		75	W
At case temperatures above 25°C		*See Fig. 2*	
TEMPERATURE RANGE:			
Storage & Operating (Junction)		−65 to 150	°C
PIN TEMPERATURE (During Soldering):			
At distances ≥1/32 in. (0.8 mm) from case for 10 s max.		230	°C

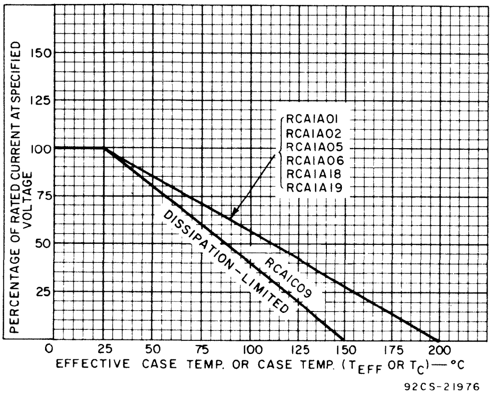


Fig.2— Derating curves for all types.

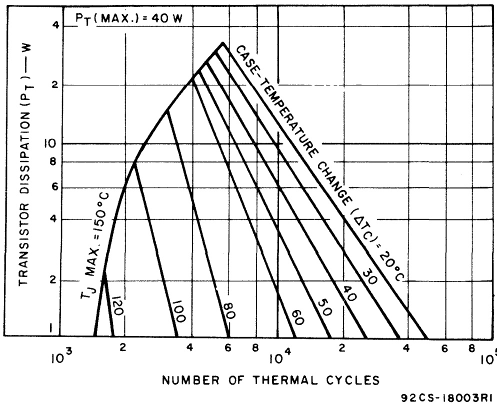


Fig.3— Thermal-cycling ratings for RCA1C09.

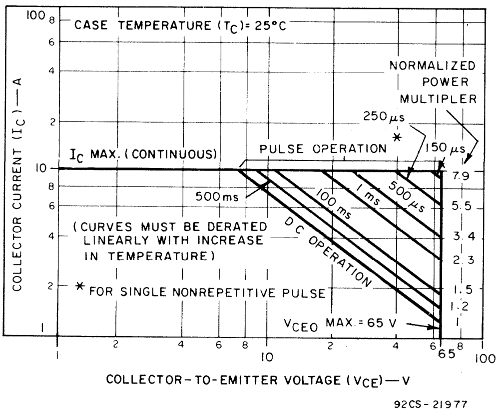
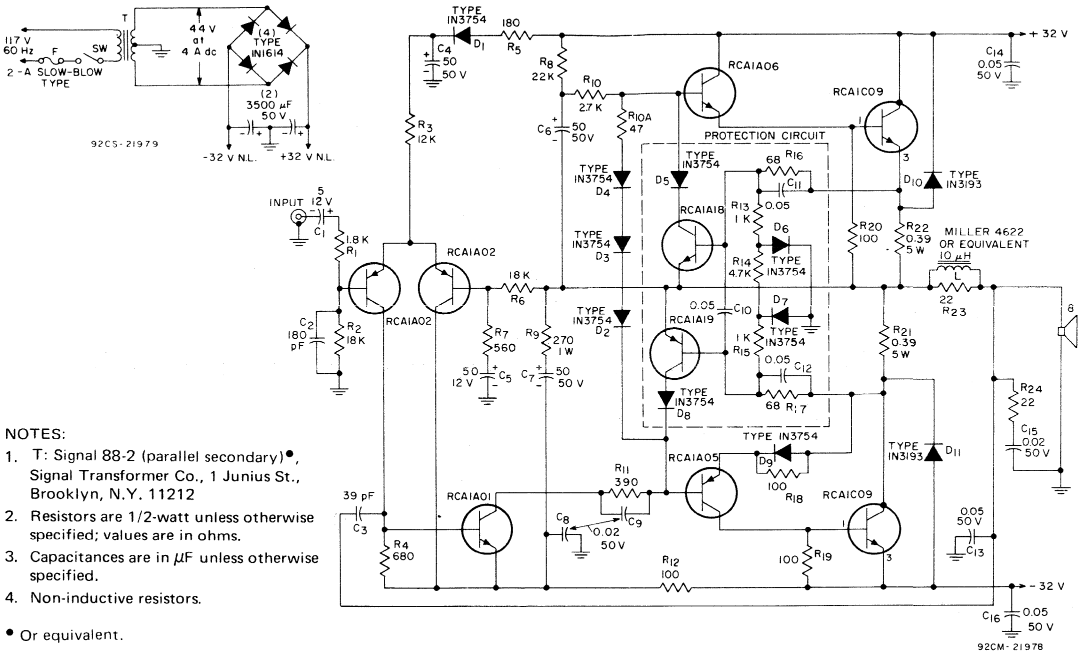


Fig.4— Maximum operating areas for RCA1C09.



NOTES:

1. T: Signal 88-2 (parallel secondary)•, Signal Transformer Co., 1 Junius St., Brooklyn, N.Y. 11212
2. Resistors are 1/2-watt unless otherwise specified; values are in ohms.
3. Capacitances are in µF unless otherwise specified.
4. Non-inductive resistors.

• Or equivalent.

Fig.5 — 40-Watt amplifier circuit featuring quasi-complementary-symmetry output.

TYPICAL PERFORMANCE DATA
For 40-Watt Audio Amplifier Circuit

Measured at a line voltage of 120 V, T_A = 25°C, and a frequency of 1 kHz, unless otherwise specified.

Power:
- Rated power (8-Ω load, at rated distortion) ..... 40 W
- Typical power (4-Ω load) .... 55 W
- Typical power (16-Ω load) .... 25 W
- Music power (8-Ω load, at 5% THD with regulated supply) .... 55 W
- Dynamic power (8-Ω load, at 1% THD with regulated supply) .... 50 W

Total Harmonic Distortion:
- Rated distortion 1.0%

IM Distortion:
- 10 dB below continuous power output at 60 Hz and 7 kHz (4:1) 0.1%

Sensitivity:
- At continuous power-output rating .... 600 mV

Hum and Noise:
- Below continuous power output:
  - Input shorted .... 80 dB
  - With 2 kΩ resistance on 20-ft. cable on input . 75 dB

Input Resistance .... 20 kΩ

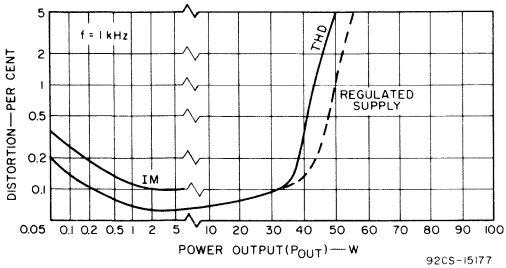


Fig.6— Distortion vs. power output.

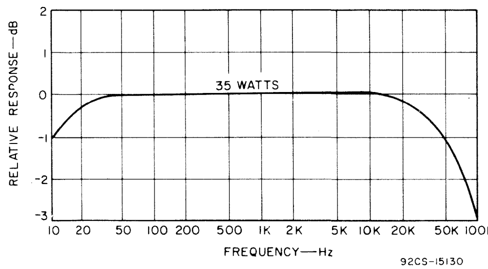


Fig.7— Response curve.

Type RCA1C09
Package: JEDEC TO-220AB
Construction: Silicon n-p-n, hometaxial base

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 65 V, R_{BE} = 100Ω	–	1	mA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 5 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = 0.2 A, R_{BE} = 100Ω	75	–	V
Gain Bandwidth Product	f_T	I_C = 0.5 A, V_{CE} = 4 V	0.8	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 4 A, V_{CE} = 4 V	20	120	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C = 4 A, I_B = 0.4 A	–	1	V
Base-to-Emitter Voltage	V_{BE}	I_C = 4 A, V_{CE} = 4 V	–	1.5	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 40 V, t = 0.5 s	1.87	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N6103 (File 485).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		RCA1A01	RCA1A02	RCA1A05	RCA1A06	RCA1A18	RCA1A19	
COLLECTOR-TO-BASE VOLTAGE . . .	V_{CBO}	–	–	–75	75	–	–	V
COLLECTOR-TO-EMITTER VOLTAGE:								
With base open	V_{CEO}	70	–50	–	–	10	–10	V
With external base-to-emitter resistance (R_{BE}) = 100Ω	V_{CER}	–	–	–75	75	–	–	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4	–4	–4	4	4	–4	V
COLLECTOR CURRENT	I_C	1	–1	–1	1	1	–1	A
BASE CURRENT	I_B	0.5	–0.5	–0.5	0.5	0.5	–0.5	A
TRANSISTOR DISSIPATION:	P_T							
At case temperatures up to 25°C . . .		5	7	5	5	7	7	W
At case temperatures above 25°C . . .		← See Fig. 2 →						
TEMPERATURE RANGE:								
Storage & Operating (Junction)		← –65 to 200 →						°C
PIN TEMPERATURE (During Soldering):								
At distances ≥1/32 in. (0.8 mm) from case for 10 s max.		← 230 →						°C

Type RCA1A01
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 60 V, I_B = 0	–	1	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 100 mA	70	–	V
Gain Bandwidth Product	f_T	V_{CE} = 4 V, I_C = 50 mA	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 mA, V_{CE} = 4 V	40	200	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C = 150 mA, I_B = 15 mA	–	1.4	V
Base-to-Emitter Voltage	V_{BE}	I_C = 10 mA, V_{CE} = 4 V	–	1	V

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

Type RCA1A02
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = –40 V, I_B = 0	–	–1	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –4 V, I_C = 0	–	–1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = –0.1 A	–50	–	V
Gain Bandwidth Product	f_T	V_{CE} = –4 V, I_C = –50 mA	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –0.1 mA, V_{CE} = –10 V	30	200	
Base-to-Emitter Voltage	V_{BE}	I_C = –0.1 mA, V_{CE} = –10 V	–	–0.8	V

For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).

Type RCA1A05
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = −66 V, R_{BE} = 100Ω	–	−10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = −4 V, I_C = 0	–	−0.1	mA
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = −0.1 A, R_{BE} = 100Ω	−75	–	V
Gain Bandwidth Product	f_T	I_C = −50 mA, V_{CE} = −4 V	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = −150 mA, V_{CE} = −4 V	50	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = −150 mA, I_B = −15 mA	–	−0.8	V
Base-to-Emitter Voltage	V_{BE}	I_C = −150 mA, V_{CE} = −4 V	–	−1.4	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = −65 V, t = 0.4 s	−0.1	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).

Type RCA1A06
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 65 V, R_{BE} = 100Ω	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	0.1	mA
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = 100 mA, R_{BE} = 100Ω	75	–	V
Gain Bandwidth Product	f_T	I_C = 50 mA, V_{CE} = 4 V	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 150 mA, V_{CE} = 4 V	50	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 150 mA, I_B = 15 mA	–	0.8	V
Base-to-Emitter Voltage	V_{BE}	I_C = 150 mA, V_{CE} = 4 V	–	1.4	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 65 V, t = 0.4 s	0.077	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

Type RCA1A18
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 5 V, I_B = 0	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 10 mA, I_B = 0	10	–	V
Gain Bandwidth Product	f_T	I_C = 50 mA, V_{CE} = 4 V	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 mA, V_{CE} = 4 V	40	250	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C = 10 mA, I_B = 0.5 mA	–	1	V
Base-to-Emitter Voltage	V_{BE}	I_C = 10 mA, V_{CE} = 4 V	–	0.78	V

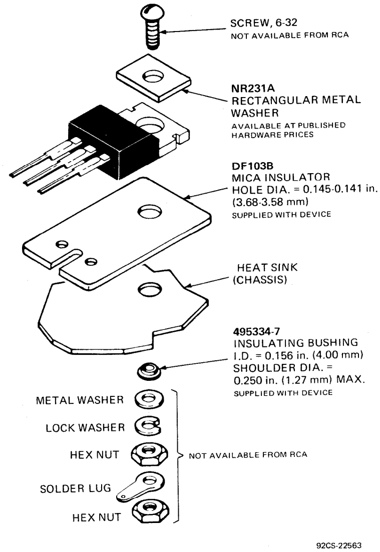
For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

Type RCA1A19
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = –5 V, I_B = 0	–	–10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –4 V, I_C = 0	–	–1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = –10 mA, I_B = 0	–10	–	V
Gain Bandwidth Product	f_T	I_C = –50 mA, V_{CE} = –4 V	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –10 mA, V_{CE} = –4 V	40	250	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C = –10 mA, I_B = –0.5 mA	–	–1	V
Base-to-Emitter Voltage	V_{BE}	I_C = –10 mA, V_{CE} = –4 V	–	–0.78	V

For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).

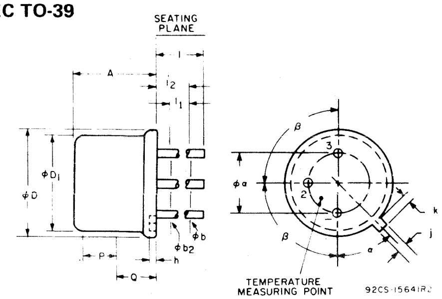


In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Suggested mounting hardware for JEDEC TO-220AB.

DIMENSIONAL OUTLINE FOR TYPES RCA1A01, RCA1A02, RCA1A05, RCA1A06, RCA1A18, RCA1A19

JEDEC TO-39



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
φa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
φb	0.016	0.021	0.406	0.533	2
φb2	0.016	0.019	0.406	0.483	2
φD	0.350	0.370	8.89	9.40	
φD1	0.315	0.335	8.00	8.51	
h	0.009	0.041	0.229	1.04	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
l	0.500		12.70		2
l1		0.050		1.27	2
l2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

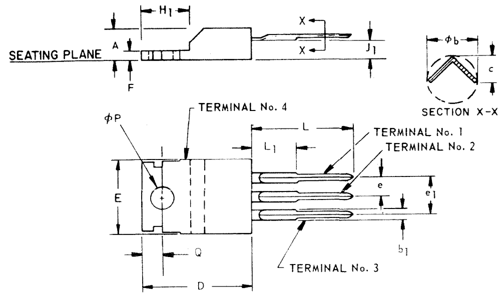
Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads) φb_2 applies between l_1 and l_2. φb applies between l_2 and 0.5 in. (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond 0.5 in. (12.70 mm) from seating plane.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

DIMENSIONAL OUTLINE FOR TYPE RCA1C09 JEDEC TO-220AB



BOTTOM VIEW

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H1	0.230	0.270	5.85	6.85	1
J1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS FOR TYPES RCA1A01, RCA1A02, RCA1A05, RCA1A06, RCA1A18, RCA1A19

Lead 1 – Emitter
Lead 2 – Base
Case, Lead 3 – Collector

TERMINAL CONNECTIONS FOR TYPE RCA1C09

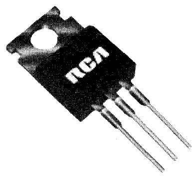
Lead 1 – Base
Lead 2 – Collector
Lead 3 – Emitter
Lead 4 – Collector

Solid State Division

Power Transistors

RCA1C07
RCA1C08

Silicon Transistors for 40-Watt Full-Complementary-Symmetry Audio Amplifiers



RCA1C07
RCA1C08

JEDEC TO-220AB H-1535R1

RCA1C07 and RCA1C08 are n-p-n and p-n-p epitaxial-base silicon power transistors, respectively, especially suitable for audio-output applications. These devices are provided in the economical JEDEC TO-220AB version of the VERSAWATT package.

The 40-watt amplifier shown in Figs. 1 and 2 uses the RCA1C07 and RCA1C08 in conjunction with seven TO-39 transistors, ten diodes, and a 64-volt split power supply. The amplifier output is directly coupled to an 8-ohm speaker. The high-frequency performance of this 40-watt amplifier will provide excellent reproduction for the most critical listener.

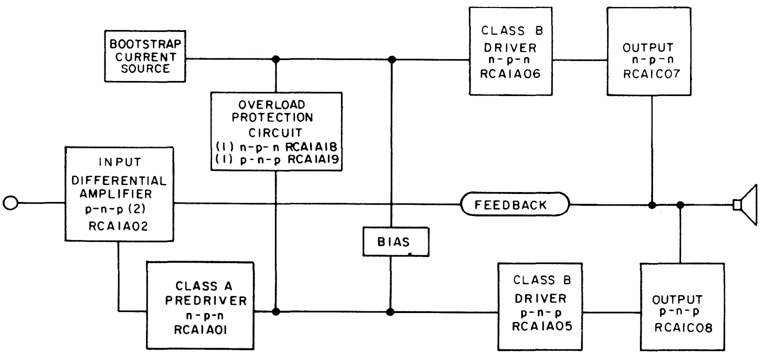


Fig.1— Block diagram and transistor complement for 40-watt full-complementary-symmetry audio amplifier.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		RCA1C07	RCA1C08	
COLLECTOR-TO-BASE-VOLTAGE	V_{CBO}	75	−75	V
COLLECTOR-TO-EMITTER VOLTAGE:				
With base open	V_{CEO}	65	−65	V
With external base-to-emitter resistance (R_{BE}) = 100Ω	V_{CER}	75	−75	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	−5	V
COLLECTOR CURRENT	I_C	10	−10	A
BASE CURRENT	I_B	4	−4	A
TRANSISTOR DISSIPATION:	P_T			
At case temperatures up to 25°C		75	75	W
At case temperatures above 25°C		← *See Fig. 5* →		
TEMPERATURE RANGE:				
Storage & Operating (Junction)		← −65 to 150 →		°C
PIN TEMPERATURE (During Soldering):				
At distances ≥1/32 in. (0.8 mm) from case for 10 s max.		← 230 →		°C

Type RCA1C07
Package: JEDEC TO-220AB
Construction: Silicon n-p-n, epitaxial base

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 65V, R_{BE} = 100Ω	–	1	mA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{BE} = 5V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = 0.1A, R_{BE} = 100Ω	75	–	V
Gain Bandwidth Product	f_T	I_C = 1 A, V_{CE} = 4V	5	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 4A, V_{CE} = 4V	20	120	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 4A, I_B = 0.4 A	–	1	V
Base-to-Emitter Voltage	V_{BE}	I_C = 4A, V_{CE} = 4V	–	1.5	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 30V, t = 0.5 s	2.5	–	A

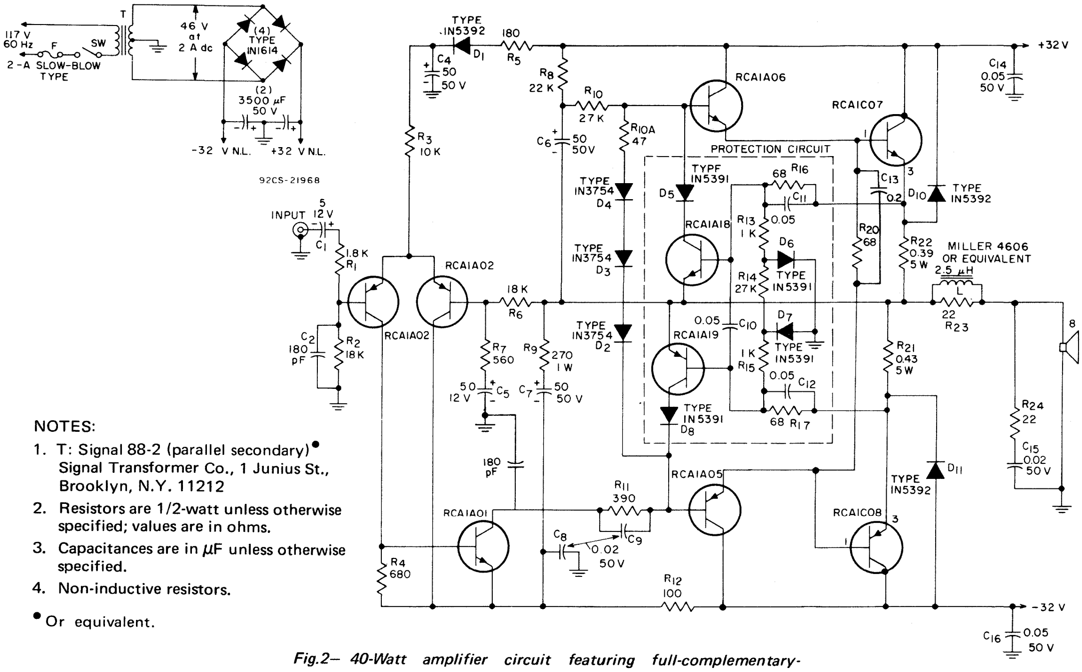
For characteristics curves and test conditions, refer to published data for prototype 2N6292 (File 542).

Type RCA1C08
Package: JEDEC TO-220AB
Construction: Silicon p-n-p, epitaxial base

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = −65V, R_{BE} = 100Ω	–	−1	mA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = −5V, I_C = 0	–	−1	mA
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = −0.1A, R_{BE} = 100Ω	−75	–	V
Gain Bandwidth Product	f_T	I_C = −1 A, V_{CE} = −4V	5	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = −4A, V_{CE} = −4V	20	120	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = −4A, I_B = −0.4A	–	−1	V
Base-to-Emitter Voltage	V_{BE}	I_C = −4A, V_{CE} = −4V	–	−1.5	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = −30V, t = 0.5 s	−2.5	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N6107 (File 488).



NOTES:

1. T: Signal 88-2 (parallel secondary)•
   Signal Transformer Co., 1 Junius St.,
   Brooklyn, N.Y. 11212
2. Resistors are 1/2-watt unless otherwise specified; values are in ohms.
3. Capacitances are in µF unless otherwise specified.
4. Non-inductive resistors.

• Or equivalent.

Fig.2— 40-Watt amplifier circuit featuring full-complementary-symmetry output using load line limiting.

TYPICAL PERFORMANCE DATA
For 40-Watt Audio Amplifier Circuit

Measured at a line voltage of 120 V, T_A = 25°C, and a frequency of 1 kHz, unless otherwise specified.

Power:	
Rated power (8-Ω load, at rated distortion)	40 W
Typical power (4-Ω load)	75 W
Typical power (16-Ω load)	25 W
Total Harmonic Distortion:	
Rated distortion	1.0%
Typical at 20 W	0.05%
IM Distortion:	
10 dB below continuous power output at 60 Hz and 7 kHz (4:1)	0.1%
IHF Power Bandwidth:	
3 dB below rated continuous power at rated distortion	80 kHz
Sensitivity:	
At continuous power-output rating	600 mV
Hum and Noise:	
Below continuous power output:	
Input shorted	80 dB
Input open	75 dB
Input Resistance	20 kΩ

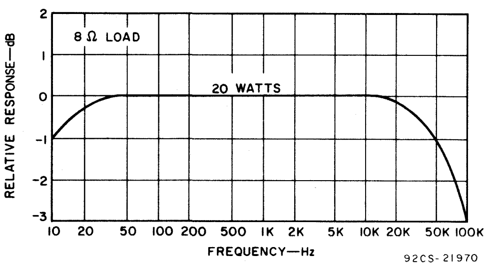


Fig.3— Response curve.

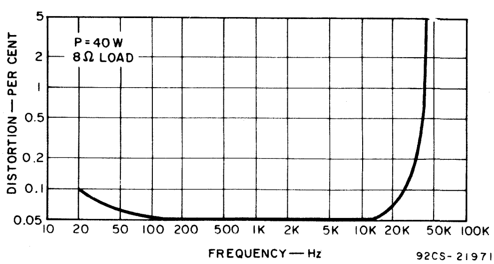


Fig.4—Typical distortion vs. frequency.

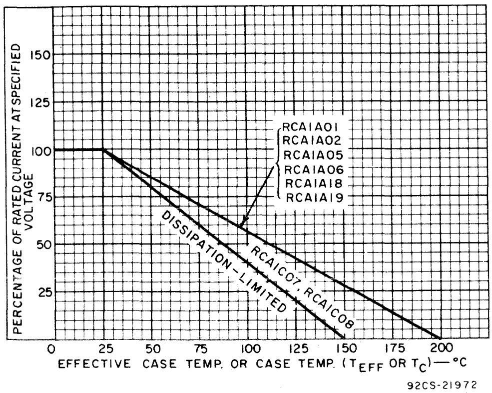


Fig.5– Derating curve for all types.

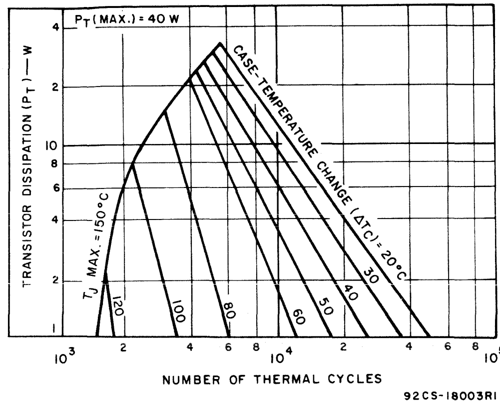


Fig.6– Thermal-cycling ratings for RCA1C07 and RCA1C08.

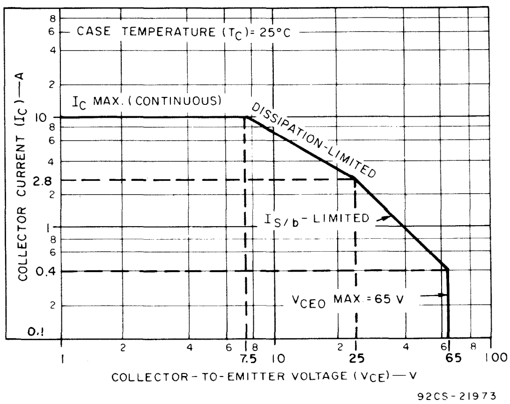


Fig.7– Maximum operating areas for RCA1C07.

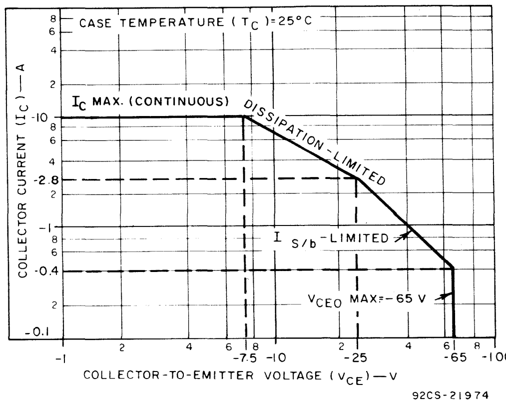


Fig.8– Maximum operating areas for RCA1C08.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		RCA1A01	RCA1A02	RCA1A05	RCA1A06	RCA1A18	RCA1A19	
COLLECTOR-TO-BASE VOLTAGE . . .	V_{CBO}	–	–	–75	75	–	–	V
COLLECTOR-TO-EMITTER VOLTAGE:								
With base open	V_{CEO}	70	–50	–	–	10	–10	V
With external base-to-emitter resistance (R_{BE}) = 100Ω	V_{CER}	–	–	–75	75	–	–	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4	–4	–4	4	4	–4	V
COLLECTOR CURRENT	I_C	1	–1	–1	1	1	–1	A
BASE CURRENT	I_B	0.5	–0.5	–0.5	0.5	0.5	–0.5	A
TRANSISTOR DISSIPATION:	P_T							
At case temperatures up to 25°C. . . .		5	7	5	5	7	7	W
At case temperatures above 25°C. . . .		← *See Fig. 2* →						°C
TEMPERATURE RANGE:								
Storage & Operating (Junction)		← –65 to 200 →						°C
PIN TEMPERATURE (During Soldering):								
At distances ≥1/32 in. (0.8 mm) from case for 10 s max.		← 230 →						°C

Type RCA1A01
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 60 V, I_B = 0	–	1	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 100 mA	70	–	V
Gain Bandwidth Product	f_T	V_{CE} = 4 V, I_C = 50 mA	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 mA, V_{CE} = 4 V	40	200	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 150 mA, I_B = 15 mA	–	1.4	V
Base-to-Emitter Voltage	V_{BE}	I_C = 10 mA, V_{CE} = 4 V	–	1	V

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

Type RCA1A02
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = –40 V, I_B = 0	–	–1	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –4 V, I_C = 0	–	–1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = –0.1 A	–50	–	V
Gain Bandwidth Product	f_T	V_{CE} = –4 V, I_C = –50 mA	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –0.1 mA, V_{CE} = –10 V	30	200	
Base-to-Emitter Voltage	V_{BE}	I_C = –0.1 mA, V_{CE} = –10 V	–	–0.8	V

For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).

Type RCA1A05
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = −65V, R_{BE} = 100Ω	–	−10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = −4V, I_C = 0	–	−0.1	mA
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = −0.1A, R_{BE} = 100Ω	−75	–	V
Gain Bandwidth Product	f_T	I_C = −50mA, V_{CE} = −4V	60		MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = −150mA, V_{CE} = −4V	50	250	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C = −150mA, I_B = −15 mA	–	−0.8	V
Base-to-Emitter Voltage	V_{BE}	I_C = −150mA, V_{CE} = −4V	–	−1.4	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = −65V, t = 0.4 s	−0.1	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).

Type RCA1A06
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 65V, R_{BE} = 100Ω	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4V, I_C = 0	–	0.1	mA
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = 100 mA, R_{BE} = 100Ω	75	–	V
Gain Bandwidth Product	f_T	I_C = 50 mA, V_{CE} = 4 V	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 150 mA, V_{CE} = 4V	50	250	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C = 150 mA, I_B = 15 mA	–	0.8	V
Base-to-Emitter Voltage	V_{BE}	I_C = 150 mA, V_{CE} = 4V	–	1.4	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 65V, t = 0.4 s	0.077	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

Type RCA1A18
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 5 V, I_B = 0	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 10 mA, I_B = 0	10	–	V
Gain Bandwidth Product	f_T	I_C = 50 mA, V_{CE} = 4V	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 mA, V_{CE} = 4 V	40	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 10 mA, I_B = 0.5 mA	–	1	V
Base-to-Emitter Voltage	V_{BE}	I_C = 10 mA, V_{CE} = 4 V	–	0.78	V

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

Type RCA1A19
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial planar

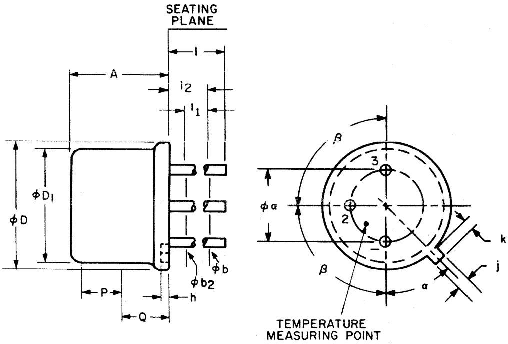
ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = –5 V, I_B = 0	–	–10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –4 V, I_C = 0	–	–1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = –10 mA, I_B = 0	–10	–	V
Gain Bandwidth Product	f_T	I_C = –50 mA, V_{CE} = –4 V	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –10 mA, V_{CE} = –4 V	40	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = –10 mA, I_B = –0.5 mA	–	–1	V
Base-to-Emitter Voltage	V_{BE}	I_C = –10 mA, V_{CE} = –4 V	–	–0.78	V

For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).

DIMENSIONAL OUTLINE FOR TYPES RCA1A01, RCA1A02, RCA1A05, RCA1A06, RCA1A18, RCA1A19

JEDEC TO-39



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
φa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
φb	0.016	0.021	0.406	0.533	2
φb2	0.016	0.019	0.406	0.483	2
φD	0.350	0.370	8.89	9.40	
φD1	0.315	0.335	8.00	8.51	
h	0.009	0.125	0.229	3.18	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
l	0.500		12.70		2
l1		0.050		1.27	2
l2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

92CS-15641R2

Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads) φb2 applies between l1 and l2. φb applies between l2 and 0.5 in. (12.70 mm) from seating plane. Diameter is uncontrolled in l1 and beyond 0.5 in. (12.70 mm) from seating plane.

Note 3: Measured from maximum diameter of the actual device.

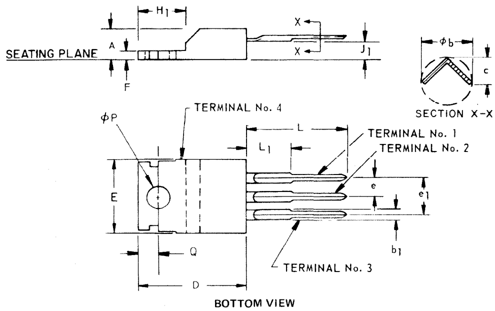
Note 4: Details of outline in this zone optional.

TERMINAL CONNECTIONS FOR TYPES RCA1A01, RCA1A02, RCA1A05, RCA1A06, RCA1A18, RCA1A19

Lead 1 – Emitter
Lead 2 – Base
Case, Lead 3 – Collector

DIMENSIONAL OUTLINE FOR TYPES RCA1C07, RCA1C08

JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H1	0.230	0.270	5.85	6.85	1
J1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

1. Tab contour optional within H1 and E.
2. Position of lead to be measured 0.250 – 0.255 (6.35 – 6.48 mm) from case.

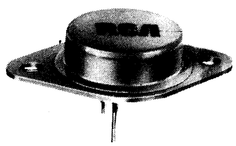
TERMINAL CONNECTIONS FOR TYPES RCA1C07, RCA1C08

Lead 1 – Base
Lead 2 – Collector
Lead 3 – Emitter
Lead 4 – Collector

Solid State
Division

Power Transistors

RCA1B01



RCA1B01

JEDEC TO-3 H-1570

Silicon Transistor for 70-Watt Quasi-Complementary-Symmetry Audio Amplifiers with Hometaxial-Base Output Transistors

RCA1B01 is an n-p-n hometaxial-base silicon transistor in a JEDEC TO-3 package. This device is particularly suitable for audio-output use, and can be driven by either the RCA1A03 n-p-n or RCA1A04 p-n-p transistor.

The 70-watt amplifier shown in Figs. 1 and 5 uses the RCA1B01 in conjunction with seven TO-39 transistors, eleven diodes, and an 84-volt split power supply. The amplifier output is directly coupled to an 8-ohm speaker. This amplifier is most useful for instrumentation applications where ruggedness and raw power are essential.

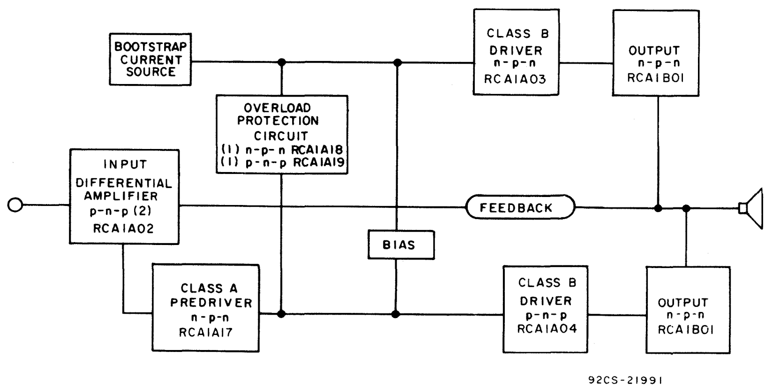


Fig. 1—Block diagram and transistor complement for 70-watt quasi-complementary-symmetry audio amplifier with hometaxial-base output transistors.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		RCA1B01	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	95	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With external base-to-emitter resistance (R_{BE}) = 100Ω	V_{CER}	95	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	7	V
COLLECTOR CURRENT	I_C	15	A
BASE CURRENT	I_B	7	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25°C		115	W
At case temperatures above 25°C		*See Fig. 2*	
TEMPERATURE RANGE:			
Storage & Operating (Junction)		–65 to 200	°C
PIN TEMPERATURE (During Soldering):			
At distances ≥ 1/32 in. (0.8 mm) from case for 10 s max		230	°C

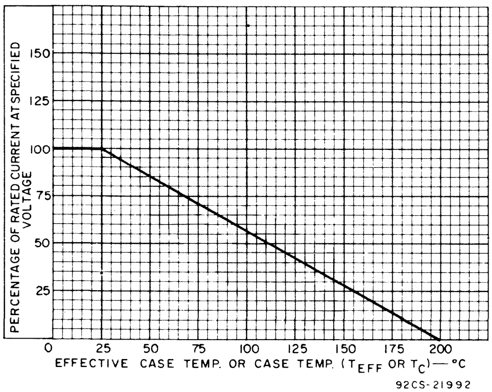


Fig.2—Derating curves for all types.

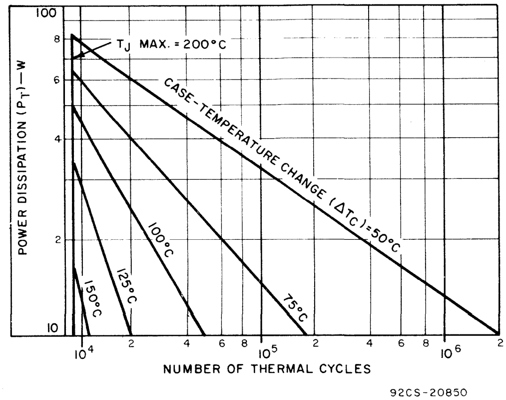


Fig.3—Thermal-cycling ratings for RCA1B01.

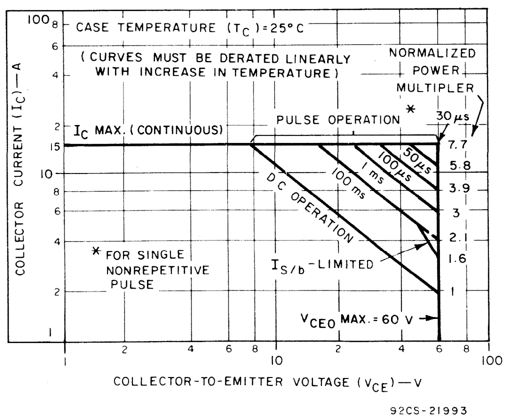
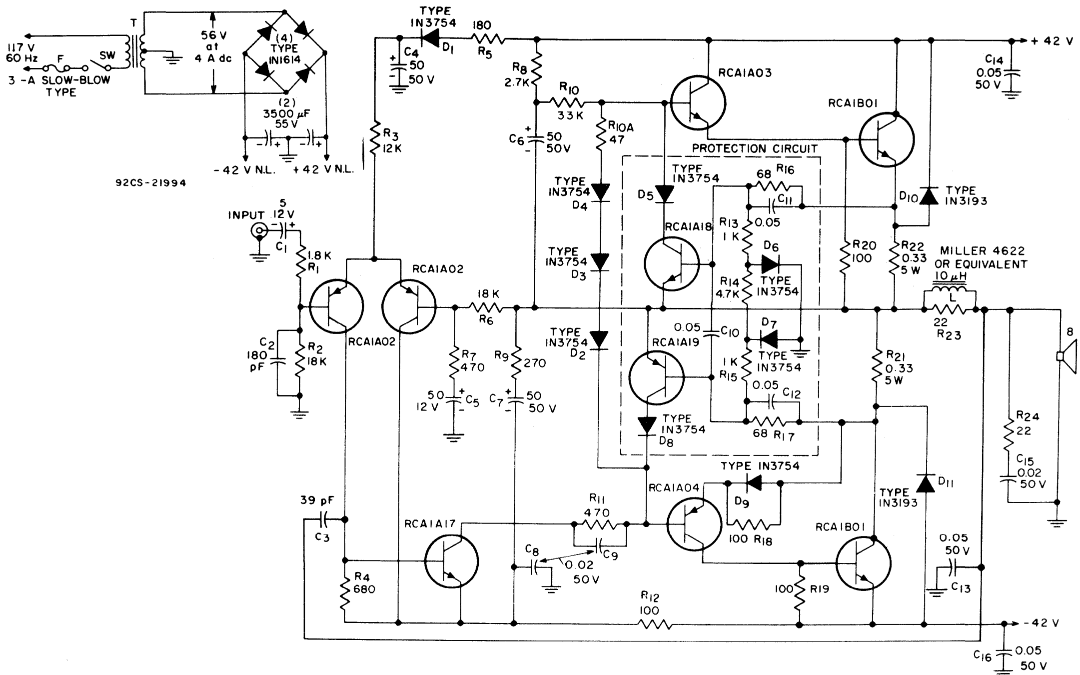


Fig.4—Maximum operating areas for RCA1B01.



NOTES:

1. T: Signal 56-4•, Signal Transformer Co., 1 Junius St., Brooklyn, N.Y. 11212
2. Resistors are 1/2-watt unless otherwise specified; values are in ohms.
3. Capacitances are in µF unless otherwise specified.
4. Non-inductive resistors.

• Or equivalent.

Fig.5—70-Watt amplifier circuit featuring quasi-complementary-symmetry output employing hometaxial-base output transistors.

TYPICAL PERFORMANCE DATA
For 70-Watt Audio Amplifier

Measured at a line voltage of 120 V, T_A = 25°C, and a frequency of 1 kHz, unless otherwise specified.

Power:
- Rated power (8-Ω load, at rated distortion) ...... 70 W
- Typical power (4-Ω load) .... 100 W
- Typical power (16-Ω load) .... 40 W
- Music power (8-Ω load, at 5% THD with regulated supply) .... 100 W
- Dynamic power (8-Ω load, at 1% THD with regulated supply) .... 88 W

Total Harmonic Distortion:
- Rated distortion 1.0%

IM Distortion:
- 10 dB below continuous power output at 60 Hz and 7 kHz (4:1) 0.1%

Sensitivity:
- At continuous power-output rating .... 700 mV

Hum and Noise:
- Below continuous power output:
  - Input shorted .... 85 dB
  - Input open .... 80 dB

Input Resistance .... 20 kΩ

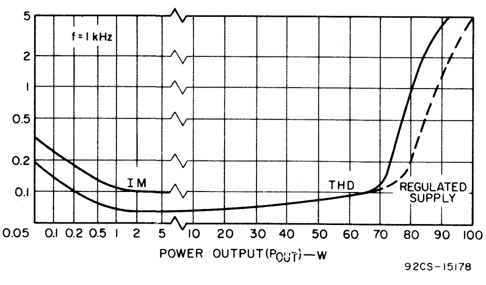


Fig.6—Distortion vs. power output.

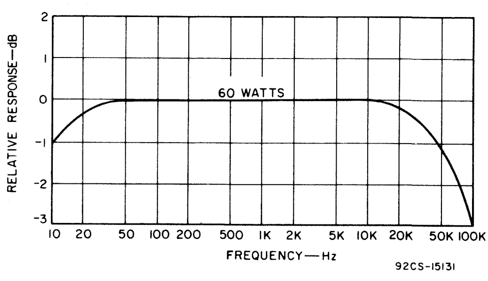


Fig.7—Response curve.

Type RCA1B01
Package: JEDEC TO-3
Construction: Silicon n-p-n, hometaxial base

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 85 V, R_{BE} = 100Ω	–	0.5	mA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = 0.2A, R_{BE} = 100Ω	95	–	V
Gain Bandwidth Product	f_T	V_{CE} = 4 V, I_C = 1 A	0.8	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 4 A, V_{CE} = 4 V	20	70	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 4 A, I_B = 0.4 A	–	1	V
Base-to-Emitter Voltage	V_{BE}	I_C = 4 A, V_{CE} = 4 V	–	1.4	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 60 V, t = l s	1.95	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N3055 (File 524).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	Symbol	RCA1A02	RCA1A03	RCA1A04	RCA1A17	RCA1A18	RCA1A19	
COLLECTOR-TO-BASE VOLTAGE ..	V_{CBO}	–	95	–95	–	–	–	V
COLLECTOR-TO-EMITTER VOLTAGE:								
With base open	V_{CEO}	–50	–	–	90	10	–10	V
With external base-to-emitter resistance (R_{BE}) = 100Ω	V_{CER}	–	95	–95	–	–	–	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	–4	4	–4	4	4	–4	V
COLLECTOR CURRENT	I_C	–1	2	–2	1	1	–1	A
BASE CURRENT	I_B	–0.5	1	–1	0.5	0.5	–0.5	A
TRANSISTOR DISSIPATION:	P_T							
At case temperatures up to 25°C ..		7	10	10	5	5	7	W
At case temperatures above 25°C ..		← *See Fig. 2* →						
TEMPERATURE RANGE:								
Storage & Operating (Junction)		← –65 to 200 →						°C
PIN TEMPERATURE (During Soldering):								
At distances ≥ 1/32 in (0.8 mm) from case for 10 s max.		← 230 →						°C

Type RCA1A02
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = −40 V, I_B = 0	–	−1	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = −4 V, I_C = 0	–	−1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = −0.1 A, I_B = 0	−50	–	V
Gain Bandwidth Product	f_T	V_{CE} = −4 V, I_C = −50 mA	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = −0.1 mA, V_{CE} = −10 V	30	200	
Base-to-Emitter Voltage	V_{BE}	I_C = −0.1 mA, V_{CE} = −10 V	–	−0.8	V

For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).

Type RCA1A03
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 85 V, R_{BE} = 100Ω	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	0.1	mA
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = 0.1 A, R_{BE} = 100Ω	95	–	V
Gain Bandwidth Product	f_T	I_C = 0.1 A, V_{CE} = 4 V	50	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 300 mA, V_{CE} = 4 V	70	300	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 300 mA, I_B = 30 mA	–	0.8	V
Base-to-Emitter Voltage	V_{BE}	I_C = 300 mA, V_{CE} = 4 V	–	1.4	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 50 V, t = 0.4 s	0.2	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N5320 (File 325).

Type RCA1A04
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial-planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = −85 V, R_{BE} = 100Ω	–	−10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	−0.1	mA
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = −0.1 A, R_{BE} = 100Ω	−95	–	V
Gain Bandwidth Product	f_T	I_C = −0.1 A, V_{CE} = −4 V	50	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = −300 mA, V_{CE} = −4 V	70	300	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = −300 mA, I_B = −30 mA	–	−0.8	V
Base-to-Emitter Voltage	V_{BE}	I_C = −300 mA, V_{CE} = −4 V	–	−1.4	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = −35 V, t = 0.4 s	−0.285	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N5322 (File 325).

Type RCA1A17
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 80 V, I_B = 0	–	1	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage : With base open	V_{CEO}	I_C = 100 mA, I_B = 0	90	–	V
Gain Bandwidth Product	f_T	V_{CE} = 4 V, I_C = 50 mA	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 mA, V_{CE} = 4 V	40	200	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 150 mA, I_B = 15 mA	–	1.4	V
Base-to-Emitter Voltage	V_{BE}	I_C = 10 mA, V_{CE} = 4 V	–	1	V

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

Type RCA1A18
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 5 V, I_B = 0	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 10 mA, I_B = 0	10	–	V
Gain Bandwidth Product	f_T	I_C = 50 mA, V_{CE} = 4 V	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 mA, V_{CE} = 4 V	40	250	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C = 10 mA, I_B = 0.5 mA	–	1	V
Base-to-Emitter Voltage	V_{BE}	I_C = 10 mA, V_{CE} = 4 V	–	0.78	V

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

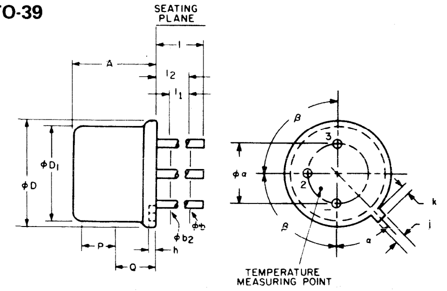
Type RCA1A19
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = –5 V, I_B = 0	–	–10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = – 4 V, I_C = 0	–	–1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = –10 mA, I_B = 0	–10	–	V
Gain Bandwidth Product	f_T	I_C = –50 mA, V_{CE} = –4 V	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –10 mA, V_{CE} = 4 V	40	250	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C = –10 mA, I_B = –0.5 mA	–	–1	V
Base-to-Emitter Voltage	V_{BE}	I_C = –10 mA, V_{CE} = –4 V	–	–0.78	V

For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).

DIMENSIONAL OUTLINE FOR TYPES RCA1A02, RCA1A03, RCA1A04, RCA1A17, RCA1A18, RCA1A19 JEDEC TO-39



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
φa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
φb	0.016	0.021	0.406	0.533	2
φb2	0.016	0.019	0.406	0.483	2
φD	0.350	0.370	8.89	9.40	
φD1	0.315	0.335	8.00	8.51	
h	0.009	0.041	0.229	1.04	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
l	0.500		12.70		2
l1		0.050		1.27	2
l2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

92CS-15641R2

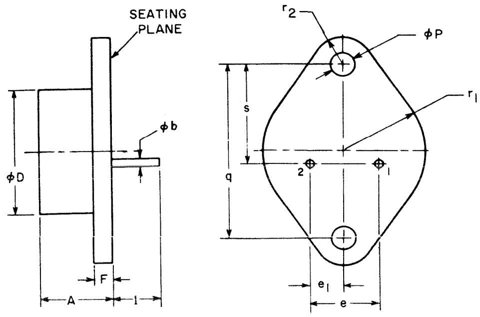
Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads) φb_2 applies between l_1 and l_2. φb applies between l_2 and 0.5 in. (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond 0.5 in. (12.70 mm) from seating plane.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

DIMENSIONAL OUTLINE FOR TYPE RCA1B01 JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
φb	0.038	0.043	0.97	1.09	2
φD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
1	0.312		7.92		2
φP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r1		0.525		13.34	
r2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

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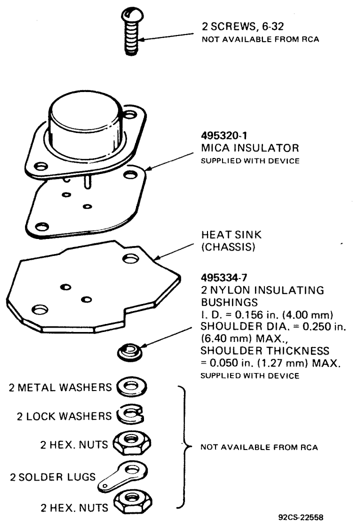
TERMINAL CONNECTIONS FOR TYPES RCA1A02, RCA1A03, RCA1A04, RCA1A17, RCA1A18, RCA1A19

Lead 1 – Emitter
Lead 2 – Base
Case, Lead 3 – Collector

TERMINAL CONNECTIONS FOR TYPE RCA1B01

Pin 1 – Base
Pin 2 – Emitter
Case – Collector
Mounting Flange – Collector



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Suggested mounting hardware for JEDEC TO-3.

RCA

Solid State
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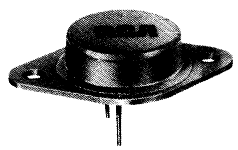
Power Transistors

RCA1B06



RCA1B06

JEDEC TO-3 H-1570

Silicon Transistor for 70-Watt Quasi-Complementary-Symmetry Audio Amplifiers with Pi-Nu Output Transistors

RCA1B06 is an n-p-n pi-nu silicon transistor in a JEDEC TO-3 package. This device is especially characterized for audio-amplifier applications, and can be driven by either RCA1C03 or RCA1C04, n-p-n and p-n-p types, respectively.

The 70-watt amplifier shown in Figs. 1 and 5 uses the RCA1B06 output device in conjunction with eleven other discrete transistors, thirteen diodes, and a 90-volt split power supply. The amplifier output is directly coupled to an 8-ohm speaker. The high-frequency RCA1B06 output transistors used in the amplifier circuit produce excellent transient response at a high power level.

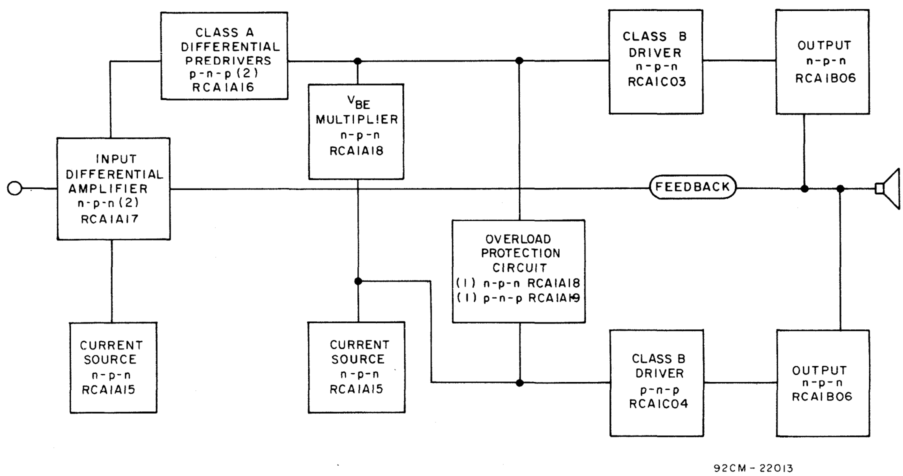


Fig. 1—Block diagram and transistor complement for 70-watt quasi-complementary-symmetry audio amplifier with pi-nu output transistors.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		RCA1B06	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	120	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With base open	V_{CEO}	100	V
With external base-to-emitter resistance (R_{BE}) = 100Ω	V_{CER}	120	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	6	V
COLLECTOR CURRENT	I_C	7	A
BASE CURRENT	I_B	2	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25°C		150	W
At case temperatures above 25°C		*See Fig. 2*	
TEMPERATURE RANGE:			
Storage & Operating (Junction)		−65 to 200	°C
PIN TEMPERATURE (During Soldering):			
At distances ≥ 1/32 in. (0.8 mm) from case for 10 s max.		230	°C

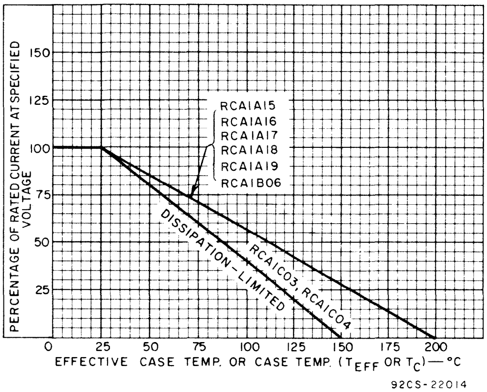


Fig.2—Derating curves for all types.

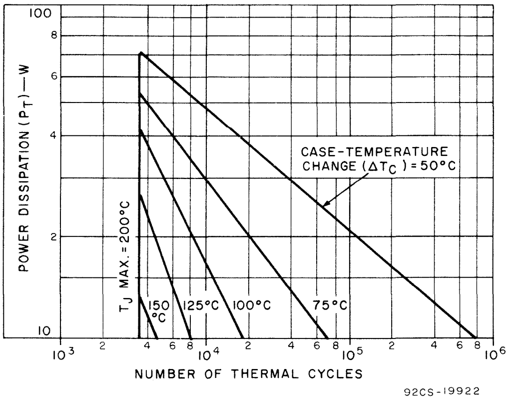


Fig.3—Thermal-cycling ratings for RCA1B06

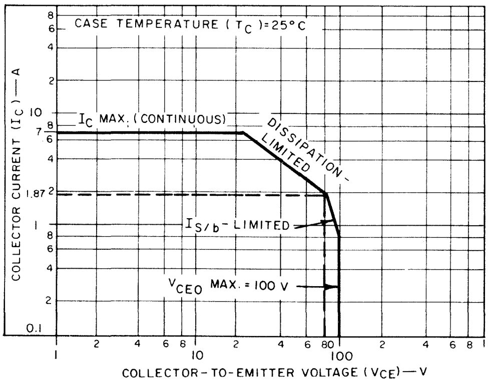
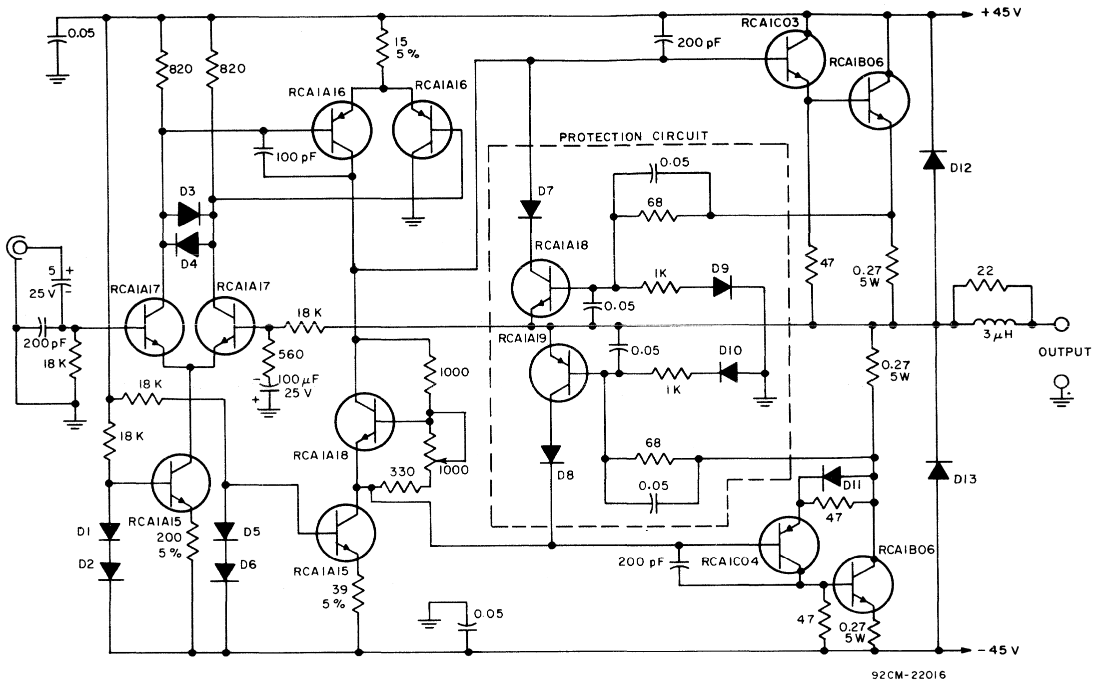
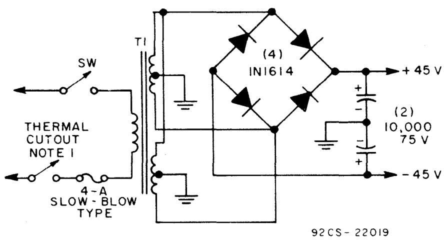


Fig.4—Maximum operating areas for RCA1B06.





NOTES:

1. 100°C thermal cutout attached to heat sink for output transistors (Elmwood Sensor part No. 2455-88-4).•
2. Power transformer: Signal 120-2 (parallel secondary),• Signal Transformer Co., 1 Junius St., Brooklyn, N.Y. 11212.
3. Resistors are 1/2-watt unless otherwise specified; values are in ohms.
4. Capacitances are in μF unless otherwise specified.
5. Non-inductive resistors.
6. D1-D8, D11-1N5391
   D9, D10, D12, D13-1N5393

• Or equivalent.

Fig.5—70-Watt amplifier circuit featuring quasi-complementary-symmetry output employing pi-nu construction output transistors.

TYPICAL PERFORMANCE DATA
For 70-Watt Audio Amplifier

Measured at a line voltage of 120 V, T_A = 25°C, and a frequency of 1 kHz, unless otherwise specified.

Power:	
Rated power (8-Ω load, at rated distortion)	70 W
Typical power (4-Ω load)	100 W
Typical power (16-Ω load)	50 W
Total Harmonic Distortion:	
Rated distortion	0.5%
IM Distortion:	
10 dB below continuous power output at 60 Hz and 7 kHz (4:1)	<0.2%
IHF Power Bandwidth:	
3 dB below rated continuous power at rated distortion	5 Hz to 50 kHz
Bandwidth at 1 W	5 Hz to 100 kHz
Sensitivity:	
At continuous power-output rating	600 mV
Hum and Noise:	
Below continuous power output:	
Input shorted	100 dB
Input open	85 dB
With 2 kΩ resistance on 20-ft. cable on input	97 dB
Input Resistance	18 kΩ

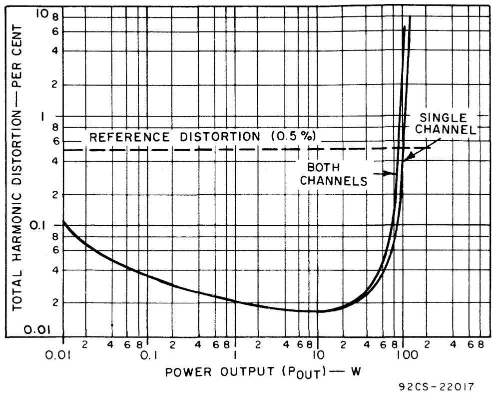


Fig.6—Typical total harmonic distortion vs. power output at 1 kHz.

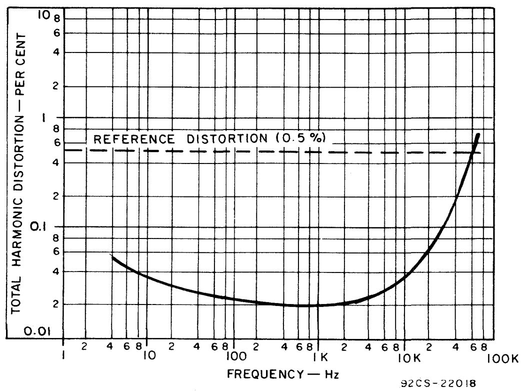


Fig.7—Typical total harmonic distortion vs. frequency at 35 W.

Type RCA1B06
Package: JEDEC TO-3
Construction: Silicon n-p-n, epitaxial, multiple-emitter-site, pi-nu

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 90 V, R_{BE} = 100Ω	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 0.2 A, I_B = 0	100	–	V
Gain Bandwidth Product	f_T	I_C = 0.2 A, V_{CE} = 10 V	5	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 4 A, V_{CE} = 4 V	10	50	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C = 4 A, I_B = 0.8 A	–	2	V
Base-to-Emitter Voltage	V_{BE}	I_C = 4 A, V_{CE} = 4 V	–	2	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 80 V, t = 1 s	1.87	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N5840 (File 410).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Rating	Symbol	RCA1A15	RCA1A16	RCA1A17	RCA1A18	RCA1A19	RCA1C03	RCA1C04	Units
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	–	–	–	–	–	120	−120	V
COLLECTOR-TO-EMITTER VOLTAGE:									
With base open	V_{CEO}	100	−100	90	10	−10	100	−100	V
With external base-to-emitter resistance (R_{BE}) = 100Ω	V_{CER}	–	–	–	–	–	120	−120	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	−5	4	4	−4	5	−5	V
COLLECTOR CURRENT	I_C	1	−1	1	1	−1	4	−4	A
BASE CURRENT	I_B	0.5	−0.1	0.5	0.5	−0.5	2	−2	A
TRANSISTOR DISSIPATION:	P_T								
At case temperatures up to 25°C		10	10	5	7	7	40	40	W
At case temperatures above 25°C		← See Fig. 2 →							
TEMPERATURE RANGE:									
Storage & Operating (Junction)		← −65 to 200 →					← −65 to 150 →		°C
PIN TEMPERATURE (During Soldering):									
At distances ≥ 1/32 in. (0.8 mm) from case for 10 s max.		← 230 →							°C

Type RCA1A15
Package: JEDEC TO-39
Construction: Silicon n-p-n, epitaxial

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 90 V	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 5 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 10 mA, I_B = 0	100	–	V
Gain Bandwidth Product	f_T	V_{CE} = 10 V, I_C = 10 mA	15	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 mA, V_{CE} = 10 V	20	100	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 10 mA, I_B = 1 mA	–	1	V
Base-to-Emitter Voltage	V_{BE}	I_C = 10 mA, V_{CE} = 10 V	–	1	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 50 V, t = 0.4 s	0.2	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N3440 (File 64).

Type RCA1A16
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = −90 V	–	−10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = −5 V, I_C = 0	–	−1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = −10 mA, I_B = 0	−100	–	V
Gain Bandwidth Product	f_T	V_{CE} = −10 V, I_C = −10 mA	15	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = −10 mA, V_{CE} = −10 V	40	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = −10 mA, I_B = −1 mA	–	−1	V
Base-to-Emitter Voltage	V_{BE}	I_C = −10 mA, V_{CE} = −10 V	–	−1	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = −50 V, t = 0.4 s	−0.2	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N5416 (File 336).

Type RCA1A17
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 80 V	–	1	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 100 mA, I_B = 0	90	–	V
Gain Bandwidth Product	f_T	V_{CE} = 4 V, I_C = 50 mA	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 mA, V_{CE} = 4V	40	200	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 150 mA, I_B = 15 mA	–	1.4	V
Base-to-Emitter Voltage	V_{BE}	I_C = 10 mA, V_{CE} = 4 V	–	1	V

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

Type RCA1A18
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 5 V, I_B = 0	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 10 mA, I_B = 0	10	–	V
Gain Bandwidth Product	f_T	I_C = 50 mA, V_{CE} = 4 V	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 mA, V_{CE} = 4 V	40	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 10 mA, I_B = 0.5 mA	–	1	V
Base-to-Emitter Voltage	V_{BE}	I_C = 10 mA, V_{CE} = 4 V	–	0.78	V

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

Type RCA1A19
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = –5 V, I_B = 0	–	–10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –4 V, I_C = 0	–	–1	mA
Collector-to-Emitter Voltage With base open	V_{CEO}	I_C = –10 mA, I_B = 0	–10	–	V
Gain Bandwidth Product	f_T	I_C = –50 mA, V_{CE} = –4 V	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –10 mA, V_{CE} = –4 V	40	250	–
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = –10 mA, I_B = –0.5 mA	–	–1	V
Base-to-Emitter Voltage	V_{BE}	I_C = –10 mA, V_{CE} = –4 V	–	–0.78	V

For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).

Type RCA1C03
Package: JEDEC TO-220AB
Construction: Silicon n-p-n, epitaxial

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

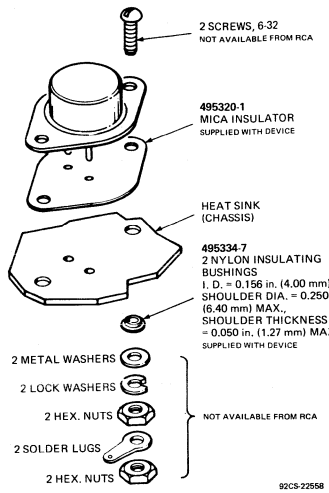
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 110 V, R_{BE} = 100Ω	–	1	mA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 5 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 0.1 A, I_B = 0	100	–	V
Gain Bandwidth Product	f_T	I_C = 0.5 A, V_{CE} = 4 V	4	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 1 A, V_{CE} = 4 V	50	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 1 A, I_B = 0.1 A	–	1	V
Base-to-Emitter Voltage	V_{BE}	I_C = 1 A, V_{CE} = 4 V	–	1.5	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 40 V, t = 0.4 s	1	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N6293 (File 542).

Type RCA1C04
Package: JEDEC TO-220AB
Construction: Silicon p-n-p, epitaxial

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

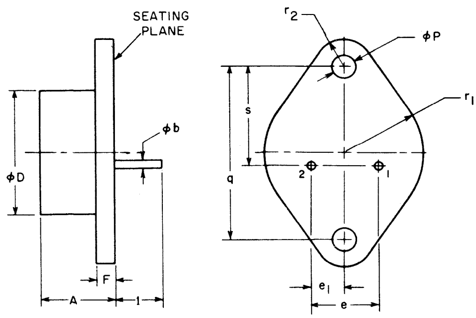
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = –110 V, R_{BE} = 100Ω	–	–1	mA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –5 V, I_C = 0	–	–1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = –0.1 A, I_B = 0	–100	–	V
Gain Bandwidth Product	f_T	I_C = –0.5 A, V_{CE} = –4 V	10	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –1 A, V_{CE} = –4 V	50	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = –1 A, I_B = –0.1 A	–	–1	V
Base-to-Emitter Voltage	V_{BE}	I_C = –1 A, V_{CE} = –4 V	–	–1.5	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = –40 V, t = 0.4 s	–1	–	A



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.9—Suggested mounting hardware for JEDEC TO-3.

DIMENSIONAL OUTLINE FOR TYPE RCA1B06 JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
φb	0.038	0.043	0.97	1.09	2
φD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
1	0.312		7.92		2
φP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r1		0.525		13.34	
r2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

TERMINAL CONNECTIONS

Pin 1 — Base
Pin 2 — Emitter
Case — Collector
Mounting Flange — Collector

NOTES:

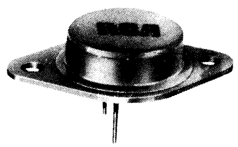
1. **These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.**
2. **Two pins.**

92CS—15222

RCA
Solid State
Division

Power Transistors

RCA1B04



RCA1B04

JEDEC TO-3 H-1570

Silicon Transistor for 120-Watt Quasi-Complementary-Symmetry Audio Amplifiers with Parallel Output Transistors

RCA1B04 is an n-p-n silicon pi-nu transistor in a JEDEC TO-3 package. This device is especially characterized for audio applications, and can be driven by RCA1C12 and RCA1C13 transistors.

The 120-watt amplifier circuit in Figs. 1 and 5 uses the RCA1B04 in conjunction with eleven other discrete transistors, twelve diodes, and a 130-volt split power supply. The amplifier output is directly coupled to an 8-ohm speaker. This RCA 120-watt audio amplifier is especially designed for top-of-the-line quadrasonic use in applications requiring ½ kW of quadrasonic sound with excellent tonal quality.

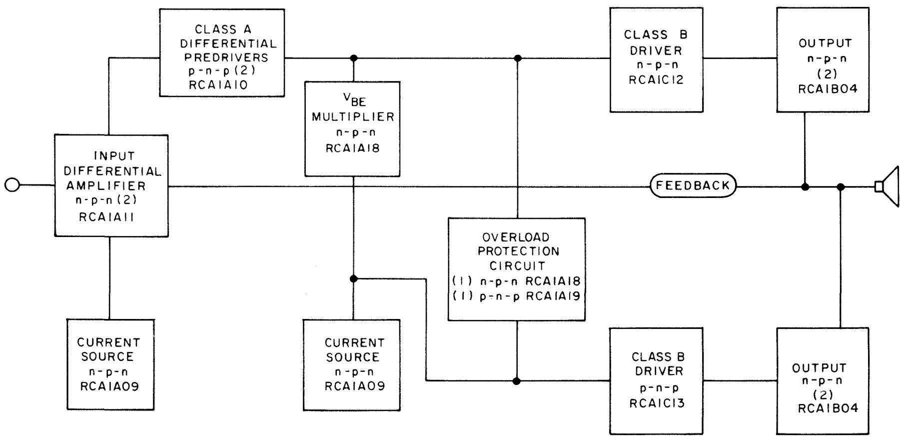


Fig. 1— Block diagram and transistor complement for 120-watt quasi-complementary-symmetry audio amplifier with parallel output transistors.

MAXIMUM RATINGS, *Absolute-Maximum Values:*		**RCA1B04**	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	225	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With base open	V_{CEO}	200	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}	225	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	V
COLLECTOR CURRENT	I_C	7	A
BASE CURRENT	I_B	2	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25°C		150	W
At case temperatures above 25°C		See Fig. 2	
TEMPERATURE RANGE:			
Storage & Operating (Junction)		−65 to 200	°C
PIN TEMPERATURE (During Soldering):			
At distances ≥ 1/32 in. (0.8 mm) from case for 10 s max.		230	°C

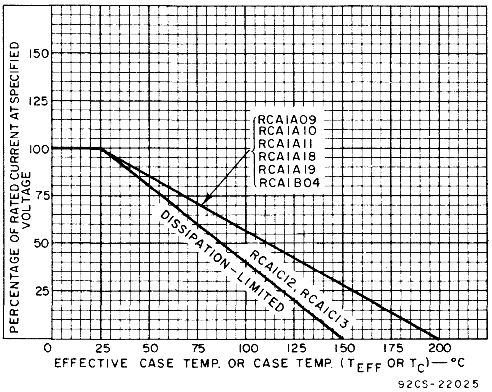


Fig. 2— Derating curves for all types.

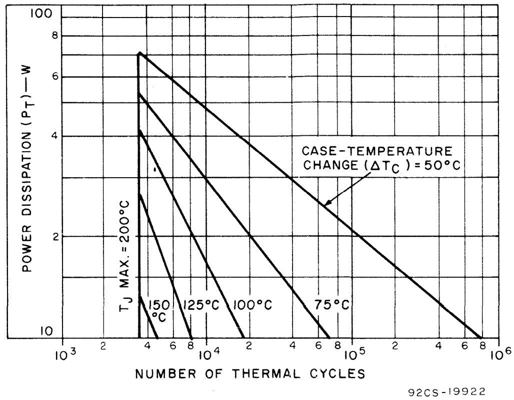


Fig. 3— Thermal-cycling ratings for RCA1B04.

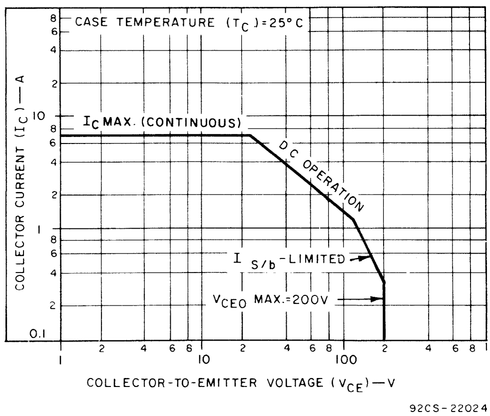


Fig. 4— Maximum operating areas for RCA1B04.

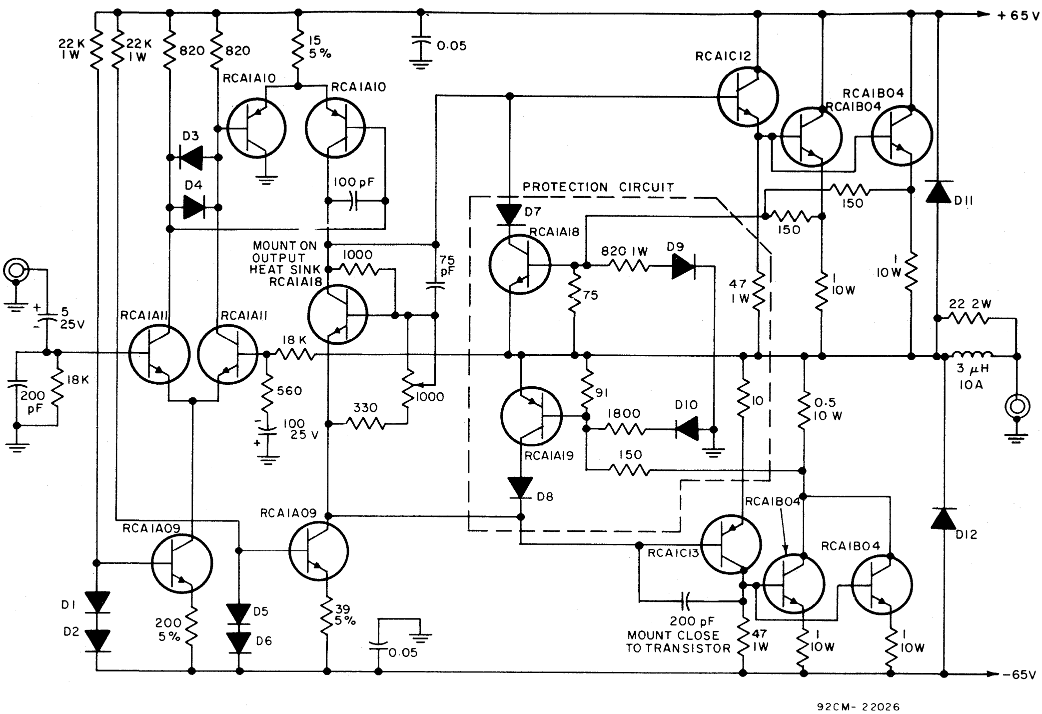
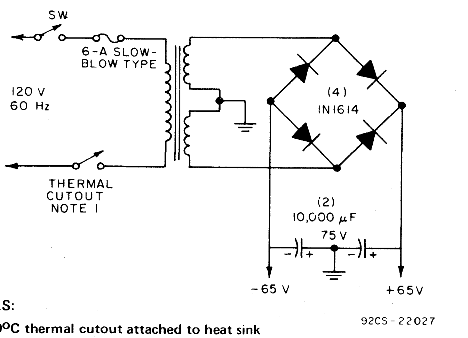


Fig. 5— 120-watt amplifier circuit featuring quasi-complementary-symmetry with parallel output transistors.

NOTES FOR FIG. 5:

1. D1–D8 · 1N5391; D9–D12 · 1N5393
2. Resistors are 1/2-watt, ± 10% unless otherwise specified; values are in ohms
3. Capacitances are in µF unless otherwise specified
4. Non-inductive resistors
5. Provide approx. 1°C/W heat sinking per output device based on mounting with mica washer and ZnO thermal compound (Dow Corning No. 340, or equivalent) with T_A = 45°C max.



NOTES:

1. 100°C thermal cutout attached to heat sink for output transistors (Elmwood Sensor part No. 2455-88-4)•
2. Power transformer: Signal 88-6, Signal Transformer Co., 1 Junius St., Brooklyn, N.Y. 11212.

• Or equivalent.

Fig. 6— Power supply for 120-watt audio amplifier.

TYPICAL PERFORMANCE DATA
For 120-Watt Audio Amplifier

Measured at a line voltage of 120 V, T_A = 25°C, and a frequency of 1 kHz, unless otherwise specified.

Power:	
Rated power (8-Ω load, at rated distortion)	120 W
Typical power (4-Ω load)	180 W
Typical power (16-Ω load)	80 W
Total Harmonic Distortion:	
Rated distortion	0.5%
IM Distortion:	
10 dB below continuous power output at 60 Hz and 7 kHz (4:1)	0.2%
IHF Power Bandwidth:	
3 dB below rated continuous power at rated distortion	5 Hz to 50 kHz
Sensitivity:	
At continuous power output rating	900 mV
Hum and Noise:	
Below continuous power output:	
Input shorted	104 dB
Input open	88 dB
With 2 kΩ resistance on 20-ft. cable on input	104 dB
Input Resistance	18 kΩ

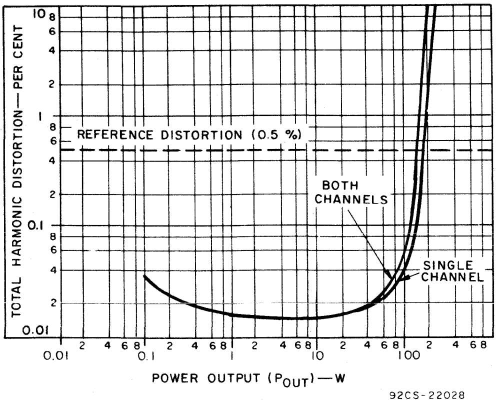


Fig. 7— Typical total harmonic distortion vs. power output for single channel (8 Ω), and both channels driven at 1 kHz.

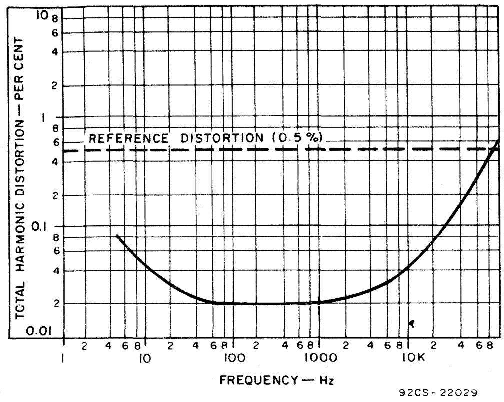


Fig. 8— Typical total harmonic distortion vs. frequency for 60-watt output.

Type RCA1B04

Package: JEDEC TO-3

Construction: Silicon n-p-n, multiple-epitaxial, pi-nu

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 120 V, R_{BE} = 100 Ω	–	1	mA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 5 V, I_B = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 0.2 A, I_B = 0	200	–	V
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = 0.2 A, R_{BE} = 100 Ω	225	–	V
Gain Bandwidth Product	f_T	I_C = 0.2 A, V_{CE} = 10 V	5	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 2 A, V_{CE} = 5 V	15	75	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 2 A, I_B = 0.255 A	–	2	V
Base-to-Emitter Voltage	V_{BE}	I_C = 2 A, V_{CE} = 5 V	1	2	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 120 V, t = 1 s	1.25	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N5239 (File 321).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		RCA1A09	RCA1A10	RCA1A11	RCA1A18	RCA1A19	RCA1C12	RCA1C13	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	–	–	–	–	–	140	–140	V
COLLECTOR-TO-EMITTER VOLTAGE:									
With base open	V_{CEO}	175	–175	175	10	–10	120	–120	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}	–	–	–	–	–	140	–140	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	6	–6	6	4	–4	5	–5	V
COLLECTOR CURRENT	I_C	1	–1	1	1	–1	4	–4	A
BASE CURRENT	I_B	0.5	–0.5	0.5	0.5	–0.5	2	–2	A
TRANSISTOR DISSIPATION:	P_T								
At case temperatures up to 25°C		10	10	10	7	7	40	40	W
At case temperatures above 25°C		← See Fig. 2 →							
TEMPERATURE RANGE:									
Storage & Operating (Junction)		← –65 to 200 →					← –65 to 150 →		°C
PIN TEMPERATURE (During Soldering):									
At distances ≥ 1/32 in. (0.8 mm) from case for 10 s max.		← 230 →							°C

Type RCA1A09
Package: JEDEC TO-39
Construction: Silicon n-p-n, epitaxial

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 90 V, I_B = 0	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 6 V, I_C = 0	–	100	μA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 10 mA, I_B = 0	175	–	V
Gain Bandwidth Product	f_T	I_C = 10 mA, V_{CE} = 10 V	15	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 mA, V_{CE} = 10 V	20	100	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 50 mA, I_B = 4 mA	–	0.5	V
Base-to-Emitter Voltage	V_{BE}	I_C = 10 mA, V_{CE} = 10 V	–	0.9	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 150 V, t = 1 s	0.065	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N3439 (File 64).

Type RCA1A10
Package: JEDEC TO-39
Construction: Silicon p-n-p

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = −120 V, I_B = 0	–	−10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = −6 V, I_C = 0	–	−100	μA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = −10 mA, I_B = 0	−175	–	V
Gain Bandwidth Product	f_T	I_C = −10 mA, V_{CE} = −10 V	15	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = −10 mA, V_{CE} = −10 V	40	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = −10 mA, I_B = −1 mA	–	−2	V
Base-to-Emitter Voltage	V_{BE}	I_C = −10 mA, V_{CE} = −10 V	–	−0.8	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = −150 V, t = 1 s	−0.04	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N5415 (File 336).

Type RCA1A11
Package: JEDEC TO-39
Construction: Silicon n-p-n, epitaxial

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 90 V, I_B = 0	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 6 V, I_C = 0	–	100	μA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 10 mA, I_B = 0	175	–	V
Gain Bandwidth Product	f_T	I_C = 10 mA, V_{CE} = 10 V	15	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 1 mA, V_{CE} = 10 V	40	250	
Base-to-Emitter Voltage	V_{BE}	I_C = 1 mA, V_{CE} = 10 V	0.5	0.7	V

For characteristics curves and test conditions, refer to published data for prototype 2N3439 (File 64).

Type RCA1A18
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 5 V, I_B = 0	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 10 mA, I_B = 0	10	–	V
Gain Bandwidth Product	f_T	I_C = 50 mA, V_{CE} = 4 V	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 mA, V_{CE} = 4 V	40	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 10 mA, I_B = 0.5 mA	–	1	V
Base-to-Emitter Voltage	V_{BE}	I_C = 10 mA, V_{CE} = 4 V	–	0.78	V

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

Type RCA1A19
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = –5 V, I_B = 0	–	–10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –4 V, I_C = 0	–	–1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = –10 mA, I_B = 0	–10	–	V
Gain Bandwidth Product	f_T	I_C = –50 mA, V_{CE} = –4 V	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –10 mA, V_{CE} = –4 V	40	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = –10 mA, I_B = –0.5 mA	–	–1	V
Base-to-Emitter Voltage	V_{BE}	I_C = –10 mA, V_{CE} = –4 V	–	–0.78	V

For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).

Type RCA1C12
Package: JEDEC TO-220AB
Construction: Silicon n-p-n, epitaxial

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

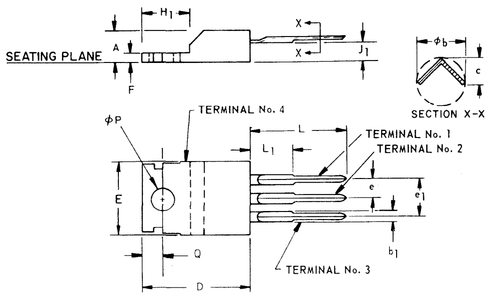
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 90 V, R_{BE} = 100 Ω	–	100	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 5 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 0.1 A, I_B = 0	120	–	V
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = 0.1 A, R_{BE} = 100 Ω	140	–	V
Gain Bandwidth Product	f_T	I_C = 0.5 A, V_{CE} = 4 V	4	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 1 A, V_{CE} = 2 V	40	250	
Base-to-Emitter Voltage	V_{BE}	I_C = 1 A, V_{CE} = 2 V	–	1.2	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 60 V, t = 0.4 s	0.66	–	A

Type RCA1C13
Package: JEDEC TO-220AB
Construction: Silicon p-n-p, epitaxial

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = –90 V, R_{BE} = 100 Ω	–	–100	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –5 V, I_C = 0	–	–1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = –0.1 A, I_B = 0	–120	–	V
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = –0.1 A, R_{BE} = 100 Ω	–140	–	V
Gain Bandwidth Product	f_T	I_C = –0.5 A, V_{CE} = –4 V	10	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –1 A, V_{CE} = –2 V	40	250	
Base-to-Emitter Voltage	V_{BE}	I_C = –1 A, V_{CE} = –2 V	–	–1.2	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = –60 V, t = 0.4 s	–0.66	–	A

DIMENSIONAL OUTLINE FOR TYPES RCA1C12, RCA1C13 JEDEC TO-220AB



BOTTOM VIEW

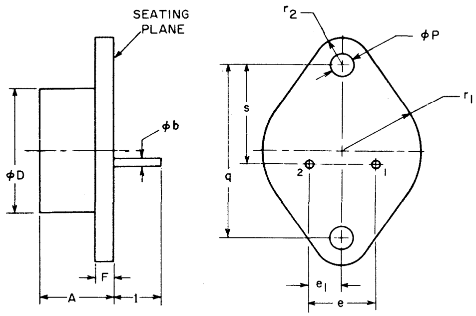
SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	0.140	0.190	3.56	4.82	–
ϕb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
ϕP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 (6.35 – 6.48 mm) from case.

DIMENSIONAL OUTLINE FOR TYPE RCA1B04 JEDEC TO-3



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	0.250	0.450	6.35	11.43	
ϕb	0.038	0.043	0.97	1.09	2
ϕD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e_1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
1	0.312		[illegible]		2
ϕP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r_1		0.525		13.34	
r_2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS–15222

TERMINAL CONNECTIONS FOR TYPES RCA1C12, RCA1C13

Lead 1 – Base
Lead 2 – Collector
Lead 3 – Emitter
Lead 4 – Collector

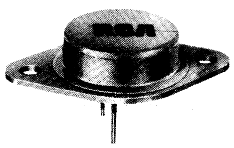
TERMINAL CONNECTIONS FOR TYPE RCA1B04

Pin 1 – Base
Pin 2 – Emitter
Case – Collector
Mounting Flange – Collector

Solid State Division

Power Transistors

RCA1B05



RCA1B05

JEDEC TO-3 H-1570

Silicon Transistor for 200-Watt Quasi-Complementary-Symmetry Audio Amplifiers with Parallel Output Transistors

RCA1B05 is a silicon n-p-n pi-nu transistor in a JEDEC TO-3 package. This device is especially suitable for applications in audio-amplifier circuits, in which it may be used as either driver or output unit.

The 200-watt amplifier shown in Figs. 1 and 5 uses eight RCA1B05 transistors, two as drivers and six as parallel units in the amplifier output stages. These devices are employed in conjunction with eleven other discrete transistors, twelve diodes, and a 160-volt split power supply. The amplifier output is directly coupled to an 8-ohm speaker. This 200-watt audio amplifier is especially designed to feature ruggedness in combination with high power output and excellent high-fidelity performance.

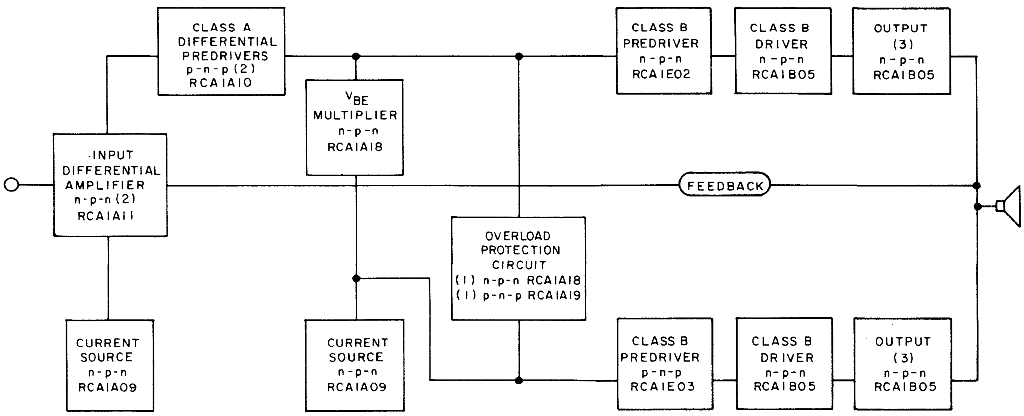


Fig. 1— Block diagram and transistor complement for 200-watt quasi-complementary-symmetry audio amplifier with parallel output transistors.

6-73

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		RCA1B05	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	275	V
COLLECTOR-TO-EMITTER VOLTAGE:			
With base open	V_{CEO}	250	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}	275	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	V
COLLECTOR CURRENT	I_C	7	A
BASE CURRENT	I_B	2	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25°C		150	W
At case temperatures above 25°C		See Fig. 2	
TEMPERATURE RANGE:			
Storage & Operating (Junction)		−65 to 200	°C
PIN TEMPERATURE (During Soldering):			
At distances ≥ 1/32 in. (0.8 mm) from case for 10 s max.		230	°C

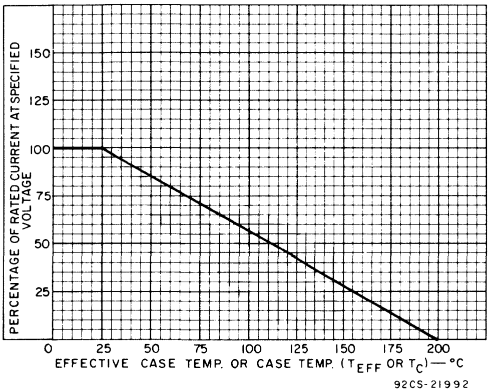


Fig. 2— Derating curves for all types.

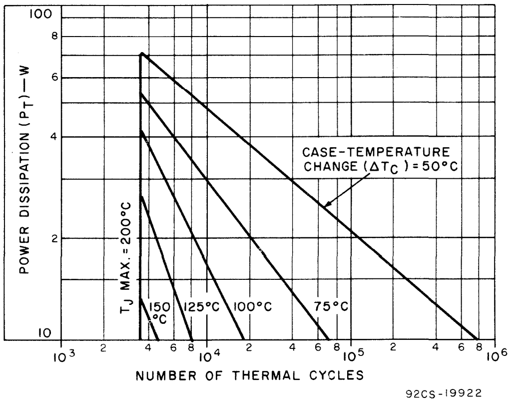


Fig. 3— Thermal-cycling ratings for RCA1B05.

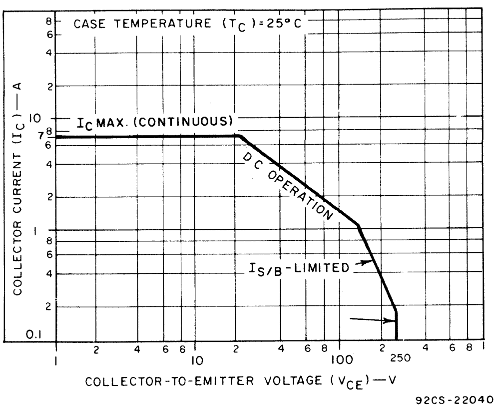


Fig. 4— Maximum operating areas for RCA1B05.

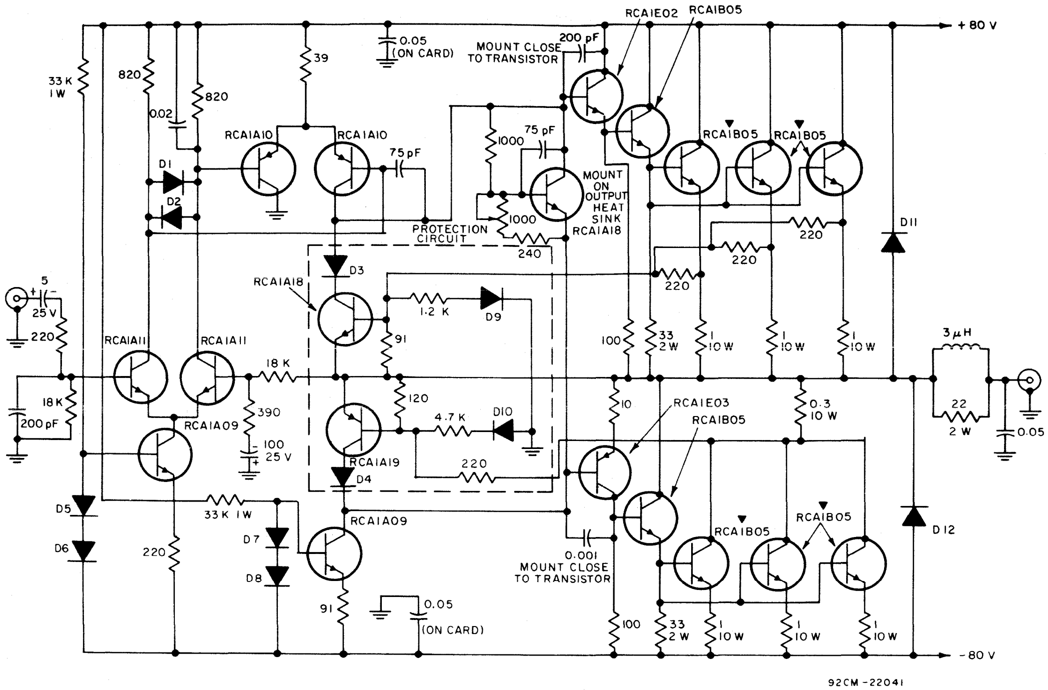
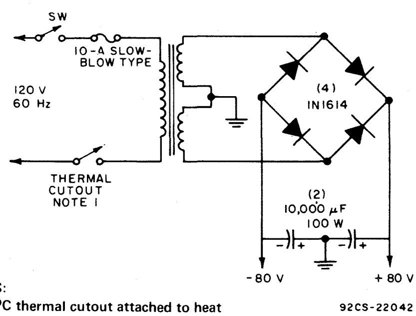


Fig. 5— 200-watt amplifier circuit featuring quasi-complementary-symmetry with parallel output transistors.

NOTES FOR FIG. 5:
1. D1–D8 - 1N5391; D9–D12 - 1N5393
2. Resistors are ½-watt, ± 10% unless otherwise specified; values are in ohms
3. Capacitances are in μF unless otherwise specified
4. Non-inductive resistors
5. ▼ Provide approx. 1°C/W heat sinking per output device based on mounting with mica washer and ZnO thermal compound (Dow Corning No. 340, or equivalent) with T_A = 45°C max.



NOTES:
1. 100°C thermal cutout attached to heat sink for output transistors (Elmwood Sensor Part No. 2455-88-4)●.
2. Power transformer: Signal 120-6,● Signal Transformer Co., 1 Junius St., Brooklyn, N.Y. 11212. Use 125-volt primary tap.

● Or equivalent.

Fig. 6— Power supply for 200-watt audio amplifier.

TYPICAL PERFORMANCE DATA
For 200-Watt Audio Amplifier

Measured at a line voltage of 120 V, T_A = 25°C, and a frequency of 1 kHz, unless otherwise specified.

Power:	
Rated power (8-Ω load, at rated distortion)	200 W
Typical power (4-Ω load)	300 W
Typical power (16-Ω load)	130 W
Total Harmonic Distortion:	
Rated distortion	0.5%
IM Distortion:	
10 dB below continuous power output at 60 Hz and 7 kHz (4:1)	0.2%
IHF Power Bandwidth:	
3 dB below rated continuous power at rated distortion	5 Hz to 35 kHz
Sensitivity:	
At continuous power output rating	900 mV
Hum and Noise:	
Below continuous power output:	
Input shorted	96 dB
Input open	84 dB
With 2 kΩ resistance on 20-ft. cable on input	94 dB
Input Resistance	18 kΩ

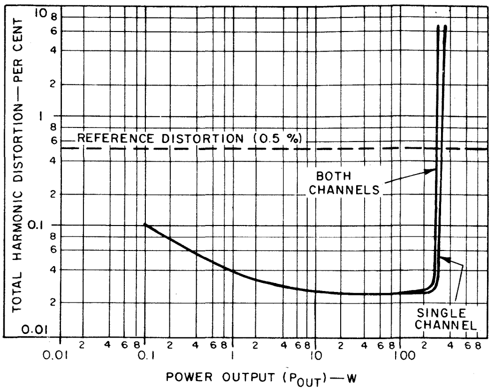


Fig. 7— Typical total harmonic distortion vs. power output for single channel and both channels driven at 1 kHz.

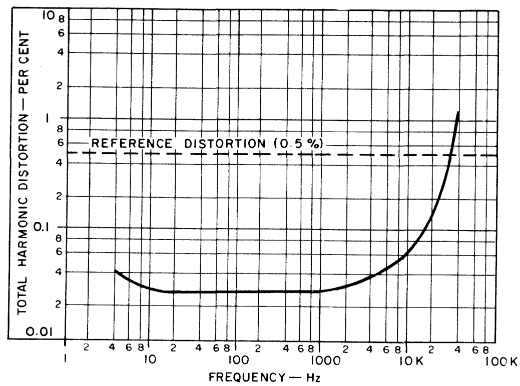


Fig. 8— Typical total harmonic distortion vs. frequency for 100-watt output.

Type RCA1B05

Package: JEDEC TO-3

Construction: Silicon n-p-n, multiple-epitaxial, pi-nu

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 200 V, R_{BE} = 100 Ω	–	1	mA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 50 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 0.2 A, I_B = 0	250	–	V
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = 0.2 A, R_{BE} = 100 Ω	275	–	V
Gain Bandwidth Product	f_T	I_C = 0.2 A, V_{CE} = 10 V	5	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 2 A, V_{CE} = 5 V	15	75	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 2 A, I_B = 0.255 A	–	2	V
Base-to-Emitter Voltage	V_{BE}	I_C = 2 A, V_{CE} = 5 V	1	2	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 140 V, t = 1 s	1.07	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N5240 (File 321).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		RCA1A09	RCA1A10	RCA1A11	RCA1A18	RCA1A19	RCA1E02	RCA1E03	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	–	–	–	–	–	200	−200	V
COLLECTOR-TO-EMITTER VOLTAGE:									
With base open	V_{CEO}	175	−175	175	10	−10	175	−175	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}	–	–	–	–	–	200	−200	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	6	−6	6	4	−4	5	−5	V
COLLECTOR CURRENT	I_C	1	−1	1	1	−1	2	−2	A
BASE CURRENT	I_B	0.5	−0.5	0.5	0.5	−0.5	1	−1	A
TRANSISTOR DISSIPATION:	P_T								
At case temperatures up to 25°C		10	10	10	7	7	35	35	W
At case temperatures above 25°C		← See Fig. 2 →							
TEMPERATURE RANGE:									
Storage & Operating (Junction)		← −65 to 200 →							°C
PIN TEMPERATURE (During Soldering):									
At distances ≥ 1/32 in. (0.8 mm) from case for 10 s max.		← 230 →							°C

Type RCA1A09
Package: JEDEC TO-39
Construction: Silicon n-p-n, epitaxial

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 90 V, I_B = 0	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 6 V, I_C = 0	–	100	μA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 10 mA, I_B = 0	175	–	V
Gain Bandwidth Product	f_T	I_C = 10 mA, V_{CE} = 10 V	15	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 mA, V_{CE} = 10 V	20	100	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 50 mA, I_B = 4 mA	–	0.5	V
Base-to-Emitter Voltage	V_{BE}	I_C = 10 mA, V_{CE} = 10 V	–	0.9	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 150 V, t = 1 s	0.065	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N3439 (File 64).

Type RCA1A10
Package: JEDEC TO-39
Construction: Silicon p-n-p

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = −120 V, I_B = 0	–	−10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = −6 V, I_C = 0	–	−100	μA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = −10 mA, I_B = 0	−175	–	V
Gain Bandwidth Product	f_T	I_C = −10 mA, V_{CE} = −10 V	15	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = −10 mA, V_{CE} = −10 V	40	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = −10 mA, I_B = −1 mA	–	−2	V
Base-to-Emitter Voltage	V_{BE}	I_C = −10 mA, V_{CE} = −10 V	–	−0.8	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = −150 V, t = 1 s	−0.04	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N5415 (File 336).

Type RCA1A11
Package: JEDEC TO-39
Construction: Silicon n-p-n, epitaxial

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 90 V, I_B = 0	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 6 V, I_C = 0	–	100	μA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 10 mA, I_B = 0	175	–	V
Gain Bandwidth Product	f_T	I_C = 10 mA, V_{CE} = 10 V	15	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 1 mA, V_{CE} = 10 V	40	250	
Base-to-Emitter Voltage	V_{BE}	I_C = 1 mA, V_{CE} = 10 V	0.5	0.7	V

For characteristics curves and test conditions, refer to published data for prototype 2N3439 (File 64).

Type RCA1A18
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 5 V, I_B = 0	–	10	µA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 10 mA, I_B = 0	10	–	V
Gain Bandwidth Product	f_T	I_C = 50 mA, V_{CE} = 4 V	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 mA, V_{CE} = 4 V	40	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 10 mA, I_B = 0.5 mA	–	1	V
Base-to-Emitter Voltage	V_{BE}	I_C = 10 mA, V_{CE} = 4 V	–	0.78	V

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

Type RCA1A19
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = –5 V, I_B = 0	–	–10	µA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –4 V, I_C = 0	–	–1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = –10 mA, I_B = 0	–10	–	V
Gain Bandwidth Product	f_T	I_C = –50 mA, V_{CE} = –4 V	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –10 mA, V_{CE} = –4 V	40	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = –10 mA, I_B = –0.5 mA	–	–1	V
Base-to-Emitter Voltage	V_{BE}	I_C = –10 mA, V_{CE} = –4 V	–	–0.78	V

For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).

Type RCA1E02
Package: JEDEC TO-66
Construction: Silicon n-p-n, double-epitaxial

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 120 V, R_{BE} = 100 Ω	–	100	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 5 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 0.1 A, I_B = 0	175	–	V
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = 0.1 A, R_{BE} = 100 Ω	200	–	V
Gain Bandwidth Product	f_T	I_C = 0.2 A, V_{CE} = 10 V	15	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 0.3 A, V_{CE} = 2 V	30	150	
Base-to-Emitter Voltage	V_{BE}	I_C = 0.3 A, V_{CE} = 2 V	–	1	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 80 V, t = 0.4 s	0.4	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N3583 (File 138).

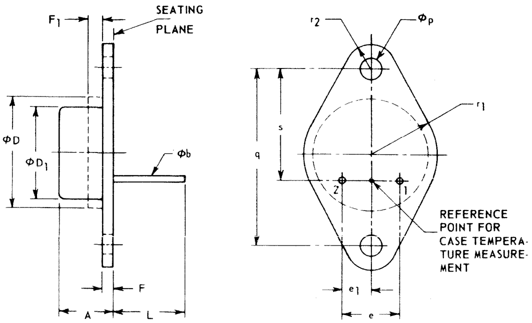
Type RCA1E03
Package: JEDEC TO-66
Construction: Silicon p-n-p

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = –120 V, R_{BE} = 100 Ω	--	–100	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –5 V, I_C = 0	–	–1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = –0.1 A, I_B = 0	–175	–	V
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = –0.1 A, R_{BE} = 100 Ω	–200	–	V
Gain Bandwidth Product	f_T	I_C = –0.2 A, V_{CE} = –10 V	20	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –0.3 A, V_{CE} = –2 V	30	150	
Base-to-Emitter Voltage	V_{BE}	I_C = –0.3 A, V_{CE} = –2 V	–	–1	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = –80 V, t = 0.4 s	–0.25	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N6211 (File 507).

DIMENSIONAL OUTLINE FOR TYPES RCA1E02, RCA1E03
JEDEC TO-66



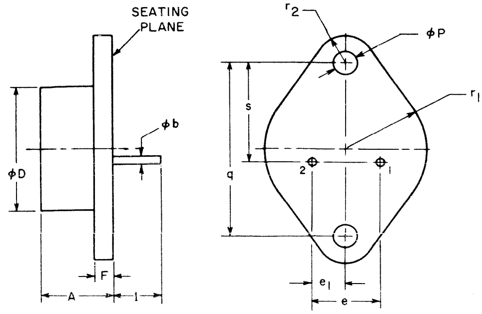
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.340	6.35	8.64	
ϕb	0.028	0.034	0.711	0.863	
ϕD	—	0.620	—	15.75	
ϕD_1	0.470	0.500	11.94	12.70	
e	0.190	0.210	4.83	5.33	
e_1	0.093	0.107	2.36	2.72	
F	0.050	0.075	1.27	1.91	2
F_1	—	0.050	—	1.27	1
L	0.360	—	9.14	—	
ϕp	0.142	0.152	3.61	3.86	
q	0.958	0.962	24.33	24.43	
r_1	—	0.350	—	8.89	
r_2	—	0.145	—	3.68	
s	0.570	0.590	14.48	14.99	

NOTES:

1. The outline contour is optional within zone defined by ϕD and F_1.
2. Dimensions does not include seating flanges.

92SS-3738

DIMENSIONAL OUTLINE FOR TYPE RCA1B05
JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
ϕb	0.038	0.043	0.97	1.09	2
ϕD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e_1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
1	0.312		7.92		2
ϕP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r_1		0.525		13.34	
r_2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS–15222

TERMINAL CONNECTIONS (All Types)

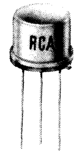
Pin 1 — Base
Pin 2 — Emitter
Mounting Flange, Case — Collector

RCA

Solid State
Division

Power Transistors

RCA1A01–RCA1A11
RCA1A15–RCA1A19



JEDEC TO-39 H-1381

Silicon Transistors for Audio-Frequency Linear-Amplifier Applications

N-P-N TYPES		P-N-P TYPES	
RCA1A01	RCA1A11	RCA1A02	RCA1A10
RCA1A03	RCA1A15	RCA1A04	RCA1A16
RCA1A06	RCA1A17	RCA1A05	RCA1A19
RCA1A07	RCA1A18	RCA1A08	
RCA1A09			

"RCA1A-Series" n-p-n and p-n-p silicon transistors are especially characterized for audio-amplifier applications. They are particularly useful as input devices, V_{BE} multipliers for biasing, current sources, load-line-limiting (protection) circuits, predrivers, and in some instances as complementary drivers. Other applications for these devices include audio power amplifiers, linear modulators, servo amplifiers, and operational amplifiers. The units are supplied in the JEDEC TO-39 package.

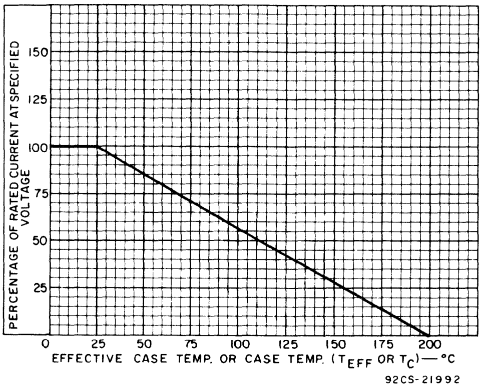


Fig. 1— Derating curve for all types.

MAXIMUM RATINGS, *Absolute-Maximum Values:*		RCA1A01	RCA1A02	RCA1A03	RCA1A04	RCA1A05	RCA1A06	RCA1A07	RCA1A08	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	–	–	95	–95	–75	75	50	–50	V
COLLECTOR-TO-EMITTER VOLTAGE:										
With base open	V_{CEO}	70	–50	–	–	–	–	40	–40	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}	–	–	95	–95	–75	75	50•	–50▲	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	4	–4	4	–4	–4	4	3	–5	V
COLLECTOR CURRENT	I_C	1	–1	2	–2	–1	1	1	–1	A
BASE CURRENT	I_B	0.5	–0.5	1	–1	–0.5	0.5	0.05	–0.05	A
TRANSISTOR DISSIPATION:	P_T									
At case temperatures up to 25°C		5	7	10	10	5	5	5	7	W
At case temperatures above 25°C		← See Fig. 1 →								
TEMPERATURE RANGE:										
Storage & Operating (Junction)		← –65 to +200 →								°C
PIN TEMPERATURE (During Soldering):										
At distances ≥ 1/32 in. (0.8 mm) from case for 10 s max.		← 230 →								°C

•R_{BE} = 10 Ω

▲R_{BE} = 300 Ω

MAXIMUM RATINGS, *Absolute-Maximum Values:*		RCA1A09	RCA1A10	RCA1A11	RCA1A15	RCA1A16	RCA1A17	RCA1A18	RCA1A19	
COLLECTOR-TO-EMITTER VOLTAGE:										
With base open	V_{CEO}	175	–175	175	100	–100	90	10	–10	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	6	–6	6	5	–5	4	4	–4	V
COLLECTOR CURRENT	I_C	1	–1	1	1	–1	1	1	–1	A
BASE CURRENT	I_B	0.5	–0.5	0.5	0.5	–0.1	0.5	0.5	–0.5	A
TRANSISTOR DISSIPATION:	P_T									
At case temperatures up to 25°C		10	10	10	10	10	5	7	7	W
At case temperatures above 25°C		← See Fig. 1 →								
TEMPERATURE RANGE:										
Storage & Operating (Junction)		← –65 to +200 →								°C
PIN TEMPERATURE (During Soldering):										
At distances ≥ 1/32 in. (0.8 mm) from case for 10 s max.		← 230 →								°C

Type RCA1A01
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 60 V, I_B = 0	–	1	µA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 100 mA	70	–	V
Gain Bandwidth Product	f_T	V_{CE} = 4 V, I_C = 50 mA	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 mA, V_{CE} = 4 V	40	200	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 150 mA, I_B = 15 mA	–	1.4	V
Base-to-Emitter Voltage	V_{BE}	I_C = 10 mA, V_{CE} = 4 V	–	1	V

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

Type RCA1A02
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = –40 V, I_B = 0	–	–1	µA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –4 V, I_C = 0	–	–1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = –0.1 A	–50	–	V
Gain Bandwidth Product	f_T	V_{CE} = –4 V, I_C = –50 mA	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –0.1 mA, V_{CE} = –10 V	30	200	
Base-to-Emitter Voltage	V_{BE}	I_C = –0.1 mA, V_{CE} = –10 V	–	–0.8	V

For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).

Type RCA1A03
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 85 V, R_{BE} = 100Ω	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	0.1	mA
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = 0.1 A, R_{BE} = 100Ω	95	–	V
Gain Bandwidth Product	f_T	I_C = 0.1 A, V_{CE} = 4 V	50	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 300 mA, V_{CE} = 4 V	70	300	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 300 mA, I_B = 30 mA	–	0.8	V
Base-to-Emitter Voltage	V_{BE}	I_C = 300 mA, V_{CE} = 4 V	–	1.4	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 50 V, t = 0.4 s	0.2	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N5320 (File 325).

Type RCA1A04
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial-planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = –85 V, R_{BE} = 100Ω	–	–10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	–0.1	mA
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = –0.1 A, R_{BE} = 100Ω	–95	–	V
Gain Bandwidth Product	f_T	I_C = –0.1 A, V_{CE} = –4 V	50	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –300 mA, V_{CE} = –4 V	70	300	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = –300 mA, I_B = –30 mA	–	–0.8	V
Base-to-Emitter Voltage	V_{BE}	I_C = –300 mA, V_{CE} = –4 V	–	–1.4	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = –35 V, t = 0.4 s	-0.285	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N5322 (File 325).

Type RCA1A05
Package: JEDEC TO-39
Construction: Silicon p-n-p epitaxial planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	$V_{CE} = -65$ V, $R_{BE} = 100\Omega$	–	–10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	$V_{EB} = -4$ V, $I_C = 0$	–	–0.1	mA
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	$I_C = -0.1$ A, $R_{BE} = 100\Omega$	–75	–	V
Gain Bandwidth Product	f_T	$I_C = -50$ mA, $V_{CE} = -4$ V	60		MHz
DC Forward-Current Transfer Ratio	h_{FE}	$I_C = -150$ mA, $V_{CE} = -4$ V	50	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	$I_C = -150$ mA, $I_B = -15$ mA	–	–0.8	V
Base-to-Emitter Voltage	V_{BE}	$I_C = -150$ mA, $V_{CE} = -4$ V	–	–1.4	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	$V_{CE} = -65$ V, t = 0.4 s	–0.1	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).

Type RCA1A06
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 65V, $R_{BE} = 100\Omega$	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4V, $I_C = 0$	–	0.1	mA
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = 100 mA, $R_{BE} = 100\Omega$	75	–	V
Gain Bandwidth Product	f_T	I_C = 50 mA, V_{CE} = 4 V	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 150 mA, V_{CE} = 4V	50	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 150 mA, I_B = 15 mA	–	0.8	V
Base-to-Emitter Voltage	V_{BE}	I_C = 150 mA, V_{CE} = 4V	–	1.4	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 65V, t = 0.4 s	0.077	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

Type RCA1A07
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 40 V	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 3 V, I_C = 0	–	0.1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 100 mA	40	–	V
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = 100 mA, R_{BE} = 10Ω	50	–	V
Gain Bandwidth Product	f_T	V_{CE} = 10 V, I_C = 50 mA	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 3 mA, V_{CE} = 10 V	50	250	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C = 20 mA, I_B = 1 mA	–	1	V
Base-to-Emitter Saturation Voltage	V_{BE}(sat)	I_C = 20 mA, I_B = 1 mA	–	1.3	V

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

Type RCA1A08
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With external base-to-emitter-resistance	I_{CER}	V_{CE} = –40 V, R_{BE} = 330Ω	–	–10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –5 V	–	–0.1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = –100 mA, I_B = 0	–40	–	V
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = –100 mA, R_{BE} = 330Ω	–50	–	V
Gain Bandwidth Product	f_T	V_{CE} = –10 V, I_C = –50 mA	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –50 mA, V_{CE} = –1.5 V	70	250	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C = –100 mA, I_B = –5 mA	–	–1.4	V
Base-to-Emitter Saturation Voltage	V_{BE}(sat)	I_C = –100 mA, I_B = –5 mA	–	–1.4	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = –35 V, t = 0.05 s	–0.12	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).

Type RCA1A09
Package: JEDEC TO-39
Construction: Silicon n-p-n, epitaxial

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 90 V, I_B = 0	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 6 V, I_C = 0	–	100	μA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 10 mA, I_B = 0	175	–	V
Gain Bandwidth Product	f_T	I_C = 10 mA, V_{CE} = 10 V	15	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 mA, V_{CE} = 10 V	20	100	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 50 mA, I_B = 4 mA	–	0.5	V
Base-to-Emitter Voltage	V_{BE}	I_C = 10 mA, V_{CE} = 10 V	–	0.9	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 150 V, t = 1 s	0.065	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N3439 (File 64).

Type RCA1A10
Package: JEDEC TO-39
Construction: Silicon p-n-p,

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = –120 V, I_B = 0	–	–10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –6 V, I_C = 0	–	–100	μA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = –10 mA, I_B = 0	–175	–	V
Gain Bandwidth Product	f_T	I_C = –10 mA, V_{CE} = –10 V	15	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –10 mA, V_{CE} = –10 V	40	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = –10 mA, I_B = –1 mA	–	–2	V
Base-to-Emitter Voltage	V_{BE}	I_C = –10 mA, V_{CE} = –10 V	–	–0.8	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = –150 V, t = 1 s	–0.04	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N5415 (File 336).

Type RCA1A11
Package: JEDEC TO-39
Construction: Silicon n-p-n, epitaxial

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 90 V, I_B = 0	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 6 V, I_C = 0	–	100	μA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 10 mA, I_B = 0	175	–	V
Gain Bandwidth Product	f_T	I_C = 10 mA, V_{CE} = 10 V	15	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 1 mA, V_{CE} = 10 V	40	250	
Base-to-Emitter Voltage	V_{BE}	I_C = 1 mA, V_{CE} = 10 V	0.5	0.7	V

For characteristics curves and test conditions, refer to published data for prototype 2N3439 (File 64).

Type RCA1A15
Package: JEDEC TO-39
Construction: Silicon n-p-n, epitaxial

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 90 V	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 5 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 10 mA, I_B = 0	100	–	V
Gain Bandwidth Product	f_T	V_{CE} = 10 V, I_C = 10 mA	15	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 mA, V_{CE} = 10 V	20	100	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 10 mA, I_B = 1 mA	–	1	V
Base-to-Emitter Voltage	V_{BE}	I_C = 10 mA, V_{CE} = 10 V	–	1	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 50 V, t = 0.4 s	0.2	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N3440 (File 64).

Type RCA1A16
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = –90 V	–	–10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –5 V, I_C = 0	–	–1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = –10 mA, I_B = 0	–100	–	V
Gain Bandwidth Product	f_T	V_{CE} = –10 V, I_C = –10 mA	15	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –10 mA, V_{CE} = –10 V	40	250	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C = –10 mA, I_B = –1 mA	–	–1	V
Base-to-Emitter Voltage	V_{BE}	I_C = –10 mA, V_{CE} = –10 V	–	–1	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = –50 V, t = 0.4 s	–0.2	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N5416 (File 336).

Type RCA1A17
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 80 V, I_B = 0	–	1	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 100 mA, I_B = 0	90	–	V
Gain Bandwidth Product	f_T	V_{CE} = 4 V, I_C = 50 mA	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 mA, V_{CE} = 4V	40	200	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C = 150 mA, I_B = 15 mA	–	1.4	V
Base-to-Emitter Voltage	V_{BE}	I_C = 10 mA, V_{CE} = 4 V	–	1	V

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

Type RCA1A18
Package: JEDEC TO-39
Construction: Silicon n-p-n, planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = 5 V, I_B = 0	–	10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 4 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 10 mA, I_B = 0	10	–	V
Gain Bandwidth Product	f_T	I_C = 50 mA, V_{CE} = 4 V	120	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 10 mA, V_{CE} = 4 V	40	250	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C = 10 mA, I_B = 0.5 mA	–	1	V
Base-to-Emitter Voltage	V_{BE}	I_C = 10 mA, V_{CE} = 4 V	–	0.78	V

For characteristics curves and test conditions, refer to published data for prototype 2N2102 (File 106).

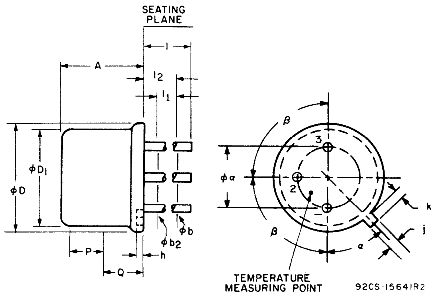
Type RCA1A19
Package: JEDEC TO-39
Construction: Silicon p-n-p, epitaxial planar

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With base open	I_{CEO}	V_{CE} = –5 V, I_B = 0	–	–10	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –4 V, I_C = 0	–	–1	mA
Collector-to-Emitter Voltage With base open	V_{CEO}	I_C = –10 mA, I_B = 0	–10	–	V
Gain Bandwidth Product	f_T	I_C = –50 mA, V_{CE} = –4 V	60	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –10 mA, V_{CE} = –4 V	40	250	
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C = –10 mA, I_B = –0.5 mA	–	–1	V
Base-to-Emitter Voltage	V_{BE}	I_C = –10 mA, V_{CE} = –4 V	–	–0.78	V

For characteristics curves and test conditions, refer to published data for prototype 2N4036 (File 216).

DIMENSIONAL OUTLINE FOR ALL TYPES JEDEC TO-39



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
ϕa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
ϕb	0.016	0.021	0.406	0.533	2
ϕb2	0.016	0.019	0.406	0.483	2
ϕD	0.350	0.370	8.89	9.40	
ϕD1	0.315	0.335	8.00	8.51	
h	0.009	0.125	0.229	3.18	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
l	0.500		12.70		2
l1		0.050		1.27	2
l2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads) $\phi\ b_2$ applies between l_1 and l_2. ϕb applies between l_2 and 0.5 in. (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond 0.5 in. (12.70 mm) from seating plane.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

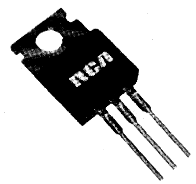
TERMINAL CONNECTIONS

Lead 1 – Emitter
Lead 2 – Base
Lead 3 – Collector, Case

Solid State Division

Power Transistors

RCA1C03 RCA1C12
RCA1C04 RCA1C13



JEDEC TO-220AB H-1535R1

Silicon Transistors for Audio-Frequency Linear-Amplifier Applications

N-P-N	and	P-N-P Complementary Types
RCA1C03		RCA1C04
RCA1C12		RCA1C13

RCA1C03, RCA1C04, RCA1C12, and RCA1C13 are complementary silicon n-p-n and p-n-p transistors especially characterized for audio-amplifier applications. These devices, singly or in pairs in complementary- or quasi-complementary-symmetry circuits, are particularly useful as drivers or pre-drivers. They may also be used in audio power amplifiers, linear modulators, servo amplifiers, and operational amplifiers. The units are supplied in the JEDEC TO-220AB version of the plastic VERSAWATT package.

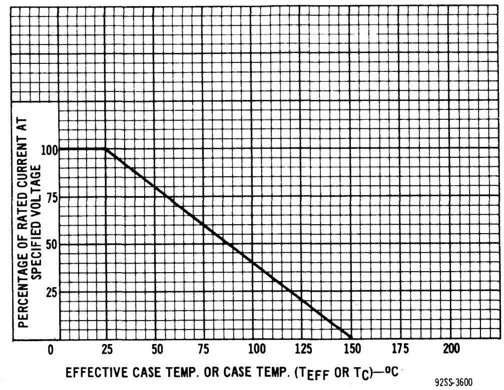


Fig. 1— Derating curve for all types.

MAXIMUM RATINGS, *Absolute-Maximum Values:*		RCA1C03	RCA1C04	RCA1C12	RCA1C13	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	120	−120	140	−140	V
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:						
With base open	V_{CEO}	100	−100	120	−120	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}	120	−120	140	−140	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	−5	5	−5	V
CONTINUOUS COLLECTOR CURRENT	I_C	4	−4	4	−4	A
CONTINUOUS BASE CURRENT	I_B	2	−2	2	−2	A
TRANSISTOR DISSIPATION:	P_T					
At case temperatures up to 25°C		40	40	40	40	W
At case temperatures above 25°C		← See Fig. 1 →				
TEMPERATURE RANGE:						
Storage and Operating (Junction)		← −65 to +150 →				°C
PIN TEMPERATURE (During Soldering):						
At distances ≥ 1/32 in. (0.8 mm) from seating plane for 10 s max.		← 230 →				°C

Type RCA1C03
Package: JEDEC TO-220AB
Construction: Silicon n-p-n, epitaxial

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 110 V, R_{BE} = 100Ω	–	1	mA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 5 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 0.1 A, I_B = 0	100	–	V
Gain Bandwidth Product	f_T	I_C = 0.5 A, V_{CE} = 4 V	4	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 1 A, V_{CE} = 4 V	50	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 1 A, I_B = 0.1 A	–	1	V
Base-to-Emitter Voltage	V_{BE}	I_C = 1 A, V_{CE} = 4 V	–	1.5	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 40 V, t = 0.4 s	1	–	A

For characteristics curves and test conditions, refer to published data for prototype 2N6293 (File 542).

Type RCA1C04
Package: JEDEC TO-220AB
Construction: Silicon p-n-p, epitaxial

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = –110 V, R_{BE} = 100Ω	–	–1	mA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –5 V, I_C = 0	–	–1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = –0.1 A, I_B = 0	–100	–	V
Gain Bandwidth Product	f_T	I_C = –0.5 A, V_{CE} = –4 V	10	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –1 A, V_{CE} = –4 V	50	250	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = –1 A, I_B = –0.1 A	–	–1	V
Base-to-Emitter Voltage	V_{BE}	I_C = –1 A, V_{CE} = –4 V	–	–1.5	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = –40 V, t = 0.4 s	–1	–	A

Type RCA1C12
Package: JEDEC TO-220AB
Construction: Silicon n-p-n, epitaxial

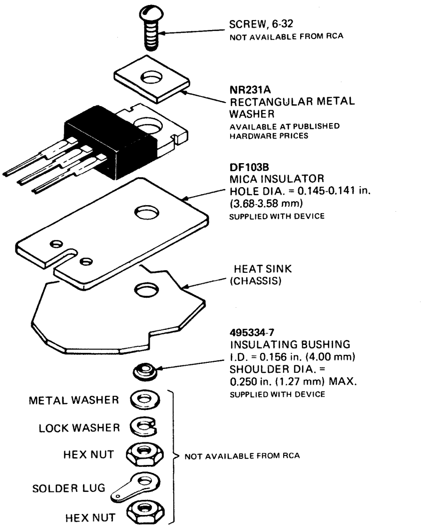
ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 90 V, R_{BE} = 100 Ω	–	100	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 5 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 0.1 A, I_B = 0	120	–	V
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = 0.1 A, R_{BE} = 100 Ω	140	–	V
Gain Bandwidth Product	f_T	I_C = 0.5 A, V_{CE} = 4 V	4	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 1 A, V_{CE} = 2 V	40	250	
Base-to-Emitter Voltage	V_{BE}	I_C = 1 A, V_{CE} = 2 V	–	1.2	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 60 V, t = 0.4 s	0.66	–	A

Type RCA1C13
Package: JEDEC TO-220AB
Construction: Silicon p-n-p, epitaxial

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = –90 V, R_{BE} = 100 Ω	–	–100	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –5 V, I_C = 0	–	–1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = –0.1 A, I_B = 0	–120	–	V
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = –0.1 A, R_{BE} = 100 Ω	–140	–	V
Gain Bandwidth Product	f_T	I_C = –0.5 A, V_{CE} = –4 V	10	–	MHz
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –1 A, V_{CE} = –2 V	40	250	
Base-to-Emitter Voltage	V_{BE}	I_C = –1 A, V_{CE} = –2 V	–	–1.2	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = –60 V, t = 0.4 s	–0.66	–	A

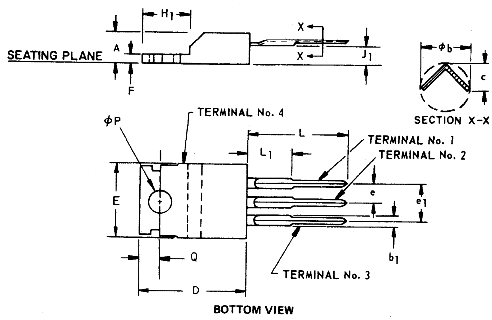


In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

92CS-22563

Fig. 2— Suggested mounting hardware for JEDEC TO-220AB.

DIMENSIONAL OUTLINE FOR ALL TYPES JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:

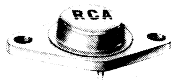
1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS

Lead 1 – Base
Lead 2 – Collector
Lead 3 – Emitter
Lead 4 – Collector

RCA Solid State Division

Power Transistors
RCA1E02
RCA1E03



JEDEC TO-66 H-1340

Silicon Transistors for Audio-Frequency Linear-Amplifier Applications

N-P-N	P-N-P
RCA1E02	RCA1E03

RCA1E02 and RCA1E03 are silicon n-p-n and p-n-p transistors, respectively. These complementary devices are especially characterized for audio-amplifier applications. They may be used singly or as a complementary pair in complementary- or quasi-complementary-symmetry circuits, and are particularly useful as drivers or predrivers. They may also be used in audio power amplifiers, linear modulators, servo amplifiers, and operational amplifiers. The units are supplied in the JEDEC TO-66 package.

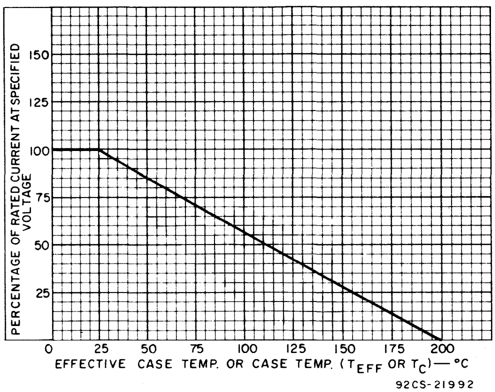


Fig.1 – Derating curve for all types.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		RCA1E02	RCA1E03	
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	200	−200	V
COLLECTOR-TO-EMITTER VOLTAGE:				
With base open	V_{CEO}	175	−175	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}	200	−200	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	−5	V
COLLECTOR CURRENT	I_C	2	−2	A
BASE CURRENT	I_B	1	−1	A
TRANSISTOR DISSIPATION:	P_T			
At case temperatures up to 25°C		35	35	W
At case temperatures above 25°C		← See Fig.1 →		
TEMPERATURE RANGE:				
Storage and Operating (Junction)		← −65 to +200 →		°C
PIN TEMPERATURE (During Soldering):				
At distances ≥ 1/32 in. (0.8 mm) from case for 10 s max.		← 230 →		°C

Type RCA1E02
Package: JEDEC TO-66
Construction: Silicon n-p-n, double-epitaxial

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25^{o}C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = 120 V, R_{BE} = 100 Ω	–	100	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = 5 V, I_C = 0	–	1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = 0.1 A, I_B = 0	175	–	V
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = 0.1 A, R_{BE} = 100 Ω	200	–	V
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 0.3 A, V_{CE} = 2 V	30	150	
Base-to-Emitter Voltage	V_{BE}	I_C = 0.3 A, V_{CE} = 2 V	–	1	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = 80 V, t = 0.4 s	0.4	–	A

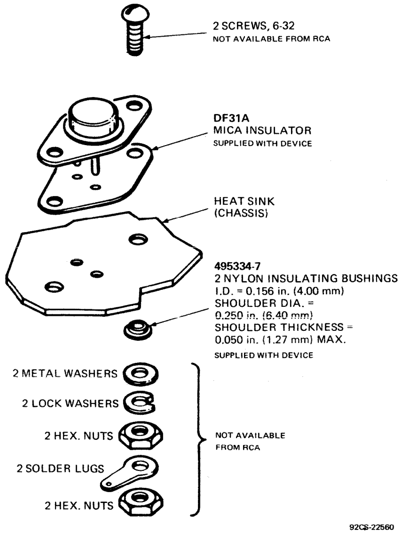
For characteristics curves and test conditions, refer to published data for prototype 2N3583 (File 138).

Type RCA1E03
Package: JEDEC TO-66
Construction: Silicon p-n-p

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25^{o}C Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Collector Cutoff Current: With external base-to-emitter resistance (R_{BE})	I_{CER}	V_{CE} = –120 V, R_{BE} = 100 Ω	–	–100	μA
Emitter Cutoff Current: With collector open	I_{EBO}	V_{EB} = –5 V, I_C = 0	–	–1	mA
Collector-to-Emitter Voltage: With base open	V_{CEO}	I_C = –0.1 A, I_B = 0	–175	–	V
Collector-to-Emitter Voltage: With external base-to-emitter resistance (R_{BE})	V_{CER}	I_C = –0.1 A, R_{BE} = 100 Ω	–200	–	V
DC Forward-Current Transfer Ratio	h_{FE}	I_C = –0.3 A, V_{CE} = –2 V	30	150	
Base-to-Emitter Voltage	V_{BE}	I_C = –0.3 A, V_{CE} = –2 V	–	–1	V
Second-Breakdown Collector Current: With base forward biased	$I_{S/b}$	V_{CE} = –80 V, t = 0.4 s	–0.25	–	A

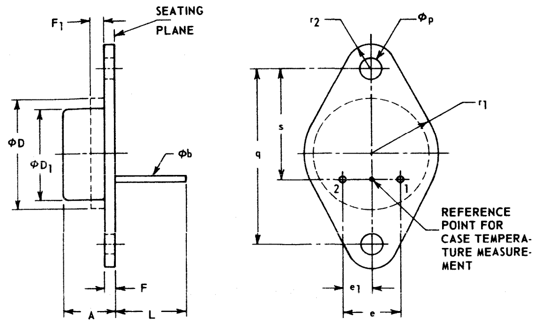
For characteristics curves and test conditions, refer to published data for prototype 2N6211 (File 507).



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.2 — Suggested mounting hardware for JEDEC TO-66.

DIMENSIONAL OUTLINE FOR BOTH TYPES JEDEC TO-66



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	0.250	0.340	6.35	8.64	
ϕb	0.028	0.034	0.711	0.863	
ϕD		0.620		15.75	
ϕD_1	0.470	0.500	11.94	12.70	
e	0.190	0.210	4.83	5.33	
e_1	0.093	0.107	2.36	2.72	
F	0.050	0.075	1.27	1.91	2
F_1		0.050		1.27	1
L	0.360		9.14		
ϕp	0.142	0.152	3.61	3.86	
q	0.958	0.962	24.33	24.43	
r_1		0.350		8.89	
r_2		0.145		3.68	
s	0.570	0.590	14.48	14.99	

NOTES:

1. The outline contour is optional within zone defined by ϕD and F_1.
2. Dimensions does not include sealing flanges.

92SS-3738

TERMINAL CONNECTIONS

Pin 1 - Base

Pin 2 - Emitter

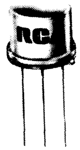
Mounting Flange, Case - Collector

RCA
Solid State
Division

Power Transistors

40309—40328
40360—40364

B



JEDEC TO-39
See Note at
right

H-1381

C

JEDEC TO-66
H-1340

A

JEDEC TO-3
H-1570

N-P-N and P-N-P Silicon Power Transistors

For Audio-Frequency Amplifier Applications

Features:

- **Hermetically-sealed packages**
- **Operation at case temperatures up to 257°F**
- **Pellet bonded to header — for greater power-handling capability for greater shock resistance**
- **Freedom from second breakdown**

NOTE:

These devices are generally available with ½-inch leads (TO-39 package). They are also available in the U.S.A., Canada, Latin America, and Far East with 1½-inch leads (TO-5 package); the shorter-lead versions are specified by a suffix letter "S" after the type number, and the longer-lead versions by a suffix letter "L".

RCA transistors 40309—40328 and 40360—40364 are diffused-junction silicon n-p-n and p-n-p transistors intended for specific applications in audio amplifiers, giving high-quality performance economically. These types cover applications from low-level input stages to high-power output stages of 5 to 50 watts. Supply voltages range from the nominal 12-volt vehicular type to 117-volt ac-dc type. The use of all-silicon devices permits more flexibility in the mechanical and electrical design of amplifiers since the output heat sinks can be held to a minimum.

40325
40363

JEDEC TO-3 PACKAGE
See page 4 for electrical characteristics

40309 40311 40314 40315 40317
40319 40320 40321 40323 40326
40327 40360 40361 40362

JEDEC TO-5 OR TO-39 PACKAGE
See page 2 for electrical characteristics

40310 40312 40313 40316 40318
40322 40324 40328 40364

JEDEC TO-66 PACKAGE
See page 3 for electrical characteristics

MAXIMUM RATINGS (Absolute-Maximum Values)

CHARACTERISTIC	40325	40363	40309	40323	40311	40315	40314	40317	40319	40320	40326	40321	40327	40360	40361	40362	40310	40324	40316	40312	40313	40318	40322	40328	40364	UNITS
V_{CEO}(sus)	35	–	18	18	30	35	40	40	-40	40	40	–	–	70	–	–	35	35	–	–	–	–	–	–	–	V
V_{CER}(sus)*	–	70	–	–	–	–	–	–	–	–	–	300	300	–	70	-70	–	–	40	60	300	300	300	300	60	V
V_{CEV}**	35	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	V
V_{EBO}	5	4	2.5	2.5	2.5	2.5	2.5	2.5	-2.5	2.5	2.5	5	5	4	4	-4	2.5	2.5	5	2.5	2.5	6	6	6	4	V
V_{CBO}	35	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	V
I_C	15	15	0.7	0.7	0.7	0.7	0.7	0.7	-0.7	0.7	0.7	1	1	0.7	0.7	-0.7	4	4	4	4	2	2	2	2	7	A
I_B	7	7	0.2	0.2	0.2	0.2	0.2	0.2	-0.2	0.2	0.2	0.5	0.5	0.2	0.2	-0.2	2	2	2	2	1	1	1	1	5	A
P_T***																										
T_C up to 25°C	117	115	5	5	5	5	5	5	5	5	5	5	5	5	5	5	29	29	29	29	35	35	35	35	35	W
T_{FA} up to 25°C	–	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	–	–	–	–	–	–	–	–	–	W
T_C of 175°C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	5	5	5	5	–	W
TEMP. RANGE: Oper. Junction	← -65 to 200°C →																									°C

*R_{BE} = 500 Ω
R_{BE} = 1,000 Ω for 40327
R_{BE} = 200 Ω for 40361, 40362, & 40363
R_{BE} = 150 Ω for 40364

**V_{BE} = -1.5V

*** At other temperatures see derating curves

ELECTRICAL CHARACTERISTICS *For RCA–40309, 40311, 40314, 40315, 40317, 40319, 40320, 40321, 40323, 40326, 40327, 40360, 40361, and 40362*

CHARACTERISTIC	TEST CONDITIONS V_{CB} (Volts)	V_{CE} (Volts)	V_{EB} (Volts)	I_C (mA)	T_C (°C)	LIMITS 40309	40311	40314	40315	40317	40319	40320	40321	40323	40326	40327	40360	40361	40362
I_{CEO}		60			25												1 μA (Max.)		
		60			150												250 μA (Max.)		
I_{CBO}	15				25	0.25 μA (Max.)	0.25 μA (Max.)	0.25 μA (Max.)	0.25 μA (Max.)	0.25 μA (Max.)		0.25 μA (Max.)		0.25 μA (Max.)	0.25 μA (Max.)				
	-15				25						-0.25 μA (Max.)								
	15				150	1 mA (Max.)	1 mA (Max.)	1 mA (Max.)	1 mA (Max.)	1 mA (Max.)		1 mA (Max.)		1 mA (Max.)	1 mA (Max.)				
	-15				150						-1 mA (Max.)								
	150				150								100 μA (Max.)			100 μA (Max.)			
I_{CER}■		150											5 μA (Max.)			5 μA (Max.)			
		60†			25													1 μA (Max.)	-1 μA (Max.)
		60†			150													100 μA (Max.)	-100 μA (Max.)
I_{EBO}			2.5			1 mA (Max.)	1 mA (Max.)	1 mA (Max.)	1 mA (Max.)	1 mA (Max.)		1 mA (Max.)		1 mA (Max.)	1 mA (Max.)				
			-2.5								-1 mA (Max.)								
			5										100 μA (Max.)			100 μA (Max.)			
			4†														1 mA (Max.)	1 mA (Max.)	-1 mA (Max.)
V_{CEO} (sus)				100*		18 V● (Min.)	30 V (Min.)	40 V (Min.)	35 V● (Min.)	40 V (Min.)		40 V (Min.)		18 V● (Min.)	40 V (Min.)		70 V (Min.)		
				-100*							-40 V♦ (Min.)								
V_{BE}		4		50		1 V (Max.)	1 V (Max.)	1 V (Max.)	1 V (Max.)					1 V (Max.)				1 V (Max.)	
		4		10						1 V (Max.)		1 V (Max.)			1 V (Max.)		1 V (Max.)		
		-4		-50							-1.0 V (Max.)								-1 V (Max.)
		10		50									2 V (Max.)			2 V (Max.)			
V_{CE} (sat)				150♦				1.4 V (Max.)			-1.4 V (Max.)						1.4V (Max.)	1.4V (Max.)	-1.4V (Max.)
V_{CER} (sus)■				50									300 V (Min.)			300 V (Min.)			
				100														70 V (Min.)	-70 V (Min.)
h_{FE}		4		50		70-350	70-350	70-350	70-350					70-350				70-350	
		-4		50							35-200								35-200
		4		10						40-200		40-200			40-200		40-200		
		10		20									25-200			40-250			
θ_{J-C}						35°C/W (Max.)	35°C/W (Max.)	35°C/W (Max.)	35°C/W (Max.)	35°C/W (Max.)	35°C/W (Max.)	35°C/W (Max.)	30°C/W (Max.)	35°C/W (Max.)	30°C/W (Max.)	30°C/W (Max.)	35°C/W (Max.)	35°C/W (Max.)	35°C/W (Max.)
θ_{J-FA}						175°C/W (Max.)	175°C/W (Max.)	175°C/W (Max.)	175°C/W (Max.)	175°C/W (Max.)	175°C/W (Max.)			175°C/W (Max.)			175°C/W (Max.)	175°C/W (Max.)	175°C/W (Max.)
f_T		10		50		100 Mc/s (Typ.)	100 Mc/s (Typ.)		100 Mc/s (Typ.)					100 Mc/s (Typ.)					
		-4		-50							100 Mc/s (Typ.)								100 Mc/s (Typ.)
		4		50				100 Mc/s (Typ.)									100 Mc/s (Typ.)	100 Mc/s (Typ.)	

* Pulsed; pulse duration = 300 μsec, duty factor ≤ 2%

♦ I_B = 15 mA

■ R_{BE} = 1,000 ohms

● BV_{CEO} value

R_{BE} = 200 Ω for 40361 & 40362

† Negative value for 40362

ELECTRICAL CHARACTERISTICS *For RCA–40310, 40312, 40313, 40316, 40318, 40322, 40324, 40328, and 40364*

CHARACTERISTIC	CONDITIONS					LIMITS								
	V_{CB}	V_{CE}	V_{EB}	I_C	T_C	40310	40312	40313	40316	40318	40322	40324	40328	40364
	Volts				°C									
I_{CEO}		150						5 mA (Max.)		5 mA (Max.)			5 mA (Max.)	
I_{CEV}		300	1.5⊕		25			10 mA (Max.)						
		300	1.5⊕		150			10 mA (Max.)						
		150	1.5⊕		150					10 mA (Max.)			10 mA (Max.)	
		150	1.5⊕		25					5 mA (Max.)			10 mA (Max.)	
I_{CER}▲		50			25									0.5 mA (Max.)
		50			150									2 mA (Max.)
I_{CBO}	15				25	10 μA (Max.)	10 μA (Max.)		10 μA			10 μA (Max.)		
	15				150	5 mA (Max.)	5 mA (Max.)		5 mA (Max.)			5 mA (Max.)		
I_{EBO}			2.5			5 mA (Max.)	5 mA (Max.)	5 mA (Max.)				5 mA (Max.)		
			5						5 mA (Max.)					
			6							5 mA (Max.)	5 mA (Max.)		5 mA (Max.)	
			4											5 mA (Max.)
V_{CEO} (sus)				100* mA		35 V● (Min.)						35 V● (Min.)		
V_{BE}		2		1 A		1.4 V (Max.)	1.4 V (Max.)		1.4 V (Max.)			1.4 V (Max.)		
		10		100 mA				1.5 V (Max.)						
		10		500 mA						1.5 V (Max.)				
		10		1 A									1.5 V (Max.)	
		5		2.5 A										1.8 V (Max.)
V_{CE} (sat)				2.5 A										2 V□ (Max.)
V_{CER} (sus)				100* mA			60 V (Min.)		40 V (Min.)					
				200 mA				300 V◆ (Min.)		300 V◆ (Min.)	300 V◆ (Min.)		300 V● (Min.)	70 V▲ (Min.)
h_{FE}		2		1 A		20-120	20-120		20-120			20-120		
		5		0.5 A										35-175
		5		2.5 A										20 (Min.)
		10		100 mA				40-250						
		10		500 mA				40 (Min.)		50 (Min.)	75 (Min.)			
		10		20 mA						40 (Min.)	40 (Min.)		40 (Min.)	
		10		1 A									20 (Min.)	
f_T		4		500 mA		750kc/s (Typ.)	750kc/s (Typ.)		750kc/s (Typ.)			750kc/s (Typ.)		
		10		2.5 A										15Mc/s (Typ.)
$I_{S/b}$#		150						150 mA (Min.)		100 mA# (Min.)	100 mA (Min.)		100 mA (Min.)	
		40												750 mA (Min.)
$E_{S/b}$■			4							50 μJ (Min.)	50 μJ (Min.)			
θ_{J-C}						6°C/W (Max.)	6°C/W (Max.)	5°C/W (Max.)	6°C/W (Max.)	5°C/W (Max.)	5°C/W (Max.)	6°C/W (Max.)	5°C/W (Max.)	5°C/W (Max.)

* Pulsed; Pulse duration = 300 μsec, duty factor 2%. ⊕R_{BE} value ◆ R_{BE} = 200 Ω, L = 5 mH

$I_{S/b}$ is defined as the current at which second breakdown occurs at a specified collector voltage with the emitter-base junction forward biased

■ $E_{S/b}$ is defined as the energy at which second breakdown occurs under specified reverse bias conditions. $E_{S/b} = \frac{1}{2}LI^2$, where L is a series load or leakage inductance and I is the peak collector current. R_{BE} = 20 ohms & L = 100 μh.

▲ R_{BE} = 150 Ω □ I_B = 0.25 A ● BV_{CEO} value.

ELECTRICAL CHARACTERISTICS *For RCA-40325 and 40363*

CHARACTERISTIC	TEST CONDITIONS					LIMITS	
	V_{CB}	V_{CE}	V_{EB}	I_C	T_C	40325	40363
	Volts			mA	°C		
I_{CBO}	30				25	5 mA (Max.)	
	30				150	10 mA (Max.)	
I_{CER}▲		60			25		1 mA (Max.)
		60			150		10 mA (Max.)
I_{EBO}			5			10 mA (Max.)	
			4				5 mA (Max.)
$BV_{CEO}(sus)$				200		35 V (Min.)	
$V_{CER}(sus)$▲				200			70 V (Min.)
BV_{CBO}				100		35 V (Min.)	
V_{BE}		4		8 A		2 V (Max.)	
		4		4 A			1.8 V (Max.)
$V_{CE}(sat)$				8 A*		1.5 V (Max.)	
				4 A**			1.1 V (Max.)
h_{FE}		4		8 A		12-60	
		4		4 A			20-70
θ_{J-C}						1.5°C/W (Max.)	1.5°C/W (Max.)
f_T		4		3 A			700 kc/s (Typ.)

*I_B = 800 mA **I_B = 400 mA ▲R_{BE} = 200 Ω

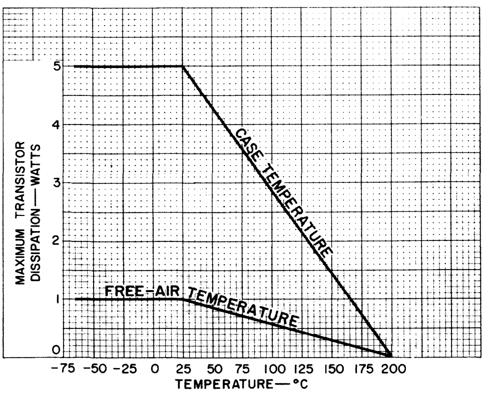


Fig.1 – Dissipation rating curves for types 40309, 40311, 40314, 40315, 40317, 40319, 40320, 40323, 40326, 40360, 40361, and 40362.

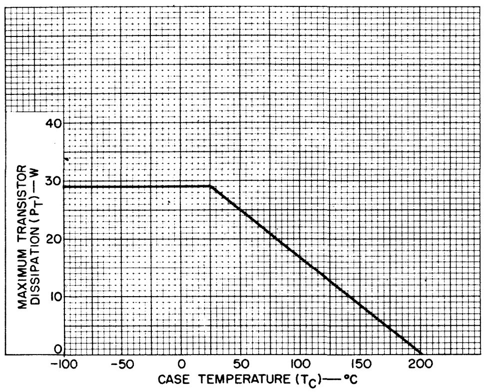


Fig.2 – Dissipation derating curve for types 40310, 40312, 40316, and 40324.

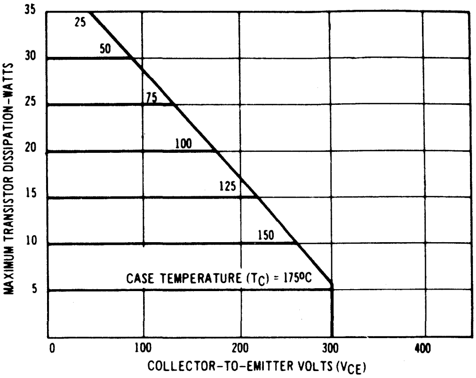


Fig.3 – Dissipation derating curve for type 40313.

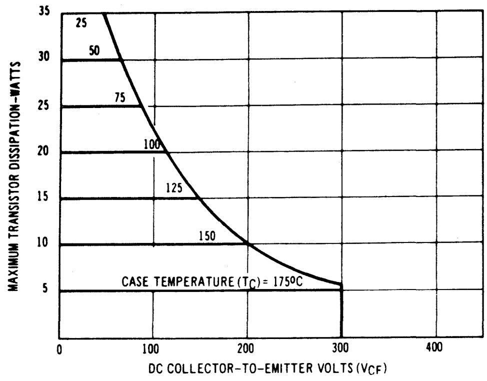


Fig.4 – Dissipation derating curve for types 40318, 40322, and 40328.

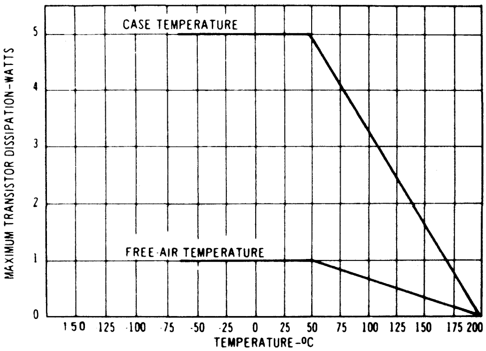


Fig.5 – Dissipation derating curves for types 40321 and 40327.

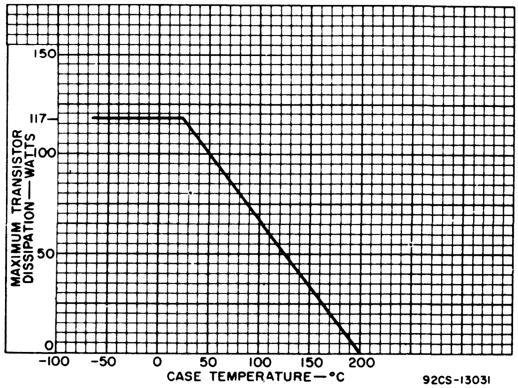


Fig.6 – Dissipation derating curve for type 40325.

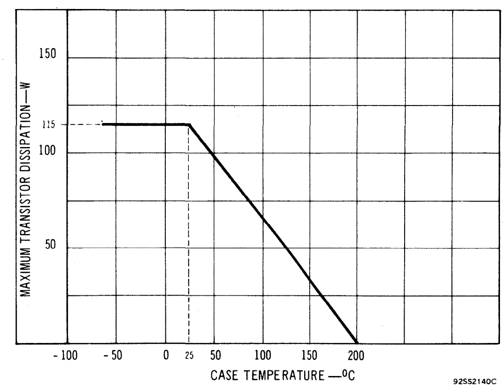


Fig.7 – Dissipation derating curve for type 40363.

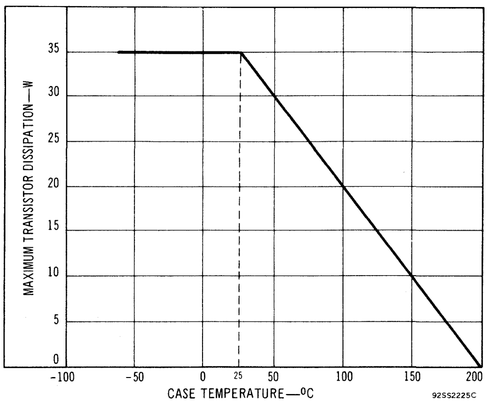
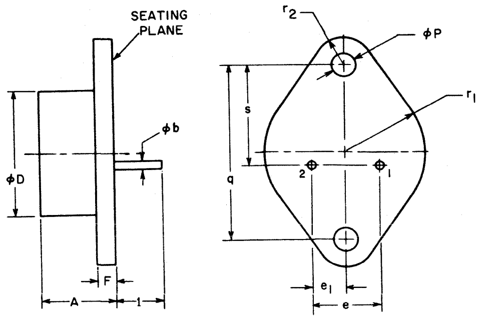


Fig.8 – Dissipation derating curve for type 40364.

DIMENSIONAL OUTLINE JEDEC TO-3 (A)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
φb	0.038	0.043	0.97	1.09	2
φD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e_1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
l	0.312		7.92		2
φP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r_1		0.525		13.34	
r_2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

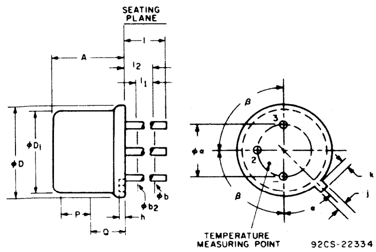
1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS–15222

TERMINAL CONNECTIONS

Pin 1 — Base
Pin 2 — Emitter
Case — Collector
Mounting Flange — Collector

DIMENSIONAL OUTLINE B (See NOTE, Page 1)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
φa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
φb	0.016	0.021	0.406	0.533	2
$φb_2$	0.016	0.019	0.406	0.483	2
φD	0.350	0.370	8.89	9.40	
$φD_1$	0.305	0.335	8.00	8.51	
h	0.009	0.041	0.229	1.04	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
L long lead	1.500		38.10		2
L short lead	0.500		12.70		2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads) $φb_2$ applies between l_1 and l_2. φb applies between l_2 and l. Diameter is uncontrolled in l_1.

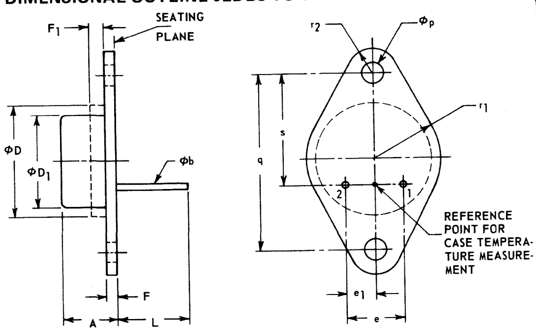
Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

TERMINAL CONNECTIONS

Lead 1 — Emitter
Lead 2 — Base
Lead 3 — Collector, case

DIMENSIONAL OUTLINE JEDEC TO-66 (C)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.340	6.35	8.64	
φb	0.028	0.034	0.711	0.863	
φD		0.620		15.75	
$φD_1$	0.470	0.500	11.94	12.70	
e	0.190	0.210	4.83	5.33	
e_1	0.093	0.107	2.36	2.72	
F	0.050	0.075	1.27	1.91	2
F_1		0.050		1.27	1
L	0.360		9.14		
φp	0.142	0.152	3.61	3.86	
q	0.958	0.962	24.33	24.43	
r_1		0.350		8.89	
r_2		0.145		3.68	
s	0.570	0.590	14.48	14.99	

NOTES:

1. The outline contour is optional within zone defined by φD and F_1.
2. Dimension does not include sealing flanges.

92SS 3738

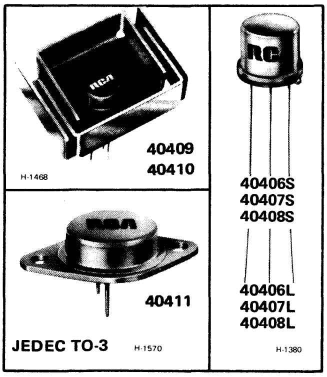
TERMINAL CONNECTIONS

Pin 1 — Base
Pin 2 — Emitter
Mounting Flange, Case-Collector

RCA
Solid State
Division

Power Transistors

40406 40408 40410
40407 40409 40411



Silicon N-P-N and P-N-P Power Transistors

For Audio-Amplifier Applications

Features:

40406 & 40407
- **$V_{CEO}(sus)$ = –50 V max. (40406)**
- **$V_{CEO}(sus)$ = 50 V max. (40407)**
- **40406 is p-n-p complement of 40407**
- **1 W dissipation rating**

These devices are generally available with ½-inch leads (TO-39 package). They are also available in the U.S.A., Canada, Latin America, and Far East with 1½-inch leads (TO-5 package); the shorter-lead versions are specified by a suffix letter "S" after the type number, and the longer-lead versions by a suffix letter "L".

RCA-40406–40411, inclusive, are diffused-junction silicon n-p-n and p-n-p transistors intended for use in audio amplifiers. Giving high-quality performance economically, these six devices have power dissipation ratings of 1 to 150 W.

40408
- **$V_{CEO}(sus)$ = 90 V max.**
- **1 W dissipation rating**

40409 & 40410
- **$V_{CER}(sus)$ = 90 V max. (40409)**
- **$V_{CER}(sus)$ = –90 V max. (40410)**
- **40410 is p-n-p complement of 40409**
- **3 W free-air dissipation rating**

40411
- **$V_{CER}(sus)$ = 90 max.**
- **Hometaxial-base construction**
- **150 W dissipation rating**

MAXIMUM RATINGS, *Absolute-Maximum Values*

		40406	40407	40408	40409	40410	40411	
Collector-to-Emitter Sustaining Voltage:								
With base open	$V_{CEO}(sus)$	–50	50	90	–	–	–	V
With R_{BE} = 100 Ω	$V_{CER}(sus)$	–	–	–	90	–90	90	V
Emitter-to-Base Voltage:								
With collector open	V_{EBO}	–4	4	4	4	–4	4	V
Collector Current	I_C	–0.7	0.7	0.7	0.7	–0.7	30	A
Base Current	I_B	–0.2	0.2	0.2	0.2	–0.2	15	A
Transistor Power Dissipation:	P_T							
At free-air temperatures up to 25° C		1	1	1	–	–	–	W
At free-air temperatures up to 50° C		–	–	–	3	3	–	W
At case temperatures up to 25° C		–	–	–	–	–	150	W
At other temperatures			See Fig. 1		See Fig. 2		See Fig. 3	
Operating Junction Temperature Range		←		–65 to +200			→	°C

ELECTRICAL CHARACTERISTICS

Characteristic	TEST CONDITIONS						LIMITS											
	V_{CB}	V_{CE}	V_{EB}	I_C	I_B	T_C	40406		40407		40408		40409		40410		40411	
	Volts			mA		°C	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
I_{CEO}		40[a]				25		-1µA		1µA								
		80				25						1µA						
		40[a]				150		-10µA		100µA								
		80				150						250µA						
I_{CER}[b]		80[a]				25								1µA		-1µA		500µA
		80[a]				150								100µA		-100µA		2 mA
I_{CBO}	10									0.25 µA								
I_{EBO}			4[a]					-1 mA		1 mA		1 mA		1 mA		-1 mA		5 mA
$V_{CEO}(sus)$				100[a]			-50 V		50 V		90 V							
$V_{CER}(sus)$[b]				100[a]									90 V		-90 V			
				200													90 V	
$V_{CE}(sat)$				150[a]	15							1.4 V		1.4 V		-1.4 V		
				4A	400													0.8 V
V_{BE}		-10		-0.1				-0.8 V										
		10		1						0.8 V								
		4		10								1V						
		4[a]		150[a]										1 V		-1 V		
		4		4 A														1.2 V
h_{FE}		-10		-0.1			30	200										
		10		1					40	200								
		4		10							40	200						
		4		150									50	250				
		-4		-150											50	250		
		4		4 A													35	100
h_{fe}[c]		10		50					6									
f_T		4[a]		50[a]			← 100 MHz (Typ) →											
		4		4 A													800 kHz (Typ)	
θ_{J-C}								35° C/W		35° C/W		35° C/W						1.17° C/W
θ_{J-FA}								175° C/W		175°C/W		175°C/W		50° C/W		50° C/W		
C_{ob}[d]	10								15 pF									
PRT[e]		40		5 A													1 sec	

[a] Negative for types 40406 & 40410
[b] $R_{BE} = 100\ \Omega$
[c] F = 20 MHz
[d] F = 1 MHz, $I_E = O$
[e] Power rating test at 200 watts

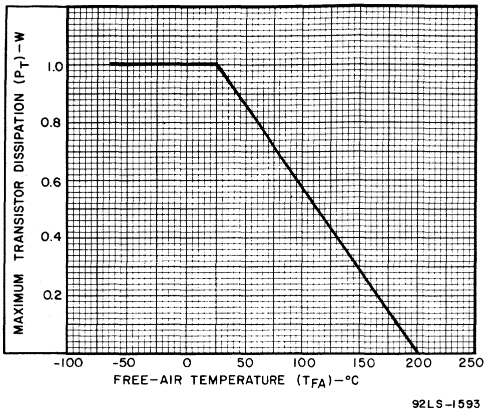


Fig. 1 — Dissipation derating curver for 40406, 40407, and 40408.

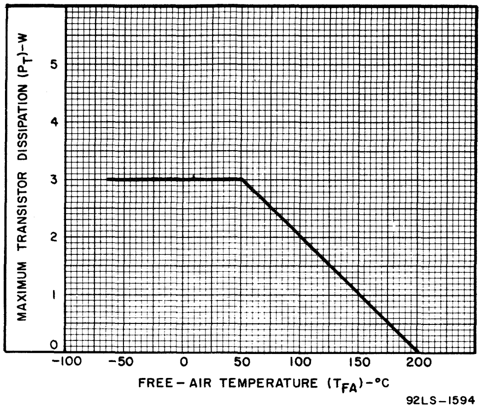


Fig. 2 — Dissipation derating curve for 40409 and 40410.

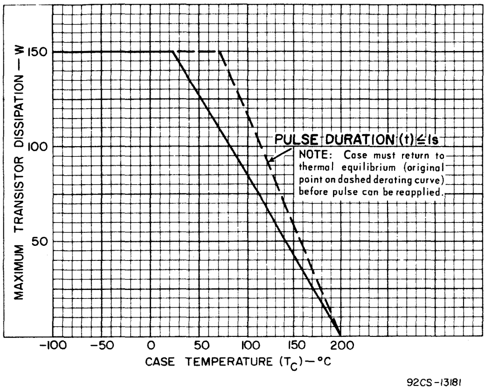


Fig. 3 — Dissipation derating curve for 40411.

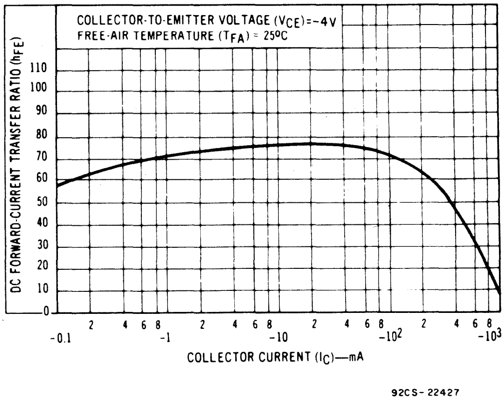


Fig. 4 — Typical dc beta characteristic for 40406 and 40410.

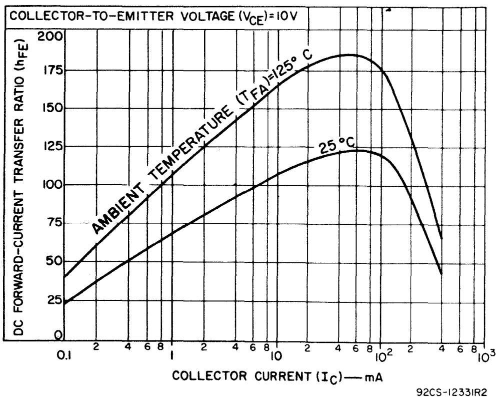


Fig. 5 — Typical dc beta characteristics for 40407, 40408, 40409.

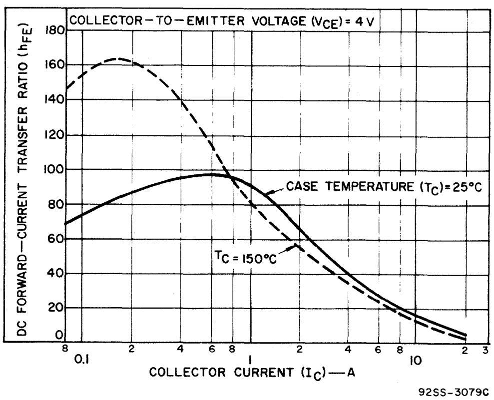


Fig. 6 — Typical dc beta characteristics for 40411.

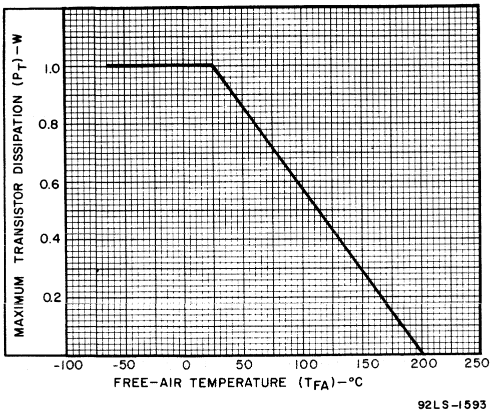


Fig. 1 — Dissipation derating curver for 40406, 40407, and 40408.

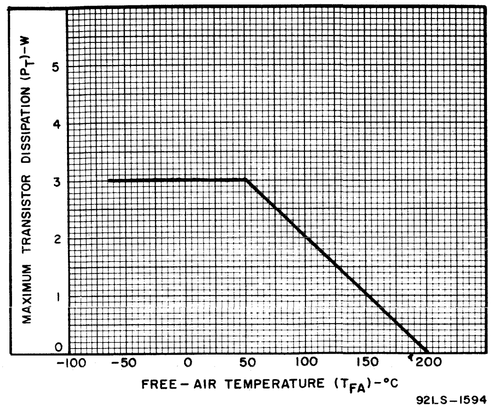


Fig. 2 — Dissipation derating curve for 40409 and 40410.

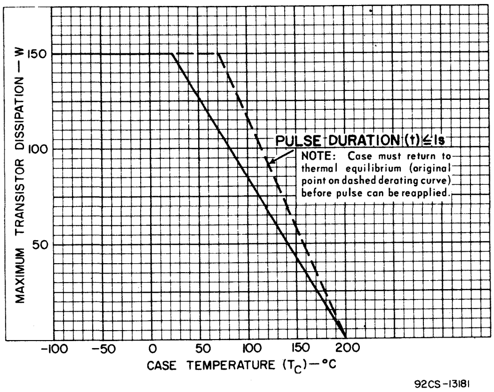


Fig. 3 — Dissipation derating curve for 40411.

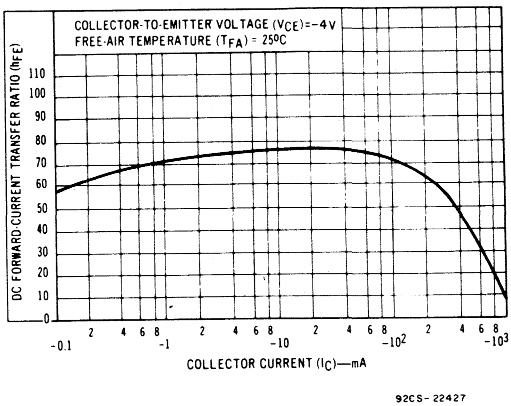


Fig. 4 — Typical dc beta characteristic for 40406 and 40410.

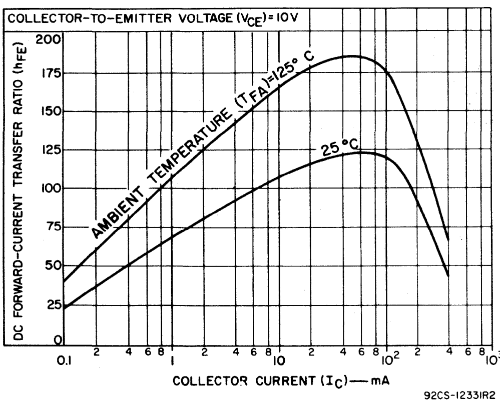


Fig. 5 — Typical dc beta characteristics for 40407, 40408, 40409.

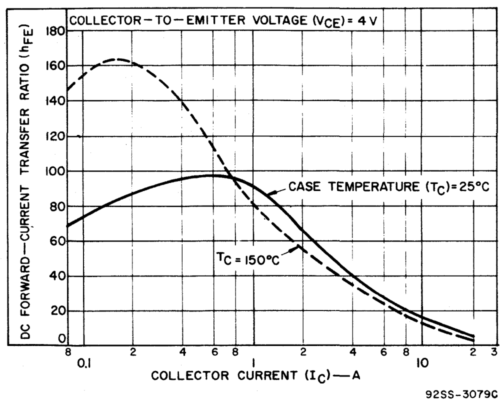


Fig. 6 — Typical dc beta characteristics for 40411.

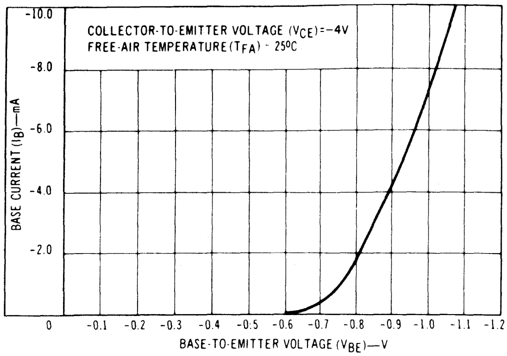


Fig. 7 – Typical input characteristic for 40406 and 40410.

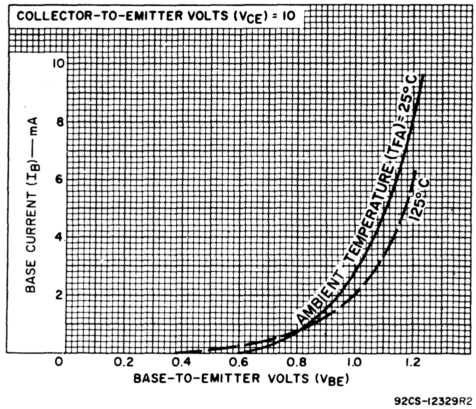


Fig. 8 – Typical input characteristics for 40407, 40408, and 40409.

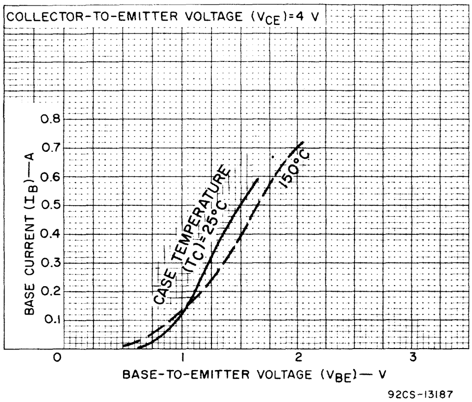


Fig. 9 – Typical input characteristics for 40411.

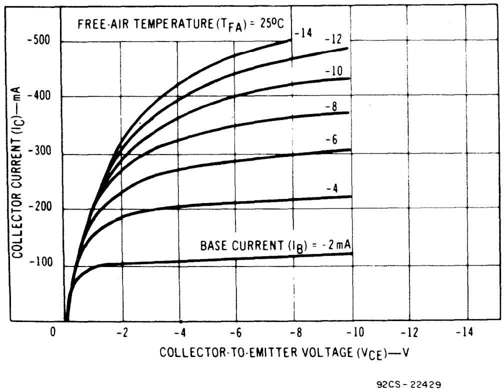


Fig. 10 – Typical output characteristics for 40406 and 40410.

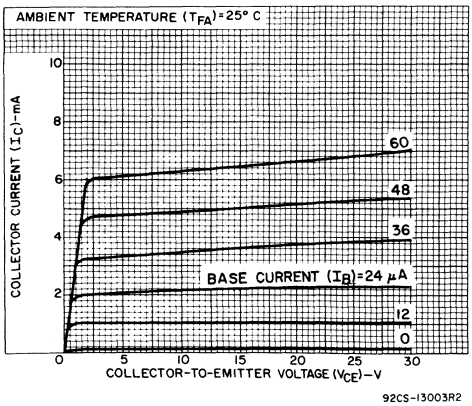


Fig. 11 – Typical output characteristics for 40407, 40408, and 40409.

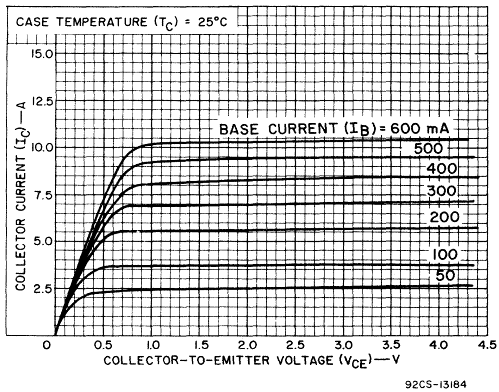
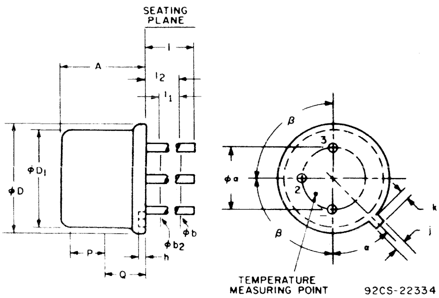


Fig. 12 – Typical output characteristics for 40411.

DIMENSIONAL OUTLINE FOR 40406, 40407, 40408



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
ϕa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
ϕb	0.016	0.021	0.406	0.533	2
ϕb_2	0.016	0.019	0.406	0.483	2
ϕD	0.350	0.370	8.89	9.40	
ϕD_1	0.305	0.335	8.00	8.51	
h	0.009	0.041	0.229	1.04	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
l {long lead	1.500		38.10		2
l {short lead	0.500		12.70		2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

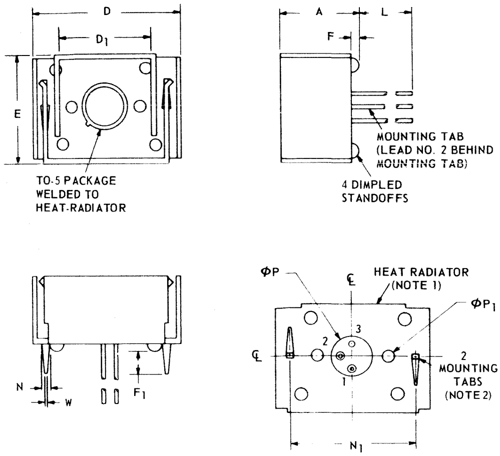
Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and l. Diameter is uncontrolled in l_1.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

DIMENSIONAL OUTLINE FOR 40409 AND 40410



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	0.630	–	16.00	
D	1.205	1.235	30.61	31.37	
D_1	0.775	0.785	19.69	19.93	
E	0.875	0.905	22.22	22.99	
F	0.040	0.055	1.02	1.40	
F_1	0.160	0.195	4.06	4.95	
L {long lead	1.410	–	35.81	–	
L {short lead	0.410	–	10.41	–	
ϕP	0.295	0.305	7.493	7.747	
ϕP_1	0.093	0.095	2.362	2.413	
N	0.048	0.062	1.21	1.57	
N_1	0.998	1.002	25.349	25.450	3
W	0.048	0.052	1.219	1.320	

NOTES:

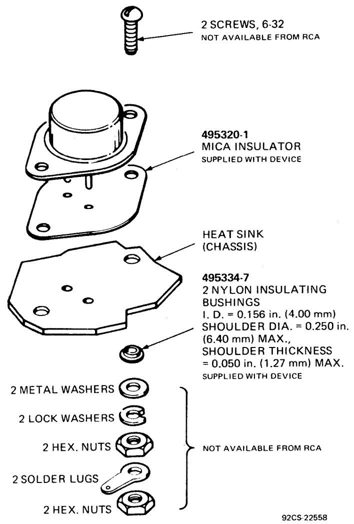
1. **0.035 C.R.S., finish—electroless nickel plate.**
2. **Recommended hole size for printed-circuit board is 0.070 in. (1.78 mm) dia.**
3. **Measured at bottom of heat-radiator.** 92CS-22335

TERMINAL CONNECTIONS

Lead 1 - Emitter
Lead 2 - Base
Case, Lead 3 - Collector

TERMINAL CONNECTIONS

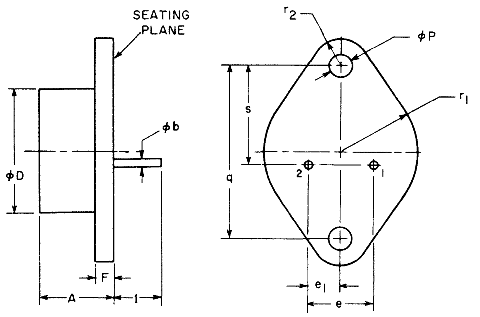
Lead 1 - Emitter
Lead 2 - Base
Heat Radiator, Lead 3 - Collector



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Suggested mounting hardware for 40411

DIMENSIONAL OUTLINE FOR 40411
JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
φb	0.038	0.043	0.97	1.09	2
φD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e_1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
l	0.312		7.92		2
φP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r_1		0.525		13.34	
r_2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS–15222

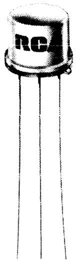
TERMINAL CONNECTIONS

Pin 1 – Base
Pin 2 – Emitter
Case – Collector
Mounting Flange – Collector

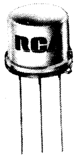
RCA
Solid State
Division

Power Transistors

40537
40538



40537L
40538L
JEDEC TO-5
H-1380



40537S
40538S
JEDEC TO-39
H-1381

Silicon P-N-P Transistors

For Driver and Output Stages in Audio-Amplifier Circuits

Features:

- **Planar construction provides low-noise and low-leakage characteristics**
- **Gain bandwidth product (f_T) = 50 MHz min.**
- **40538 is p-n-p complement of 40539***
- **Low saturation voltage:**
  V_{CE}(sat) = -1.1 V max. (40537)
  = -2.0 V max. (40538)
- **High pulse beta at high collector current:**
  h_{FE} = 50 min. at I_C = –50 mA (40537)
  = 15 min. at I_C = –500 mA (40538)

These devices are generally available with ½-inch leads (TO-39 package). They are also available in the U.S.A., Canada, Latin America, and Far East with 1½-inch leads (TO-5 package); the shorter-lead versions are specified by a suffix letter "S" after the type number, and the longer-lead versions by a suffix letter "L".

RCA-40537 and 40538 are double-diffused, epitaxial-planar, silicon p-n-p transistors. They differ in the current at which the parameters are controlled.

The 40537 is designed specifically for use as a driver in audio-amplifier circuits. The 40538 is intended as a complement to n-p-n type 40539 in complementary-symmetry output stages*

* Data for type 40539 appear in File No. 303.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		40537 40538	
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:			
With external base-to-emitter resistance (R_{BE}) = 500 Ω	V_{CER}(sus)	-55	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	-5	V
COLLECTOR CURRENT	I_C	-0.7	A
BASE CURRENT	I_B	-0.2	A
TRANSISTOR DISSIPATION:	P_T		
At case temperatures up to 25° C		5	W
At free-air temperatures up to 25° C		1	W
At temperatures above 25° C		Derate linearly to 0 W at 200° C	
TEMPERATURE RANGE:			
Storage and Operating (Junction)		-65 to 200	°C
LEAD TEMPERATURE (During soldering):			
At distance ⩾ 1/32 in. (0.8 mm) from seating plane for 10 s max.		230	°C

9-73

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS				UNITS
		DC VOLTAGE (V)		DC CURRENT (mA)		TYPE 40537		TYPE 40538		
		V_{CE}	V_{EB}	I_C	I_B	MIN.	MAX.	MIN.	MAX.	
Collector Cutoff Current With external base-to-emitter resistance (R_{BE}) = 500 Ω	I_{CER}	-45				–	-10	–	-10	μA
Emitter Cutoff Current	I_{EBO}		-5	0		–	-1	–	-1	mA
DC Forward-Current Transfer Ratio	h_{FE}	-4 -4		-50 -500[a]		50 –	300 –	– 15	– 90	
Collector-to-Emitter Sustaining Voltage With external base-to-emitter resistance (R_{BE}) = 500 Ω	$V_{CER}(sus)$			-100		-55	–	-55	–	V
Base-to-Emitter Voltage	V_{BE}	-4 -4		-50 -500		– –	-1.8 –	– –	– -2.7	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$			-50 -500	-5 -50	– –	-1.1 –	– –	– -2.0	V
Gain-Bandwidth Product	f_T	-4		-50		100 (Typ.)		100 (Typ.)		MHz
Thermal Resistance (Junction-to-Free Air)	$R_{\theta JA}$					–	175	–	175	°C/W

[a]Pulsed; pulse duration = 300 μs, duty factor < 2%.

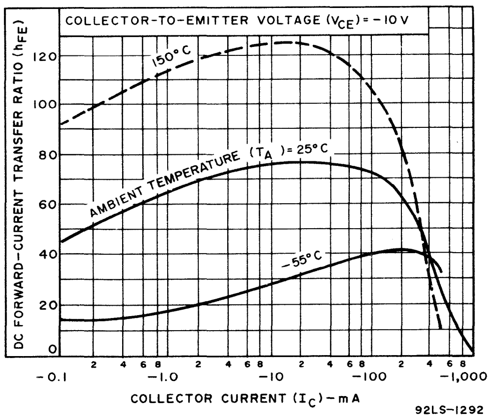


Fig.1 — Typical dc beta characteristics for both types.

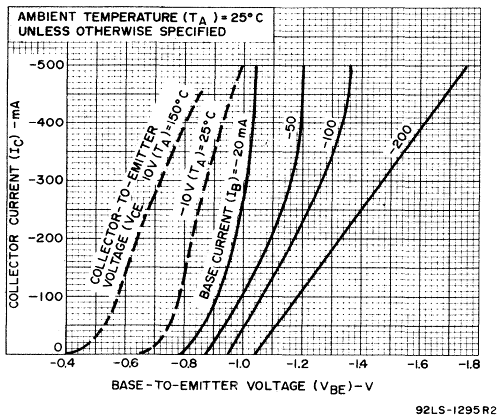


Fig.2 — Typical transfer characteristics for both types.

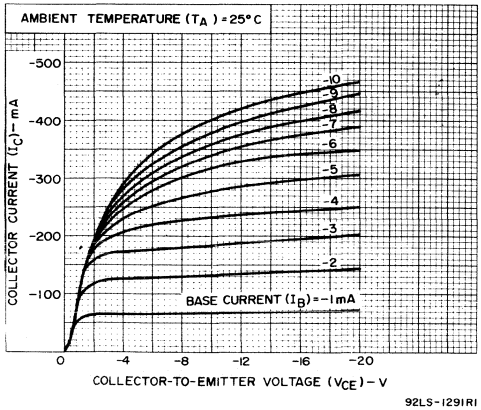


Fig.3 — Typical output characteristics for both types.

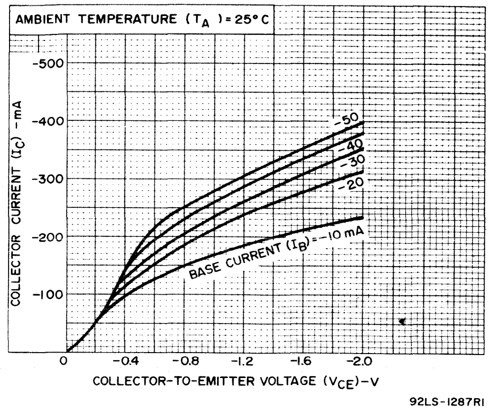
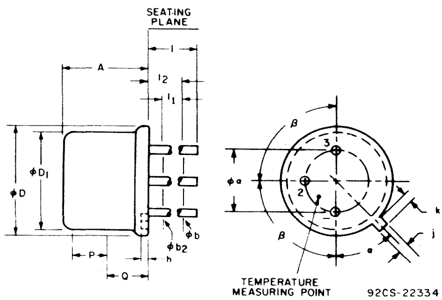


Fig.4 — Typical output characteristics for both types.

DIMENSIONAL OUTLINE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
φa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
φb	0.016	0.021	0.406	0.533	2
φb2	0.016	0.019	0.406	0.483	2
φD	0.350	0.370	8.89	9.40	
φD1	0.305	0.335	8.00	8.51	
h	0.009	0.041	0.229	1.04	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
L (long lead)	1.500		38.10		2
L (short lead)	0.500		12.70		2
l1		0.050		1.27	2
l2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads) φb_2 applies between l_1 and l_2. φb applies between l_2 and l. Diameter is uncontrolled in l_1.

Note 3: Measured from maximum diameter of the actual device.

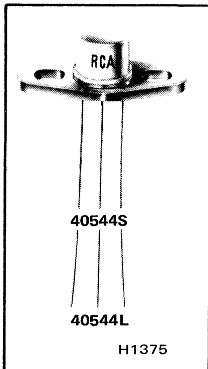
Note 4: Details of outline in this zone optional.

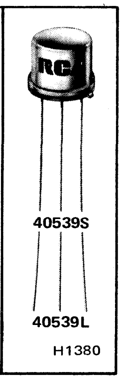
TERMINAL CONNECTIONS

Lead 1 — Emitter
Lead 2 — Base
Case, Lead 3 — Collector

RCA
Solid State
Division

Power Transistors
40539
40544





Medium-Power Silicon N-P-N Planar Transistors

For Driver and Output Stages in Audio-Amplifier Circuits

Features:

- **Low leakage current**
- **Low saturation voltage:**
  $V_{CE}(sat)$ = 1.0 V Max. (40544)
  = 2.0 V Max. (40539)
- **40539 is n-p-n complement of 40538***

These devices are generally available with ½-inch leads (TO-39 package). They are also available in the U.S.A., Canada, Latin America, and Far East with 1½-inch leads (TO-5 package); the shorter-lead versions are specified by a suffix letter "S" after the type number, and the longer-lead versions by a suffix letter "L".

RCA-40539 and 40544 are silicon n-p-n planar transistors. Type 40539 employs the JEDEC TO-39 (40539S) or TO-5 (40539L) package; type 40544 is supplied with a factory-attached, diamond-shaped mounting flange.

The 40539 is intended as a complement to p-n-p type 40538 in complementary-symmetry output stages. The 40544 was designed specifically as a driver in audio-amplifier circuits.

* Data for type 40538 appears in File No. 302.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		40539	40544	
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:				
With external base-to-emitter resistance				
(R_{BE}) = 100 Ω	V_{CER}(sus)	–	50	V
(R_{BE}) = 500 Ω	V_{CER}(sus)	55	–	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	5	V
COLLECTOR CURRENT	I_C	0.7	0.7	A
TRANSISTOR DISSIPATION:	P_T			
At case temperatures up to 25° C		5	7	W
At free-air temperatures up to 25° C		1	–	W
At temperatures above 25° C		Derate linearly to 0 W at 200°C		
TEMPERATURE RANGE:				
Storage and operating (Junction)		← -65 to + 200 →		°C
LEAD TEMPERATURE (During soldering):				
At distance ⩾ 1/32 in. (0.8 mm) from seating plane for 10 s max.		← 255 →		°C

9-73

ELECTRICAL CHARACTERISTICS, *at Case Temperature (T_C) = 25°C*

Characteristic	Symbol	TEST CONDITIONS: DC Voltage (V) V_{CE}	DC Voltage (V) V_{EB}	DC Current (mA) I_C	DC Current (mA) I_B	LIMITS: Type 40539 Min.	Type 40539 Max.	Type 40544 Min.	Type 40544 Max.	Units
Collector-Cutoff Current With external base-to-emitter resistance (R_{BE}) = 100 Ω	I_{CER}	40				–	–	–	10	μA
= 500 Ω		45				–	10	–	–	
Emitter-Cutoff Current	I_{EBO}		5	0		–	1.0	–	1.0	mA
DC Forward-Current Transfer Ratio	h_{FE}		4	500		15	90	–	–	
			4	50		–	–	35	200	
Collector-to-Emitter Sustaining Voltage With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$			100		–	–	50	–	V
= 500 Ω				100		55	–	–	–	
Base-to-Emitter Voltage	V_{BE}	4		500		–	2.7	–	–	V
		4		50		–	–	–	1.7	
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$			500	50	–	2.0	–	–	V
				150	15	–	–	–	1.0	
Gain-Bandwidth Product	f_T	4		50		100 (Typ.)		100 (Typ.)		MHz
Thermal Resistance (Junction-to-Case)	θ_{J-C}					–	35	–	25	°C/W

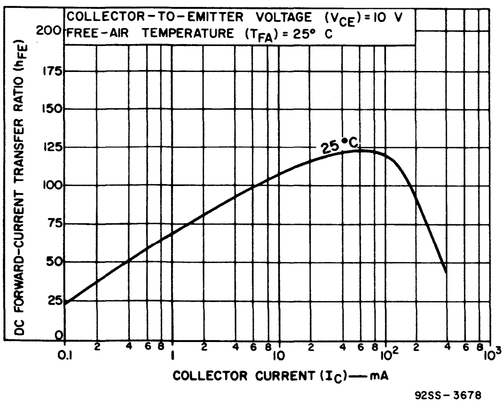


Fig.1 — Typical dc-beta characteristics for both types.

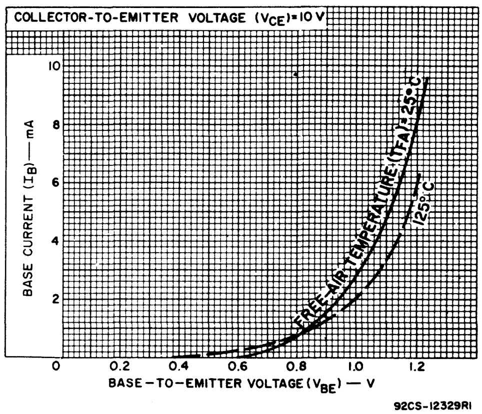


Fig.2 — Typical input characteristics for both types.

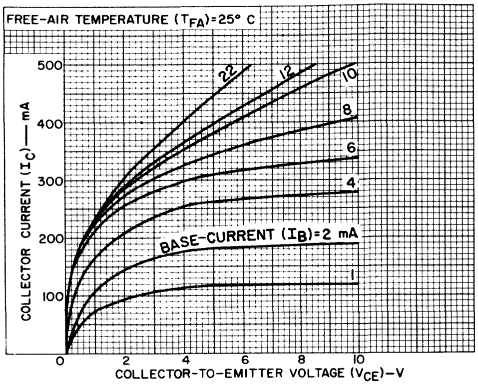


Fig.3 — Typical output characteristics for all types.

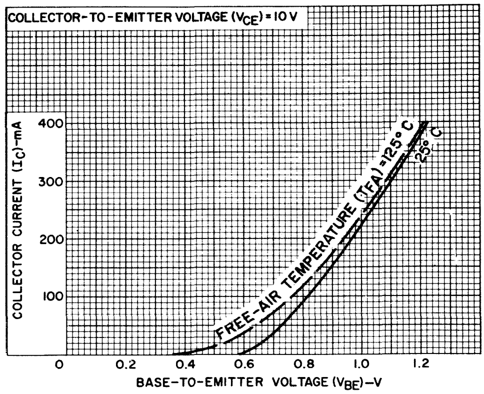
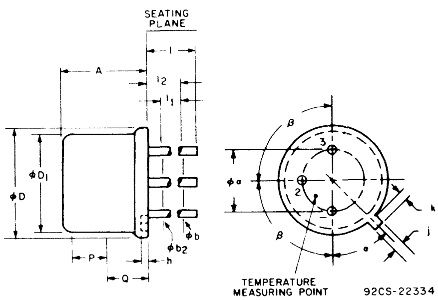


Fig.4 — Typical transfer characteristics for all types.

DIMENSIONAL OUTLINE FOR 40539



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
φa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
φb	0.016	0.021	0.406	0.533	2
φb_2	0.016	0.019	0.406	0.483	2
φD	0.350	0.370	8.89	9.40	
φD_1	0.305	0.335	8.00	8.51	
h	0.009	0.041	0.229	1.04	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
L {long lead	1.500		38.10		2
L {short lead	0.500		12.70		2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

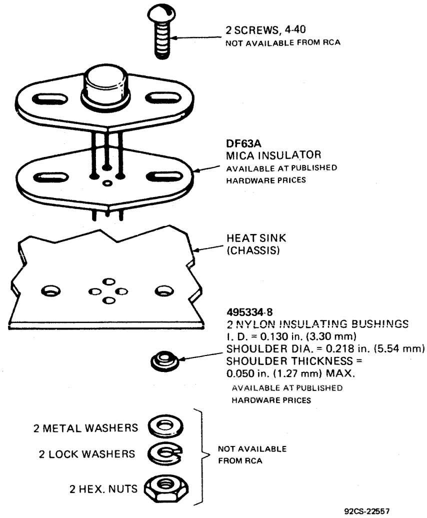
Note 2: (Three leads)φb_2 applies between l_1 and l_2. φb applies between l_2 and l. Diameter is uncontrolled in l_1.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

TERMINAL CONNECTIONS

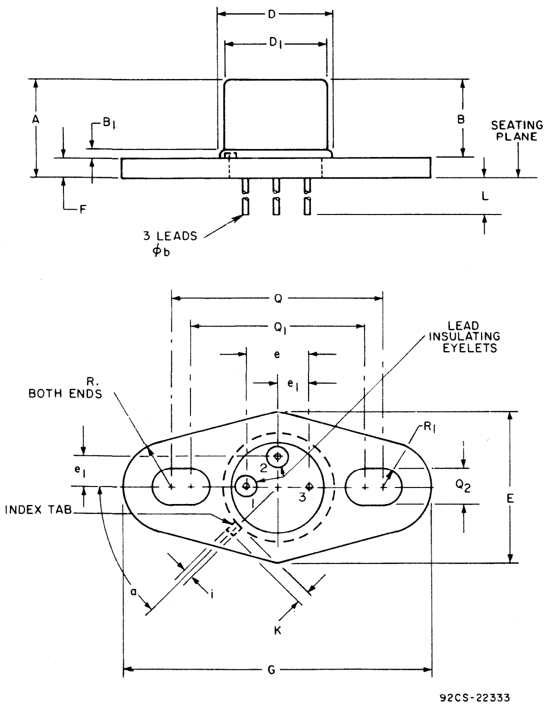
Lead 1 — Emitter
Lead 2 — Base
Case, Lead 3 — Collector



In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig.5 — Suggested mounting hardware for 40544.

DIMENSIONAL OUTLINE FOR 40544



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	0.328	–	8.33	
B	0.240	0.260	6.10	6.60	
B_1	0.009	0.125	0.229	3.18	
ϕ_b	0.016	0.019	0.406	0.483	
D	0.335	0.370	8.51	9.40	
D_1	0.305	0.335	7.75	8.51	
E	0.495	0.505	12.57	12.83	
e	0.200 T.P.		5.08 T.P.		1
e_1	0.100 T.P.		2.54 T.P.		1
F	0.062	0.068	1.57	1.74	
G	0.995	1.005	25.27	25.53	
i	0.028	0.034	0.711	0.864	
k	0.029	0.045	0.737	1.14	
L {long lead	1.430	–	36.32	–	
L {short lead	0.430	–	10.92	–	
Q	0.685	0.691	17.40	17.55	
Q_1	0.559	0.565	14.20	14.35	
Q_2	0.128	0.132	3.25	3.35	
R	0.156 T.P.		3.96 T.P.		1
R_1	0.064	0.066	1.63	1.67	
α	45° T.P.				1, 2

NOTES:
1. True position.
2. Tab centerline.

TERMINAL CONNECTIONS

Lead 1 — Emitter
Lead 2 — Base
Flange, Lead 3 — Collector

RCA

Solid State
Division

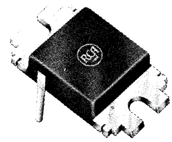
Power Transistors

40542
40543

SILICON N-P-N, MOLDED SILICONE-PLASTIC HOMETAXIAL-BASE TRANSISTORS

FOR OUTPUT STAGES IN AUDIO-AMPLIFIER CIRCUITS

40542 -- N-P-N Complement of 40051*



40542 & 40543
For TO-3 Sockets

RCA-40542 and -40543 are hometaxial**-base silicon n-p-n power transistors employing a new plastic package with formed leads which can be inserted into a TO-3 socket.

These types differ in voltage ratings and in the current at which the parameters are controlled. The 40542 is intended as a complement to p-n-p type 40051 in complementry-symmetry output stages of audio-amplifier circuits. The 40543 was designed specifically for amplifier applications.

- **Molded silicone-plastic package**
- **Low saturation voltage:**
  $V_{CE}(sat)$ = 1.0 V max. at I_C = 2.5 A (40542)
  = 1.0 V max. at I_C = 3.0 A (40543)
- **Low thermal resistance:**
  $\theta_{J\text{-}C}$ = 1.5 °C/W max.

*Data for type 40051 appears in File No. 67.

**"HOMETAXIAL" was coined by RCA from two words, "homogeneous" and "axial," to provide a name for a transistor structure in which the base region comprises homogeneous resistivity silicon material in the axial direction (emitter-to-collector). Hometaxial types provide greater power-handling capability, lower saturation resistance, and freedom from second breakdown.

MAXIMUM RATINGS

Absolute-Maximum Values:		40542	40543	
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:				
With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$	50	[illegible]	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	5	5	V
COLLECTOR CURRENT	I_C	6	8	A
TRANSISTOR DISSIPATION:	P_T			
At case temperatures up to 25° C		83	83	W
At temperatures above 25° C		Derate linearly to 0 W at 150° C.		
TEMPERATURE RANGE:				
Storage & Operating (Junction)		−65 to 150		°C
LEAD TEMPERATURE (During Soldering):				
At distances ≥ 1/16 in. from seating plane for 10 s max.		235		°C

10-67

ELECTRICAL CHARACTERISTICS

Case Temperature (T_C) = 25° C

Characteristic	Symbol	TEST CONDITIONS				LIMITS				Units
		DC Voltage (V)		DC Current (A)		Type 40542		Type 40543		
		V_{CE}	V_{EB}	I_C	I_B	Min.	Max.	Min.	Max.	
Collector-Cutoff Current With external base-to-emitter resistance (R_{BE}) = 100 Ω	I_{CER}	40 50				– –	1.0 –	– –	– 1.0	mA
Emitter-Cutoff Current	I_{EBO}		5	0		–	5.0	–	5.0	mA
DC Forward-Current Transfer Ratio	h_{FE}	4 4		2.5[a] 3.0[a]		20 –	70 –	– 20	– 70	
Collector-to-Emitter Sustaining Voltage With external base-to-emitter resistance (R_{BE}) = 100 Ω	$V_{CER}(sus)$			0.2[a]		50	–	60	–	V
Base-to-Emitter Voltage	V_{BE}	4 4		2.5[a] 3.0[a]		– –	1.7 –	– –	– 1.7	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$			2.5[a] 3.0[a]	0.25 0.3	– –	1.0 –	– –	– 1.0	V
Gain-Bandwidth Product	f_T	4		0.5		0.8	2.8	0.8	2.8	MHz
Thermal Resistance (Junction-to-Case)	θ_{J-C}					–	1.5	–	1.5	°C/W

[a]Pulsed; pulse duration = 300 μs, duty factor = 1.8%.

TYPICAL DC BETA
FOR TYPE 40542

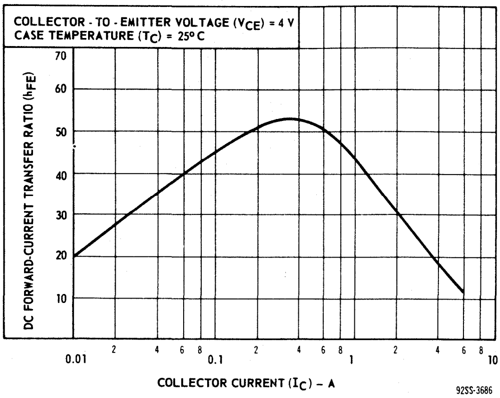


Fig. 1

TYPICAL INPUT CHARACTERISTICS
FOR TYPE 40542

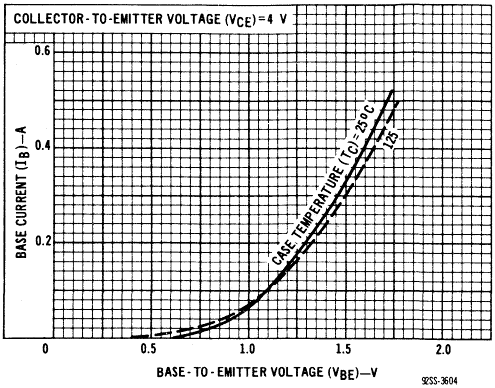


Fig. 2

TYPICAL OUTPUT CHARACTERISTICS
FOR TYPE 40542

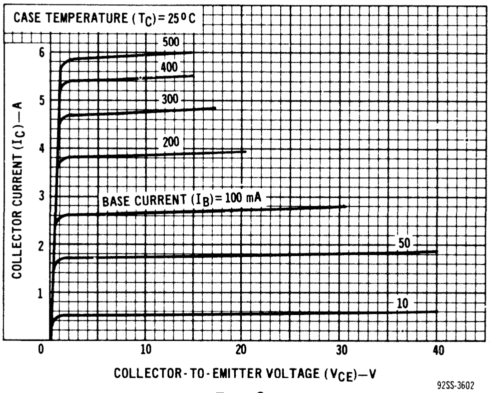


Fig. 3

TYPICAL TRANSFER CHARACTERISTICS
FOR TYPE 40542

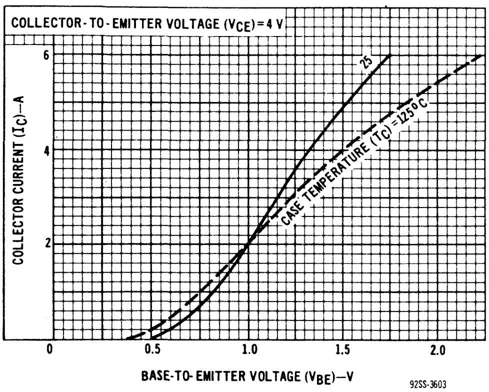


Fig. 4

TYPICAL GAIN-BANDWIDTH PRODUCT
FOR TYPE 40542

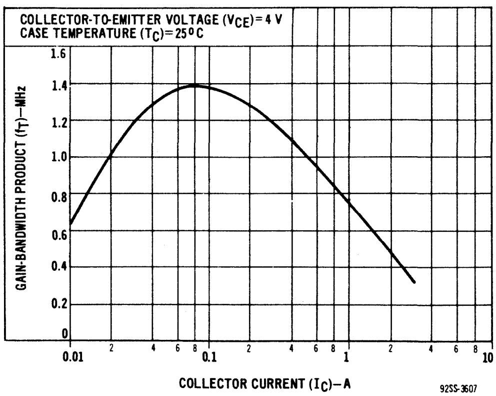


Fig. 5

TYPICAL DC BETA
FOR TYPE 40543

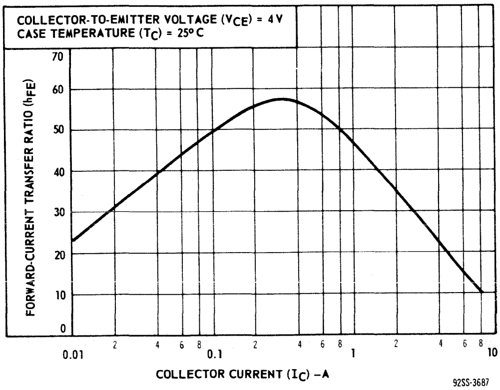


Fig. 6

TYPICAL INPUT CHARACTERISTICS
FOR TYPE 40543

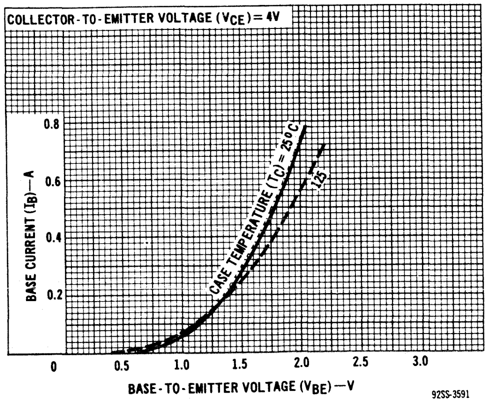


Fig. 7

TYPICAL OUTPUT CHARACTERISTICS
FOR TYPE 40543

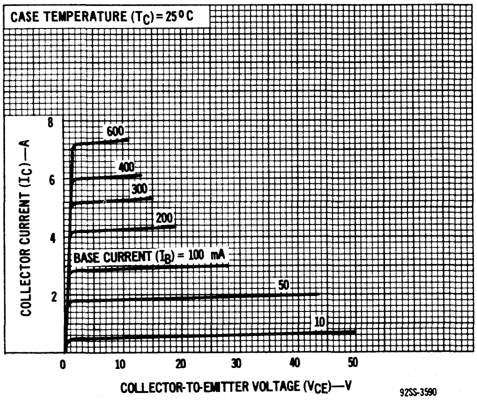


Fig. 8

TYPICAL TRANSFER CHARACTERISTICS
FOR TYPE 40543

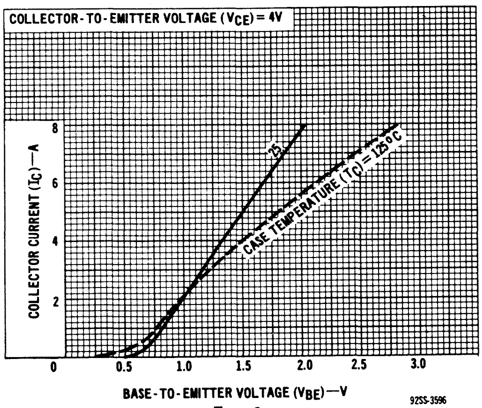


Fig. 9

TYPICAL GAIN-BANDWIDTH PRODUCT
FOR TYPE 40543

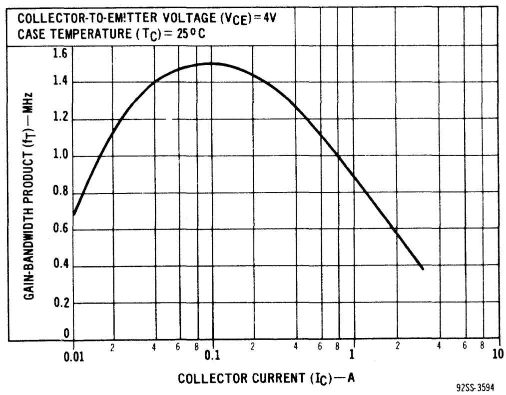
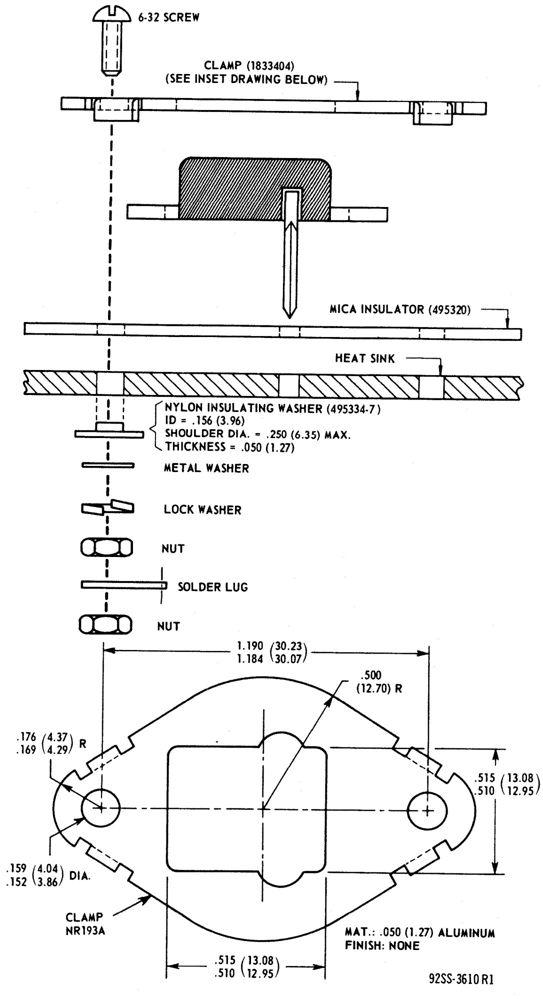


Fig. 10

SUGGESTED HARDWARE FOR MOUNTING
TYPES 40542 & 40543
IN PLACE OF TO-3 TYPES

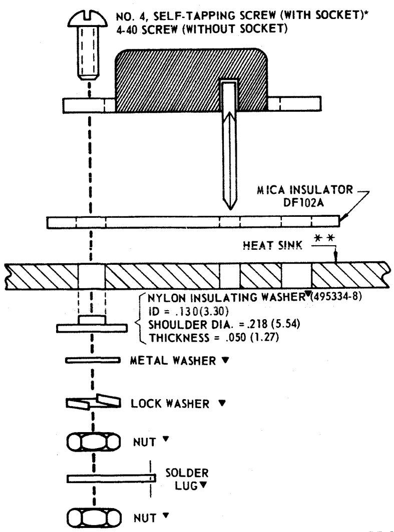


Dimensions in Inches and Millimeters

Note: *Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.*

Fig. 11

SUGGESTED HARDWARE FOR MOUNTING TYPES 40542 & 40543



*SOCKET NO. XA1521 (INDUSTRIAL ELECTRONICS HARDWARE CORP. 109 PRINCE STREET., NEW YORK, N.Y.) OR EQUIV.

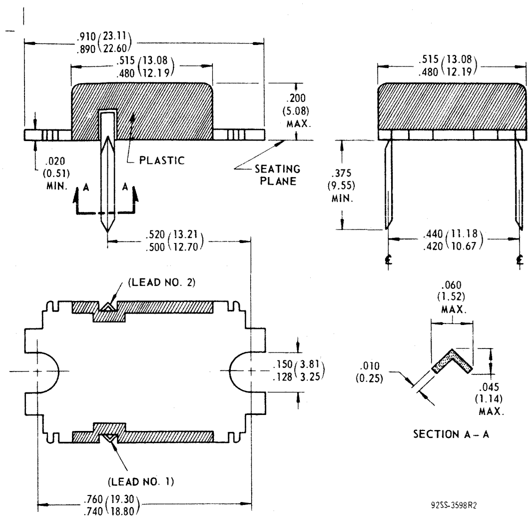
**.130 (3.30) MAX. THICKNESS

▼NOT REQUIRED WITH SOCKET (USE SELF - TAPPING SCREW) 92SS-3611R1

In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 12

DIMENSIONAL OUTLINE FOR TYPES 40542 & 40543



Dimensions in Inches and Millimeters

Note: *Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.*

TERMINAL CONNECTIONS FOR TYPES 40542 & 40543

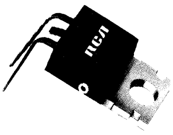
Lead No. 1 – Base
Lead No. 2 – Emitter
Mounting Flange – Collector

RCA

Solid State Division

Power Transistors

40594 40595 40611 40613
40616 40618 40621 40622
40624 40625 40627–40632
40634–40636



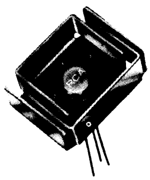
H-1534

40613 40627
40618 40629
40621 40630
40622 40631
40624 40632

JEDEC TO-220AA
(For TO-66 Sockets)

H-1570

40636
JEDEC TO-3



H-1468

40625L or S
40628L or S

With Heat-Radiator

See NOTE at right above

40594L
40595L
40611L
40616L
40635L

JEDEC TO-5

H-1380

40594S
40595S
40611S
40616S
40634S
40635S

JEDEC TO-39

See NOTE at right

H-1381

RCA-40594, 40595, 40611, 40613, 40616, 40618, 40621, 40622, 40624, 40627–40632, and 40634–40636, inclusive are silicon n-p-n and p-n-p transistors intended for driver and output stages in high-fidelity amplifier circuits.

These devices have been specifically designed for use in complementary-and-quasi-complementary-symmetry audio-amplifier circuits.

Silicon Transistors for Audio-Frequency Linear-Amplifier Applications

Transistors for Driver Applications:

N-P-N Types

40594 40616 40628
40611 40625 40635

P-N-P Types

40595 40634

NOTE:

These devices are available with either 1½-inch leads (TO-5 package) or ½-inch leads (TO-39 package). The longer-lead versions are specified by suffix "L" after the type number; the shorter-lead versions are specified by suffix "S" after the type number.

Transistors for Output Applications:

N-P-N Types

40613 40624 40631
40618 40627 40632
40621 40629 40636
40622 40630

MAXIMUM RATINGS, *Absolute-Maximum Values:*

RCA Type	$V_{CEO}(sus)$ V	$V_{CER}(sus)$* V	V_{EBO} V	I_C A	I_B A	P_T – W● $T_C = 25^oC$	$T_A = 25^oC$	Temp. Range (Storage & Operating) °C –		+
40594	–	95	4	2	1	10	1.2	65	to	200
40595	–	−95	−4	−2	−1	10	1.2	65	to	200
40611	25	–	2.5	0.7	0.2	5	1	65	to	200
40613	25	–	5	4	2	36	1.8	65	to	150
40616	32	–	2.5	0.7	0.2	5	1	65	to	200
40618	30	–	5	4	2	36	1.8	65	to	150
40621	32	–	5	4	2	36	1.8	65	to	150
40622	40	–	5	4	2	36	1.8	65	to	150
40624	45	–	5	6	3	50	1.8	65	to	150
40625	45	–	7	1	–	–	3.5	65	to	200
40627	55	–	5	6	3	50	1.8	65	to	150
40628	55	–	7	1	–	–	3.5	65	to	200
40629	–	35	5	4	2	36	1.8	65	to	150
40630	–	40	5	4	2	36	1.8	65	to	150
40631	–	45	5	4	2	36	1.8	65	to	150
40632	–	60	5	6	3	50	1.8	65	to	150
40634	–	−75	−7	−0.7	−0.2	5	1	65	to	200
40635	–	75	7	0.7	0.2	5	1	65	to	200
40636	–	95	7	15	7	115	–	65	to	200

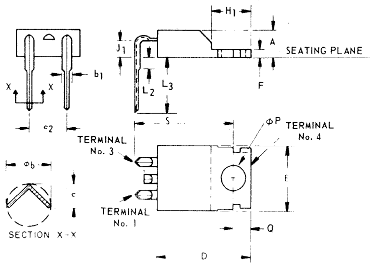
* R_{BE} = 100 Ω (40594, 40595, 40629, 40630, 40631, 40632, 40634, 40635, & 40636)

● P_T at temperatures above 25°C, derate linearly to 0 watts at maximum temperature (e.g. + 100, + 150, or + 200°C).

RCA Type	I_{CBO} Max.		I_{CER} Max.				I_{EBO} Max.			V_{CEO}(sus) Min.	
	μA	V_{CB} V	μA	mA	V_{CE} V	R_{BE} Ω	μA	mA	V_{EB} V	V	I_C mA
40611	0.5	15	–	–	–	–	–	1	2.5	25	100
40613	2	25	–	–	–	–	–	1	5	25	100
40616	0.5	15	–	–	–	–	–	1	5	32	100
40618	2	30	–	–	–	–	–	1	5	30	100
40621	0.5	30	–	–	–	–	–	1	5	32	100
40622	–	–	500	–	40	100	–	1	5	40	100
40624	–	–	500	–	45	100	–	1	5	45	100
40625	0.25	60	–	–	–	–	1	–	5	45	100
40627	–	–	500	–	55	100	–	1	5	55	100
40628	0.25	60	–	–	–	–	1	–	5	55	100
40629	–	–	–	0.5	30	100	–	1	5	–	–
40630	–	–	–	0.5	35	100	–	1	5	–	–
40631	–	–	–	0.5	40	100	–	1	5	–	–
40632	–	–	–	0.5	50	100	–	1	5	–	–
40634	–	–	– 10	–	– 65	100	–	– 0.1	– 4	–	–
40635	–	–	10	–	65	100	–	0.1	4	–	–
40636	–	–	–	0.5	85	100	–	1	4	–	–
40594	–	–	10	–	85	100	–	0.1	4	–	–
40595	–	–	– 10	–	– 85	100	–	– 0.1	– 4	–	–

V_{CER}(sus) Min.			V_{CE}(sat) Max.			V_{BE} Max.			h_{FE}				RCA Type
V	I_C mA	R_{BE} Ω	V	I_C mA	I_B mA	V	V_{CE} V	I_C mA	Min.	Max.	I_C mA	V_{CE} V	
–	–	–	–	–	–	–	–	–	70	500	50	4	40611
–	–	–	–	–	–	1.3	4	1000	30	120	1000	4	40613
–	–	–	–	–	–	–	–	–	70	500	50	4	40616
–	–	–	–	–	–	–	–	–	30	120	1000	4	40618
–	–	–	1	1500	150	1.5	4	1500	25	100	1500	4	40621
–	–	–	1	1500	150	1.5	4	1500	25	100	1500	4	40622
–	–	–	1	2500	250	1.7	4	2500	20	100	2500	4	40624
–	–	–	0.5	150	15	1	4	150	100	300	150	10	40625
–	–	–	1	2500	250	1.7	4	2500	20	100	2500	4	40627
–	–	–	0.5	150	15	1	4	150	100	300	150	10	40628
35	100	100	1	1000	100	1.3	4	1000	20	70	1000	4	40629
40	100	100	1	1500	150	1.4	4	1500	20	70	1500	4	40630
45	100	100	1	2000	200	1.5	4	2000	20	70	2000	4	40631
60	100	100	1	3000	300	1.4	4	3000	20	70	3000	4	40632
– 75	– 100	100	– 0.8	– 150	– 15	– 1.4	– 4	– 150	50	250	– 150	– 4	40634
75	100	100	0.8	150	15	1.4	4	150	50	250	150	4	40635
95	200	100	1	4000	400	1.4	4	4000	20	70	4000	4	40636
95	100	100	0.8	300	30	1.4	4	300	70	350	300	4	40594
– 95	– 100	100	– 0.8	– 300	– 30	– 1.4	– 4	– 300	70	350	– 300	– 4	40595

DIMENSIONAL OUTLINE
JEDEC TO-220AA



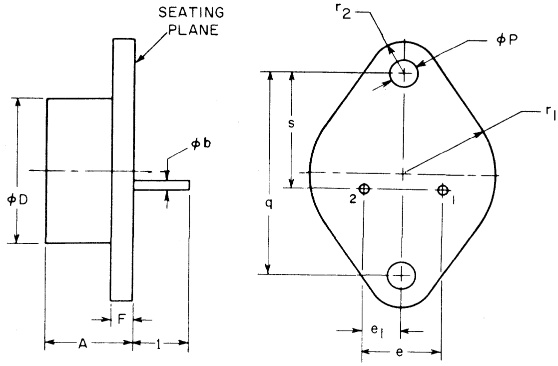
Bottom View

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
ϕb	0.02	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e_2	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L_2	–	0.050	–	1.27	–
L_3	0.360	0.422	9.15	10.71	–
ϕP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–
S	0.580	0.610	14.74	15.49	–

NOTES: 92CS-17990R1

1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.050 – 0.055 (1.27 – 1.40 mm) below seating plane.

DIMENSIONAL OUTLINE
JEDEC TO-3



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.43	
ϕb	0.038	0.043	0.97	1.09	2
ϕD		0.875		22.23	
e	0.420	0.440	10.67	11.18	
e_1	0.205	0.225	5.21	5.72	
F		0.135		3.43	
1	0.312		7.92		2
ϕP	0.151	0.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
r_1		0.525		13.34	
r_2		0.188		4.78	
s	0.655	0.675	16.64	17.15	1

NOTES:

1. These dimensions should be measured at points 0.050 in. (1.27 mm) to 0.055 in. (1.40 mm) below seating plane. When gage is not used, measurement will be made at seating plane.
2. Two pins.

92CS–15222

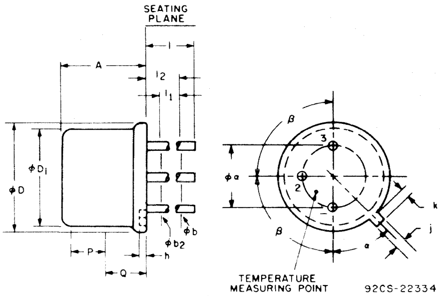
TERMINAL CONNECTIONS

Lead No.1 – Base
Stub – Do not use stub as tie point.
Lead No.3 – Emitter
Mounting Flange – Collector

TERMINAL CONNECTIONS

Pin 1 – Base
Pin 2 – Emitter
Case – Collector
Mounting Flange – Collector

DIMENSIONAL OUTLINE FOR 40594, 40595, 40611, 40616, 40634, 40635



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
φa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
φb	0.016	0.021	0.406	0.533	2
φb_2	0.016	0.019	0.406	0.483	2
φD	0.350	0.370	8.89	9.40	
φD_1	0.305	0.335	8.00	8.51	
h	0.009	0.041	0.229	1.04	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
L long lead	1.500		38.10		2
L short lead	0.500		12.70		2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

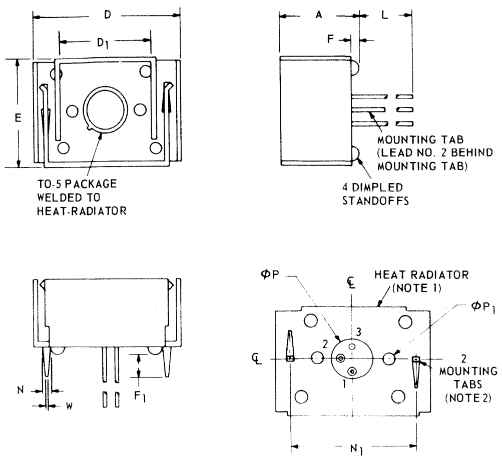
Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads)φb_2 applies between l_1 and l_2. φb applies between l_2 and l. Diameter is uncontrolled in l_1.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

DIMENSIONAL OUTLINE FOR 40625, 40628



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	0.630	–	16.00	
D	1.205	1.235	30.61	31.37	
D_1	0.775	0.785	19.69	19.93	
E	0.875	0.905	22.22	22.99	
F	0.040	0.055	1.02	1.40	
F_1	0.160	0.195	4.06	4.95	
L long lead	1.410	–	35.81	–	
L short lead	0.410	–	10.41	–	
φP	0.295	0.305	7.493	7.747	
φP_1	0.093	0.095	2.362	2.413	
N	0.048	0.062	1.21	1.57	
N_1	0.998	1.002	25.349	25.450	3
W	0.048	0.052	1.219	1.320	

NOTES:

1. 0.035 C.R.S., finish—electroless nickel plate.
2. Recommended hole size for printed-circuit board is 0.070 in. (1.78 mm) dia.
3. Measured at bottom of heat-radiator. 92CS-22335

TERMINAL CONNECTIONS

Lead 1 – Emitter
Lead 2 – Base
Case, Lead 3 – Collector

TERMINAL CONNECTIONS FOR TYPE 40391

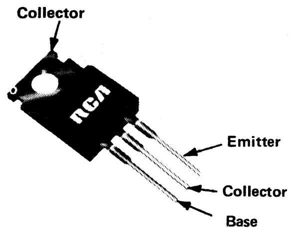
Lead 1 – Emitter
Lead 2 – Base
Heat-Radiator, Lead 3 – Collector

RCA
Solid State
Division

Power Transistors

40871 40873 40875
40872 40874 40876

40871–40876



JEDEC TO-220AB H-1535R1

Epitaxial-Base, Silicon N-P-N and P-N-P VERSAWATT Transistors

General-Purpose Types for Medium-Power Switching and Amplifier Service in Consumer, Automotive, and Industrial Applications

Features:

- **40871, 40873, 40875 complements of 40872, 40874, 40876**
- **Low saturation voltage**
- **VERSAWATT package**
- **Maximum safe-operating-area curves**
- **Thermal-cycling ratings**

RCA-40871, 40873, and 40875 are epitaxial-base silicon n-p-n transistors. RCA-40872, 40874, and 40876 are epitaxial-base p-n-p transistors. These devices are intended for a wide variety of medium-power switching and amplifier applications, such as switching regulators and inverters and driver and output stages of high-fidelity amplifiers. These plastic power transistors differ in voltage ratings and in the currents at which the parameters are controlled. They are supplied in the JEDEC TO-220AB VERSAWATT package.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		N-P-N P-N-P	40871 40872*	40873 40874*	40875 40876*	
COLLECTOR-TO-EMITTER SUSTAINING VOLTAGE:						
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}(sus)		120	80	60	V
With base open	V_{CEO}(sus)		100	70	50	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}		5	5	5	V
COLLECTOR CURRENT (Continuous)	I_C		7	7	7	A
BASE CURRENT (Continuous)	I_B		3	3	3	A
TRANSISTOR DISSIPATION:	P_T					
At case temperatures up to 25°C			40	40	40	W
At ambient temperatures up to 25°C			1.8	1.8	1.8	W
At case temperatures above 25°C		Derate linearly at 0.32W/°C, or see Fig. 1.				
At ambient temperatures above 25°C			Derate linearly at 0.0144 W/°C			
TEMPERATURE RANGE:						
Storage & Operating (Junction)			←	–65 to 150	→	°C
LEAD TEMPERATURE (During Soldering):						
At distance ≥ 1/8 in. (3.17 mm) from case for 10 s max.			←	235	→	°C

* For p-n-p devices, voltage and current values are negative.

11-73

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C, Unless Otherwise Specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS VOLTAGE V dc V_{CE}	VOLTAGE V dc V_{EB}	CURRENT A dc I_C	CURRENT A dc I_B	LIMITS 40871 40872* MIN.	40871 40872* MAX.	40873 40874* MIN.	40873 40874* MAX.	40875 40876* MIN.	40875 40876* MAX.	UNITS
Collector-Cutoff Current: With external base-to-emitter resistance (R_{BE}) = 100 Ω	I_{CER}	110 70 50				– – –	1 – –	– – –	– 1 –	– – –	– – 1	mA
Emitter-Cutoff Current	I_{EBO}		5	0		–	1	–	1	–	1	mA
Collector-to-Emitter Sustaining Voltage: With base open	V_{CEO}(sus)			0.1	0	100	–	70	–	50	–	V
With external base-to-emitter resistance (R_{BE}) = 100 Ω	V_{CER}(sus)			0.1		120	–	80	–	60	–	V
DC Forward-Current Transfer Ratio	h_{FE}	4 4 4		1[a] 2[a] 3[a]		50 – –	250 – –	– 30 –	– 150 –	– – 20	– – 120	
Base-to-Emitter Voltage	V_{BE}	4 4 4		1[a] 2[a] 3[a]		– – –	1.5 – –	– – –	– 1.5 –	– – –	– – 1.5	V
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)			1[a] 2[a] 3[a]	0.1 0.2 0.3	– – –	1.0 – –	– – –	– 1.0 –	– – –	– – 1.0	V
Gain-Bandwidth Product	f_T	4		0.5		4	–	4	–	4	–	MHz
Thermal Resistance: Junction-to-Case	$R_{\theta JC}$					–	3.125	–	3.125	–	3.125	°C/W
Junction-to-Ambient	$R_{\theta JA}$						70		70		70	°C/W

* For p-n-p devices, voltage and current values are negative.

a Pulsed: Pulse duration = 300 μs, duty factor = 0.018.

CAUTION: The sustaining voltages V_{CEO}(sus) and V_{CER}(sus) MUST NOT be measured on a curve tracer.

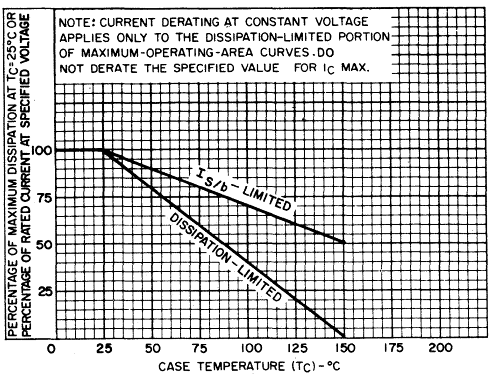


Fig.1 – Derating curves for all types.

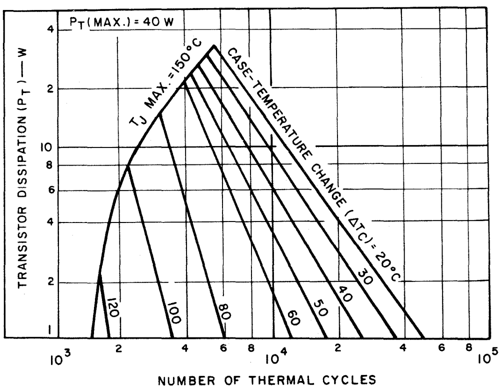


Fig.2 – Thermal-cycling ratings for all types.

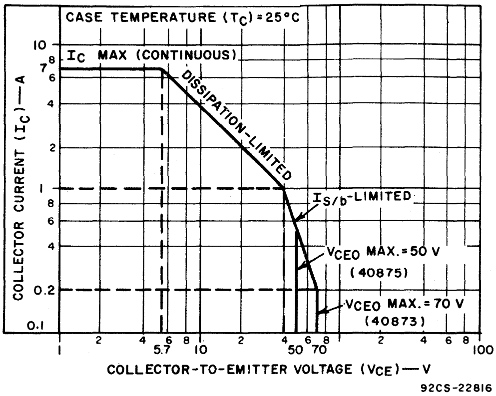


Fig.3 — Maximum operating areas for 40873 and 40875.

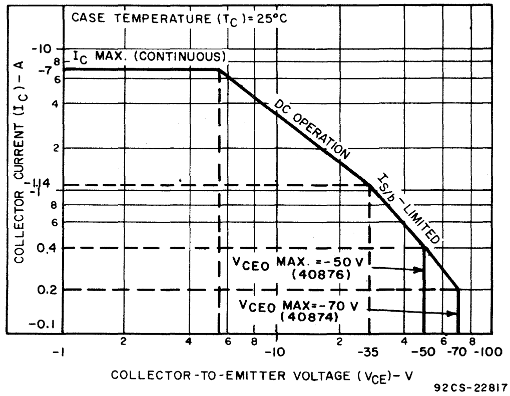


Fig.4 — Maximum operating areas for 40874 and 40876.

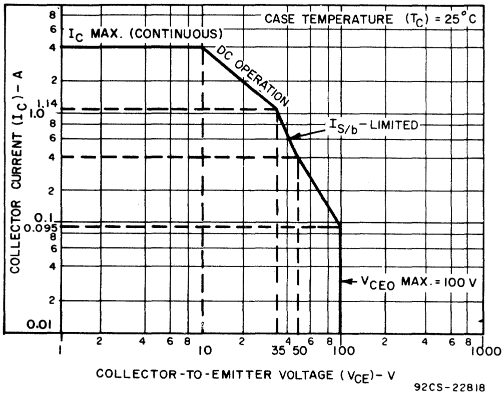


Fig.5 — Maximum operating areas for 40871.

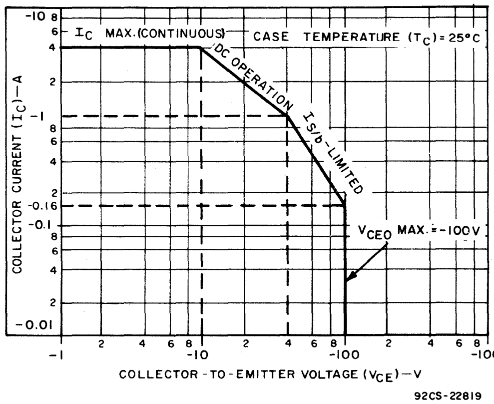


Fig.6 — Maximum operating areas for 40872.

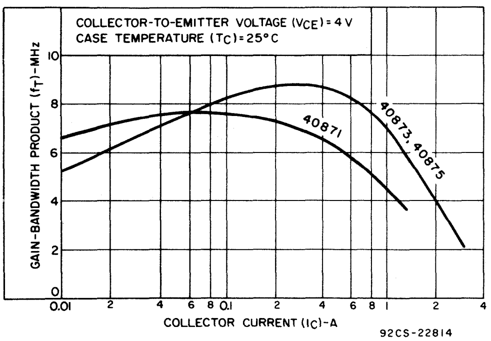


Fig.7 — Typical gain-bandwidth product for 40871, 40873, and 40875.

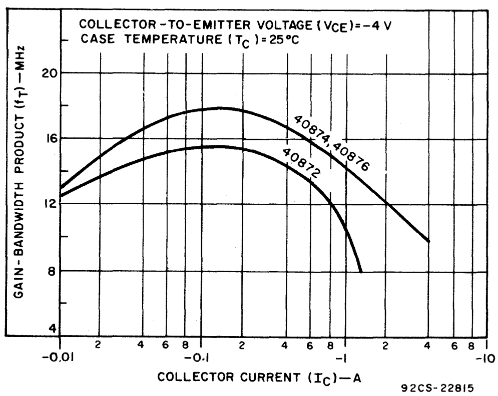


Fig.8 — Typical gain-bandwidth product for 40872, 40874, and 40876.

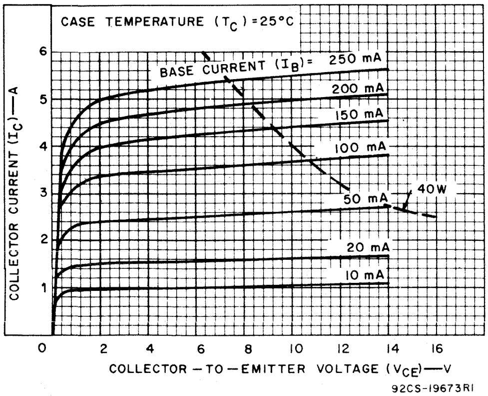


Fig.9 — Typical output characteristics for 40873, 40875.

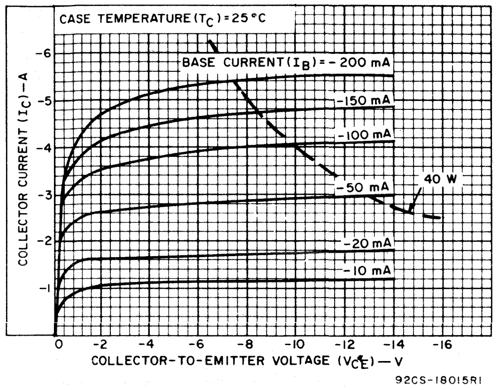


Fig.10 — Typical output characteristics for 40874, 40876.

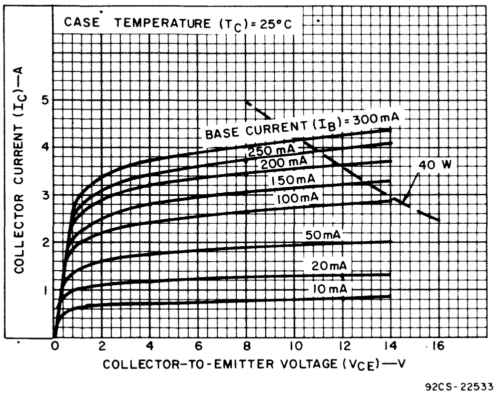


Fig.11 — Typical output characteristics for 40871.

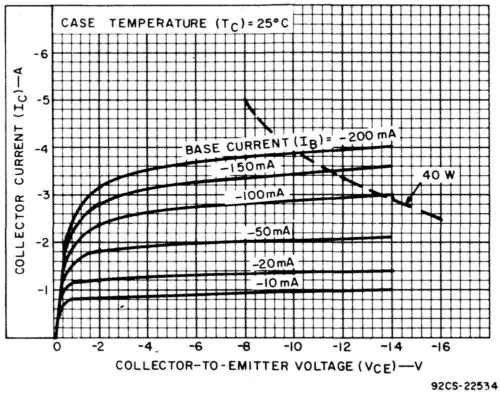


Fig.12 — Typical output characteristics for 40872.

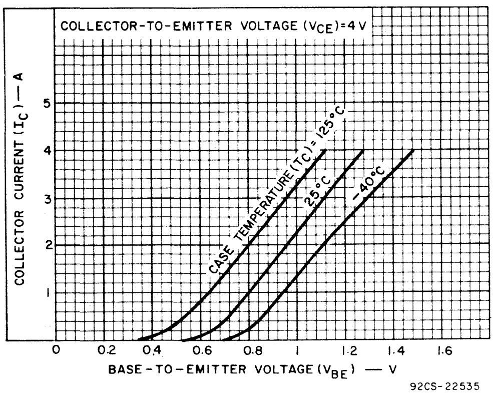


Fig.13 — Typical transfer characteristics of types 40873, 40875.

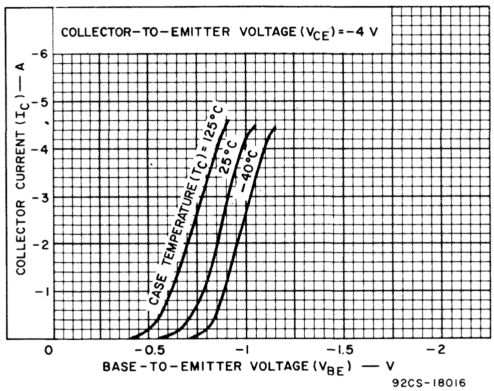


Fig.14 — Typical transfer characteristics for types 40874, 40876.

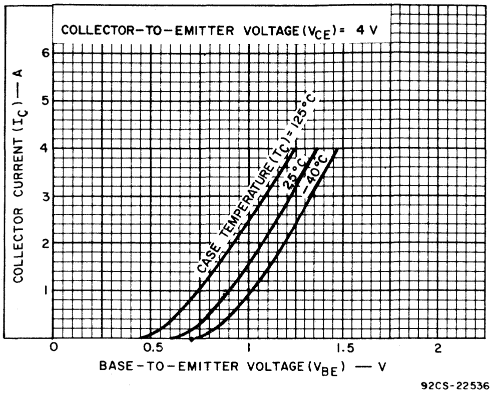


Fig.15 — Typical transfer characteristics for 40871.

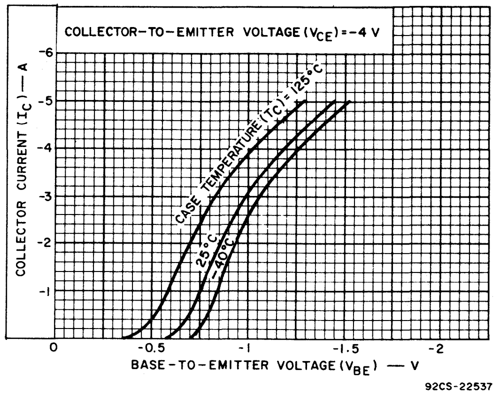


Fig.16 — Typical transfer characteristics for 40872.

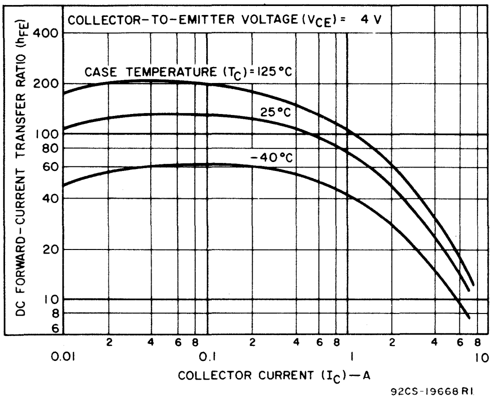


Fig.17 — Typical dc beta characteristics for 40873, 40875.

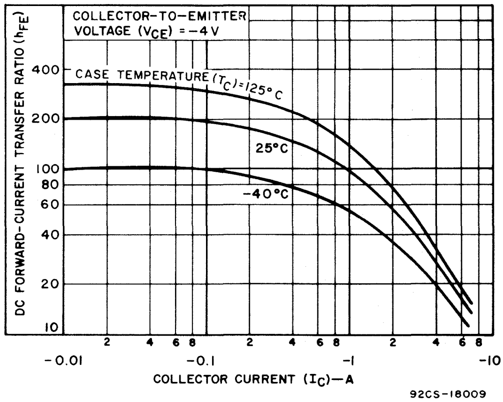


Fig.18 — Typical dc beta characteristics for 40874, 40876.

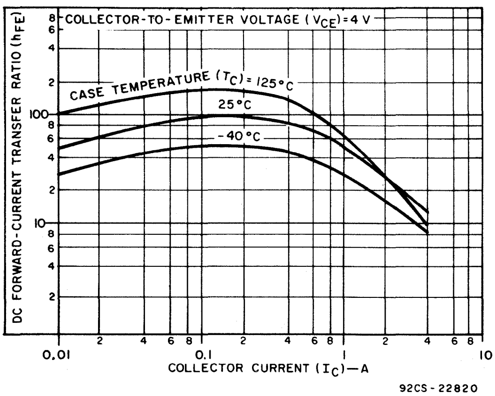


Fig.19 — Typical dc beta characteristics for 40871.

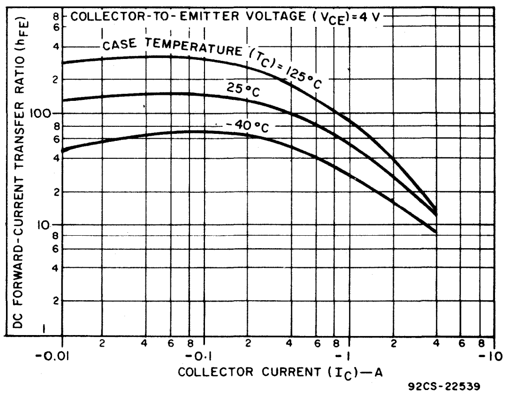


Fig.20 — Typical dc beta characteristics for 40872.

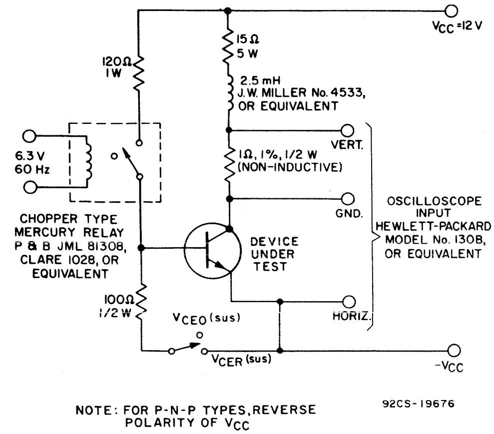
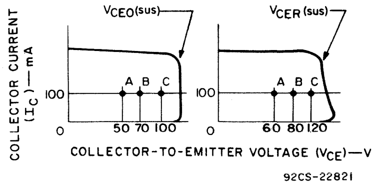


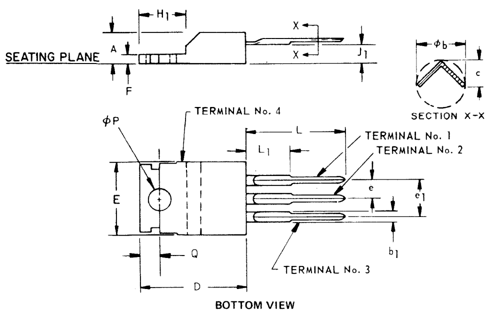
Fig.21 – Circuit used to measure sustaining voltages V_{CEO}(sus) and V_{CER}(sus) for all types.



The sustaining voltages V_{CEO}(sus) and V_{CER}(sus) are acceptable when the traces fall to the right and above point "A" for types 40875 and 40876, point "B" for types 40873 and 40874, and point "C" for types 40871 and 40872.

Fig.22 – Oscilloscope display for measurement of sustaining voltages (test circuit shown in Fig.21).

DIMENSIONAL OUTLINE
JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	–
φb	0.020	0.045	0.51	1.14	–
b_1	0.045	0.070	1.15	1.77	–
c	0.015	0.030	0.38	0.762	–
D	0.560	0.625	14.23	15.87	–
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.15	1.39	–
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	–
L	0.500	0.562	12.70	14.27	–
L_1	–	0.250	–	6.35	–
φP	0.139	0.147	3.531	3.733	–
Q	0.100	0.120	2.54	3.04	–

92CS-17991R1

NOTES:
1. Tab contour optional within H_1 and E.
2. Position of lead to be measured 0.250 – 0.255 in. (6.35 – 6.48 mm) from case.

TERMINAL CONNECTIONS

Lead No.1 – Base
Lead No.2 – Collector
Lead No.3 – Emitter
Mounting Flange – Collector

Small-Signal Low-Power Transistors

RCA Solid State Division

RF Power Transistors

2N918
2N3600

RCA-2N918 and RCA-2N3600 are double-diffused epitaxial planar transistors of the silicon n-p-n type. They are extremely useful in low-noise-amplifier, oscillator, and converter applications at VHF frequencies.

These devices utilize a hermetically sealed four-lead JEDEC TO-72 package. All active elements of the transistor are insulated from the case, which may be grounded by means of the fourth lead in applications requiring minimum feedback capacitance, shielding of the device, or both.

MAXIMUM RATINGS, Absolute-Maximum Values:

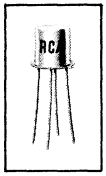
	2N918	2N3600		
COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	30	30	max.	V
COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO}	15	15	max.	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}	3	3	max.	V
COLLECTOR CURRENT, I_C	50	*	max.	mA
TRANSISTOR DISSIPATION, P_T:				
For operation with heat sink:				
At case temperatures** up to 25°C	300	300	max.	mW
At case temperatures** above 25°C	Derate at 1.71 mW/°C			
For operation at ambient temperatures:				
At ambient temperatures up to 25°C	200	200	max.	mW
At ambient temperatures above 25°C	Derate at 1.14 mW/°C			
TEMPERATURE RANGE:				
Storage and Operating (Junction)	-65 to +200			°C
LEAD TEMPERATURE (During Soldering):				
At distances ≥ 1/16 inch from seating surface for 60 seconds max.	300	300	max.	°C

* Limited by transistor dissipation.

** Measured at center of seating surface.

SILICON N-P-N EPITAXIAL PLANAR TRANSISTORS

For VHF Applications In Military, Communications, and Industrial Equipment



JEDEC TO-72

FEATURES

- high gain-bandwidth product
- hermetically sealed four-lead package
- low leakage current
- high 200-MHz power gain

2N3600

- low noise figure
  NF = 4.5 dB max. at 200 MHz
- low collector-to-base time constant
  $r_b'C_c$ = 15 ps max.
- high power gain as neutralized amplifier
  G_{pe} = 17 dB min. at 200 MHz

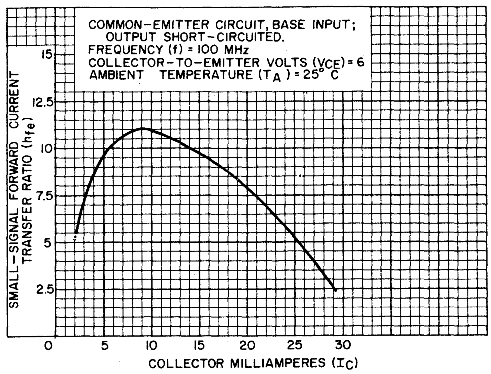


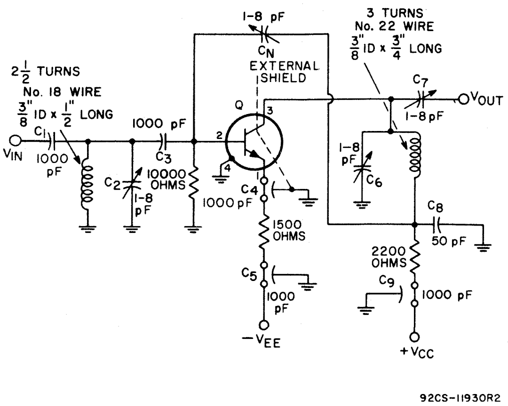
Fig. 1 - Small-signal beta characteristic for types 2N918 and 2N3600.

10-66

ELECTRICAL CHARACTERISTICS

Characteristics	Symbols	TEST CONDITIONS								LIMITS						Units
		Ambient Temperature T_A	Frequency f	DC Collector-to-Base Voltage V_{CB}	DC Collector-to-Emitter Voltage V_{CE}	DC Emitter-to-Base Voltage V_{EB}	DC Emitter Current I_E	DC Collector Current I_C	DC Base Current I_B	Type 2N918			Type 2N3600			
		°C	MHz	V	V	V	mA	mA	mA	Min.	Typ.	Max.	Min.	Typ.	Max.	
Collector-Cutoff Current	I_{CBO}	25 150		15 15			0 0			- -	- -	0.01 1	- -	- -	0.01 1	µA µA
Collector-to-Base Breakdown Voltage	BV_{CBO}	25					0	0.001		30	-	-	30	-	-	V
Collector-to-Emitter Sustaining Voltage	$BV_{CEO}(sus)$	25						3	0	15	-	-	15	-	-	V
Emitter-to-Base Breakdown Voltage	BV_{EBO}	25					0.01	0		3	-	-	3	-	-	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	25						10	1	-	-	0.4	-	-	0.4	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$	25						10	1	-	-	1	-	-	1	V
Static Forward Current-Transfer Ratio	h_{FE}	25			1			3		20	-	-	20	-	150	
Small-Signal Forward Current-Transfer Ratio[a]	h_{fe}	25	100 100 1 kHz		10 6 6			4 5 2		6 - -	- - -	- - -	- 8.5 40	- - -	- 15 200	
Common-Base Output Capacitance[b]	C_{ob}	25	0.1 to 1	10 0			0 0			- -	- -	1.7 3	- -	- -	- -	pF pF
Collector-to-Base Feedback Capacitance[b]	C_{cb}	25	0.1 to 1	10			0			-	-	-	-	-	1	pF
Common-Base Input Capacitance[c]	C_{ib}	25	0.1 to 1			0.5		0		-	-	2	-	1.4	-	pF
Collector-to-Base Time Constant[a]	$r_b'C_c$	25	40 31.9	6 6				2 5		- -	15 -	- -	- 4	- -	- 15	ps ps
Small-Signal Power Gain in Neutralized Common-Emitter Amplifier Circuit[a] (See Fig.2 & Fig.3)	G_{pe}	25	200		12 6			6 5		15 -	21 -	- -	- 17	- -	- 24	dB dB
Small-Signal Power Gain in Unneutralized Common-Emitter Amplifier Circuit[a] (See Fig.4)	G_{pe}	25	200		10			5		-	13	-	-	-	-	dB
Power Output in Common-Emitter Oscillator Circuit[c] (See Fig.5)	P_o	25	≥ 500	10			12			30	-	-	20	-	-	mW
Nose Figure[a] (See Fig.2)	NF	25	200		6			1.5		-	-	-	-	-	4.5	dB
Noise Figure[a,d]	NF	25	60		6			1		-	-	6	-	-	3	dB

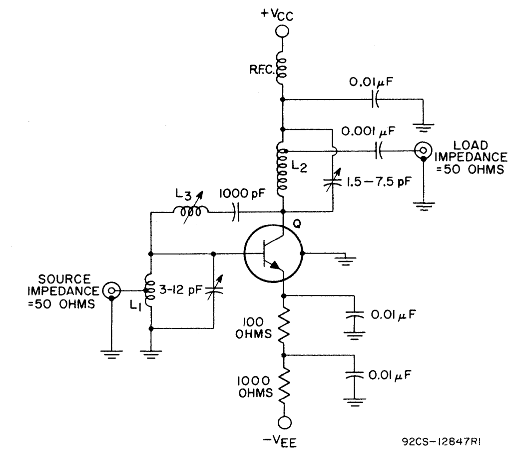
[a] Lead No.4 (case) grounded.
[b] Three-terminal measurement of the collector-to-base capacitance with the case and emitter leads connected to the guard terminal.
[c] Lead No.4 (case) floating.
[d] Generator Resistance (R_g) = 400 ohms.



NOTE: (Neutralization Procedure): (a) Connect a 50-Ω rf voltmeter to the output of a 200-MHz signal generator (R_g = 50 Ω), and adjust the generator output to 5 mV. (b) Connect the generator to the input and the rf voltmeter to the output of the amplifier, as shown above. (c) Apply V_{EE} and V_{CC}, and adjust the generator output to provide an amplifier output of 5 mV. (d) Tune C_2, C_6, and C_7 for maximum amplifier output, readjusting the generator output, as required, to maintain an output of 5 mV from the amplifier. (e) Interchange the connections to the signal generator and the rf voltmeter. (f) With sufficient signal applied to the output terminals of the amplifier, adjust C_N for a minimum indication at the amplifier input. (g) Repeat steps (a), (b), (c), and (d) to determine if retuning is necessary.

Q = Type 2N3600

Fig.2 - Neutralized amplifier circuit used to measure power gain and noise figure at 200 MHz for type 2N3600.



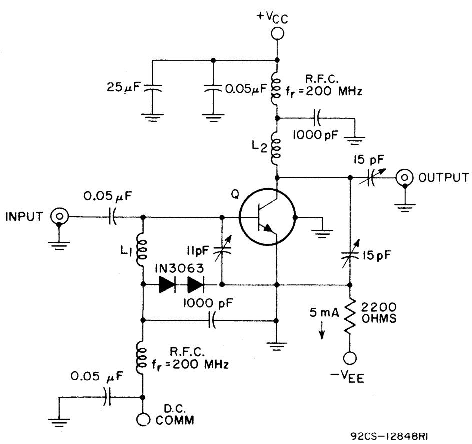
L_1 - 3.5 turns No.16 tinned copper wire; 5/16" dia.; 7/16" long; turns ratio ≃ 4:2

L_2 - 8 turns No.16 tinned copper wire; 1/8" dia.; 7/8" long; turns ratio ≃ 8:1

L_3 - MILLER #4303 (0.4 - 0.65 µH) or equivalent

Q = Type 2N918

Fig.3 - Neutralized amplifier circuit used to measure power gain at 200 MHz for type 2N918.

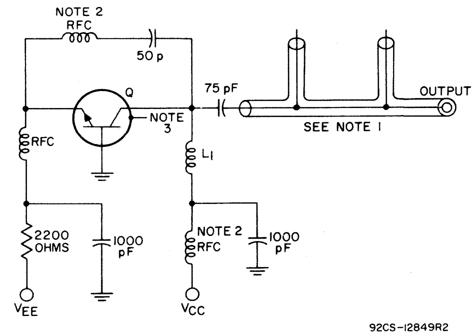


L_1 - 1 loop #12 AWG wire; I_D = 13/16"

L_2 - 1/2 loop #12 AWG wire; I_D = 1-3/16"

Q = 2N918

Fig.4 - Circuit used to measure 200-MHz unneutralized power gain for type 2N918.



Note 1 - Coaxial-Line output network consisting of:
- 2 General Radio Type 874 TEE or equivalent
- 1 General Radio Type 874-D20 Adjustable Stub or equivalent
- 1 General Radio Type 874-LA Adjustable Line or equivalent
- 1 General Radio Type 874-WN3 Short-circuit termination or equivalent

Note 2 - RFC = 0.2 µH Ohmite #2-460 or equivalent

Note 3 - Lead Number 4 (case) floating

L_1 - 2 turns #16AWG wire, 3/8 inch OD, 1-1/4 inch long

Q = 2N918 or 2N3600

Fig.5 - Circuit used to measure 500-MHz oscillator power output for types 2N918 and 2N3600.

TWO-PORT ADMITTANCE (y) PARAMETERS AS FUNCTIONS OF COLLECTOR CURRENT (I_C) FOR RCA TYPES 2N918 AND 2N3600

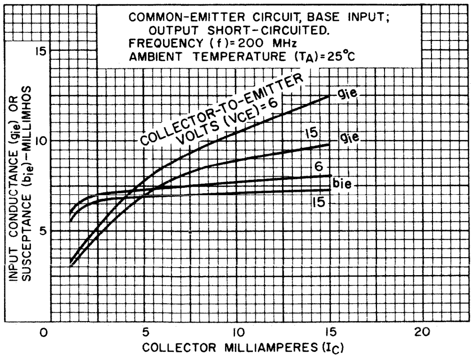


Fig.6 - Input admittance (y_{ie}).

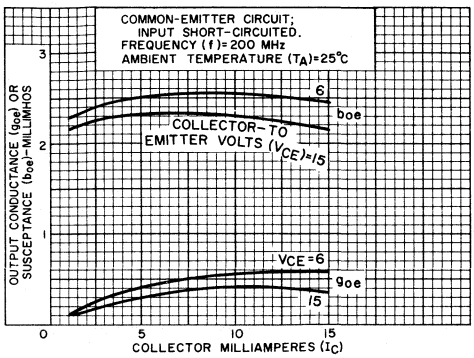


Fig.7 - Output admittance (y_{oe}).

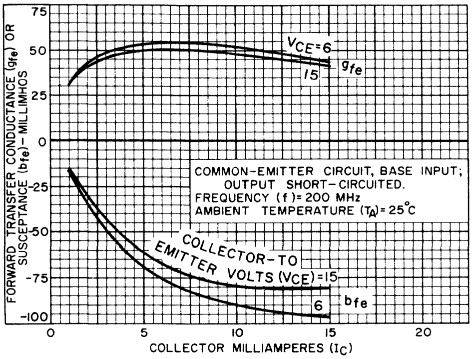


Fig.8 - Forward transadmittance (y_{fe}).

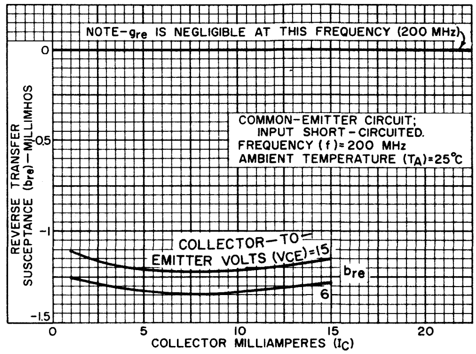
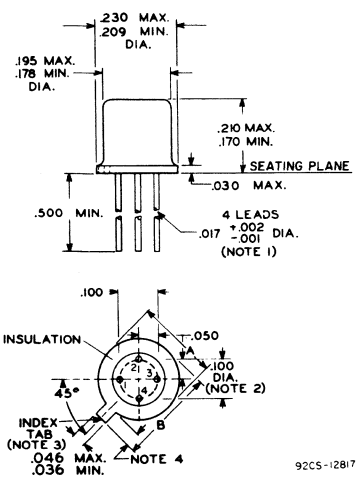


Fig.9 - Reverse transadmittance (y_{re}).

DIMENSIONAL OUTLINE TO-72



Dimensions in Inches

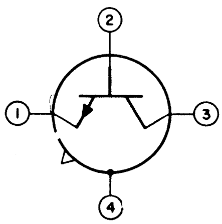
NOTE 1: THE SPECIFIED LEAD DIAMETER APPLIES IN THE ZONE BETWEEN 0.050" AND 0.250" FROM THE SEATING PLANE. FROM 0.250" TO THE END OF THE LEAD A MAXIMUM DIAMETER OF 0.021" IS HELD. OUTSIDE OF THESE ZONES, THE LEAD DIAMETER IS NOT CONTROLLED.

NOTE 2: MAXIMUM DIAMETER LEADS AT A GAUGING PLANE 0.054" + 0.001" - 0.000" BELOW SEATING PLANE TO BE WITHIN 0.007" OF THEIR TRUE LOCATION RELATIVE TO MAX. WIDTH TAB AND TO THE MAXIMUM 0.230" DIAMETER MEASURED WITH A SUITABLE GAUGE. WHEN GAUGE IS NOT USED, MEASUREMENT WILL BE MADE AT SEATING PLANE.

NOTE 3: FOR VISUAL ORIENTATION ONLY.

NOTE 4: TAB LENGTH TO BE 0.028" MINIMUM - 0.048" MAXIMUM, AND WILL BE DETERMINED BY SUBTRACTING DIAMETER A FROM DIMENSION B.

TERMINAL DIAGRAM (Bottom View)



LEAD 1 - EMITTER

LEAD 2 - BASE

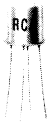
LEAD 3 - COLLECTOR

LEAD 4 - CONNECTED TO CASE

RCA
Solid State
Division

RF Power Transistors

2N3478



JEDEC TO-72 H-1299

SILICON N-P-N EPITAXIAL PLANAR TRANSISTOR

For VHF/UHF Applications
in Industrial and Commercial Equipment

Features:

- **high gain-bandwidth product – f_T = 900 MHz typ.**
- **low noise figure**
  NF = 5 dB typ. at 470 MHz
  4.5 dB max. at 200 MHz
  2.5 dB typ. at 60 MHz
- **high unneutralized power gain G_{pe} = 11.5 dB min. at 200 MHz**
- **hermetically sealed four-lead package**
- **all active elements insulated from case**
- **low collector-to-base feedback capacitance, C_{cb} 0.7 pF max.**

RCA-2N3478 is an epitaxial planar transistor of the silicon n-p-n type with characteristics which make it extremely useful as a general purpose rf amplifier at frequencies up to 470 MHz. These characteristics include an exceptionally low noise figure at high frequencies, low leakage current, and a high gain-bandwidth product.

The 2N3478 utilizes a hermetically sealed four-lead package in which active elements of the transistor are insulated from the case. The case may be grounded by means of a fourth lead in applications requiring minimum feedback capacitance, shielding of the device, or both.

Maximum Ratings, *Absolute-Maximum Values:*

Collector-to-Base Voltage, V_{CBO}	30 max.	V
Collector-to-Emitter Voltage, V_{CEO}	15 max.	V
Emitter-to-Base Voltage, V_{EBO}	2 max.	V
Collector Current, I_C	limited by dissipation	
Transistor Dissipation, PT:		
at ambient temperatures up to 25° C	200 max.	mW
at ambient temperatures above 25° C	See *Fig. 1*	
Temperature Range:		
Storage and Operating (Junction)	−65 to 200	°C
Lead Temperature (During Soldering):		
At distances not closer than 1/32" to seating surface for 10 seconds max.	265 max.	°C

ELECTRICAL CHARACTERISTICS, *At an Ambient Temperature (T_A) of 25° C*

Characteristics	Symbols	TEST CONDITIONS					LIMITS			Units
		Frequency f	DC Collector-to-Base Voltage V_{CB}	DC Collector-to-Emitter Voltage V_{CE}	DC Emitter Current I_E	DC Collector Current I_C	Type 2N3478			
		MHz	V	V	mA	mA	Min.	Typ.	Max.	
Collector-Cutoff Current	I_{CBO}		1		0		–	–	0.02	μA
Collector-to-Base Breakdown Voltage	BV_{CBO}				0	0.001	30	–	–	V
Collector-to-Emitter Breakdown Voltage	BV_{CEO}					0.001	15	–	–	V
Emitter-to-Base Breakdown Voltage	BV_{EBO}				-0.001	0	2	–	–	V
Static Forward-Current Transfer Ratio	h_{FE}			8		2	25	–	150	
Magnitude of Small-Signal Forward-Current Transfer Ratio	h_{fe}[a]	100		8		2	7.5	9	16	
Collector-to-Base Feedback Capacitance	C_{cb}[b]	1	10		0		–	–	1	pF
Small-Signal, Common-Emitter Power Gain in Unneutralized Amplifier Circuit (See *Fig. 3*)	G_{pe}[a]	200		8		2	11.5	–	17	dB
Small-Signal, Common-Emitter Power Gain in Neutralized Amplifier Circuit	G_{pe}[a, c]	470		6		1.5	–	12	–	dB
UHF Noise Figure	NF[a, c]	470		6		1.5	–	5	–	dB
VHF Noise Figure (See *Fig. 3*)	NF[a] NF[a, d]	200 60		8 8		2 1	– –	 2.5	4.5 –	dB dB

[a] Fourth lead (case) grounded.

[b] C_{cb} is a three terminal measurement of the collector-to-base capacitance with the emitter and case connected to the guard terminal.

[c] Source Resistance, R_s = 50 ohms.

[d] Source Resistance, R_s = 400 ohms.

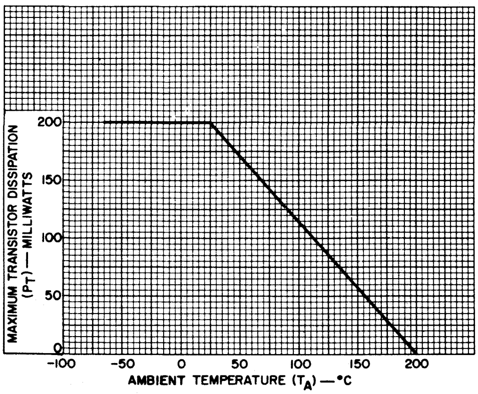


Fig. 1 - Rating chart for type 2N3478

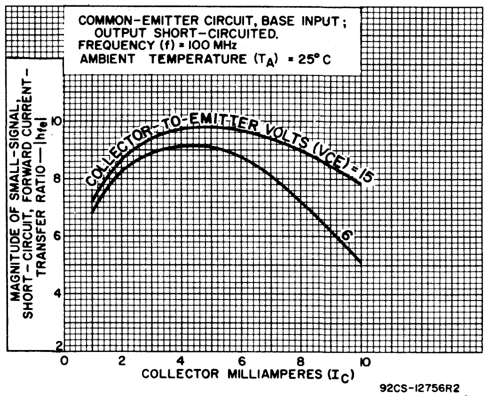
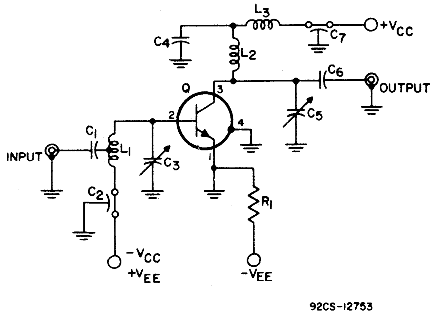


Fig. 2 - Typical small-signal beta characteristics for type 2N3478



C_1, C_4 = 510 pF
C_2, C_7 = 2300 pF
C_3, C_5 = 2-25 pF
C_6 = 10 pF
R_1 = 2000 ohms
Q = 2N3478
L_1 = ½ Turn #14 Formvar● center tapped
$Length_1$, ℓ_1 = 2 inches
L_2 = ½ Turn #14 Formvar●
$Length_2$, ℓ_2 = 1 ½ inches
L_3 = 1 μH RF choke
Source (Generator) Resistance R_g = 50 ohms
Load Resistance R_L = 50 ohms
● Trademark, Shawindian Products Corporation.

Fig. 3 - 200 MHz power gain and noise figure test circuit for type 2N3478

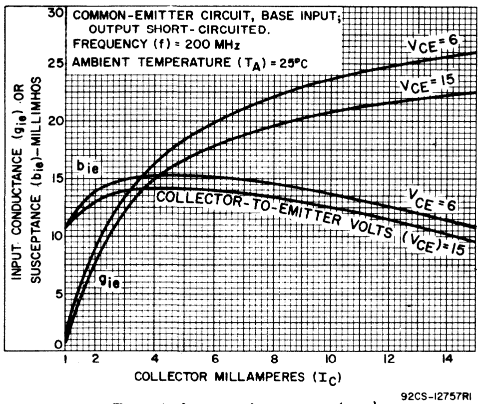


Fig. 4 - Input admittance (y_{ie})

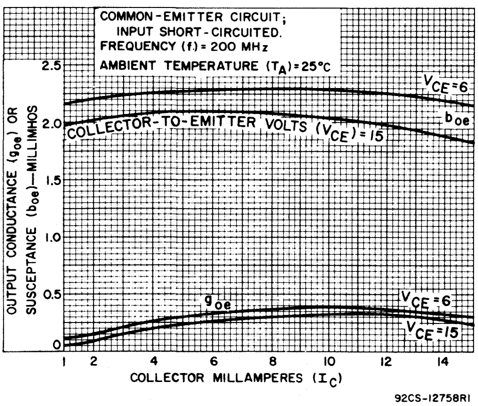


Fig. 5 - Output admittance (y_{oe})

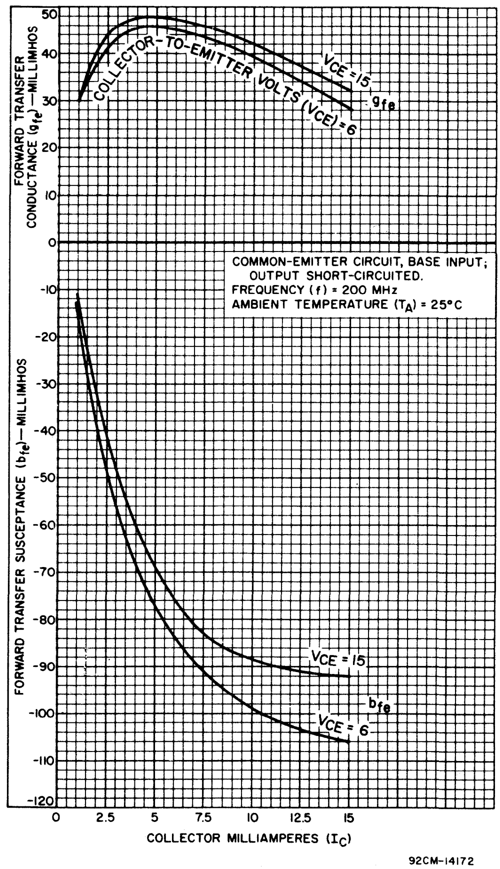


Fig. 6 - Forward transadmittance (y_{fe})

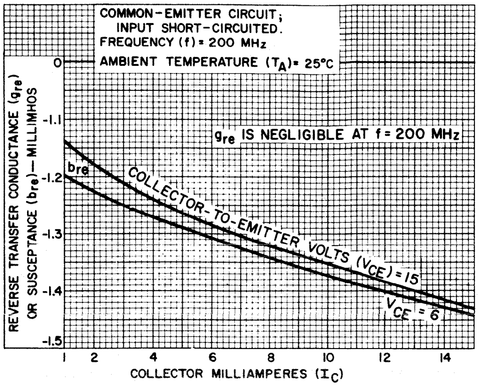
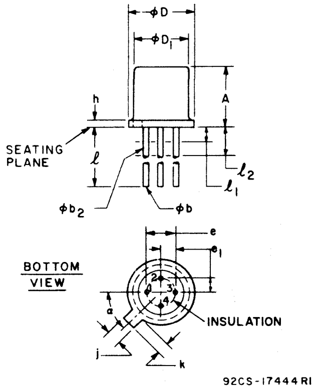


Fig. 7 - Reverse transadmittance (y_{re})

DIMENSIONAL OUTLINE

JEDEC TO–72



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.170	0.210	4.32	5.33	
φb	0.016	0.021	0.406	0.533	2
φb2	0.016	0.019	0.406	0.483	2
φD	0.209	0.230	5.31	5.84	
φD1	0.178	0.195	4.52	4.95	
e	0.100 T.P.		2.54 T.P.		4
e1	0.050 T.P.		1.27 T.P.		4
h		0.030		0.762	
j	0.036	0.046	0.914	1.17	
k	0.028	0.048	0.711	1.22	3
l	0.500		12.70		2
l1		0.050		1.27	2
l2	0.250		6.35		2
α	45° T.P.		45° T.P.		4, 6

Note 1: (Four leads). Maximum number leads omitted in this outline, "none" (0). The number and position of leads actually present are indicated in the product registration. Outline designation determined by the location and minimum angular or linear spacing of any two adjacent leads.

Note 2: (All leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and 0.50 in. (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond 0.50 in. (12.70 mm) from seating plane.

Note 3: Measured from maximum diameter of the product.

Note 4: Leads having maximum diameter 0.019 in. (0.484 mm) measured in gaging plane 0.054 in. (1.37 mm) +0.001 in. (0.025 mm) - 0.000 in. (0.000 mm) below the seating plane of the product shall be within 0.007 in. (0.178 mm) of their true position relative to a maximum width tab.

Note 5: The product may be measured by direct methods or by gage.

Note 6: Tab centerline.

TERMINAL CONNECTIONS

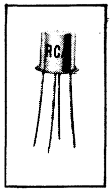
Lead 1 — Emitter
Lead 2 — Base
Lead 3 — Collector
Lead 4 — Connected to case

RCA
Solid State
Division

RF Power Transistors

2N5179

SILICON N-P-N EPITAXIAL PLANAR TRANSISTOR



JEDEC TO-72

For UHF Applications in Military, Communications, and Industrial Equipment

RCA-2N5179* is a double-diffused epitaxial planar transistor of the silicon n-p-n type. It is extremely useful in low-noise tuned-amplifier and converter applications at UHF frequencies, and as an oscillator up to 500 MHz.

The 2N5179 utilizes a hermetically sealed four-lead JEDEC TO-72 package. All active elements of the transistor are insulated from the case, which may be grounded by means of the fourth lead in applications requiring minimum feedback capacitance, shielding of the device, or both.

* Formerly Dev. No. TA7319.

Maximum Ratings, Absolute-Maximum Values:

COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	20 max.	V
COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO}	12 max.	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}	2.5 max.	V
COLLECTOR CURRENT, I_C	50 max.	mA
TRANSISTOR DISSIPATION, P_T:		
For operation with heat sink:		
At case temperatures** up to 25°C	300 max.	mW
At case temperatures** above 25°C	Derate at 1.71mW/°C	
For operation at ambient temperatures:		
At ambient temperatures up to 25°C	200 max.	mW
At ambient temperatures above 25°C	Derate at 1.14mW/°C	
TEMPERATURE RANGE:		
Storage and Operating (Junction)	−65 to +200	°C
LEAD TEMPERATURE (During Soldering):		
At distances ≥ 1/32″ from seating surface for 10 seconds max.	265 max.	°C

** Measured at center of seating surface.

- **high gain-bandwidth product — 1000MHz min.**
- **hermetically sealed TO-72 four-lead metal package**
- **low leakage current**
- **high power gain as neutralized amplifier —** G_{pe} **= 15dB min. at 200MHz**
- **high power output as UHF oscillator — 20mW typ. at 500MHz**
- **low noise figure — NF = 4.5dB max. at 200MHz**
- **low collector-to-base time constant —** $r_b'C_c$ **= 14ps max.**
- **high reliability — production lots of RCA-2N5179 are subjected to and meet the minimum mechanical, environmental, and life-test requirements of the basic MILITARY specification MIL-S-19500. See page 5 for a description of the Group A and Group B Tests.**

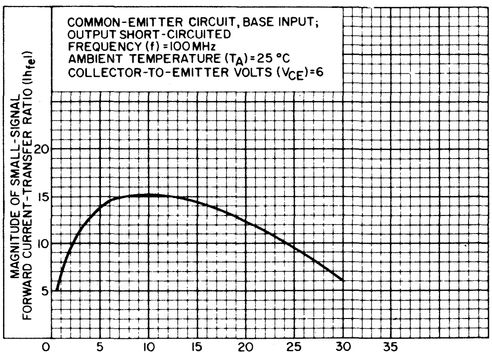


Fig. 1 – Small-Signal Beta Characteristic for Type 2N5179

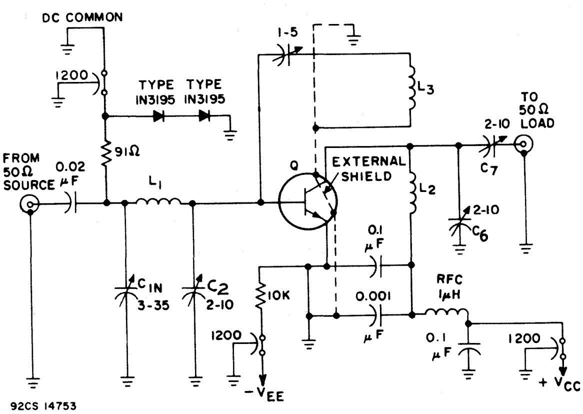
ELECTRICAL CHARACTERISTICS

Characteristics	Symbols	TEST CONDITIONS: Ambient Temp. T_A (°C)	Frequency f (MHz)	DC Collector-to-Base Voltage V_{CB} (V)	DC Collector-to-Emitter Voltage V_{CE} (V)	DC Emitter-to-Base Voltage V_{EB} (V)	DC Emitter Current I_E (mA)	DC Collector Current I_C (mA)	DC Base Current I_B (mA)	LIMITS Type 2N5179 Min.	Typ.	Max.	Units
Collector-Cutoff Current	I_{CBO}	25 150		15 15			0 0			- -	- -	0.02 1	µA µA
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	25					0	0.001		20	-	-	V
Collector-to-Emitter Sustaining Voltage	$V_{CEO}(sus)$	25						3	0	12	-	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	25					−0.01	0		2.5	-	-	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	25						10	1	-	-	0.4	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$	25						10	1	-	-	1	V
Static Forward Current-Transfer Ratio	h_{FE}	25			1			3		25	70	250	
Magnitude of Small-Signal Forward Current-Transfer Ratio[a]	$\|h_{fe}\|$	25	100 1 kHz		6 6			5 2		9 25	14 90	20 300	
Collector-to-Base Feedback Capacitance[b]	C_{cb}	25	0.1 to 1	10			0			-	0.7	1	pF
Common-Base Input Capacitance[c]	C_{ib}	25	0.1 to 1			0.5		0		-	-	2	pF
Collector-to-Base Time Constant[a]	$r_b'C_c$	25	31.9	6				2		3	7	14	ps
Small-Signal Power Gain in Neutralized Common-Emitter Amplifier Circuit[a] (See Fig. 2)	G_{pe}	25	200		12			5		15	21	-	dB
Power Output in Common-Emitter Oscilator Circuit[c] (See Fig. 3)	P_o	25	>500	10			−12			20	-	-	mW
Noise Figure[a]	NF	25	200		6			1.5		-	3	4.5	dB

[a] Lead No.4(case) grounded; R_g = 125Ω

[b] Three-terminal measurement of the collector-to-base capacitance with the case and emitter leads connected to the guard terminal.

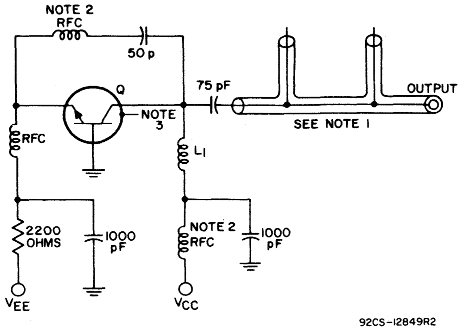
[c] Lead No. 4 (case) floating.



NOTE: (Neutralization Procedure): (a) Connect a 50-Ω rf voltmeter to the output of a 200-MHz signal generator (R_g = 50Ω), and adjust the generator output to 5mV. (b) Connect the generator to the input and the rf voltmeter to the output of the amplifier, as shown above. (c) Apply V_{EE} and V_{CC}, and adjust the generator output to provide an amplifier output of 5mV. (d) Tune C_2, C_6, and C_7 for maximum amplifier output, readjusting the generator output, as required, to maintain an output of 5mV from the amplifier. (e) Interchange the connections to the signal generator and the rf voltmeter. (f) With sufficient signal applied to the output terminals of the amplifier, adjust C_N for a minimum indication at the amplifier input. (g) Repeat steps (a), (b), (c), and (d) to determine if retuning is necessary.

Q = Type 2N5179

Fig. 2 – Neutralized Amplifier Circuit Used to Measure Power Gain and Noise Figure at 200MHz for Type 2N5179



Note 1 — Coaxial-Line output network consisting of:

- 2 General Radio Type 874 TEE or equivalent
- 1 General Radio Type 874-D20 Adjustable Stub or equivalent
- 1 General Radio Type 874-LA Adjustable Line or equivalent
- 1 General Radio Type 874-WN3 Short-circuit termination or equivalent

Note 2 — RFC = 0.2μH Ohmite #2-460 or equivalent

Note 3 — Lead Number 4 (case) floating

L_1 — 2 turns #16AWG wire, 3/8 inch OD, 1¼ inch long

Q = 2N5179

Fig. 3 – Circuit Used to Measure 500MHz Oscillator Power Output for Type 2N5179

TWO-PORT ADMITTANCE (y) PARAMETERS AS FUNCTIONS OF COLLECTOR CURRENT (I_C) FOR RCA TYPE 2N5179

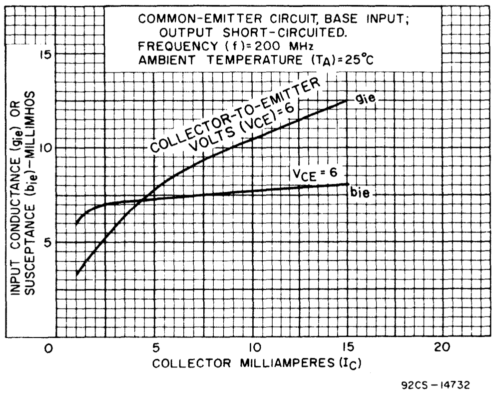


Fig. 4 – Input Admittance (y_{ie})

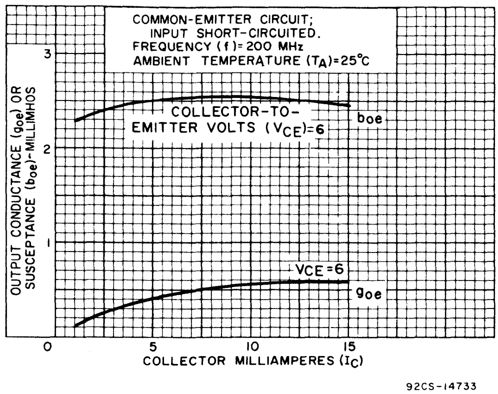


Fig. 5 – Output Admittance (y_{oe})

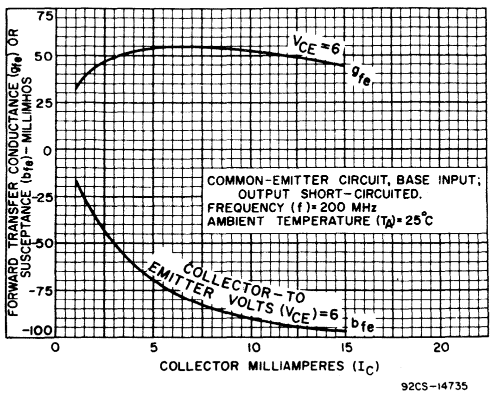


Fig. 6 – Forward Transadmittance (y_{fe})

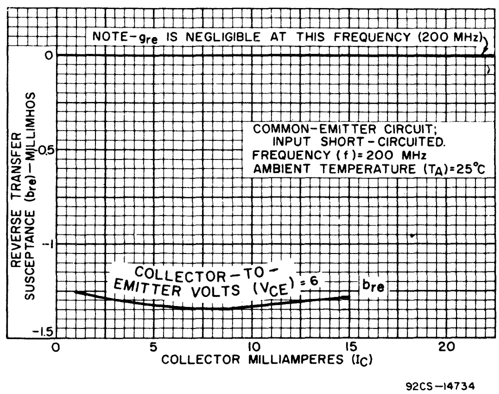


Fig. 7 – Reverse Transadmittance (y_{re})

TWO-PORT ADMITTANCE (y) PARAMETERS AS FUNCTIONS OF FREQUENCY (f) FOR RCA TYPE 2N5179

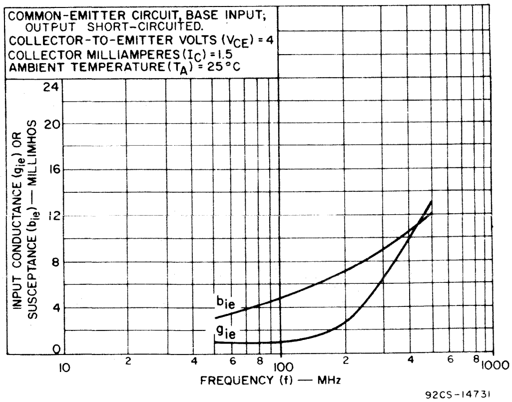


Fig. 8 – Input Admittance (y_{ie})

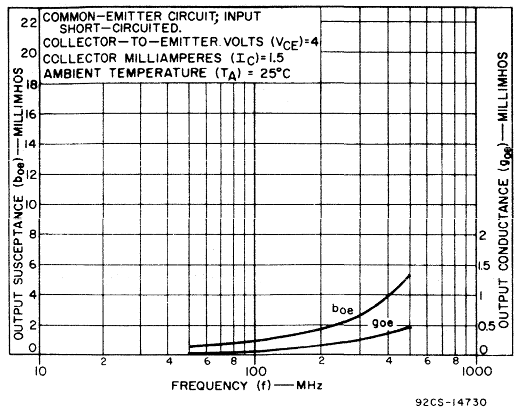


Fig. 9 – Output Admittance (y_{oe})

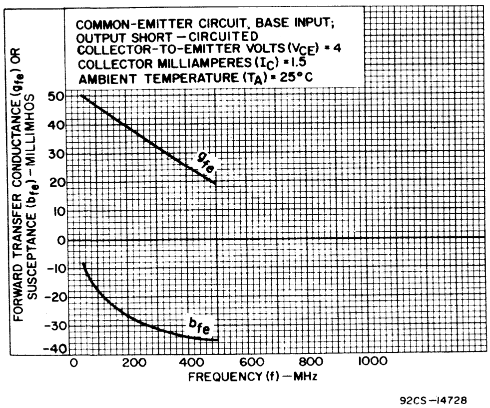


Fig. 10 – Forward Transadmittance (y_{fe})

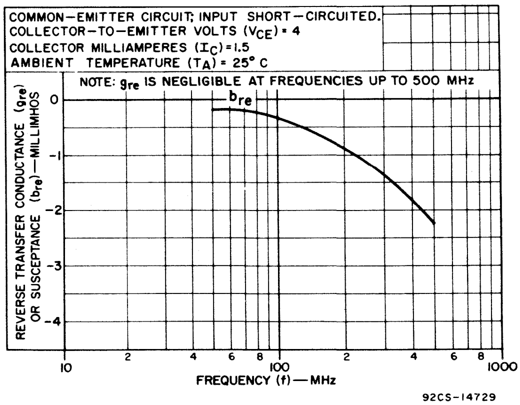
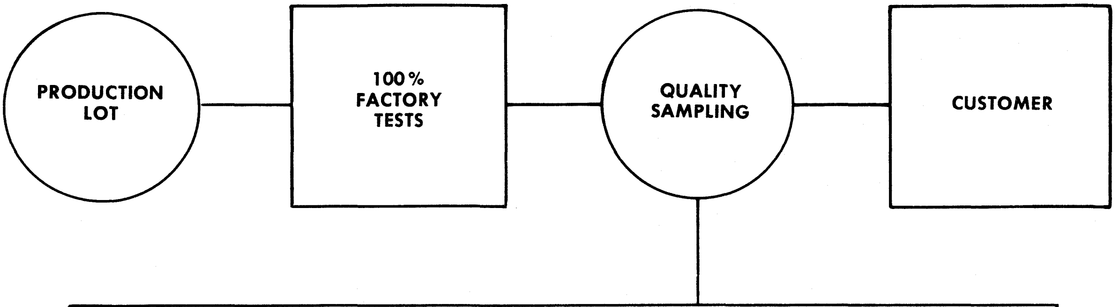


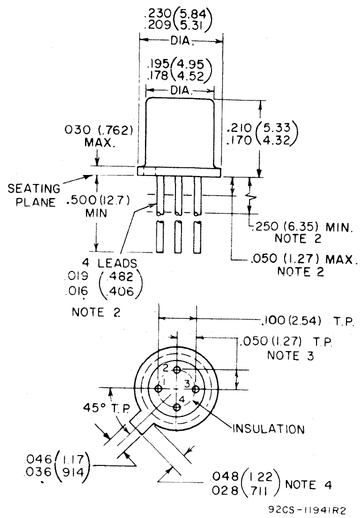
Fig. 11 – Reverse Transadmittance (y_{re})

GROUP A AND GROUP B QUALITY SAMPLING TESTS



ITEM	TEST DESCRIPTION	LTPD
GROUP A TESTS		
Subgroup 1.	Visual and Mechanical Examination	5%
Subgroup 2.	Electrical	10%
GROUP B TESTS		
Subgroup 1.	Physical Dimensions	20%
Subgroup 2.	Solderability, Temperature Cycling, Thermal Shock, Moisture Resistance	20%
Subgroup 3.	Shock, Vibration Fatigue, Vibration Variable Frequency, Constant Acceleration	20%
Subgroup 4.	Terminal Strength	20%
Subgroup 5.	Salt Atmosphere	20%
Subgroup 6.	High-Temperature Life, Non-Operating ($T_A = 200°C$)	$\lambda = 10\%$
Subgroup 7.	Steady-State-Operation Life ($P_D = 300mW$, $T_A = 25°C$)	$\lambda = 10\%$

DIMENSIONAL OUTLINE
JEDEC TO-72



Dimensions in inches and millimeters

Note 1: *Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.*

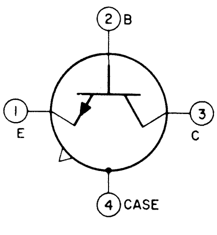
Note 2: The specified lead diameter applies in the zone between 0.050" (1.27 mm) and 0.250" (6.35 mm) from the seating plane. From 0.250" (6.35 mm) to the end of the lead a maximum diameter of 0.021" (0.533 mm) is held. Outside of these zones, the lead diameter is not controlled.

Note 3: Leads having a maximum diameter of 0.019" (0.482 mm) at a gauging plane of 0.054" (1.372 mm) + 0.001" (0.025 mm) - 0.000" (0.000 mm) below seating plane shall be within 0.007" (0.177 mm) of their true position (location) relative to a maximum width of tab.

Note 4: Measured from actual maximum diameter.

TERMINAL DIAGRAM
Bottom View

LEAD 1 – EMITTER
LEAD 2 – BASE

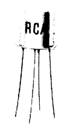


LEAD 3 – COLLECTOR
LEAD 4 – CONNECTED TO CASE

RCA Solid State Division

RF Power Transistors

40894 40896
40895 40897



JEDEC TO-72 H-1299

High - Frequency Silicon N-P-N Transistors

For TV-Tuner, FM and AM/FM "Front-End", and IF Amplifier, Oscillator, and Converter Service

Features:

- **High gain-bandwidth products:**
  f_T = 1200 MHz typ. for tuner types
  = 800 MHz typ. for if-amplifier types
- **Very low collector-to-base feedback capacitance:**
  C_{cb} = 0.7 pF typ. for 40894, 40895
- **Low noise figure:**
  3 dB typ. at 200 MHz for rf amplifier type
- **High power gain as neutralized amplifier:**
  G_{PE} = 15 dB min. at 200 MHz (40894)
- **High power output as uhf oscillator:**
  P_{OE} = 20 mW typ. at 500 MHz (40896)
- **Low noise figure:**
  NF = 4.5 dB max. at 200 MHz (40894)
- **Low collector-to-base time constant:**
  $r_b'C_c$ = 14 ps max.

RCA-40894, 40895, 40896, and 40897 are high-frequency n-p-n silicon devices characterized especially for rf, mixer, oscillator, and if stages of vhf, SSB, and FM receivers.

These devices utilize a hermetically sealed four-lead JEDEC TO-72 package. All active elements of the transistor are insulated from the case, which may be grounded by means of the fourth lead in applications requiring minimum feedback capacitance, shielding of the device, or both.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-EMITTER VOLTAGE	V_{CEO}	12	V
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	20	V
EMITTER-TO-BASE VOLTAGE	V_{EBO}	2.5	V
CONTINUOUS COLLECTOR CURRENT	I_C	50	mA
TRANSISTOR DISSIPATION	P_T		
With heat sink, at case temperatures up to 25°C		300	mW
With heat sink, at case temperatures above 25°C		Derate linearly 1.71	mW/°C
At ambient temperatures up to 25°C		200	mW
At ambient temperatures above 25°C		Derate linearly 1.14	mW/°C
TEMPERATURE RANGE:			
Storage & Operating (Junction)		-65 to +200	°C
CASE TEMPERATURE (During soldering):			
At distances ⩾ 1/32 in. (0.8 mm) from seating surface for 10 seconds max.		265	°C

ELECTRICAL CHARACTERISTICS at Ambient Temperature (T_A) = 25°C unless otherwise specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS							LIMITS												UNITS
		FREQUENCY MHz	DC COLLECTOR OR EMITTER VOLTAGE V			DC CURRENT mA			TYPE 40894 RF AMPLIFIER			TYPE 40895 MIXER			TYPE 40896 OSCILLATOR			TYPE 40897 IF AMPLIFIER			
			V_{CB}	V_{CE}	V_{EB}	I_E	I_C	I_B	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Collector-Cutoff Current	I_{CBO}		15			0			-	-	0.02	-	-	0.02	-	-	0.02	-	-	0.02	μA
T_A = 150°C			15			0			-	-	1	-	-	1	-	-	1	-	-	1	
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$					0	0.001		20	-	-	20	-	-	20	-	-	20	-	-	V
Collector-to-Emitter Sustaining Voltage	$V_{CEO}(sus)$						3	0	15	-	-	15	-	-	15	-	-	15	-	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$					0.01	0		2.5	-	-	2.5	-	-	2.5	-	-	2.5	-	-	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$						10	1	-	-	0.4	-	-	0.4	-	-	0.4	-	-	0.4	V
Base-to-Emitter Saturation Voltage	$V_{BE}(sat)$						10	1	-	-	1	-	-	1	-	-	1	-	-	1	V
Static Forward Current-Transfer Ratio	h_{FE}			6			1		50	80	250	40	70	250	27	50	250	70	120	250	
Magnitude of Common-Emitter, Small-Signal Short-Circuit, Forward Current Transfer Ratio[a]	h_{fe}	100 1 kHz		6 6			5 2		9 25	14 90	20 300	9 25	14 90	20 300	9 25	14 90	20 300	9 25	14 90	20 300	
Collector-to-Base Feedback Capacitance[b]	C_{cb}	0.1 to 1	10			0			-	0.7	1	-	0.7	1	-	0.7	1	-	0.7	1	pF
Common-Base Input Capacitance[c]	C_{ib}	0.1 to 1			0.5		0		-	-	2	-	-	2	-	-	2	-	-	2	pF
Collector-to-Base Time Constant[a]	$r_b'C_c$	31.9	6				2		3	7	14	3	7	14	3	7	14	3	7	14	ps
Small-Signal Power Gain in Neutralized Common-Emitter Amplifier Circuit[a] (see Fig. 6)	G_{PE}	10.7 200		12 12			5 5		- 15	- 21	- -	- 15	- 21	- -	- 15	- 21	- -	18 -	25 -	- -	dB
Noise Figure[a]	NF	200		6			1.5		-	3	4.5	-	-	-	-	-	-	-	-	-	dB

[a] Lead No. 4 (case) grounded; R_g = 125Ω

[b] Three-terminal measurement of the collector-to-base capacitance with the case and emitter leads connected to the guard terminal.

[c] Lead No. 4 (case) floating.

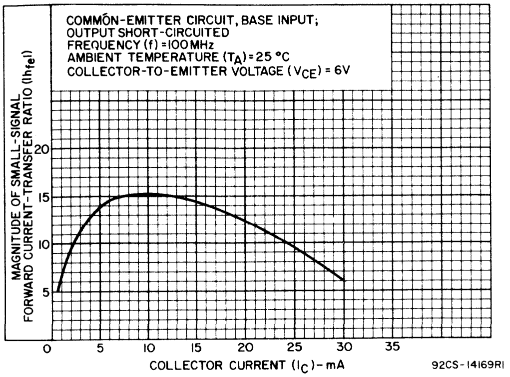


Fig. 1–Small-signal beta characteristic for all types

TWO-PORT ADMITTANCE (y) PARAMETERS AS FUNCTIONS OF FREQUENCY (f) FOR ALL TYPES

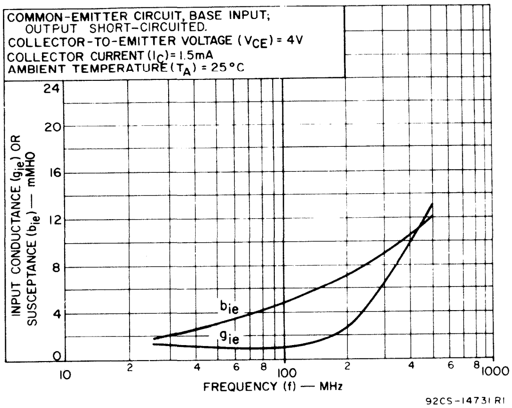


Fig. 2–Input admittance (y_{ie})

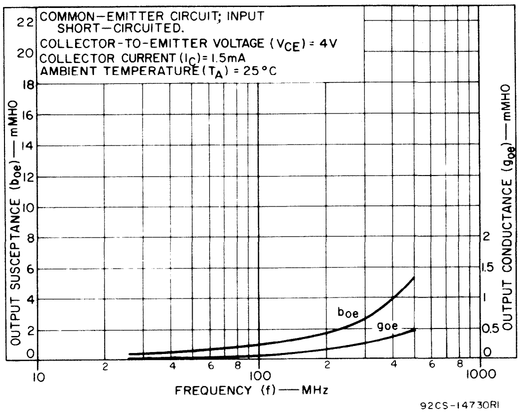


Fig. 3–Output admittance (y_{oe})

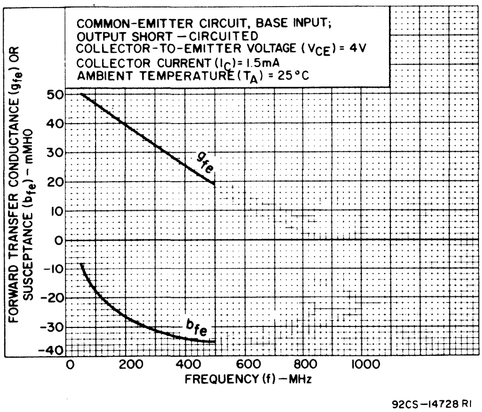


Fig. 4–Forward transadmittance (y_{fe})

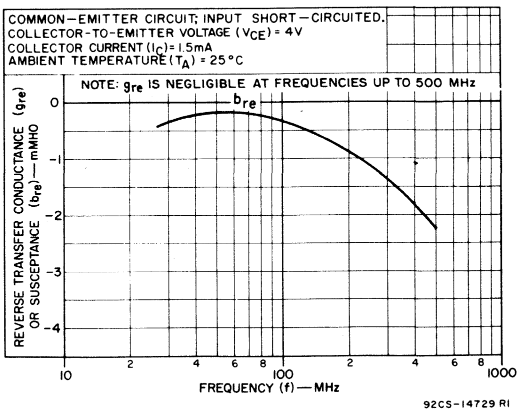
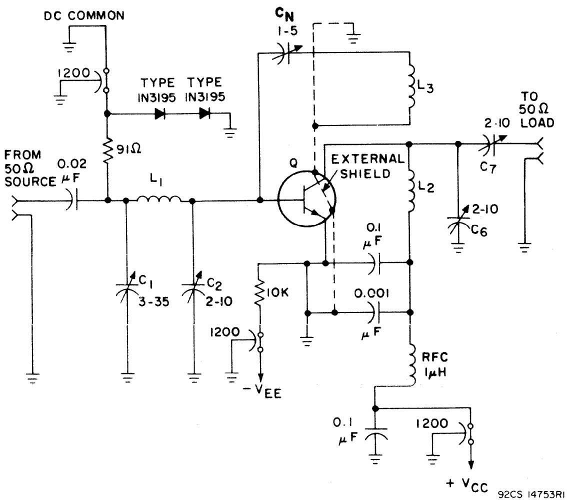


Fig. 5–Reverse transadmittance (y_{re})



NOTE: (Neutralization Procedure): (a) Connect a 50-Ω rf voltmeter to the output of a 200-MHz signal generator (R_g = 50Ω), and adjust the generator output to 5 mV. (b) Connect the generator to the input and the rf voltmeter to the output of the amplifier, as shown above. (c) Apply V_{EE} and V_{CC}, and adjust the generator output to provide an amplifier output of 5 mV. (d) Tune C2, C6, and C7 for maximum amplifier output, readjusting the generator output as required to maintain an output of 5 mV from the amplifier. (e) Interchange the connections to the signal generator and the rf voltmeter. (f) With sufficient signal applied to the output terminals of the amplifier, adjust C_N for a minimum indication at the amplifier input. (g) Repeat steps (a), (b), (c), and (d) to determine if retuning is necessary.

Q = Type 40894, 40895, 40896, or 40897

L_1: 1-3/4 turns No. 18 wire 0.5 in. (12.7 mm) long, 0.5 in. (12.7 mm) ID

L_2: 2 turns No. 16 wire, 0.5 in. (12.7 mm) long, 0.5 in. (12.7 mm) ID

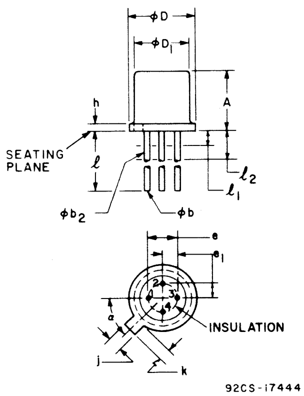
L_3: 2 turns No. 18 wire, 0.25 in. (6.35 mm) long, 0.5 in. (12.7 mm) ID. Position approximately 1/4 in. (6.35 mm) from L_2.

All capacitances in pF unless otherwise specified.

Fig. 6—Neutralized amplifier circuit used to measure power gain and noise figure at 200 MHz for all types

DIMENSIONAL OUTLINE

JEDEC TO–72



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	0.170	0.210	4.32	5.33	
φb	0.016	0.021	0.406	0.533	2
φb2	0.016	0.019	0.406	0.483	2
φD	0.209	0.230	5.31	5.84	
φD1	0.178	0.195	4.52	4.95	
e	0.100 T.P.		2.54 T.P.		4
e1	0.050 T.P.		1.27 T.P.		4
h		0.030		0.762	
j	0.036	0.046	0.914	1.17	
k	0.028	0.048	0.711	1.22	3
l	0.500		12.70		2
l1		0.050		1.27	2
l2	0.250		6.35		2
α	45° T.P.		45° T.P.		4, 6

Note 1: (Four leads). Maximum number leads omitted in this outline, "none" (0). The number and position of leads actually present are indicated in the product registration. Outline designation determined by the location and minimum angular or linear spacing of any two adjacent leads.

Note 2: (All leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and 0.50 in. (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond 0.50 in. (12.70 mm) from seating plane.

Note 3: Measured from maximum diameter of the product.

Note 4: Leads having maximum diameter 0.019 in. (0.484 mm) measured in gaging plane 0.054 in. (1.37 mm) +0.001 in. (0.025 mm) – 0.000 (0.000 mm) below the seating plane of the product shall be within 0.007 in. (0.178 mm) of their true position relative to a maximum width tab.

Note 5: The product may be measured by direct methods or by gage.

Note 6: Tab centerline.

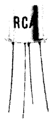
TERMINAL CONNECTIONS

Lead 1 – Emitter
Lead 2 – Base
Lead 3 – Collector
Lead 4 – Connected to case

Solid State
Division

RF Transistors

40915



JEDEC TO-72 H-1299

0.2-to-1.4-GHz Low-Noise Silicon N-P-N Transistor

For High-Gain Small-Signal Applications

Features:

- **Low noise figure:**
  NF = 2.5 dB (max.) with 11 dB gain at 450 MHz
  = 3.0 dB (typ.) at 890 MHz
  = 4.5 dB (typ.) at 1.3 GHz
- **High gain (tuned, unneutralized):**
  G_{PE} = 14 dB (min.) at 450 MHz
  = 6.5 dB (typ.) at 1.3 GHz
- **High gain-bandwidth product**
- **Large dynamic range**
- **Low distortion**

RCA-40915* is an epitaxial silicon n-p-n planar transistor intended for low-power, small-signal applications where both low noise and high gain are desirable. It utilizes a hermetically sealed four-lead JEDEC TO-72 package. All of the elements of the transistor are insulated from the case, which may be grounded by means of the fourth lead.

*Formerly RCA Dev. No. TA8104.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Collector-to-Base Voltage	V_{CBO}	35	V
Collector-to-Emitter Voltage	V_{CEO}	15	V
Emitter-to-Base Voltage	V_{EBO}	3.5	V
Collector Current (Continuous)	I_C	40	mA
Transistor Dissipation:	P_T		
At ambient temperatures up to 25°C		200	mW
At ambient temperatures above 25°C		Derate linearly at 1.14 mW/°C	
Temperature Range:			
Storage and Operating (Junction)		−65 to +200	°C

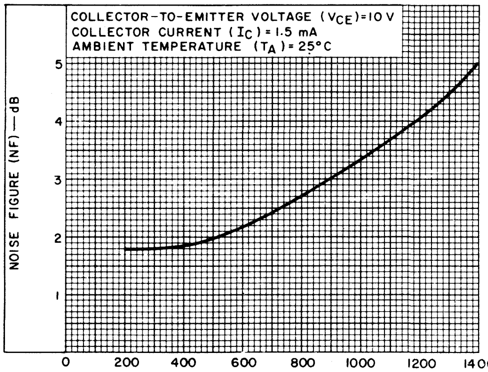


Fig. 1—Typical noise figure vs. frequency.

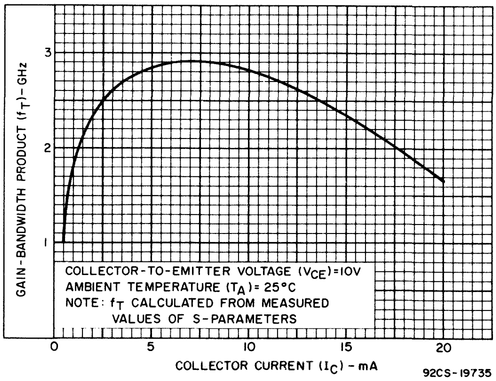


Fig.2—Gain-bandwidth product vs. collector current.

ELECTRICAL CHARACTERISTICS at Ambient Temperature (T_A) = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: DC COLLECTOR VOLTAGE (V)		DC CURRENT (mA)			LIMITS		UNITS
		V_{CB}	V_{CE}	I_E	I_B	I_C	MIN.	MAX.	
STATIC									
Collector-Cutoff Current	I_{CBO}	10		0			–	20	nA
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		0.01	35	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$				0	0.1	15	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.01		0	3.5	–	V
DC Forward-Current Transfer Ratio	h_{FE}		10			3	20	–	–
Thermal Resistance: (Junction-to-Ambient)	$R_{\theta JA}$						–	880	°C/W
DYNAMIC									
Device Noise Figure (f = 450 MHz)	NF		10			1.5	–	2.5	dB
Small-Signal Common-Emitter Power Gain (f = 450 MHz) Unneutralized Amplifier	G_{PE}		10			1.5	14	–	dB
At minimum noise figure	G_{PE}		10			1.5	11.0	–	dB
Collector-to-Base Output Capacitance (f = 1 MHz)	C_{obo}	10		0			–	1.0	pF

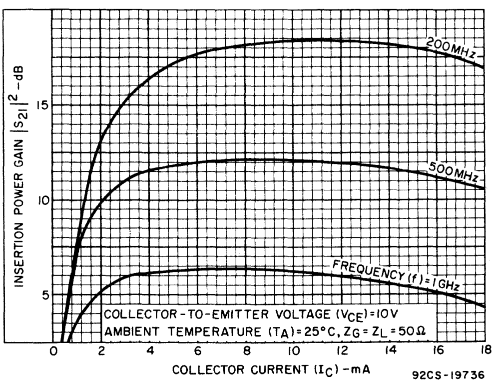


Fig.3—Typical insertion power gain vs. collector current.

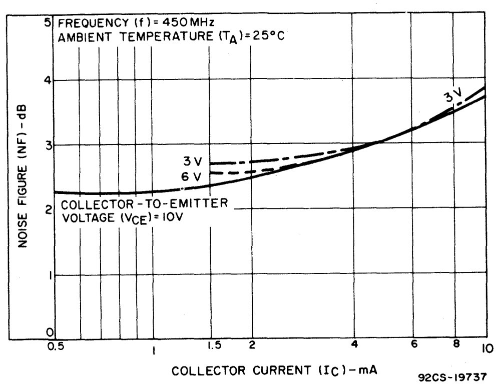


Fig.4—Typical noise figure vs. collector current.

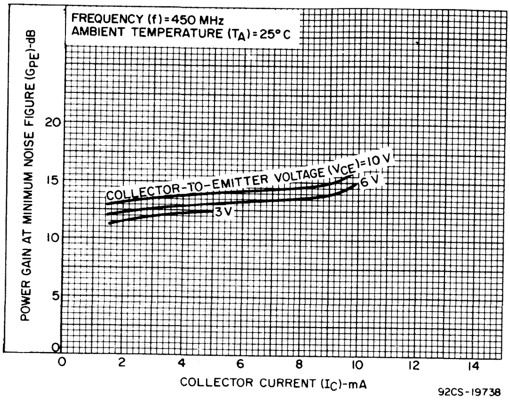


Fig.5—Typical power gain (at minimum noise figure) vs. collector current.

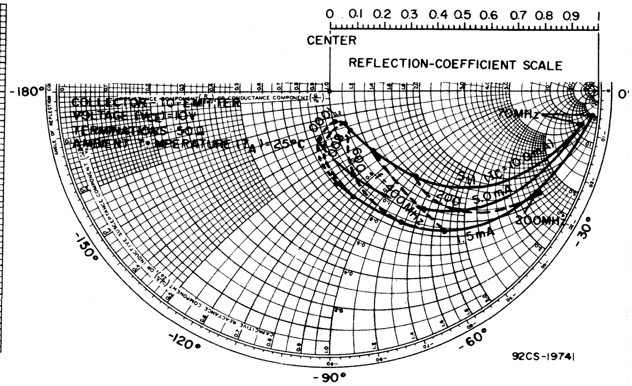


Fig.8—Typical input reflection coefficient.

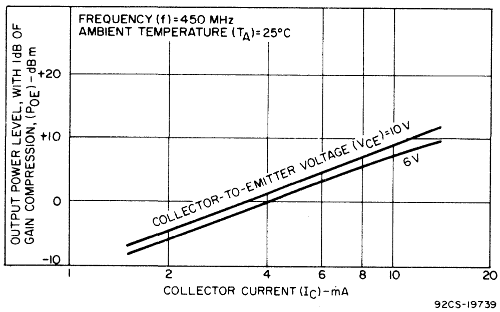


Fig.6—Typical output power level (with 1 dB of gain compression) vs. collector current.

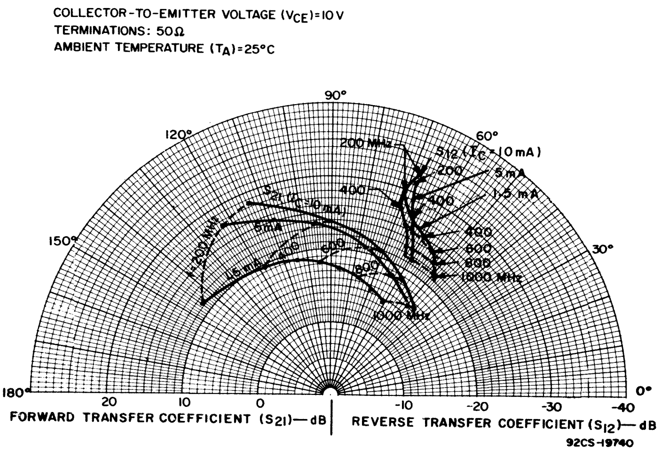
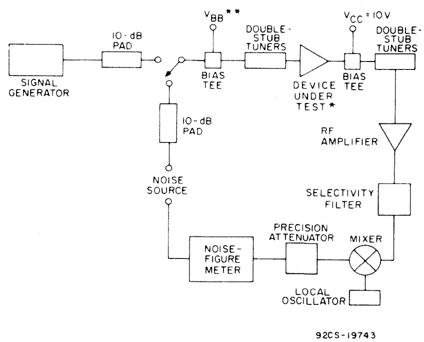


Fig.7—Typical forward and reverse transfer coefficients.



* In General Radio type 1607-P44 transistor mount, or equivalent.

** V_{BB} adjusted for I_C = 1.5 mA.

Fig.9—Block diagram of test setup for measurement of power gain and noise figure.

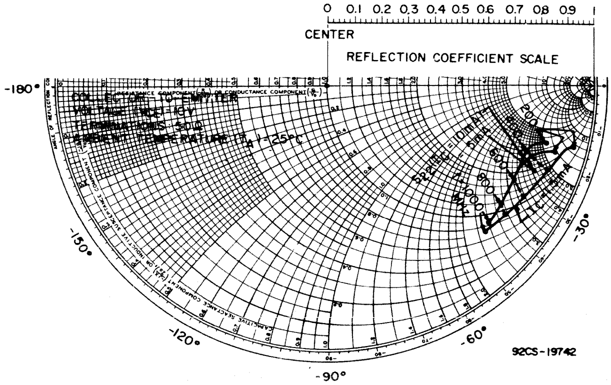
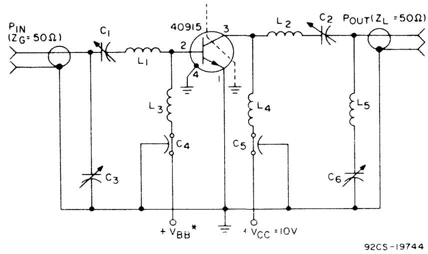


Fig. 10—Typical output reflection coefficient.



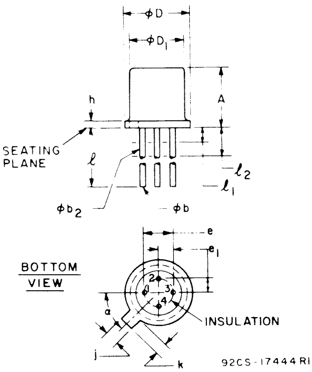
C_1: 1.0- 30 pF
C_2,C_3: 1.0-20 pF
C_4,C_5: 0.04 μF
C_6: 1-10 pF

L_1: 2 turns No. 18 wire, 3/16 in. (0.188 mm) ID, 0.10 in. (2.54 mm) long
L_2: 3 turns No. 18 wire, 3/16 in. (0.188 mm) ID, 0.15 in. (3.81 mm) long
L_3,L_4: 0.22-μH rf choke
L_5: 3 turns No. 18 wire, 3/16 in. (0.188 mm) ID, 0.15 in. (3.81 mm) long

* V_{BB} adjusted for I_C = 1.5 mA

Fig. 11—Circuit diagram of 450-MHz amplifier (unneutralized) used for measurement of power gain and noise figure.

DIMENSIONAL OUTLINE
JEDEC TO–72



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	0.170	0.210	4.32	5.33	
φb	0.016	0.021	0.406	0.533	2
φb2	0.016	0.019	0.406	0.483	2
φD	0.209	0.230	5.31	5.84	
φD1	0.178	0.195	4.52	4.95	
e	0.100 T.P.		2.54 T.P.		4
e1	0.050 T.P.		1.27 T.P.		4
h		0.030		0.762	
j	0.036	0.046	0.914	1.17	
k	0.028	0.048	0.711	1.22	3
l	0.500		12.70		2
l1		0.050		1.27	2
l2	0.250		6.35		2
α	45 T.P.		45 T.P.		4, 6

TERMINAL CONNECTIONS

Lead 1 – Emitter
Lead 2 – Base
Lead 3 – Collector
Lead 4 – Case

Note 1: (Four leads). Maximum number leads omitted in this outline, "none" (0). The number and position of leads actually present are indicated in the product registration. Outline designation determined by the location and minimum angular or linear spacing of any two adjacent leads.

Note 2: (All leads) φb_2 applies between l_1 and l_2. φb applies between l_2 and 0.50 in. (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond 0.50 in. (12.70 mm) from seating plane.

Note 3: Measured from maximum diameter of the product.

Note 4: Leads having maximum diameter 0.019 in. (0.484 mm) measured in gaging plane 0.054 in. (1.37 mm) +0.001 in. (0.025 mm) – 0.000 in. (0.000 mm) below the seating plane of the product shall be within 0.007 in. (0.178 mm) of their true position relative to a maximum width tab.

Note 5: The product may be measured by direct methods or by gage.

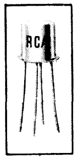
Note 6: Tab centerline.

RCA
Solid State Division

RF Power Transistors

2N2857

SILICON N-P-N EPITAXIAL PLANAR TRANSISTOR



JEDEC TO-72

For UHF Applications in Industrial and Military Equipment

RCA-2N2857 is a double-diffused epitaxial planar transistor of the silicon n-p-n type. It is extremely useful in low-noise-amplifier, oscillator, and converter applications at frequencies up to 500 MHz in the common-emitter configuration, and up to 1200 MHz in the common-base configuration.

The 2N2857 utilizes a hermetically sealed four-lead JEDEC TO-72 package. All active elements of the transistor are insulated from the case, which may be grounded by means of the fourth lead in applications requiring shielding of the device.

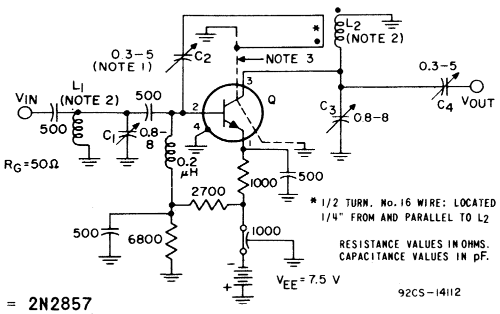
Maximum Ratings, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	30 max.	V
COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO}	15 max.	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}	2.5 max.	V
COLLECTOR CURRENT, I_C	40 max.	mA
TRANSISTOR DISSIPATION, P_T:		
At case temperatures* up to 25° C.	300 max.	mW
At case temperatures* above 25° C.	Derate at 1.72	mW/°C
At ambient temperatures up to 25°C.	200 max.	mW
At ambient temperatures above 25° C.	Derate at 1.14	mW/°C
TEMPERATURE RANGE:		
Storage and Operating (Junction)	-65 to +200	°C
LEAD TEMPERATURE (During soldering): At distances ≥ 1/32 inch from seating surface for 10 seconds max	265 max.	°C

* Measured at center of seating surface.

FEATURES

- high gain-bandwidth product— f_T = 1000 MHz min.
- high converter (450-to-30 MHz) gain— G_c = 15 dB typ. for circuit bandwidth of approximately 2 MHz
- high power gain as neutralized amplifier— G_{pe} = 12.5 dB min. at 450 MHz for circuit bandwidth of 20 MHz
- high power output as uhf oscillator— P_o = { 30 mW min., 40 mW typ. at 500 MHz; 20 mW typ., at 1 GHz }
- low device noise figure— NF = { 4.5 dB max. as 450 MHz amplifier; 7.5 dB typ. as 450-to-30 MHz converter }
- low collector-to-base time constant — $r_b'C_c$ = 7 ps typ.
- low collector-to-base feedback capacitance— C_{cb} = 0.6 pF typ.



Q = 2N2857

NOTE 1: (NEUTRALIZATION PROCEDURE): (A) CONNECT A 450-MHz SIGNAL GENERATOR (WITH R_G = 50 Ω) TO THE INPUT TERMINALS OF THE AMPLIFIER. (B) CONNECT A 50-Ω RF VOLTMETER ACROSS THE OUTPUT TERMINALS OF THE AMPLIFIER. (C) APPLY V_{EE}, AND WITH THE SIGNAL GENERATOR ADJUSTED FOR 5 mV OUTPUT FROM THE AMPLIFIER, TUNE C_1, C_3, AND C_4 FOR MAXIMUM OUTPUT. (D) INTERCHANGE THE CONNECTIONS TO THE SIGNAL GENERATOR AND THE RF-VOLTMETER. (E) WITH SUFFICIENT SIGNAL APPLIED TO THE OUTPUT TERMINALS OF THE AMPLIFIER, ADJUST C_2 FOR A MINIMUM INDICATION AT THE INPUT. (F) REPEAT STEPS (A), (B), AND (C) TO DETERMINE IF RETUNING IS NECESSARY.

NOTE 2: L_1 & L_2 — SILVER-PLATED BRASS ROD, 1-1/2" LONG x 1/4" DIA. INSTALL AT LEAST 1/2" FROM NEAREST VERTICAL CHASSIS SURFACE.

NOTE 3: EXTERNAL INTERLEAD SHIELD TO ISOLATE THE COLLECTOR LEAD FROM THE EMITTER AND BASE LEADS.

Fig. 1 - Neutralized amplifier circuit used to measure 450 MHz power gain and noise figure for type 2N2857.

9-66

ELECTRICAL CHARACTERISTICS, *At an Ambient Temperature, $T_A = 25^o$ C, Unless Otherwise Specified*

Characteristic	Symbol	Frequency f	TEST CONDITIONS: DC Collector-to-Base Voltage V_{CB}	DC Collector-to-Emitter Voltage V_{CE}	DC Emitter-to-Base Voltage V_{EB}	DC Emitter Current I_E	DC Base Current I_B	DC Collector Current I_C	LIMITS Type 2N2857 Min.	Typ.	Max.	Units
		MHz	V	V	V	mA	mA	mA	Min.	Typ.	Max.	
Collector-Cutoff Current	I_{CBO}	$T_A = 25^oC$ $T_A = 150^oC$	15 15			0 0			-	-	10 1.0	nA µA
Collector-to-Base Breakdown Voltage	BV_{CBO}					0		0.001	30	-	-	V
Collector-to-Emitter Breakdown Voltage	BV_{CEO}						0	3	15	-	-	V
Emitter-to-Base Breakdown Voltage	BV_{EBO}					-0.01		0	2.5	-	-	V
Static Forward-Current Transfer Ratio	h_{FE}			1				3	30	-	150	
Small-Signal Forward-Current Transfer Ratio	h_{fe}	0.001[c] 100[c]		6 6				2 5	50 10	- -	220 19	
Collector-to-Base Feedback Capacitance	C_{cb}	0.1 to 1[b]	10			0			-	0.6	1.0	pF
Input Capacitance	C_{ib}	0.1 to 1[a]			0.5			0	-	1.4	-	pF
Collector-to-Base Time Constant	$r_b'C_c$	31.9[c]	6			-2			4	7	15	ps
Small-Signal, Common-Emitter Power Gain in Neutralized Amplifier Circuit (See Fig. 1)	G_{pe}	450[c]		6				1.5	12.5	-	19	dB
Power Output as Oscillator (See Fig. 2)	P_O	$\geq$ 500[a]	10			-12			30	-	-	mW
UHF Device Noise Figure	NF	450[c,d,f]		6				1.5	-	3.8	4.5	dB
UHF Measured Noise Figure	NF	450[c,d]		6				1.5	-	-	5.0	dB
VHF Device Noise Figure	NF	60[b,d]		6				1	-	2.2	-	dB

[a] Fourth lead (case) not connected

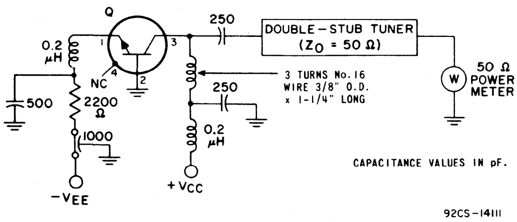
[b] Three-terminal measurement: Lead No. 1 (Emitter) and lead No. 4 (Case) connected to guard terminal.

[c] Fourth lead (case) grounded.

[d] Generator resistance, R_g = 50 ohms.

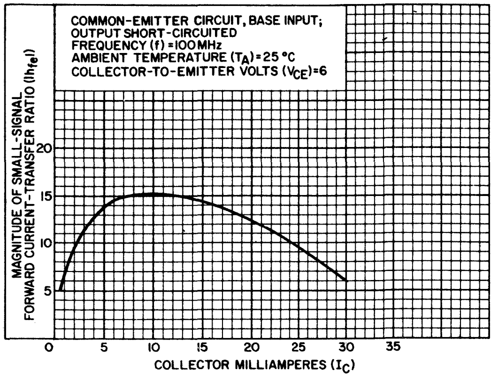
[e] Generator resistance, R_g = 400 ohms.

[f] Device noise figure is approximately 0.5 dB lower than the measured noise figure. The difference is due to the insertion loss at the input of the test circuit (0.25 dB) and the contribution of the following stages in the test set-up (0.25 dB).



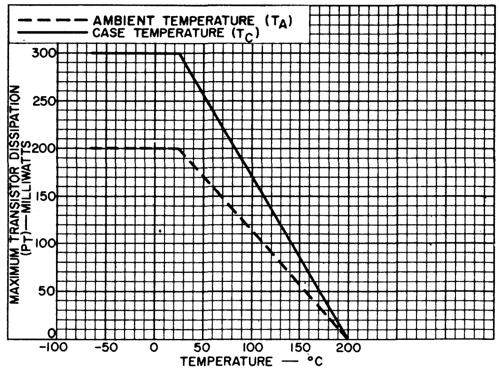
Q = 2N2857

Fig. 2 - Oscillator circuit used to measure 500-MHz power output for type 2N2857.



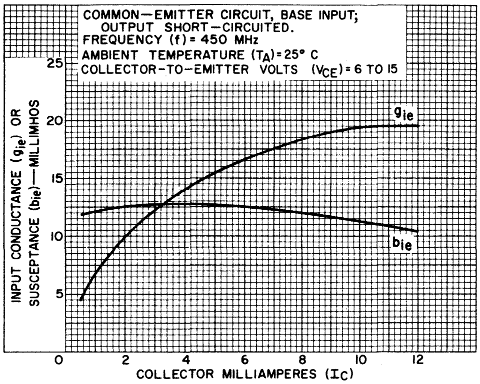
92CS-14169

Fig.3 - Small-signal beta characteristic for type 2N2857.



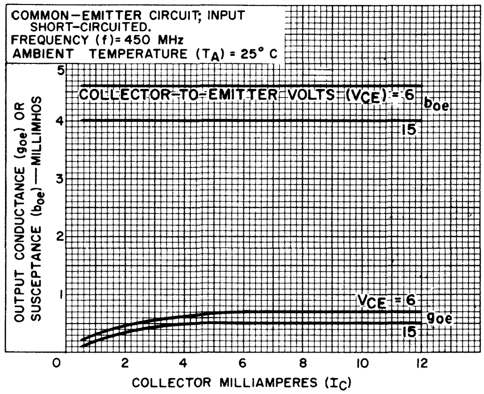
92CS-12483R1

Fig.4 - Rating chart for type 2N2857.



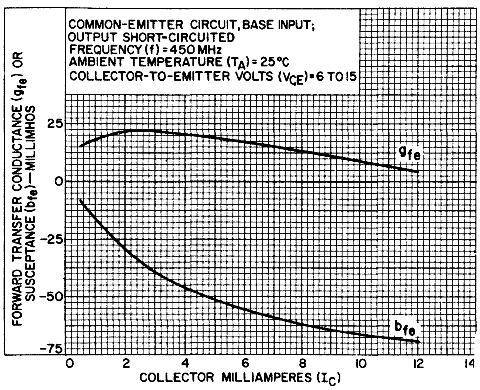
92CS-12150R1

Fig.5 - Input admittance (y_{ie}).



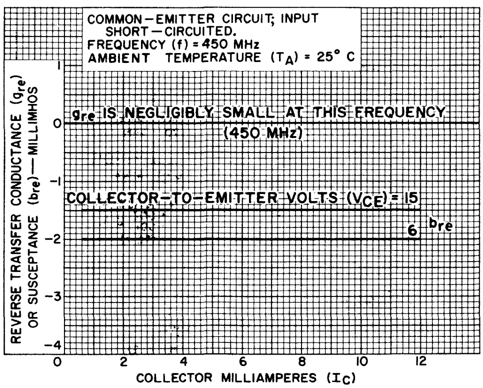
92CS-12148R1

Fig.6 - Output admittance (y_{oe}).



92CS-12149R1

Fig.7 - Forward transadmittance (y_{fe}).



92CS-12154R2

Fig.8 - Reverse transadmittance (y_{re}).

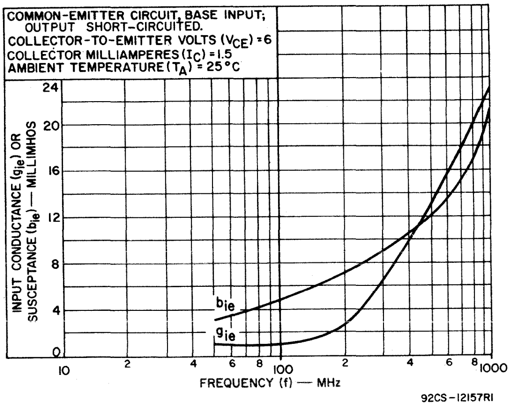


Fig.9 - Input admittance (y_{ie}).

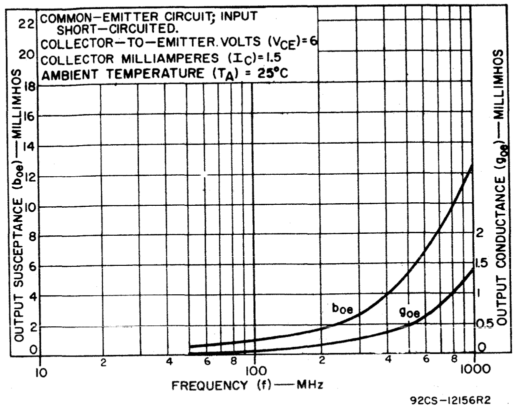


Fig. 10 - Output admittance (y_{oe}).

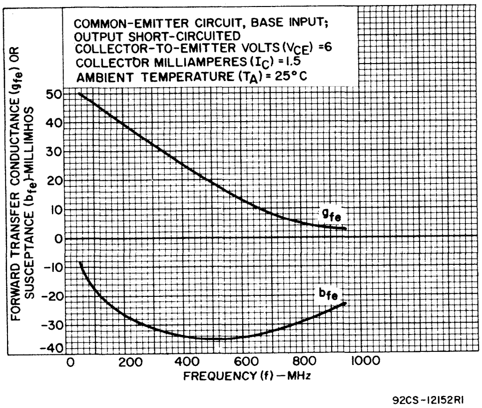


Fig. 11 - Forward transadmittance (y_{fe}).

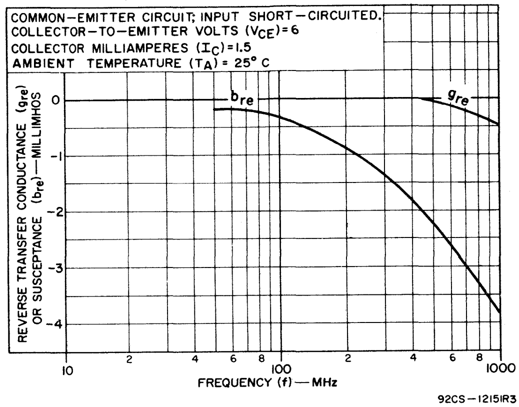
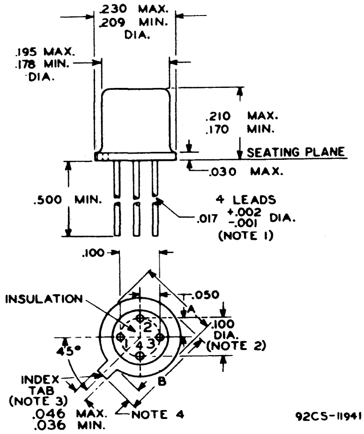


Fig. 12 - Reverse transadmittance (y_{re}).

DIMENSIONAL OUTLINE

JEDEC TO-72



NOTE 1: THE SPECIFIED LEAD DIAMETER APPLIES IN THE ZONE BETWEEN 0.050" AND 0.250" FROM THE SEATING PLANE. FROM 0.250" TO THE END OF THE LEAD A MAXIMUM DIAMETER OF 0.021" IS HELD. OUTSIDE OF THESE ZONES, THE LEAD DIAMETER IS NOT CONTROLLED.

NOTE 2: MAXIMUM DIAMETER LEADS AT A GAUGING PLANE 0.054" + 0.001" − 0.000" BELOW SEATING PLANE TO BE WITHIN 0.007" OF THEIR TRUE LOCATION RELATIVE TO MAX. WIDTH TAB AND TO THE MAXIMUM 0.230" DIAMETER MEASURED WITH A SUITABLE GAUGE. WHEN GAUGE IS NOT USED, MEASUREMENT WILL BE MADE AT SEATING PLANE.

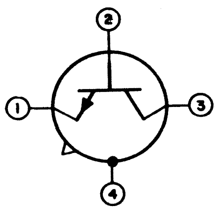
NOTE 3: FOR VISUAL ORIENTATION ONLY.

NOTE 4: TAB LENGTH TO BE 0.028" MINIMUM − 0.048" MAXIMUM, AND WILL BE DETERMINED BY SUBTRACTING DIAMETER A FROM DIMENSION B.

TERMINAL DIAGRAM

Bottom View

LEAD 1 – EMITTER
LEAD 2 – BASE
LEAD 3 – COLLECTOR
LEAD 4 – CONNECTED TO CASE



RCA Solid State Division

RF Power Transistors

2N3839

RCA-2N3839* is a double-diffused epitaxial planar transistor of the silicon n-p-n type. It is extremely useful in low-noise-amplifier, oscillator, and converter applications at frequencies up to 500 MHz in the common-emitter configuration, and up to 1200 MHz, in the common-base configuration.

The 2N3839 is mechanically and electrically like the 2N2857, but has a substantially lower noise figure.

The 2N3839 utilizes a hermetically sealed four-lead JEDEC TO-72 package. All active elements of the transistor are insulated from the case, which may be grounded by means of the fourth lead in applications requiring shielding of the device.

Maximum Ratings, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	30 max.	V
COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO}	15 max.	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}	2.5 max.	V
COLLECTOR CURRENT, I_C	40 max.	mA
TRANSISTOR DISSIPATION, P_T:		
For operation with heat sink:		
At case temperatures** up to 25°C	300 max.	mW
At case temperatures** above 25°C	Derate at 1.72	mW/°C
For operation at ambient temperatures:		
At ambient temperatures up to 25°C	200 max.	mW
At ambient temperatures above 25°C	Derate at 1.14	mW/°C
TEMPERATURE RANGE:		
Storage and Operating (Junction)	-65 to +200	°C
LEAD TEMPERATURE (During Soldering):		
At distances ≥ 1/32 inch from seating surface for 10 seconds max.	265 max.	°C

* **Formerly Dev. No. TA-2363**

** Measured at center of seating surface.

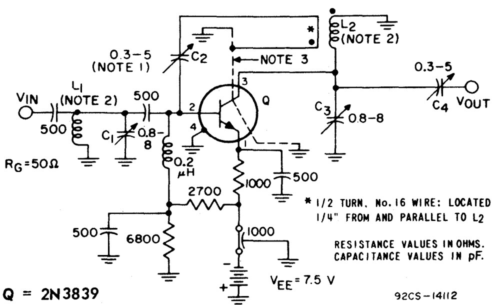
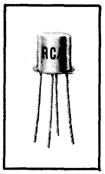


Fig.1 - Neutralized amplifier circuit used to measure 450-MHz power gain and noise figure for type 2N3839.

SILICON N-P-N EPITAXIAL PLANAR TRANSISTOR



JEDEC TO-72

For Low-Noise UHF Applications in Industrial and Military Equipment

FEATURES

- very low device noise figure —
  NF = 3.4 dB max. as 450-MHz amplifier
- high gain-bandwidth product —
  f_T = 1000 MHz min.
- high converter (450-to-30 MHz) gain —
  G_c = 15 dB typ. for circuit bandwidth of approximately 2 MHz
- high power gain as neutralized amplifier —
  G_{pe} = 12.5 dB min. at 450 MHz for circuit bandwidth of 20 MHz
- high power output as UHF oscillator —
  P_o = 30 mW min., 40 mW typ. at 500 MHz
  = 20 mW typ. at 1 GHz
- low collector-to-base time constant —
  $r_b'C_c$ = 7 ps typ.
- low collector-to-base feedback capacitance —
  C_{cb} = 0.6 pF typ.

NOTE 1: (NEUTRALIZATION PROCEDURE): (A) CONNECT A 450-MHz SIGNAL GENERATOR (WITH R_g = 50 OHMS) TO THE INPUT TERMINALS OF THE AMPLIFIER. (B) CONNECT A 50-OHM RF VOLTMETER ACROSS THE OUTPUT TERMINALS OF THE AMPLIFIER. (C) APPLY V_{EE}, AND WITH THE SIGNAL GENERATOR ADJUSTED FOR 5 mV OUTPUT FROM THE AMPLIFIER, TUNE C_1, C_3, AND C_4 FOR MAXIMUM OUTPUT. (D) INTERCHANGE THE CONNECTIONS TO THE SIGNAL GENERATOR AND THE RF VOLTMETER. (E) WITH SUFFICIENT SIGNAL APPLIED TO THE OUTPUT TERMINALS OF THE AMPLIFIER, ADJUST C_2 FOR A MINIMUM INDICATION AT THE INPUT. (F) REPEAT STEPS (A), (B), AND (C) TO DETERMINE IF RETUNING IS NECESSARY.

NOTE 2: L_1 & L_2—SILVER-PLATED BRASS ROD, 1-1/2" LONG x 1/4" DIA. INSTALL AT LEAST 1/2" FROM NEAREST VERTICAL CHASSIS SURFACE.

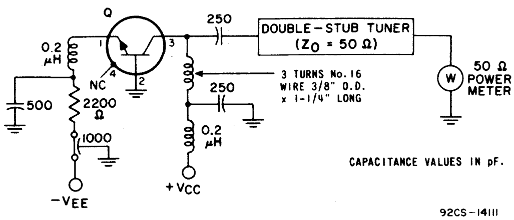
NOTE 3: EXTERNAL INTERLEAD SHIELD TO ISOLATE THE COLLECTOR LEAD FROM THE EMITTER AND BASE LEADS.

10-66

ELECTRICAL CHARACTERISTICS, *At an Ambient Temperature, T_A, of 25°C, Unless Otherwise Specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS: FREQUENCY f (MHz)	DC COLLECTOR-TO-BASE VOLTAGE V_{CB} (V)	DC COLLECTOR-TO-EMITTER VOLTAGE V_{CE} (V)	DC EMITTER-TO-BASE VOLTAGE V_{EB} (V)	DC EMITTER CURRENT I_E (mA)	DC BASE CURRENT I_B (mA)	DC COLLECTOR CURRENT I_C (mA)	LIMITS TYPE 2N3839 Min.	Typ.	Max.	UNITS
Collector-Cutoff Current T_A = 25°C	I_{CBO}		15			0			-	-	10	nA
T_A = 150°C			15			0			-	-	1.0	μA
Collector-to-Base Breakdown Voltage	BV_{CBO}					0		0.001	30	-	-	V
Collector-to-Emitter Breakdown Voltage	BV_{CEO}						0	3	15	-	-	V
Emitter-to-Base Breakdown Voltage	BV_{EBO}					0.01		0	2.5	-	-	V
Static Forward Current-Transfer Ratio	h_{FE}			1				3	30	-	150	
Small-Signal Forward Current-Transfer Ratio	h_{fe}	0.001[c]		6				2	50	-	220	
		100[c]		6				5	10	-	20	
Collector-to-Base Feedback Capacitance	C_{cb}	0.1 to 1.0[b]	10			0			-	0.6	1.0	pF
Input Capacitance	C_{ib}	0.1 to 1.0			0.5			0	-	1.4	-	pF
Collector-to-Base Time Constant	$r_b'C_c$	31.9[c]	6			-2			1	7	15	ps
Small-Signal, Common-Emitter Power Gain in Neutralized Amplifier Circuit (See *Fig.1*)	G_{pe}	450[c]		6				1.5	12.5	-	19	dB
Power Output as Oscillator (See *Fig 2*)	P_o	≥500[a]	10			-12			30	-	-	mW
UHF Measured Noise Figure (See *Fig.1*)	NF	450[c,d]		6				1.5	-	-	3.9	dB
UHF Device Noise Figure	NF	450[c,d,f]		6				1.5	-	-	3.4	dB
VHF Measured Noise Figure	NF	60[c,e]		6				1	-	2	-	dB

[a] Lead No.4 (case) not connected.
[b] 3-terminal measurement with emitter and case connected to guard terminal.
[c] Lead No.4 (case) grounded.
[d] Generator resistance, R_g = 50 ohms.
[e] Generator resistance, R_g = 400 ohms.
[f] Device noise figure is approximately 0.5 dB lower than the meas-- sured noise figure. The difference is due to the insertion loss at the input of the test circuit (0.25 dB) and the contribution of the following stages in the test setup (0.25 dB).



Q = 2N3839

Fig.2 - Oscillator circuit used to measure 500-MHz power output for type 2N3839.

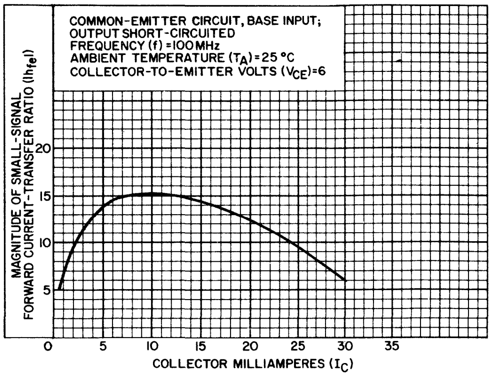


Fig.3 - Small-Signal Beta Characteristic for Type 2N3839.

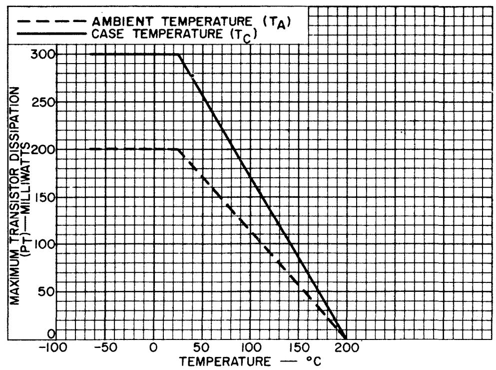


Fig.4 - Rating Chart for Type 2N3839.

TWO-PORT ADMITTANCE (y) PARAMETERS AS FUNCTIONS OF COLLECTOR CURRENT (I_C)

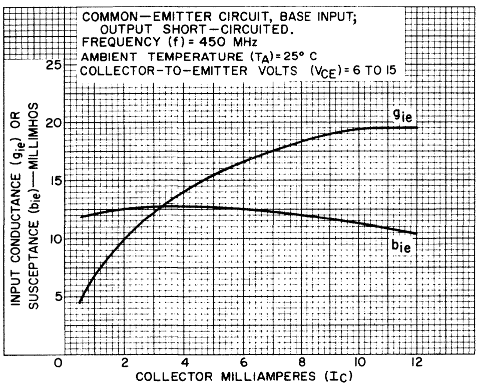


Fig.5 - Input Admittance (y_{ie}).

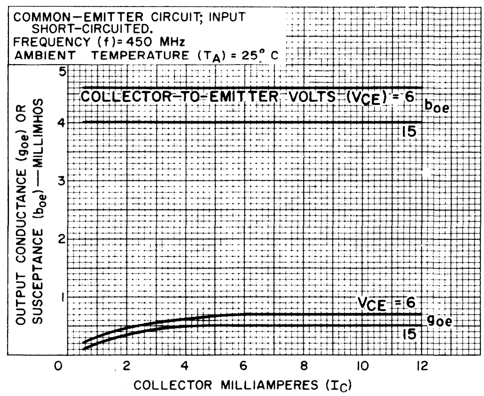


Fig.6 - Output Admittance (y_{oe}).

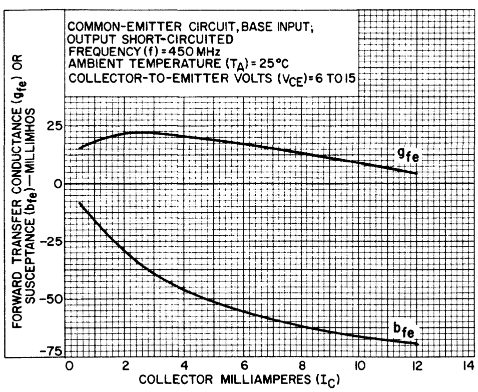


Fig.7 - Forward Transadmittance (y_{fe}).

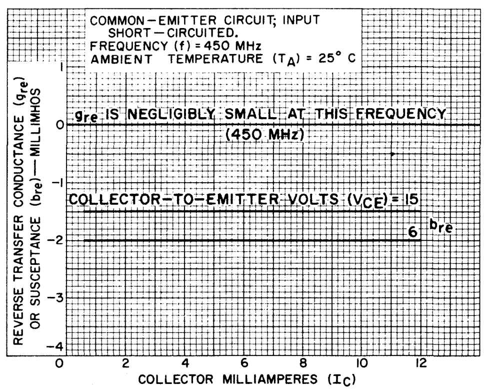


Fig.8 - Reverse Transadmittance (y_{re}).

TWO-PORT ADMITTANCE (y) PARAMETERS AS FUNCTIONS OF FREQUENCY (f)

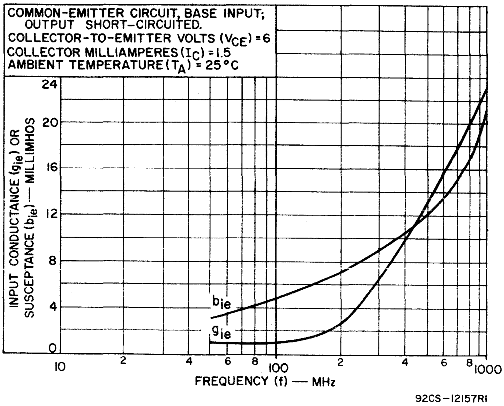


Fig.9 - Input Admittance (y_{ie}).

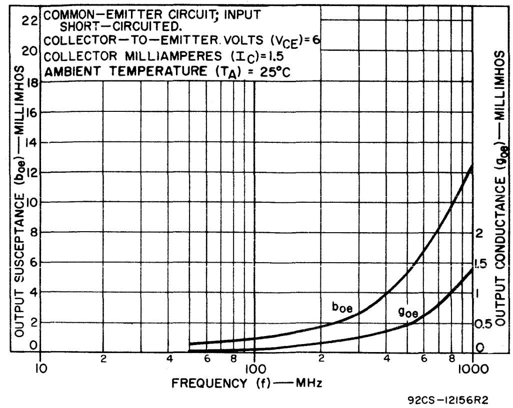


Fig.10 - Output Admittance

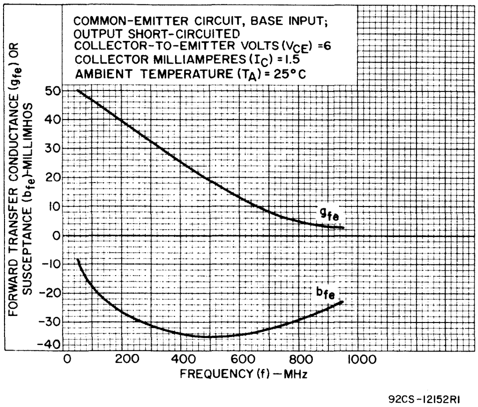


Fig.11 - Forward Transadmittance (y_{fe}).

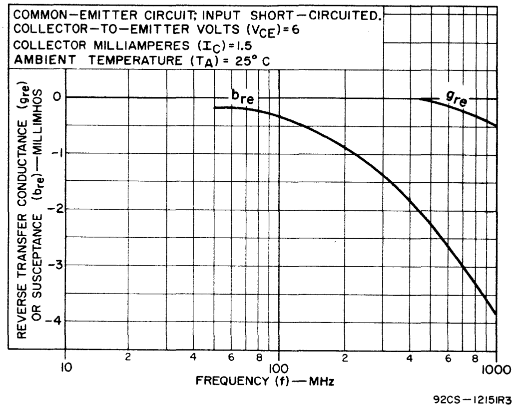
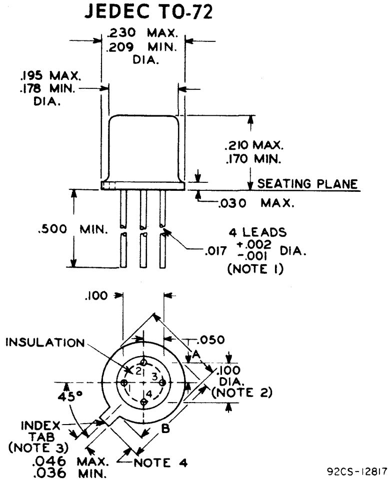
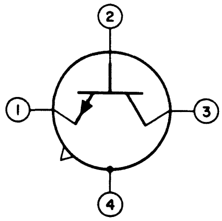


Fig.12 - Reverse Transadmittance (y_{re}).

DIMENSIONAL OUTLINE JEDEC TO-72



TERMINAL DIAGRAM Bottom View



LEAD 1 - EMITTER
LEAD 2 - BASE
LEAD 3 - COLLECTOR
LEAD 4 - CONNECTED TO CASE

Note 1: The specified lead diameter applies in the zone between 0.050" and 0.250" from the seating plane. From 0.250" to the end of the lead a maximum diameter of 0.021" is held. Outside of these zones, the lead diameter is not controlled.

Note 2: Maximum diameter leads at a gauging plane 0.054" + 0.001" - 0.000" below seating plane to be within 0.007" of their true location relative to max. width tab and to the maximum 0.230" diameter measured with a suitable gauge. When gauge is not used, measurement will be made at seating plane.

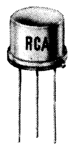
Note 3: For visual orientation only.

Note 4: Tab length to be 0.028" minimum - 0.048" maximum, and will be determined by subtracting diameter A from dimension B.

RCA
Solid State
Division

RF Power Transistors

2N5109



JEDEC TO-39 H 1381

Silicon N-P-N Overlay Transistor

High Gain for Line Amplifiers in CATV and MATV Equipment

Features:

- **High gain-bandwidth product**
- **Large dynamic range**
- **Low distortion**
- **Low noise**

RCA-2N5109* is an epitaxial silicon n-p-n planar transistor employing "overlay" emitter electrode construction. It is especially designed to provide large dynamic range, low distortion, and low noise as a wideband amplifier into the vhf range.

A high gain-bandwidth product over a wide range of collector current makes the 2N5109 ideally suited for such applications as CATV and MATV line amplifiers and low-noise linear amplifiers.

*Formerly RCA Dev. No. TA2800.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

* COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	40	V
COLLECTOR-TO-EMITTER VOLTAGE:			
* With base open	V_{CEO}	20	V
With external base-to-emitter resistance (R_{BE}) = 10 Ω	V_{CER}	40	V
* EMITTER-TO-BASE VOLTAGE..........	V_{EBO}	3	V
* CONTINUOUS COLLECTOR CURRENT...	I_C	0.4	A
* CONTINUOUS BASE CURRENT	I_B	0.4	A
* TRANSISTOR DISSIPATION:	P_T		
At case temperature up to 75°C		2.5	W
At case temperature above 75°C		See Fig. 10	
* TEMPERATURE RANGE:			
Storage and operating (Junction)		-65 to +200	°C
* LEAD TEMPERATURE (During Soldering):			
At distances ≥ 1/32 in. (0.8 mm) from the seating plane for 10 s max		230	°C

* In accordance with JEDEC registration data

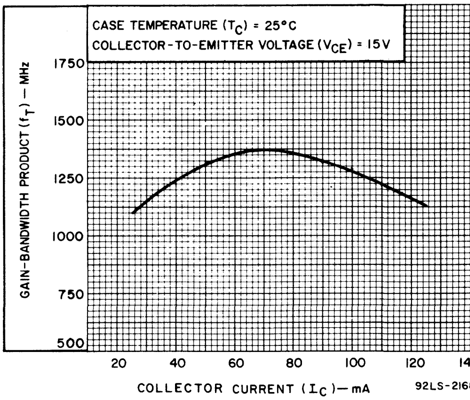


Fig. 1—Gain-bandwidth vs. collector current for type 2N5109.

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C) = 25°C Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: DC COLLECTOR OR BASE VOLTAGE – V				TEST CONDITIONS: DC CURRENT (mA)			LIMITS		UNITS
		V_{CB}	V_{BE}	V_{CE}	V_{EB}	I_E	I_B	I_C	MIN.	MAX.	
Collector-Cutoff Current: With base open	I_{CEO}			15			0		–	20	μA
* With base-emitter junction reverse-biased	I_{CEV}		-1.5	35					–	5	mA
* T_C = 150°C			-1.5	15					–	5	mA
* Emitter-Cutoff Current	I_{EBO}				3				–	0.1	mA
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$					0		0.1	40	–	V
* Collector-to-Emitter Sustaining Voltage: With external base-to-emitter resistance (R_{BE}) = 10 Ω	$V_{CER}(sus)^a$							5	40	–	V
With base open	$V_{CEO}(sus)$						0	5	20	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$					0.1		0	3	–	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$						10	100	–	0.5	V
* Collector-to-Base Capacitance (f = 1 MHz)	C_{cb}	15				0			–	3.5	pF
* DC Forward-Current Transfer Ratio	h_{FE}			15 5				50 360	40 5	120 –	
Small-Signal Common-Emitter Forward Current Transfer Ratio (f = 200 MHz)	h_{fe}			15 15 15				25 50 100	4.8 6 4.8	– – –	
* Magnitude of Common-Emitter Small-Signal Forward Current Transfer Ratio (f = 200 MHz)	$\|h_{fe}\|$			15				50	6	–	
* Available Amplifier Signal Input Power (See Fig. 9) (P_{out} = 1.26 mW, Source Impedance = 50 Ω, f = 200MHz)	P_i	15 (V_{CC})						50	–	0.1	mW
* Voltage Gain, Wideband, 50 to 216 MHz (See Fig. 8.)	G_{VE}			15				50	11		dB
Cross Modulation @ 54 dBmV[b] Output (See Fig. 14.)	CM			15				50	–57 (typ.)		dB
Power Gain, Narrowband (f = 200 MHz, P_{IN} = –10 dBm)	G_{PE}			15				10	11		dB
Noise Figure (f = 200 MHz) (See Fig. 9.)	NF			15				10	3 (typ.)		dB

[a]Pulsed through a 25 mH inductor; duty factor = 50%

[b] O dBmV = 1 millivolt

* In accordance with JEDEC registration data

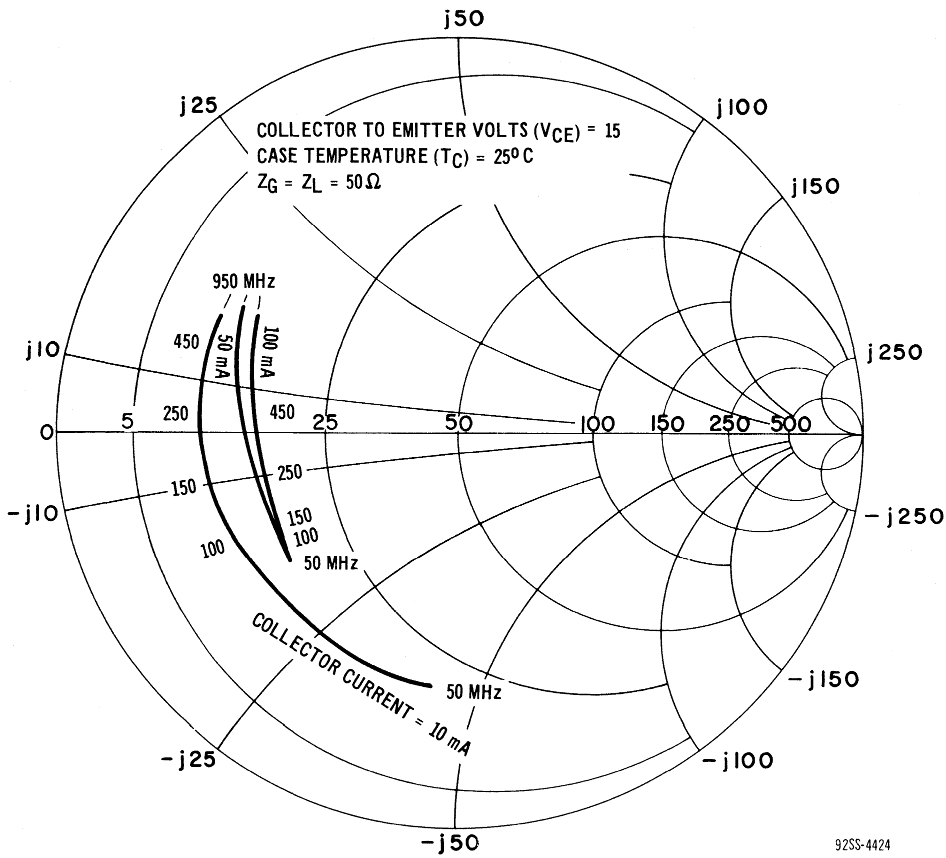


Fig.2—Input reflection coefficient (S'_{11e}) vs. frequency for type 2N5109.

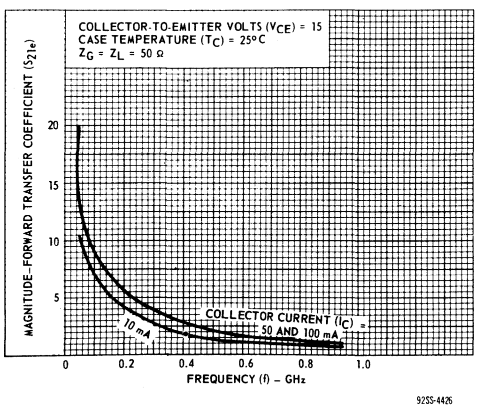


Fig.3—Magnitude of common-emitter forward transfer coefficient (S_{21e}) vs. frequency for type 2N5109.

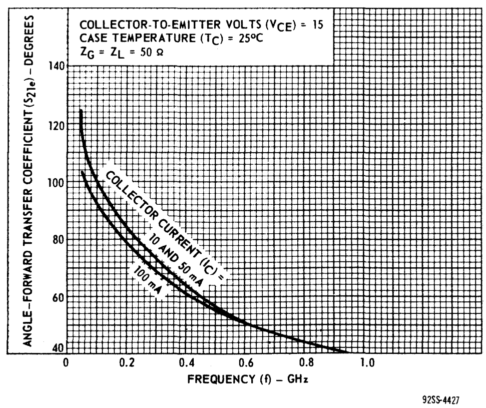


Fig.4—Angle of common-emitter forward transfer coefficient (S_{21e}) vs. frequency for type 2N5109.

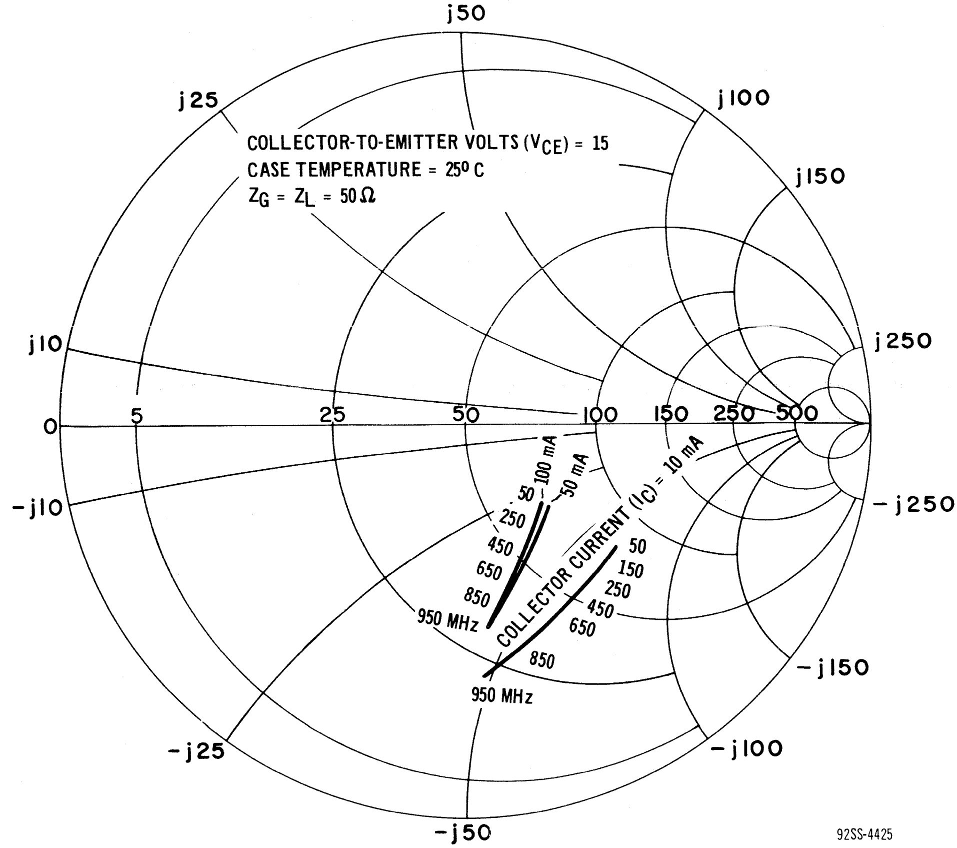


Fig.5—Output reflection coefficient (S_{22e}) vs. frequency for type 2N5109.

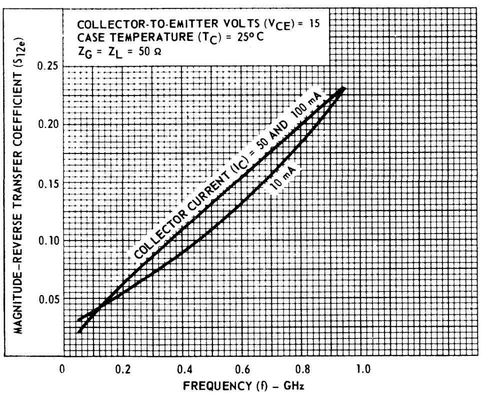


Fig.6—Magnitude of common-emitter, reverse transfer coefficient (S_{12e}) for type 2N5109.

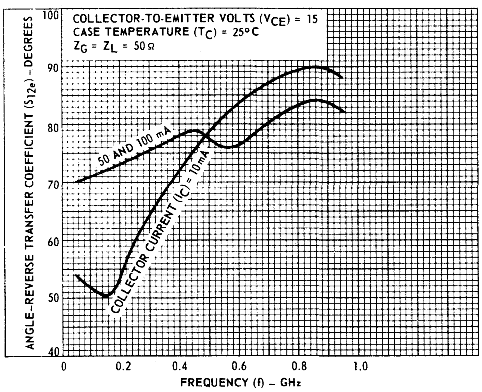
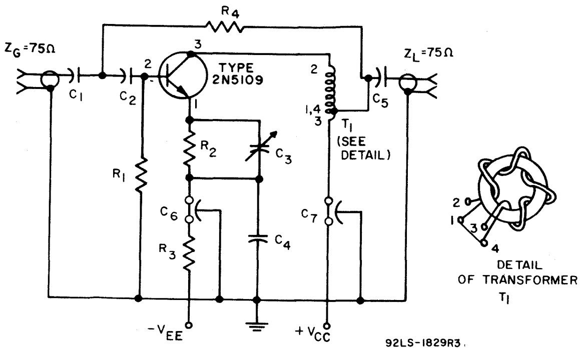
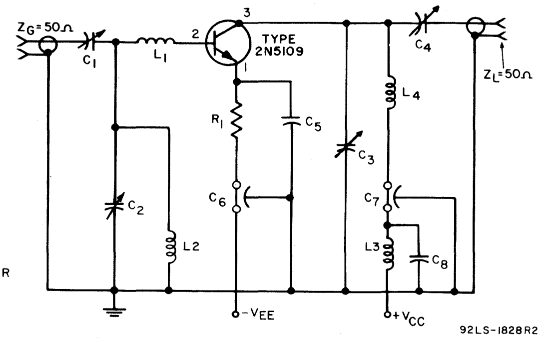


Fig.7—Angle of common-emitter reverse transfer coefficient (S_{12e}) vs. frequency for type 2N5109.



C_1, C_2, C_5: 0.002 μF, disc ceramic
C_3: 8–60 pF, ARCO 404, or equivalent
C_4: 0.03 μF, disc ceramic
C_6, C_7: 1,500 pF, feedthrough
R_1: 390 Ω, 1/2W, carbon
R_2: 6.8 Ω, 1/2W, carbon
R_3: 330Ω, 1 W, carbon
R_4: 270Ω, 1/2 W, carbon
T_1: 4 turns No. 30 wire bifilar wound on "Indiana General" Core No. CF-102-Q1, or equivalent

Fig.8–RF amplifier for voltage-gain testing of type 2N5109.



C_1, C_2, C_3: 1.0–30 pF, mica trimmer, ARCO or equivalent
C_4: 1.0–20 pF disc ceramic
C_5: 10,000 pF disc ceramic
C_6, C_7: 1,000 pF disc ceramic
C_8: 0.01 μF disc ceramic
L_1: 4-1/2 turns, No. 22 wire, 3/16 in. (4.76 mm) I.D.
L_4: 3-1/2 turns, No. 22 wire, 3/16 in. (4.76 mm) I.D.
L_2, L_3: 0.82 μH RFC
R_1: 240 Ω, 2 W, carbon

Fig.9–200-MHz amplifier for power-gain and noise-figure testing of type 2N5109.

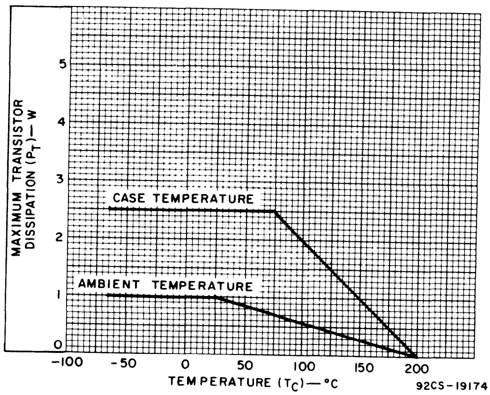


Fig.10–Dissipation derating curve for type 2N5109.

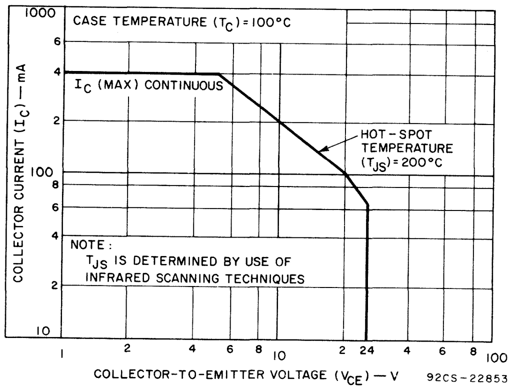


Fig. 11-Maximum operating area for type 2N5109.

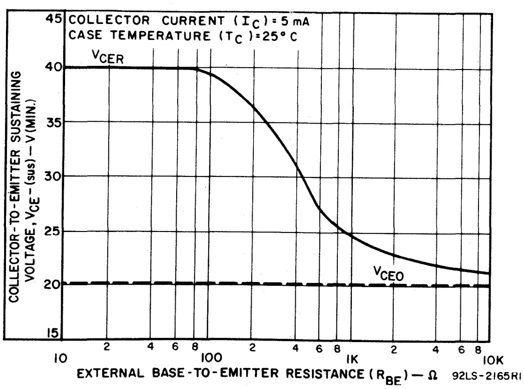


Fig. 12–Sustaining voltage vs. base-to-emitter resistance for type 2N5109.

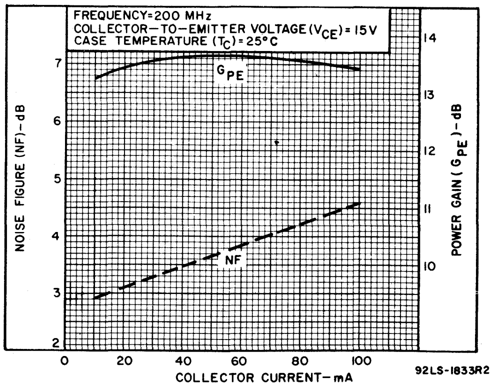
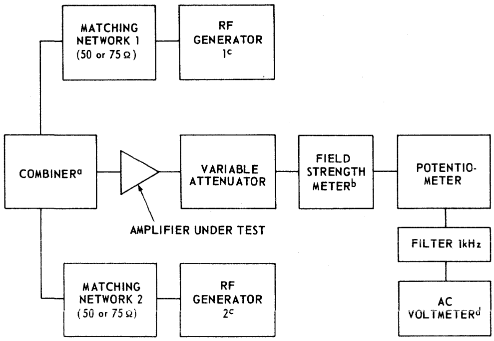


Fig. 13–Power gain and noise figure vs. collector current for type 2N5109.



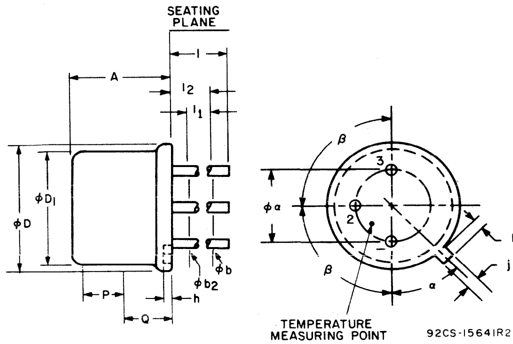
a Provides 20 db isolation between generators
b 50—220 MHz with detector output
c Hewlett—Packard HP 608 D or equivalent
d Ballantine 861 or equivalent

Fig. 14—Test set-up for measuring cross modulation in type 2N5109.

CROSS-MODULATION TEST PROCEDURE:

1. Set up equipment as shown in Fig. 14.
2. Set generator 1 to 150 MHz modulated 30% by 1,000 Hertz, and tune field strength meter to 150 MHz.
3. Adjust output level of generator 1 to give rated output from the amplifier under test.
4. Adjust potentiometer and AC voltmeter for a convenient level. This level then corresponds to 100% cross modulation.
5. Remove modulation. Readjust output level of generator 1 if necessary, to obtain the AC voltmeter "100% level". Do not readjust generator 1 during the following steps.
6. Set generator 2 to 210 MHz modulated 30% by 1,000 Hertz and tune field strength meter to 210 MHz.
7. Adjust output level of generator 2 to give rated output of the amplifier; i.e., the AC voltmeter indicates the " 100% level".
8. Tune field strength meter to 150 MHz CW and read the AC voltmeter (a change of the AC voltmeter scale may be necessary).
9. Calculate percentage of cross modulation by comparing the reading of step 8 to the "100% level".

DIMENSIONAL OUTLINE JEDEC No. TO-39



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
φa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
φb	0.016	0.021	0.406	0.533	2
φb2	0.016	0.019	0.406	0.483	2
φD	0.350	0.370	8.89	9.40	
φD1	0.315	0.335	8.00	8.51	
h	0.009	0.125	0.229	1.04	
j	0.028	0.034	0.711	0.318	
k	0.029	0.040	0.737	1.02	3
l	0.500		12.70		2
l1		0.050		1.27	2
l2	0.250		6.35		2
P	0.100		2.54		1
Q					4
α	45° NOMINAL				
β	90° NOMINAL				

Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

Note 2: (Three leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and 0.5 in. (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond 0.5 in.(12.70 mm) from seating plane.

Note 3: Measured from maximum diameter of the actual device.

Note 4: Details of outline in this zone optional.

TERMINAL CONNECTIONS

Lead No.1 — Emitter
Lead No.2 — Base
Lead No.3 — Collector
Case — Collector

RCA
Solid State
Division

RF Power Transistors

40608

RCA-40608 is an epitaxial silicon n-p-n planar transistor. It is especially designed for operation as a Class A, wide-band power amplifier in VHF circuits.

The features of high gain-bandwidth product and low cross-modulation make the 40608 especially suited for use in CATV and MATV systems.

*Formerly RCA Dev. Type No. TA2761

SILICON N-P-N "overlay" TRANSISTOR

For Class A Wide-Band CATV and MATV Applicatiations

H-1381

JEDEC TO-39

Features:

- High Gain-Bandwidth Product
- Low Cross-Modulation

MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE . .	V_{CBO}	40	V
COLLECTOR-TO-EMITTER VOLTAGE: With external base-to-emitter resistance, (R_{BE}) = 100Ω	V_{CER}	40	V
EMITTER-TO-BASE VOLTAGE.	V_{EBO}	2	V
COLLECTOR CURRENT	I_C	0.4	A
TRANSISTOR DISSIPATION	P_T		
At case temperatures up to 25°C		3.5	W
At case temperatures above 25°C.		See *Fig. 1.*	
TEMPERATURE RANGE:			
Storage & Operating (Junction).		-65 to +200	°C
LEAD TEMPERATURE (During soldering): At distances ≥ 1/32 in. (0.79 mm) from seating plane for 10 s max.		230	°C

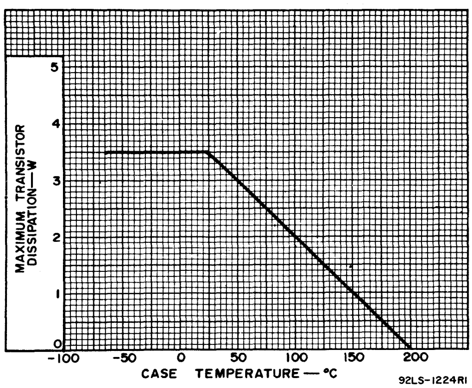
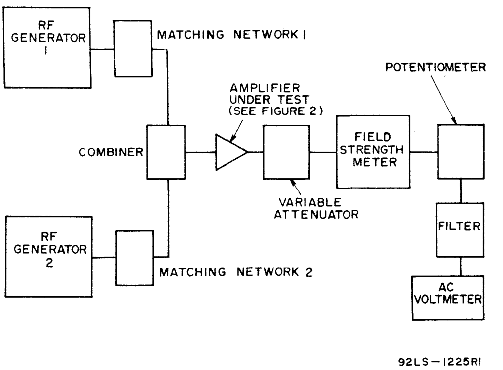


Fig. 1 - Dissipation Derating Curve

ELECTRICAL CHARACTERISTICS, *Case Temperature = 25° C*

Characteristic	Symbol	Test Conditions: DC Collector Volts		DC Current (mA)			Limits		Units
		V_{CB}	V_{CE}	I_E	I_B	I_C	Min.	Max.	
Collector-Cutoff Current	I_{CEO}		20		0			100	μA
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		0.1	40		V
Collector-to-Emitter Voltage (Sustaining)	$V_{CER}(sus)$					50[a]	40		V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.1		0	2		V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$				10	50		1.0	V
Collector-to-Base Capacitance (Measured at 1MHz)	C_{ob}	30		0				3.0	pF
Gain-Bandwidth Product	f_T		15			50	700		MHz
DC Forward-Current Transfer Ratio	h_{FE}		15			50	35	120	
Voltage Gain (See Fig. 2.)	VG		15			50	11		dB
Cross Modulation @46 dBmV (See Fig. 3.)	CM		15			50	−57 (Typ.)		dB

[a] Pulsed through an inductor (20 mH); duty factor = 50%; R_{BE} = 100 Ω.

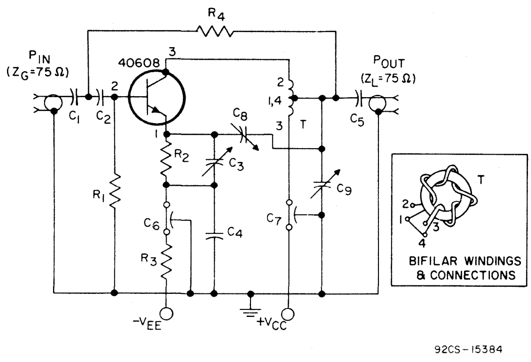


Generator No. 1 & No. 2	Hewlett-Packard, HP608D, or equivalent
Matching Network No. 1 & No. 2:	50 to 75 Ω
Combiner:	20 dB isolation between generators
Variable Attenuator:	As required
Field Strength Meter, with Detector Output:	50-220 MHz
Potentiometer:	100 kΩ
Filter:	1000 Hz
AC Voltmeter:	Ballantine 861, or equivalent

Fig. 2 - Block Diagram for Cross-Modulation Test Set-Up

OPERATING INSTRUCTIONS FOR CROSS-MODULATION TEST

1. Set up equipment as shown in Fig. 2.
2. Set generator No. 1 to 150 MHz modulated 30% by 1000 Hz, and tune field strength meter to 150 MHz.
3. Adjust output of generator No. 1 to give rated output of the amplifier.
4. Adjust potentiometer to calibrate voltmeter for a convenient level. This level then corresponds to 100% cross modulation.
5. Remove modulation.
6. Set generator No. 2 to 210 MHz modulated 30% by 1000 Hz and tune field strength meter to 210 MHz.
7. Adjust output of generator No. 2 to give rated output of the amplifier. (If the amplifier has a flat response then the output of the two signal generators will be equal.)
8. Tune field strength meter to 150 MHz CW and read voltmeter.
9. Turn voltmeter to proper scale for reading. Calculate percentage of cross modulation based upon 100% level set in step 4.



C_1, C_2, C_5: 0.002 μF
C_3: 7-100 pF, ARCO 423, or equivalent
C_4: .03 μF
C_6, C_7: 1,500 pF
C_8, C_9: 8-60 pF, ARCO 404, or equivalent
R_1: 390 Ω, ½ W
R_2: 6.8 Ω, ½ W
R_3: 330 Ω, 1 W
R_4: 270 Ω, ½ W
T: 4 turns No. 30 wire, bifilar wound; toroidal core: 3/8 in. OD, 3/16 in. ID, 1/8 in. thick, IGC* type Q-1, or equivalent.

*Indiana General Corp., Electronics/Ferrites Div., Keasbey, N.J.

Fig. 3 - RF Amplifier Circuit for Voltage Gain Test

TYPICAL ADMITTANCE CHARACTERISTICS

(Common-Emitter Circuit)

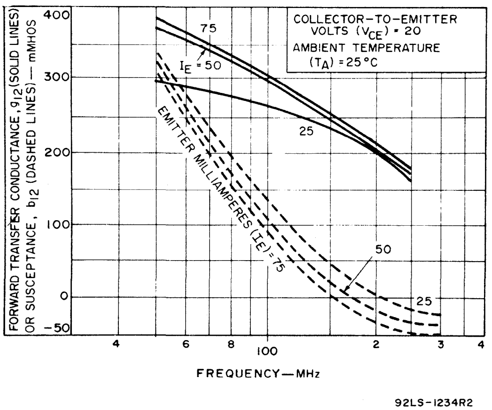


Fig. 4 - Forward Transfer Admittance

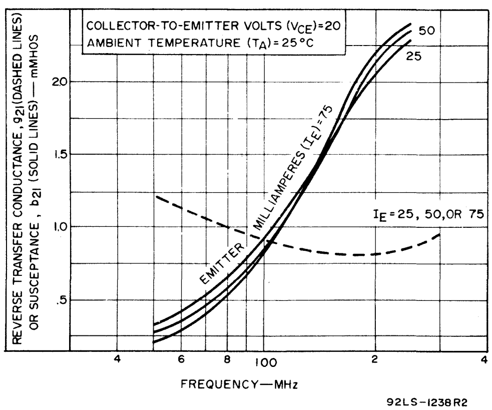


Fig. 5 - Reverse Transfer Admittance

TYPICAL ADMITTANCE CHARACTERISTICS

(Common-Emitter Circuit)

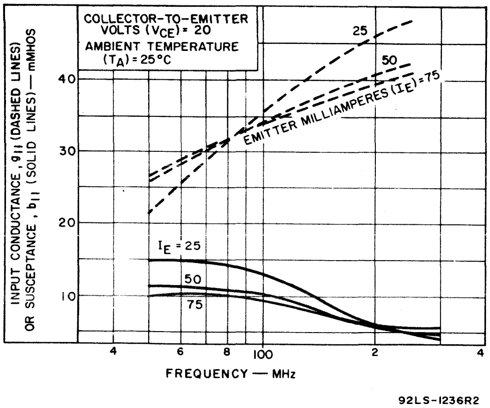


Fig. 6 - Input Admittance

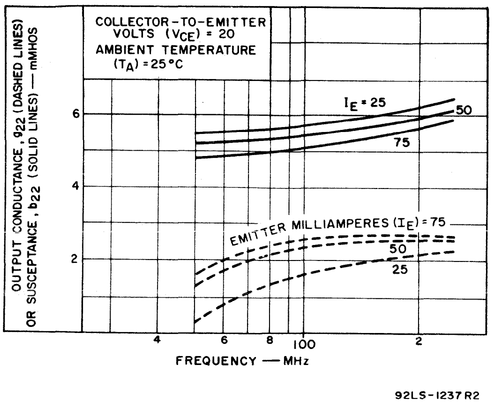
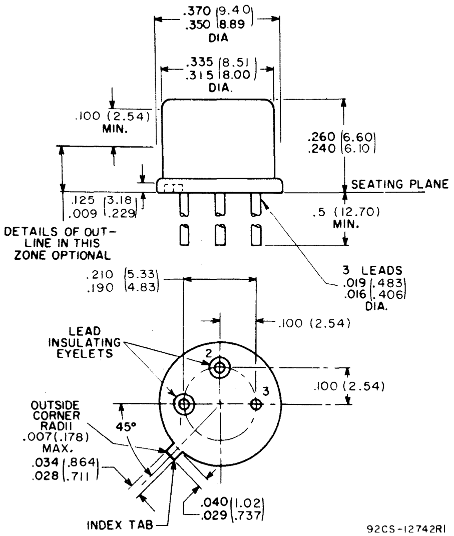


Fig. 7 - Output Admittance

DIMENSIONAL OUTLINE JEDEC TO-39



DIMENSIONS IN INCHES AND MILLIMETERS

Note: *Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.*

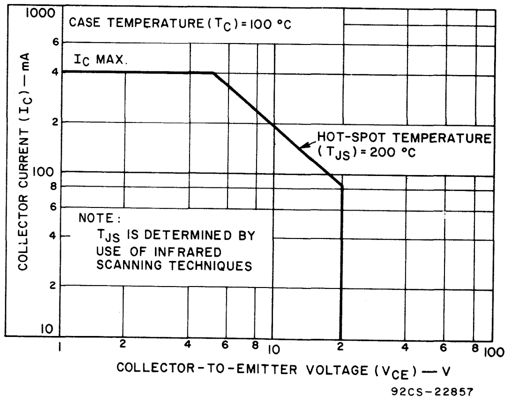
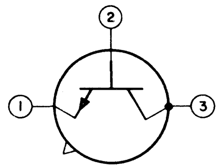


Fig. 8 - Safe Area for DC Operation

TERMINAL DIAGRAM

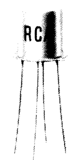


Lead 1 - Emitter
Lead 2 - Base
Lead 3 - Collector, Case

RCA
Solid State
Division

RF Transistors

2N6389



JEDEC TO-72 H-1299

UHF/MATV Low-Noise Silicon N-P-N Transistor

For High-Gain Small-Signal Applications in UHF TV RF Amplifiers and UHF MATV Amplifiers

Features:

- **Low noise figure:**
  NF = 3 dB (typ.) at 450 MHz, 1.5 mA
  = 4 dB (typ.) at 890 MHz, 1.5 mA
  = 6 dB (typ.) at 890 MHz, 10 mA
- **High gain (tuned, unneutralized):**
  G_{PE} = 15 dB (min.) at 890 MHz

RCA 2N6389• is an epitaxial silicon n-p-n planar transistor intended for low-power, small-signal applications where both low noise and high gain are desirable. It utilizes a hermetically sealed four-lead JEDEC TO-72 package. All of the elements of the transistor are insulated from the case, which may be grounded by means of the fourth lead.

- **High gain-bandwidth product**
- **Large dynamic range**
- **Low distortion**
- **Low collector-base capacitance**

•Formerly RCA No. 40989.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

*COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	20	V
*COLLECTOR-TO-EMITTER VOLTAGE	V_{CEO}	12	V
*EMITTER-TO-BASE VOLTAGE	V_{EBO}	2.5	V
*COLLECTOR CURRENT (Continuous)	I_C	40	mA
*TRANSISTOR DISSIPATION:	P_T		
At ambient temperatures up to 25°C		200	mW
At ambient temperatures above 25°C		Derate linearly at 1.14 mW/°C	
*TEMPERATURE RANGE:			
Storage and Operating (Junction)		−65 to +200° C	
*LEAD TEMPERATURE (During soldering):			
At distances ≥ 1/16 in. (1.59 mm) from seating plane for 60 s max.		300° C	

*In accordance with JEDEC registration data format JS-9 RDF-1.

3-73

ELECTRICAL CHARACTERISTICS, *At Ambient Temperature (T_A) = 25°C*

	CHARACTERISTIC	SYMBOL	TEST CONDITIONS: VOLTAGE V dc V_{CB}	V_{CE}	CURRENT mA dc I_E	I_B	I_C	LIMITS MIN.	MAX.	UNITS
	STATIC									
*	Collector Cutoff Current	I_{CBO}	15		0			–	20	nA
*	Emitter Cutoff Current	I_{EBO}	(V_{EB}) 1				0	–	1	μA
*	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$			0		0.001	20	–	V
*	Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$				0	3	12	–	V
*	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$			0.01		0	2.5	–	V
*	DC Forward Current Transfer Ratio	h_{FE}		1			3	25	250	
	Thermal Resistance: (Junction-to-Case)	$R_{\theta JC}$						–	880	°C/W
	DYNAMIC									
	Device Noise Figure: f = 890 MHz	NF	10				1.5	–	4(typ.)	dB
	= 890 MHz	NF	10				10	–	6(typ.)	dB
	= 450 MHz	NF	10				1.5	–	3(typ.)	dB
	Small-Signal Common-Base Power Gain (f = 890 MHz)	G_{PB}	10				10	15	–	dB
*	Small-Signal, Short Circuit Forward Current Transfer Ratio (f = 1 kHz)	h_{fe}		1			3	25	250	
*	Magnitude of Small-Signal Short Circuit Forward Current Transfer Ratio (f = 200 MHz)	$\lvert h_{fe} \rvert$		10			1.5	5	15	
*	Collector-to-Base Time Constant (f = 31.9 MHz)	$r_b C_c$	10		1.5			1	15	ps
*	Collector-to-Base Capacitance (f = 1 MHz)	C_{cb}	10		0			0.4	0.55	pF

* In accordance with JEDEC registration data format JS-9 RDF-1.

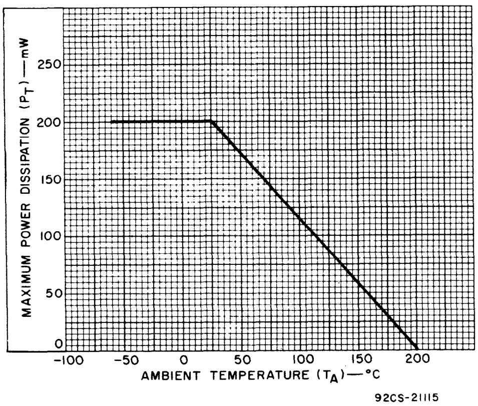


Fig. 1 — Power dissipation vs. ambient temperature.

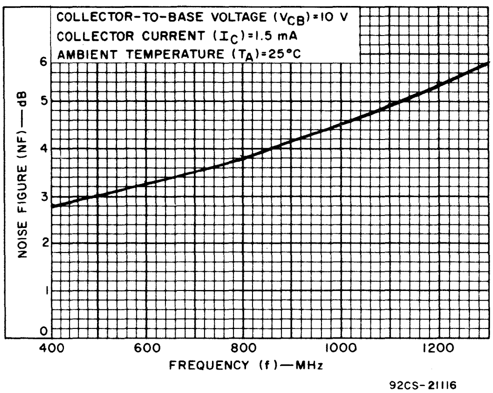


Fig. 2 — Typical common-base noise figure vs. frequency.

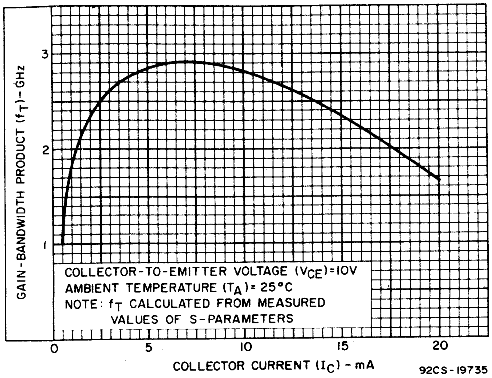
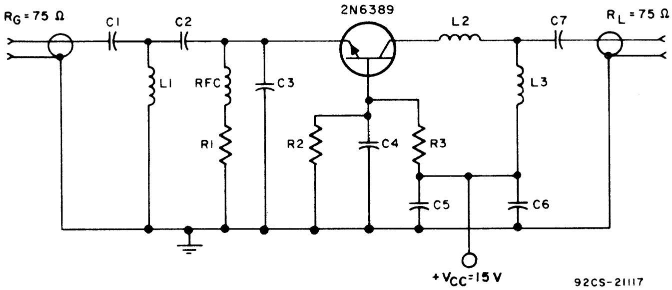


Fig. 3 — Gain-bandwidth product vs. collector current.

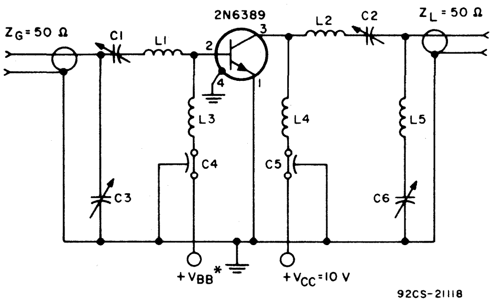


C_1, C_7: 3.3 pF disc ceramic
C_2, C_3: 2.7 pF disc ceramic
C_4, C_5, C_6: 25 pF, ATC-100 or equivalent

L_1, L_3: 2.5 turns, No. 18 wire, 0.125 in. (3.175 mm) ID
L_2: 1 turn, No. 18 wire, 0.125 in. (3.175 mm) ID
RFC: 8 turns No. 28 wire, 0.062 in. (1.57 mm) ID

R_1: 470 Ω
R_2: 2.4 kΩ
R_3: 5.1 kΩ

Fig. 4—890-MHz common-base test circuit for gain and noise figure.



C_1: 1.0–30 pF
C_2, C_3: 1.0–20 pF
C_4, C_5: 0.04 μF
C_6: 1–10 pF

L_1: 2 turns No. 18 wire, 3/16 in. (0.188 mm) ID, 0.10 in. (2.54 mm) long
L_2: 3 turns No. 18 wire, 3/16 in. (0.188 mm) ID, 0.15 in. (3.81 mm) long
L_3, L_4: 0.22-μH rf choke
L_5: 3 turns No. 18 wire, 3/16 in. (0.188 mm) ID, 0.15 in. (3.81 mm) long

R_1: 200Ω, 1/4 W

* $V_{(BB)}$ adjusted for I_C = 1.5 mA

Fig. 5—Circuit diagram of 450-MHz amplifier used for measurement of noise figure.

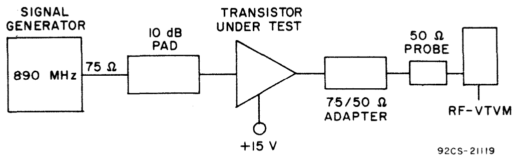


Fig. 6—Block diagram of test setup for measurement of gain.

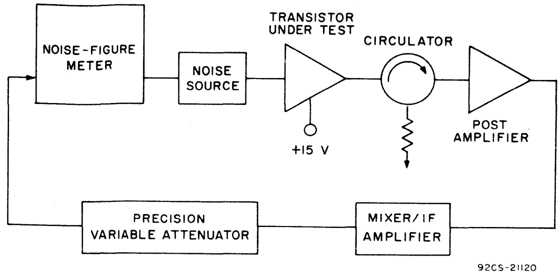
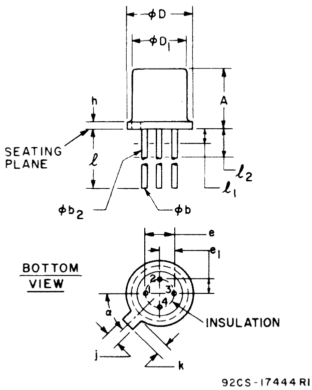


Fig. 7—Block diagram of noise-figure test set.

DIMENSIONAL OUTLINE

JEDEC TO–72



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.170	0.210	4.32	5.33	
φb	0.016	0.021	0.406	0.533	2
$φb_2$	0.016	0.019	0.406	0.483	2
φD	0.209	0.230	5.31	5.84	
$φD_1$	0.178	0.195	4.52	4.95	
e	0.100 T.P.		2.54 T.P.		4
e_1	0.050 T.P.		1.27 T.P.		4
h		0.030		0.762	
j	0.036	0.046	0.914	1.17	
k	0.028	0.048	0.711	1.22	3
l	0.500		12.70		2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
α	45° T.P.		45° T.P.		4, 6

Note 1: (Four leads). Maximum number leads omitted in this outline, "none" (0). The number and position of leads actually present are indicated in the product registration. Outline designation determined by the location and minimum angular or linear spacing of any two adjacent leads.

Note 2: (All leads) $φb_2$ applies between l_1 and l_2. φb applies between l_2 and 0.50 in. (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond 0.50 in. (12.70 mm) from seating plane.

Note 3: Measured from maximum diameter of the product.

Note 4: Leads having maximum diameter 0.019 in. (0.484 mm) measured in gaging plane 0.054 in. (1.37 mm) +0.001 in. (0.025 mm) – 0.000 (0.000 mm) below the seating plane of the product shall be within 0.007 in. (0.178 mm) of their true position relative to a maximum width tab.

Note 5: The product may be measured by direct methods or by gage.

Note 6: Tab centerline.

TERMINAL CONNECTIONS

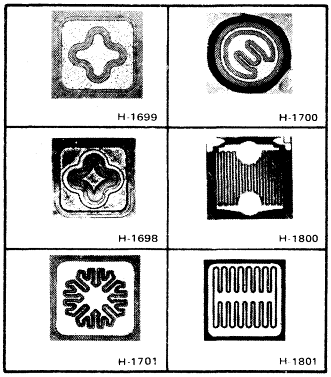
Lead 1 – Emitter
Lead 2 – Base
Lead 3 – Collector
Lead 4 – Connected to case

Power-Transistor Chips

Solid State
Division

Power Transistors

CH2102 CH2270 CH2405 CH3053 CH3439 CH3440 CH4036 CH4037 CH5262 CH5320 CH5321 CH5322 CH5323 CH6479



Unmounted and Unencapsulated N-P-N and P-N-P Silicon Power Transistor Chips

Features:

- Prepared and tested for use in hybrid circuits
- h_{FE} ratings from 30 to 50 (min.)
- I_{CBO} leakage ratings in the 10 μA to 1 mA range
- V_{CEO} ratings up to 90 V on planar transistor chips; up to 325 V on passivated mesa types
- I_C up to 12 A (CH6479)

The transistor chip families described in this bulletin are selected from the broad line of RCA discrete power transistors. Known also as pellets or dies, these chips represent the essential electronic portion of the transistor. They are especially suited for direct mounting on a heat sink in hybrid circuits. The n-p-n and p-n-p types can be used either singly or in complementary-pair configurations for large-signal medium-power applications.

All of the chip families shown are double-diffused epitaxial types. Six of the families are of planar construction; the other is of a passivated mesa construction. The oxide layer that results from conventional planar processing protects the planar types. The junctions and surfaces of the mesa transistor chips are protected by deposited glass-passivated coverings.

Aluminum has been deposited at the base and emitter electrodes of all the transistor chips for ease of bonding. The base and emitter bonding areas on each chip will accommodate up to a 0.003-inch (0.076-mm)-diameter bond wire except for the CH6479 which will accommodate a 0.010-inch (0.254-mm) wire. Either thermo-compression or ultrasonic bonding can be used to attach gold wires to these electrodes; aluminum wires can also be bonded by conventional ultrasonic techniques.

The collector contact, which is on the underside of the chip, has been metallized with gold for all of the chips except CH6479. For all of the chips, the collector can be attached directly to a heat sink by adhesive or by gold-silicon or gold-germanium eutectic bonding methods.

The CH6479, because of its large size, must be mounted on a heat sink made of material with thermal expansion coefficient close to that of silicon; suitable materials are molybdenum or beryllium oxide. A special cleaning step is required in mounting the CH6479, as noted on page 5.

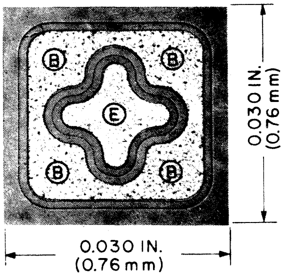
All of the chips must be mounted in an inert or reduced atmosphere. The chips must not be subjected to more than 400°C for a maximum of 1 minute. Because of the specially prepared surfaces of the chips (except as noted for the CH6479), etching of the pellets or the use of flux is not recommended.

The chips are supplied in plastic containers. Each chip is securely held in a recessed partition of the container by a clear plastic cover that also protects the surface from dust and abrasion. For additional protection, the container is sealed in a clear plastic bag. If the sealed shipping container is opened or broken, ruptured, punctured, or damaged in any way, the chips must be stored at a temperature of not more than 40°C and a relative humidity of not more than 50% in a clean, dust-free environment. If the sealed shipping container is damaged on receipt as described above, the product should be immediately returned to RCA.

These unmounted and unencapsulated chips are tested electrically and visually inspected to meet the specifications shown on the following pages. Written notification of non-conformance to such specifications must be made to RCA within 90 days of the date of the shipment by RCA. RCA assumes no responsibility for chips which have been subjected to further processing, such as, but not limited to, lead-bonding or pellet-mounting operations.

RCA has the right to change the chip design and processing without notification.

Assistance in determining proper mounting and bonding procedures is available from RCA.



2N2102 Family (n-p-n)

CH2102 CH2405
CH2270 CH3053

RCA-CH2102, CH2270, CH2405, and CH3053 are double-diffused n-p-n epitaxial planar transistor chips similar to RCA-2N2102, 2N2270, 2N2405, and 2N3053 transistors, respectively. They can be used either singly or in complementary-pair configurations with RCA p-n-p chips CH4036 and CH4037 for large-signal medium-power applications.

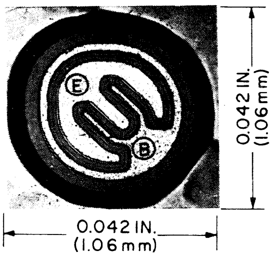
(B) 4 Base Bonding Areas 0.008 in. (0.20 mm) diameter

(E) Emitter Bonding Area 0.008 in. (0.20 mm) diameter

ELECTRICAL CHARACTERISTICS, at Chip Temperature = 25°C

Characteristic	Symbol	Test Conditions				Limits								Units
		Voltage V dc		Current mA dc		CH2102		CH2270		CH2405		CH3053		
		V_{CB}	V_{CE}	I_C	I_E	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Collector Cutoff Current	I_{CBO}	60					10		10		10		10	μA
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$				0.01	5		5		5		5		V
Collector-to-Emitter Sustaining Voltage: Base open[a]	$V_{CEO(sus)}$			20		60		45		90		30		V
DC Forward-Current Transfer Ratio[b]	h_{FE}		10	150		50		50		50		50		

[a]CAUTION: This voltage MUST NOT be measured on a curve tracer. [b]Pulse tested; 2% duty factor, less than or equal to 300 μs duration.



2N3439 Family (n-p-n)

CH3439
CH3440

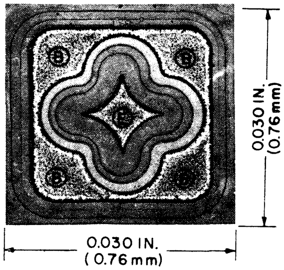
RCA-CH3439 and CH3440 are passivated mesa n-p-n transistor chips similar to those used in RCA-2N3439 and 2N3440 high-voltage transistors. Because of their high breakdown voltages, good high-frequency response, and fast switching speeds, these transistor chips can be used in high-voltage differential and operational amplifiers, high-voltage inverters and high-voltage, low-current switching regulators.

(B) Base Bonding Area 0.005 in. (0.13 mm) diameter

(E) Emitter Bonding Area 0.005 in. (0.13 mm) diameter

ELECTRICAL CHARACTERISTICS, at Chip Temperature = 25°C

Characteristic	Symbol	Test Conditions				Limits				Units
		Voltage V dc		Current mA dc		CH3439		CH3440		
		V_{CB}	V_{CE}	I_C	I_E	Min.	Max.	Min.	Max.	
Collector Cutoff Current	I_{CBO}	200					20		50	μA
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$				0.02	5		5		V
Collector-to-Emitter Sustaining Voltage: Base open [a]	$V_{CEO(sus)}$			20		325		250		V
DC Forward-Current Transfer Ratio [b]	h_{FE}		10	20		30		30		



2N4036 Family (p-n-p)

CH4036
CH4037

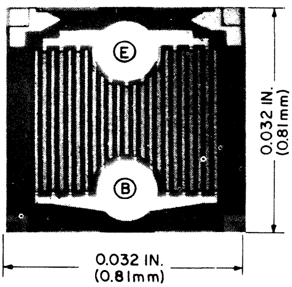
RCA-CH4036 and CH4037 are double-diffused p-n-p epitaxial planar transistor chips similar to RCA-2N4036 and 2N4037 transistors. Their high-voltage ratings and heat-dissipating ability make them ideal for amplifying large signals at a medium power level. They can be used singly or as complements of RCA n-p-n chips CH2102, CH2270, CH2405, and CH3053.

(B) 4 Base Bonding Areas 0.008 in. (0.13 mm) diameter

(E) Emitter Bonding Area 0.008 in. (0.13 mm) diameter

ELECTRICAL CHARACTERISTICS, at Chip Temperature = 25°C

Characteristic	Symbol	Test Conditions				Limits				Units
		Voltage V dc		Current mA dc		CH4036		CH4037		
		V_{CB}	V_{CE}	I_C	I_E	Min.	Max.	Min.	Max.	
Collector Cutoff Current	I_{CBO}	60					-10		-10	μA
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$				-0.01	-6.5		-6.6		V
Collector-to-Emitter Sustaining Voltage: Base open [a]	$V_{CEO(sus)}$			-20		-65		-40		V
DC Forward-Current Transfer Ratio [b]	h_{FE}		-10	-150		35		35		



2N5262 Family (n-p-n)

CH5262

RCA-CH5262 is a double-diffused n-p-n epitaxial planar transistor chip similar to the RCA-2N5262 transistor. Its high speed and high current capability make it ideal for use in driving magnetic systems and in other applications requiring the switching of high currents through inductive loads.

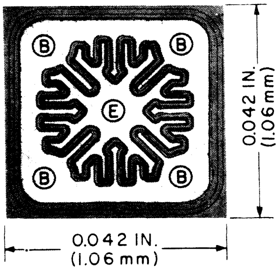
(B) Base Bonding Areas 0.005 in. (0.13 mm) diameter

(E) Emitter Bonding Area 0.005 in. (0.13 mm) diameter

ELECTRICAL CHARACTERISTICS, at Chip Temperature = 25°C

Characteristic	Symbol	Test Conditions				Limits		Units
		Voltage V dc		Current mA dc		CH5320		
		V_{CB}	V_{CE}	I_C	I_E	Min.	Max.	
Collector Cutoff Current	I_{CBO}	60					10	μA
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$				0.01	5		V
Collector-to-Emitter Sustaining Voltage: Base open [a]	$V_{CEO(sus)}$			10		35		V
DC Forward-Current Transfer Ratio [b]	h_{FE}		6	100		30		

[a] CAUTION: This voltage MUST NOT be measured on a curve tracer. [b] Pulse tested; 2% duty factor, less than or equal to 300 μs duration.



2N5320 Family (n-p-n)

CH5320
CH5321

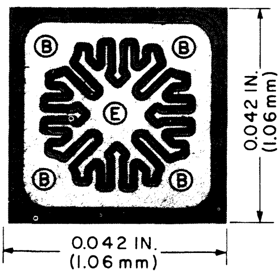
RCA-CH5320 and CH5321 are double-diffused n-p-n epitaxial planar transistor chips similar to RCA-2N5320 and 2N5321 transistors. They can be used singly or as complements of RCA p-n-p chips CH5322 and CH5323.

(B) 4 Base Bonding Areas 0.008 in. (0.20 mm) diameter

(E) Emitter Bonding Area 0.008 in. (0.20 mm) diameter

ELECTRICAL CHARACTERISTICS, at Chip Temperature = 25°C

Characteristic	Symbol	Test Conditions				Limits				Units
		Voltage V dc		Current mA dc		CH5320		CH5321		
		V_{CB}	V_{CE}	I_C	I_E	Min.	Max.	Min.	Max.	
Collector Cutoff Current	I_{CBO}	60					10		10	μA
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$				0.01	5		5		V
Collector-to-Emitter Sustaining Voltage: Base open [a]	$V_{CEO(sus)}$			20		80		55		V
DC Forward-Current Transfer Ratio [b]	h_{FE}		10	250		30		30		



2N5323 Family (p-n-p)

CH5322
CH5323

RCA-CH5322 and CH5323 are double-diffused p-n-p epitaxial planar transistor chips similar to RCA-2N5322 and 2N5323 transistors. They can be used singly or as complements of RCA n-p-n chips CH5320 and CH5321 for amplifying large signals at a medium power level.

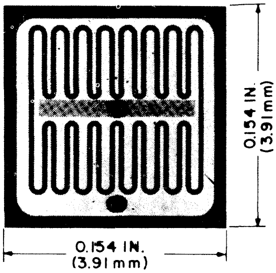
(B) 4 Base Bonding Areas 0.008 in. (0.20 mm) diameter

(E) Emitter Bonding Area 0.008 in. (0.20 mm) diameter

ELECTRICAL CHARACTERISTICS, at Chip Temperature = 25°C

Characteristic	Symbol	Test Conditions				Limits				Units
		Voltage V dc		Current mA dc		CH5322		CH5323		
		V_{CB}	V_{CE}	I_C	I_E	Min.	Max.	Min.	Max.	
Collector Cutoff Current	I_{CBO}	-60					-10		-10	μA
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$				-0.01	-5		-5		V
Collector-to-Emitter Sustaining Voltage: Base open [a]	$V_{CEO(sus)}$			-20		-80		-55		V
DC Forward-Current Transfer Ratio [b]	h_{FE}		-10	-250		30		30		

[a]CAUTION: This voltage MUST NOT be measured on a curve tracer. [b]Pulse tested; 2% duty factor, less than or equal to 300 μs duration.



CH6479 Family (n-p-n)

CH6479

RCA-CH6479 is a double-diffused n-p-n epitaxial planar transistor chip similar to the RCA-2N6479 transistor. Radiation hardening makes this type suitable for aerospace applications, and high-switching speeds make it ideal for use in high-speed inverters, switching regulators, and military hybrid applications.

(B) Base Bonding Area 0.013 in. (0.33 mm) x 0.091 in. (2.31 mm)

(E) Emitter Bonding Area 0.013 in. (0.33 mm) x 0.091 in. (2.31 mm)

ELECTRICAL CHARACTERISTICS, at Chip Temperature = 25°C

Characteristic	Symbol	Test Conditions				Limits		Units
		Voltage V dc		Current mA dc		CH6479		
		V_{CB}	V_{CE}	I_C	I_E	Min.	Max.	
Collector Cutoff Current	I_{CBO}	100					1	mA
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$				1	5		V
Collector-to-Emitter Sustaining Voltage: Base open [a]	$V_{CEO(sus)}$			25		60		V
DC Forward-Current Transfer Ratio [b]	h_{FE}		2	500		40		

[a]CAUTION: This voltage MUST NOT be measured on a curve tracer.

[b]Pulse tested; 2% duty factor, less than or equal to 300 μs duration.

CH6479 Chip Special Clean-Up Schedule:

Before eutectic mounting, the CH6479 chip must be etched for 30 seconds in a 10% (by volume) electronic-grade hydrofluoric acid solution at 25°C ± 5°C with agitation. Normal precautions for using hydrofluoric acid should be observed. The chip must then be dried and mounted within 8 hours.

CHIP INSPECTION INFORMATION

Each lot is inspected to a 2.5% AQL (cumulative) according to Mil Std. 105 using 20 times magnification. The following defects determine the inspection criteria:

Foreign matter adhering to the base and emitter bond areas.

Improperly cut pellets that include a portion of another pellet.

Bridging by the metallization which causes a short.

Blistering, lifting or absence of the aluminum metallization.

Fractures or edges within 0.0005 in. (0.013) mm of the base collector junction.

Severed base-contact rings that isolate all the bonding pads and most of the base area.

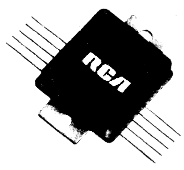
Oxide missing from the junction area.

Power Hybrid Circuits

RCA
Solid State
Division

Power Hybrid Circuits

HC2000H



H-1777

Multi-Purpose 7-Ampere Operational Amplifier

Linear Amplifiers for Applications in Industrial and Commercial Equipment

Features:

- **Bandwidth: 30 kHz at 60 W**
- **High power output: up to 100 W(rms)**
- **High output current: 7 A (peak)**
- **Built-in load-line-limiting circuit to protect amplifiers from accidentally short-circuited output terminals**
- **Stability with resistive or reactive loads**
- **Reactive-load fault protection**
- **Single or split power supply (30 to 75 V, total)**
- **Provision for feedback control**
- **Direct coupling to load**
- **Class B output stage**
- **Rugged package with heavy leads**
- **Light weight: 100 grams**
- **Low crossover distortion**

RCA-HC2000H* is a complete solid-state hybrid operational amplifier in a metal hermetic package. The HC2000H is intended for military and critical industrial applications and can be supplied in accordance with applicable portions of MIL-STD.883.

The amplifier employs a quasi-complementary-symmetry class B output circuit with built-in load-fault protection and hometaxial output transistors. The circuit may be operated from a single or split power supply.

Type HC2000H is recommended for the following applications: servo amplifiers (ac, dc, PWM); deflection amplifiers; power operational amplifiers; audio amplifiers; voltage regulators; and driven inverters.

Additional information on hybrid power amplifiers is contained in RCA Application Notes AN-4474, AN-4483, and AN-4782. Single copies of these publications are available upon request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.

* Formerly RCA Dev. No. TA7626A.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

SUPPLY VOLTAGE:	
Between leads 1 & 10	75 V
OUTPUT CURRENT (Peak)	7 A
TOTAL DISSIPATION:	
Per Output Device	See Fig. 4 & 5
TEMPERATURE RANGE:	
Storage	−55 to +125 °C
Output-Transistor Junction	−55 to +150 °C
LEAD TEMPERATURE (During Soldering):	
At distance ≥ 1/8 in. (3.17 mm) from case for 10 s max.	235 °C
LEAD-BENDING RADIUS (Min.)	
At distance ≥ 0.075 (1.91 mm) from case	0.04 in. (1.02 mm)

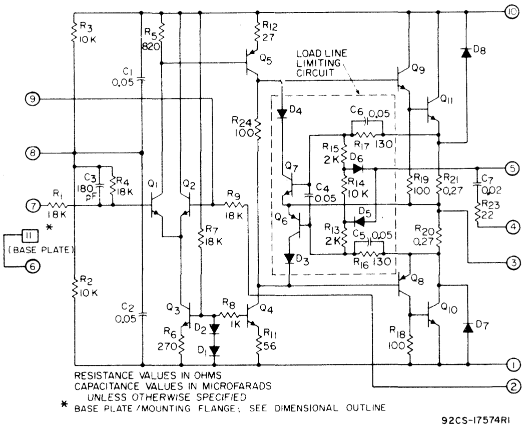


Fig. 1—Schematic diagram of type HC2000H power hybrid circuit operational amplifier.

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25ºC*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS				LIMITS			UNITS
		SUPPLY VOLTAGE (V_S)–V	FREQ. (f)–kHz	OUTPUT POWER (P_O)–W	LOAD RESIST. (R_L)–Ω	MIN.	TYP.	MAX.	
Open-Loop Voltage Gain	$\frac{V_{OUT}}{V_{IN}}$	±37.5	4	25	4	4000	5000	–	–
Closed-Loop Voltage Gain (See Fig. 3)	$\frac{V_{OUT}}{V_{IN}}$	±37.5	1	1	4	26	30	–	–
Input Impedance Measured between leads 7 & 8 (See Fig. 3)	Z_{IN}	–	–	–	0	16	18	–	kΩ
Quiescent Current	I_o	±37.5	–	–	–	15	–	30	mA
Initial Offset Voltage Measured between leads 4 & 5 (See Fig. 3)	V_{offset}	±37.5	–	–	4	0	±30	±250	mV
Offset Voltage Drift with Temperature	$\Delta V_{offset}/\Delta T$	±37.5	–	–	4	–	0.5	0.7	mV/ºC
Bandwidth (See Figs. 3 & 8)	f_H	±37.5	–	1	4	43	–	–	kHz
Total Harmonic Distortion (See Figs. 3 & 9)	THD	±37.5	1	60	4	–	0.4	0.5	%
Short-Circuit Current (See Fig. 11)	I_S	±37.5	1	–	0	2	–	3	A
Signal-to-Noise Ratio Signal Source Impedance = 600 Ω	S/N	±37.5	–	–	–	–	+78	–	dB
Slew Rate (Unity gain with peak output current of 4A)	SR	±37.5	1	100	4	10	25	–	V/μs
Thermal Resistance Per Output Device (Junction-to-Case) (See Figs. 4 & 5)	$R_{\theta J\text{-}C}$	–	–	–	–	–	–	2	ºC/W

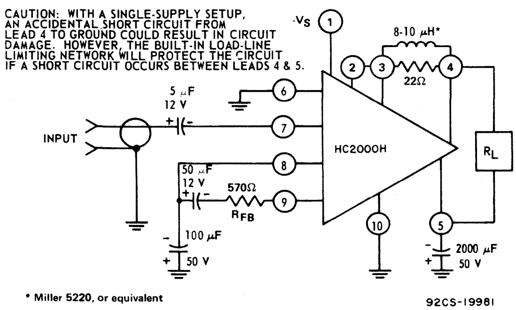


Fig. 2—Type HC2000H power hybrid circuit with external connections for operation with a single power supply.

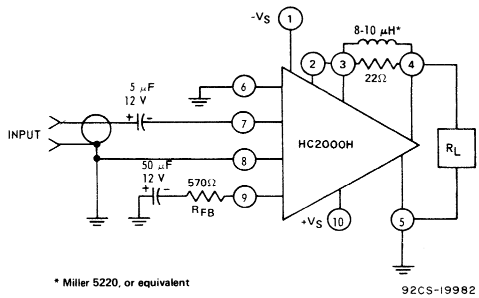


Fig. 3—Type HC2000H power hybrid circuit with external connections (and split power supply) for measuring relative response and distortion; see Figs. 8 & 9.

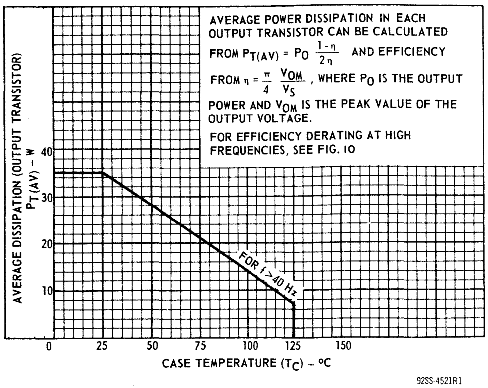


Fig. 4—Dissipation (average) derating curve for each output transistor (for symmetrical waveforms with f > 40 Hz).

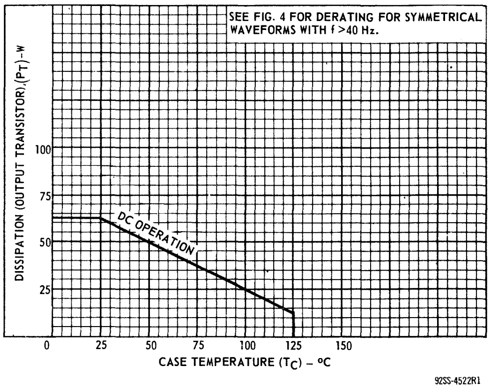


Fig. 5—Dissipation (dc) derating curve for each output transistor.

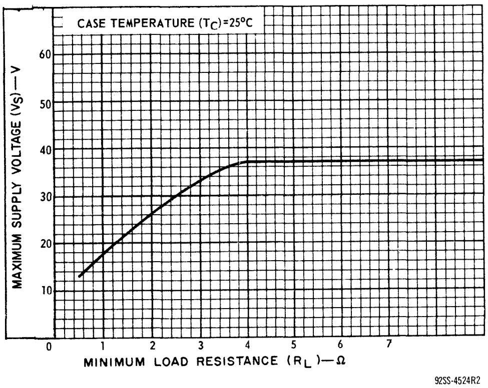


Fig. 6—Maximum allowable supply voltage vs. load resistance.

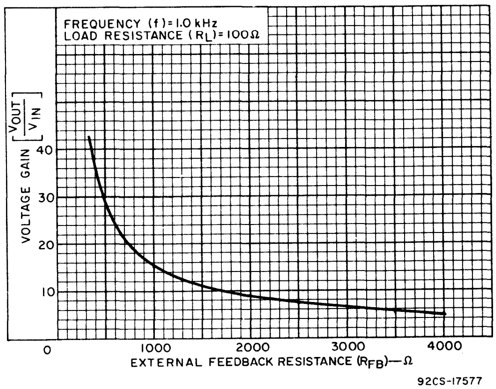


Fig. 7—Closed-loop voltage gain vs. external feedback resistance.

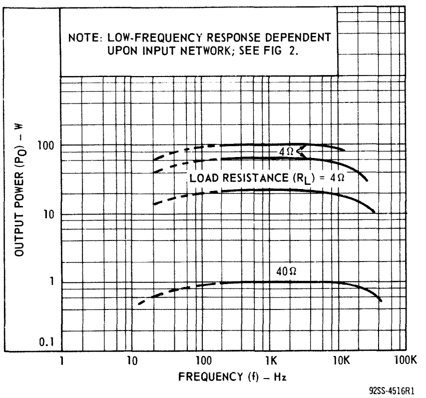


Fig. 8—Output power vs. frequency.

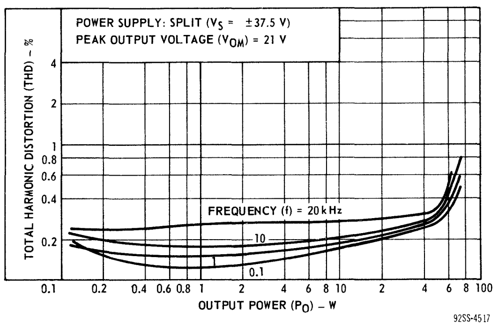


Fig. 9—Total harmonic distortion with split power supply.

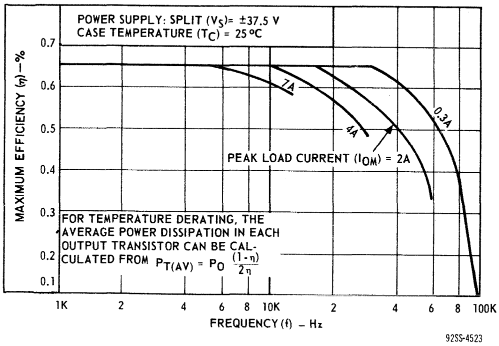


Fig. 10—Maximum efficiency vs. frequency for several values of peak load current.

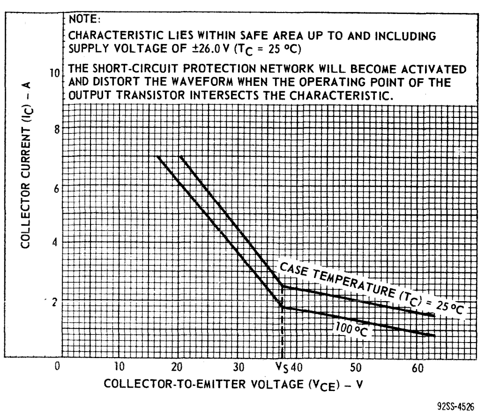


Fig. 11—Characteristics of built-in load-line-limiting circuit.

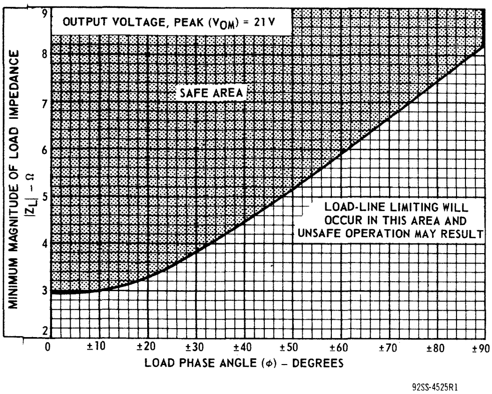


Fig. 12—Minimum load impedance vs. load phase angle and safe area of operation.

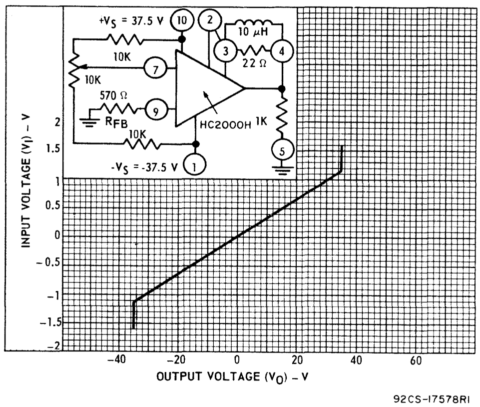


Fig. 13—Gain linearity characteristic.

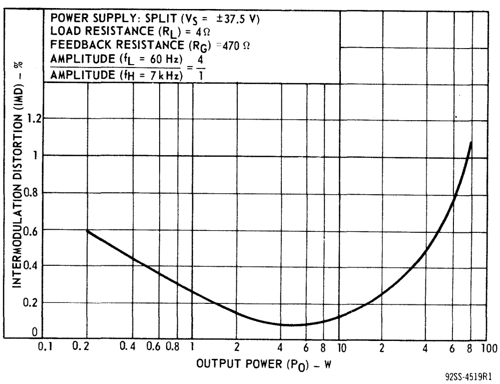


Fig. 14—Intermodulation distortion with split supply and 4-ohm load.

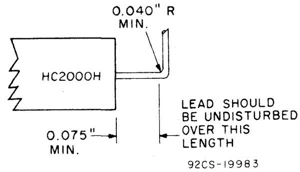
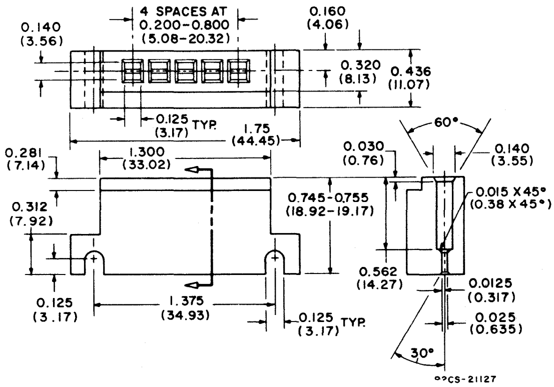


Fig. 15—Recommended lead-bending specification.

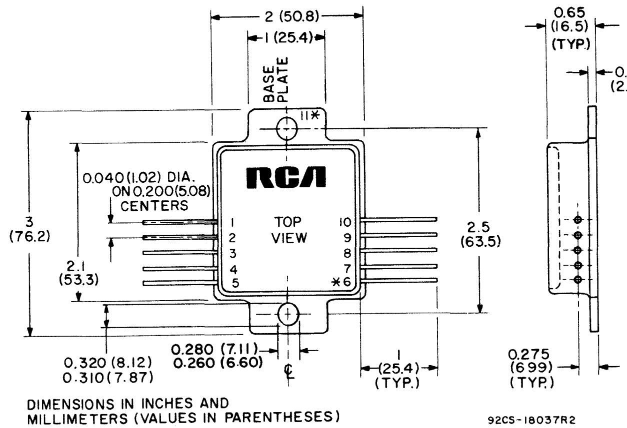


Dimensions in inches and millimeters
(values in parentheses)

Socket: RCA DF-293A; or
Electronic Essentials
220 Elizabeth St.
New York, N. Y. 10012
Part No. MS5-1000

Fig. 16 — Socket for use with HC2000H.

DIMENSIONAL OUTLINE
HC2000H



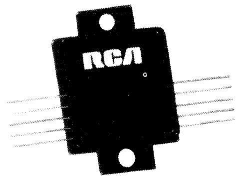
DIMENSIONS IN INCHES AND
MILLIMETERS (VALUES IN PARENTHESES)

*TERMINALS 6 AND 11 ARE CONNECTED INTERNALLY

RCA Solid State Division

Power Hybrid Circuits

HC2500



(Approx. 1/2 Actual Size) H-1697

Multi-Purpose, Low-Distortion 7-Ampere Operational Amplifier

Linear Amplifier for Applications in Industrial and Commercial Equipment

Features:

- Bandwidth: 30 kHz at 60 W
- High power output: up to 100 W(rms)
- High output current: 7 A (peak)
- Low IMD and THD
- Adjustable idling current
- Stability with resistive or reactive loads
- Single or split power supply (30 to 75 V, single, ±15 to ±37.5, split)
- Class AB output stage
- Direct coupling to load
- Socket available
- Rugged package with heavy leads
- Light weight: 100 grams

RCA type HC2500● is a complete solid-state hybrid amplifier in a compact hermetic package. It employs a quasi-complementary-symmetry output circuit with hometaxial-base output transistors.

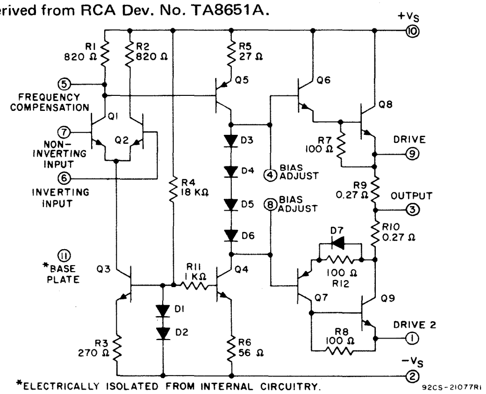
The HC2500 is a low-distortion, 100-watt linear amplifier. The output section can be externally biased class AB for low intermodulation and total harmonic distortion. Terminals are available for external frequency compensation, external short-circuit protection, and inverting and non-inverting inputs.

The HC2500 is recommended for the following applications; servo amplifiers (ac, dc, PWM), deflection amplifiers, power operational amplifiers, voltage regulators, driven inverters, hi-fi amplifiers, PA systems, and solenoid drivers.

● Derived from RCA Dev. No. TA8651A.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

SUPPLY VOLTAGE:		
Between leads 1 and 10	75	V
OUTPUT CURRENT (Peak)	7	A
TOTAL DISSIPATION:		
Per output device	See Figs. 4 & 5	
TEMPERATURE RANGE:		
Storage	−55 to +125°C	
Output junction	−55 to +150°C	
LEAD TEMPERATURE (During Soldering):		
At distance ⩾ 1/8 in. (3.17 mm) from case for 10 s max.	235°C	



*ELECTRICALLY ISOLATED FROM INTERNAL CIRCUITRY.

Fig. 1 – Schematic diagram of type HC2500 operational amplifier.

COMPARISON CHART

TYPE	IM DIST. @ 50 mW	OUTPUT PROTECTION NETWORK	OPERATING MODE	FREQUENCY COMPENSATION	COMMUTATING DIODES
HC2500	0.06%	NO	CLASS AB	CAPACITOR ON SIGNAL TERMINALS	NO
HC2000H	5.8%	YES	CLASS B	LC FILTER ON OUTPUT	YES

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ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C and Supply Voltage (V_S) = ±37.5 V*

CHARACTERISTIC	SYMBOL	REFERENCE FIG. NO.	TEST CONDITIONS: SPECIAL NOTES	FREQ. (f)–kHz	OUTPUT POWER (P_O)–W	LOAD RESIST. (R_L)–Ω	LIMITS: MIN.	TYP.	MAX.	UNITS
Offset Voltage	V_{offset}	3	Measured Pin 3 to Gnd	–	–	4	–	–	±250	mV
Quiescent Current	I_o	3	Idling Current < 1 mA	–	–	Open	–	–	±30	mA
Output Voltage Swing	V_{OUT}		Peak dc voltage	0	200	4	28	–	–	V
Closed-Loop Bandwidth	f_H	3		–	1	4	43	–	–	kHz
Total Harmonic Distortion	THD	15		1	60	4	–	0.3	0.5	%
Closed-Loop Voltage Gain	A_{CL}	3		1	1	4	31	32	–	
Thermal Resistance	$R_{\theta JC}$	5		–	–	–	–	–	2	°C/W

ELECTRICAL CHARACTERISTICS
Typical Values (for Design Guidance), *At Case Temperature (T_C) = 25°C and Supply Voltage (V_S) = ±37.5*

CHARACTERISTIC	SYMBOL	REFERENCE FIG. NO.	SPECIAL NOTES	FREQ. (f)–kHz	OUTPUT POWER (P_O)–W	LOAD RESIST. (R_L)–Ω	MIN.	TYP.	MAX.	UNITS
Open-Loop Voltage Gain	A_{OL}	8, 19	Idling current = 50 mA	1	25	4	–	70	–	dB
Input Offset Voltage	V_{IO}	20		–	0	Open	–	±10	–	mV
Input Offset Current	I_{IO}	20		–	0	Open	–	7	–	μA
Input Bias Current	I_{IB}	20		–	0	Open	–	20	–	μA
Common-Mode Input Impedance	R_{CM}	22		0.005	0	Open	–	1	–	MΩ
Common-Mode Input-Voltage Range	V_{ICR}			0.5	100	4	–	32	–	V
Common-Mode-Rejection Ratio	CMRR			0.005	0	Open	–	50	–	dB
Supply-Voltage Ripple-Rejection Ratio	V_{RR}			0.06	0	4	–	30	–	dB
Intermodulation Distortion	IMD	14	Idling current = 50 mA	–	0.05	4	–	0.06	–	%
Slew Rate	SR	18	A_{CL} = 2, C_c = 100 pF	0.5 Square Wave	–	4	–	4.3	–	V/μs
Idling-Current Drift	ΔI_i	17	25°C to 100°C	–	–	4	–	1	–	mA/°C

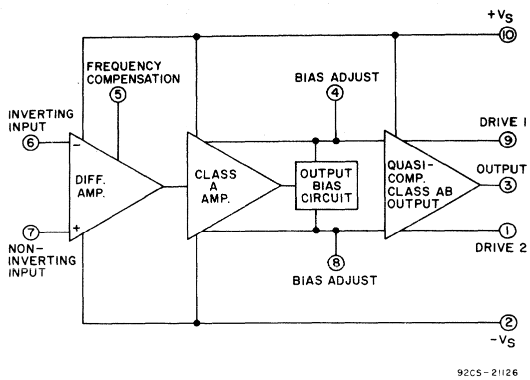


Fig. 2 – Block diagram of HC2500 100-watt class AB amplifier.

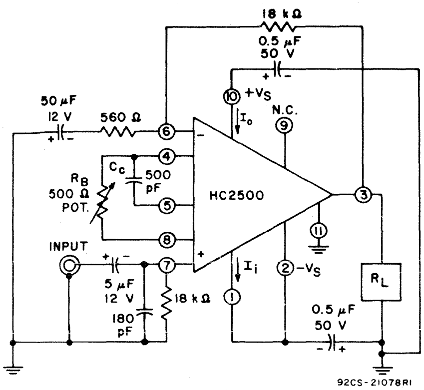


Fig. 3 – Typical test circuit with split supply for measuring A_{CL}, I_i, I_o, V_{offset}, f_H, THD, and IMD.

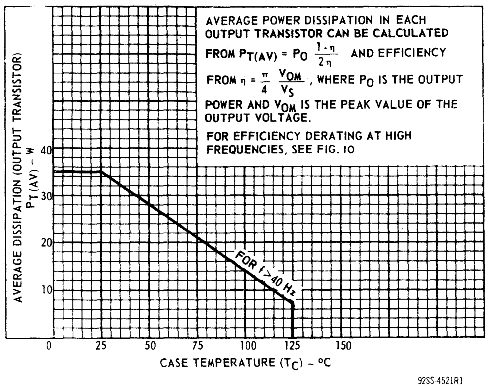


Fig. 4 – Dissipation (average) derating curve for each output transistor (for symmetrical waveforms with f >40 Hz).

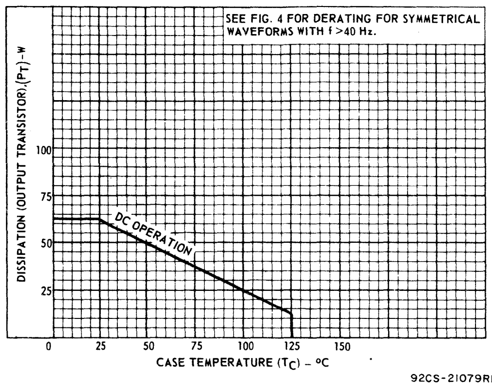


Fig. 5 – Dissipation derating curve for each output transistor.

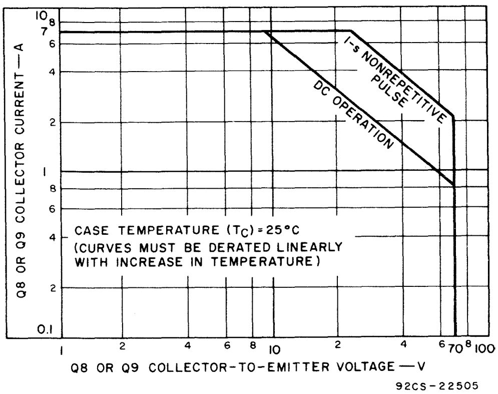


Fig. 6 – Maximum operating area for HC2500.

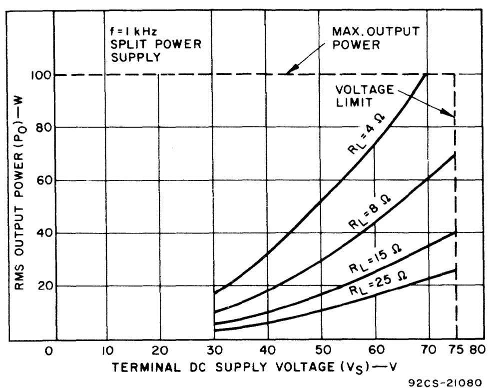


Fig. 7 – Output power as a function of supply voltage, with various values of load resistance, for symmetrical sine-wave operation.

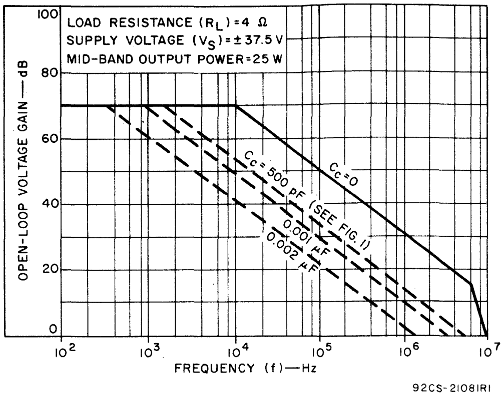


Fig. 8 — Typical open-loop voltage gain vs. frequency.

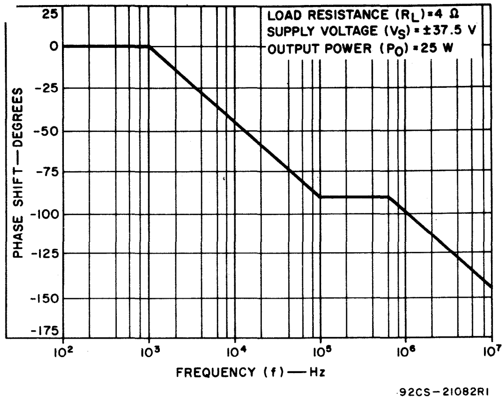


Fig. 9 — Typical open-loop phase shift vs. frequency.

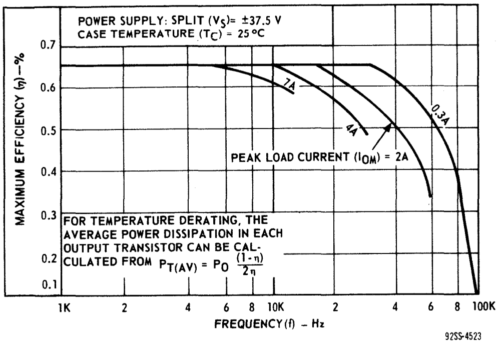


Fig. 10 — Maximum efficiency vs. frequency for several values of peak load current.

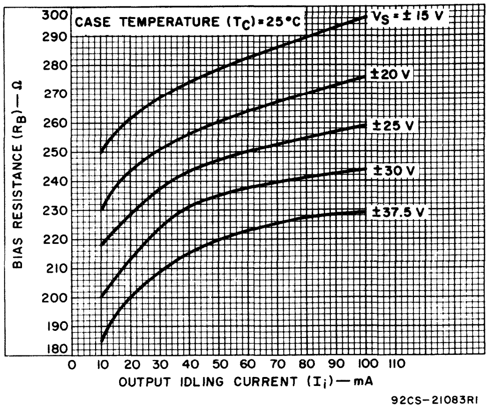


Fig. 11 — Bias resistor (R_B in Fig. 3) value vs. output idling current (I_i).

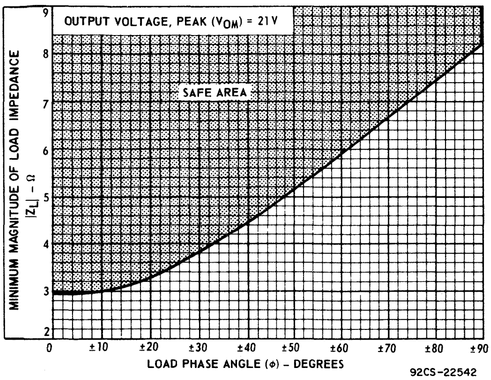


Fig. 12 — Minimum load impedance vs. load phase angle and safe area of operation.

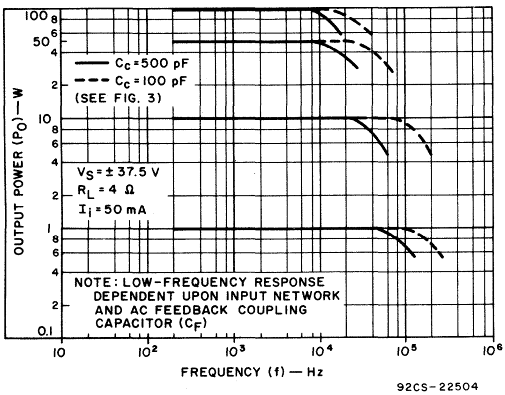


Fig. 13 — Output power vs. frequency.

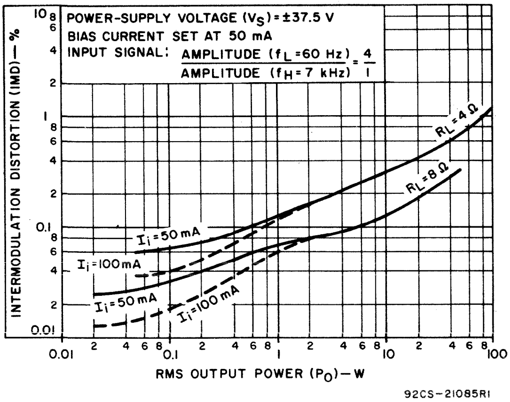


Fig. 14 — Typical intermodulation distortion vs. rms output power.

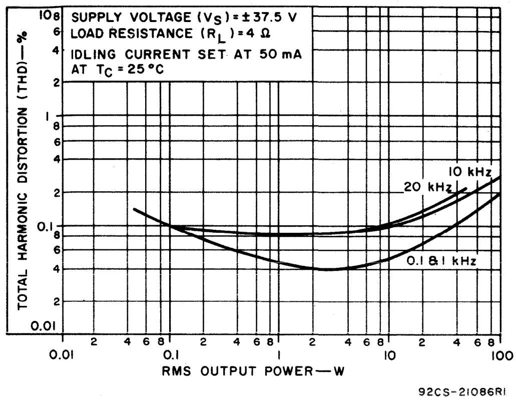


Fig. 15 — Typical total harmonic distortion vs. rms output power.

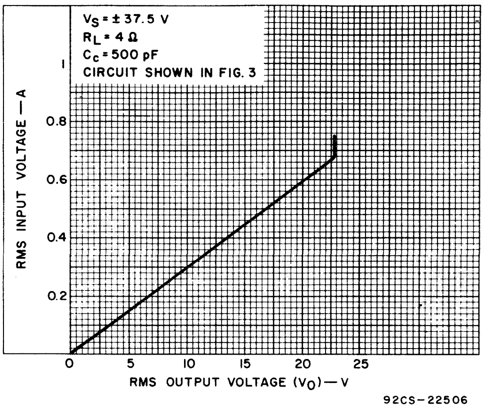


Fig. 16 — Input sensitivity.

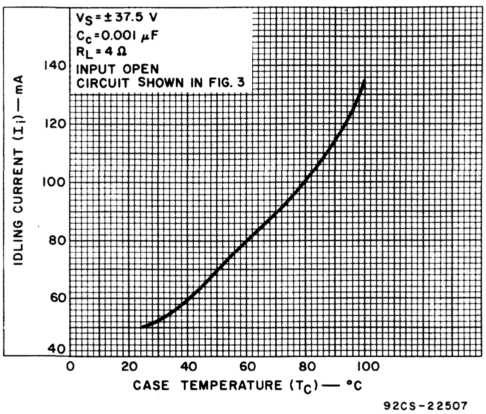


Fig. 17 — Typical idling-current dirft.

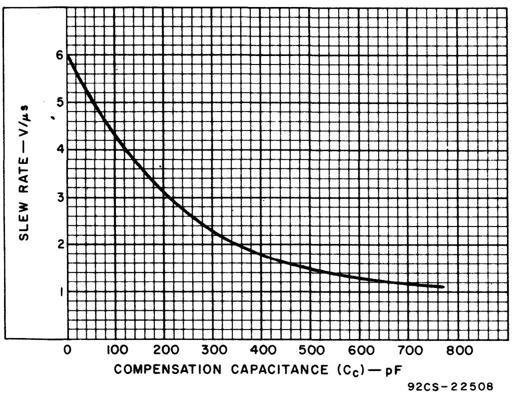


Fig. 18 — Typical slew rate vs. value of compensation capacitor, C_c (test circuit shown in Fig. 21).

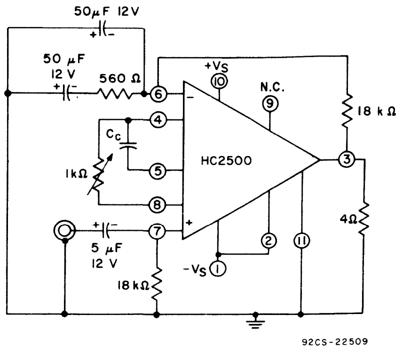
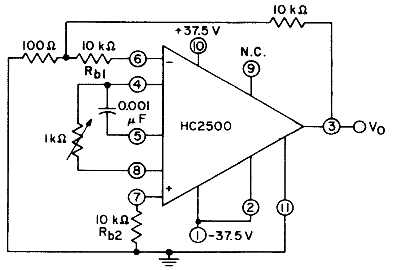


Fig. 19 — Test circuit for open-loop gain and phase response.



$V_{IO} = -\frac{V_O}{100}$ with R_{b1} and R_{b2} shorted

$I_{IO} = -\frac{V_O}{100\,R_{b2}}$

$I_{Ib} = \frac{\pm V_O}{100\,R_{b2}}$ with R_{b1} shorted

92CS-22510

Fig. 20 — Test circuit for input offset voltage and current test.

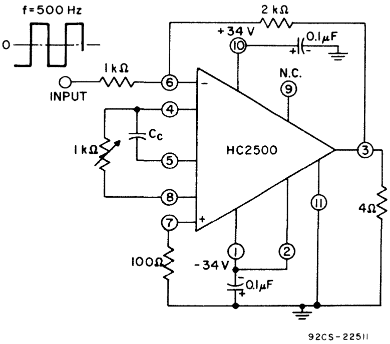
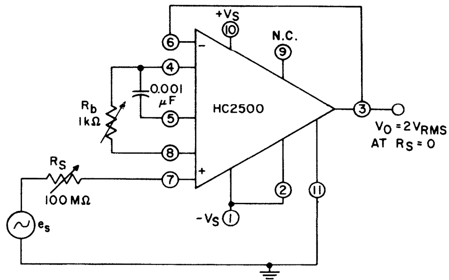


Fig. 21 — Circuit used to test slew rate.

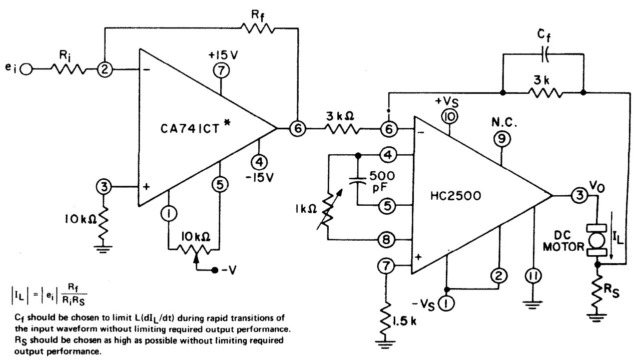


$R_{CM} = 9\,R_S$ with series resistance (R_S) increased from zero until output voltage (V_O) is reduced by 10%.

92CS-22512

Fig. 22 — Test circuit for measuring common-mode input resistance.

TYPICAL APPLICATION CIRCUITS



$|I_L| = |e_i| \frac{R_f}{R_i R_S}$

C_f should be chosen to limit $L(dI_L/dt)$ during rapid transitions of the input waveform without limiting required output performance.
R_S should be chosen as high as possible without limiting required output performance.

*See Data Bulletin File 531.

92CM-22513

Fig. 23 — Current-feedback motor-control circuit.

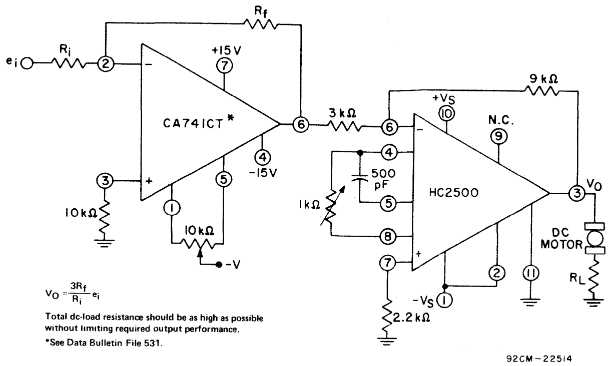


Fig. 24 – Voltage-feedback motor-control circuit.

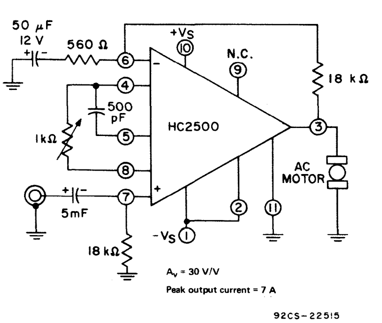


Fig. 25 – AC motor control.

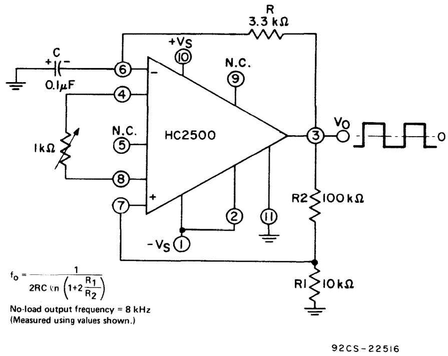


Fig. 26 – High-power astable multivibrator.

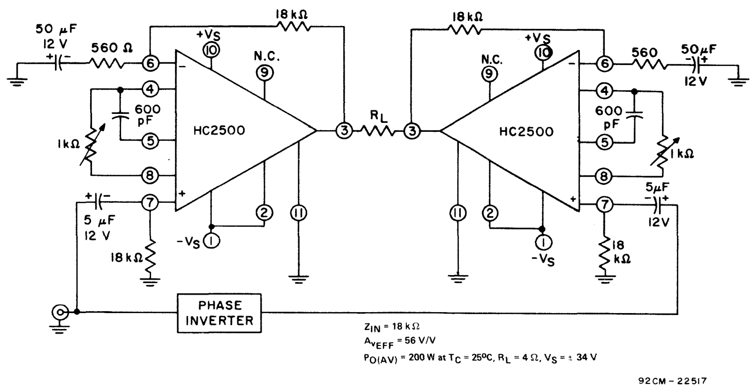
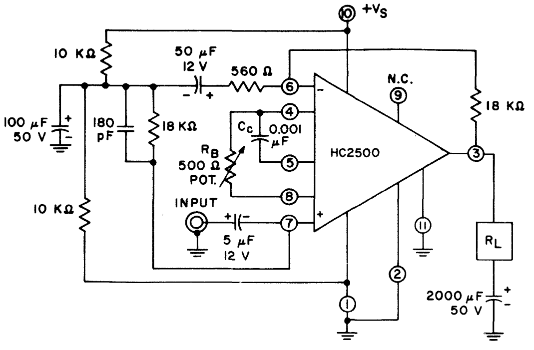


Fig. 27 – Bridge circuit for loads greater than 100 watts.



V_S	54 V
P_{out}	60 W
Idling Current (R_B = 168 Ω)	50 mA
THD	0.15%
IMD @ 50 mW	0.06%
V_{offset} Pin 3 To Gnd.	+ 100 mV
Efficiency	64%
R_L	4 ohms

Fig. 28 – Typical circuit connections for operation of HC2500 with single-ended supply, and performance data.

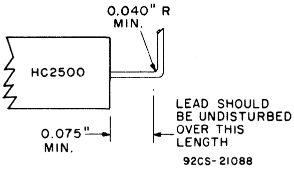
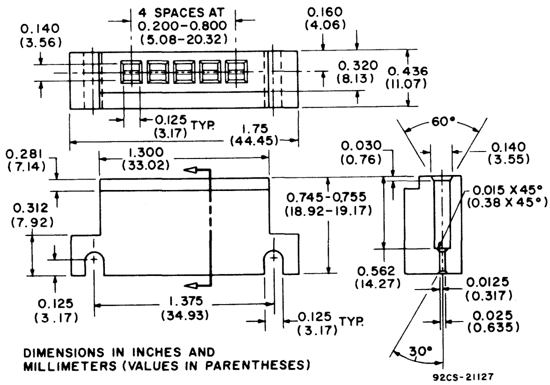


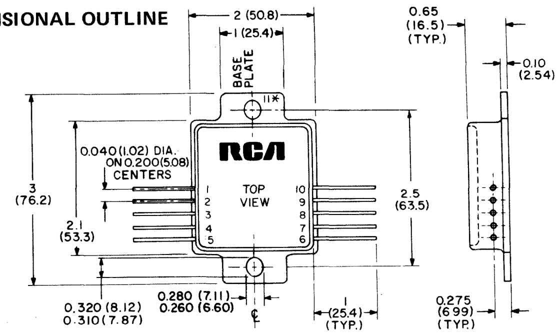
Fig. 29 – Recommended lead-bending specification.



Socket: RCA DF-293A, or
Electronic Essentials,
210 Elizabeth St.
New York, N. Y. 10012
Part No. MS5-1000.

Fig. 30 – Socket for use with HC2500.

DIMENSIONAL OUTLINE



DIMENSIONS IN INCHES AND
MILLIMETERS (VALUES IN PARENTHESES)

*CASE (TERMINAL No. 11) IS ELECTRICALLY ISOLATED FROM INTERNAL CIRCUITRY.

Application Notes

RCA
Solid State
Division

Solid State Devices
Operating Considerations
1CE-402

Operating Considerations for RCA Solid State Devices

Solid state devices are being designed into an increasing variety of electronic equipment because of their high standards of reliability and performance. However, it is essential that equipment designers be mindful of good engineering practices in the use of these devices to achieve the desired performance.

This Note summarizes important operating recommendations and precautions which should be followed in the interest of maintaining the high standards of performance of solid state devices.

The ratings included in RCA Solid State Devices data bulletins are based on the Absolute Maximum Rating System, which is defined by the following Industry Standard (JEDEC) statement:

Absolute-Maximum Ratings are limiting values of operating and environmental conditions applicable to any electron device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

The device manufacturer chooses these values to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in device characteristics.

The equipment manufacturer should design so that initially and throughout life no absolute-maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply-voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in device characteristics.

It is recommended that equipment manufacturers consult RCA whenever device applications involve unusual electrical, mechanical or environmental operating conditions.

GENERAL CONSIDERATIONS

The design flexibility provided by these devices makes possible their use in a broad range of applications and under many different operating conditions. When incorporating these devices in equipment, therefore, designers should anticipate the rare possibility of device failure and make certain that no safety hazard would result from such an occurrence.

The small size of most solid state products provides obvious advantages to the designers of electronic equipment. However, it should be recognized that these compact devices usually provide only relatively small insulation area between adjacent leads and the metal envelope. When these devices are used in moist or contaminated atmospheres, therefore, supplemental protection must be provided to prevent the development of electrical conductive paths across the relatively small insulating surfaces. For specific information on voltage creepage, the user should consult references such as the JEDEC Standard No. 7 "Suggested Standard on Thyristors," and JEDEC Standard RS282 "Standards for Silicon Rectifier Diodes and Stacks".

The metal shells of some solid state devices operate at the collector voltage and for some rectifiers and thyristors at the anode voltage. Therefore, consideration should be given to the possibility of shock hazard if the shells are to operate at voltages appreciably above or below ground potential. In general, in any application in which devices are operated at voltages which may be dangerous to personnel, suitable precautionary measures should be taken to prevent direct contact with these devices.

Devices should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

TESTING PRECAUTIONS

In common with many electronic components, solid-state devices should be operated and tested in circuits which have reasonable values of current limiting resistance, or other forms of effective current overload protection. Failure to observe these precautions can cause excessive internal heating of the device resulting in destruction and/or possible shattering of the enclosure.

TRANSISTORS WITH FLEXIBLE LEADS

Flexible leads are usually soldered to the circuit elements. It is desirable in all soldering operations to provide some slack or an expansion elbow in each lead, to prevent excessive tension on the leads. It is important during the soldering operation to avoid excessive heat in order to prevent possible damage to the devices. Some of the heat can be absorbed if the flexible lead of the device is grasped between the case and the soldering point with a pair of pliers.

TRANSISTORS WITH MOUNTING FLANGES

The mounting flanges of JEDEC-type packages such as the TO-3 or TO-66 often serve as the collector or anode terminal. In such cases, it is essential that the mounting flange be securely fastened to the heat sink, which may be the equipment chassis. Under no circumstances, however, should the mounting flange be soldered directly to the heat sink or chassis because the heat of the soldering operation could permanently damage the device.

Such devices can be installed in commercially available sockets. Electrical connections may also be made by soldering directly to the terminal pins. Such connections may be soldered to the pins close to the pin seals provided care is taken to conduct excessive heat away from the seals; otherwise the heat of the soldering operation could crack the pin seals and damage the device.

During operation, the mounting-flange temperature is higher than the ambient temperature by an amount which depends on the heat sink used. The heat sink must have sufficient thermal capacity to assure that the heat dissipated in the heat sink itself does not raise the device mounting-flange temperature above the rated value. The heat sink or chassis may be connected to either the positive or negative supply.

In many applications the chassis is connected to the voltage-supply terminal. If the recommended mounting hardware shown in the data bulletin for the specific solid-state device is not available, it is necessary to use either an anodized aluminum insulator having high thermal conductivity or a mica insulator between the mounting-flange and the chassis. If an insulating aluminum washer is required, it should be drilled or punched to provide the two mounting holes for the terminal pins. The burrs should then be removed from the washer and the washer anodized. To insure that the anodized insulating layer is not destroyed during mounting, it is necessary to remove the burrs from the holes in the chassis.

It is also important that an insulating bushing, such as glass-filled nylon, be used between each mounting bolt and the chassis to prevent a short circuit. However, the insulating bushing should not exhibit shrinkage or softening under the operating temperatures encountered. Otherwise the thermal resistance at the interface between transistor and heat sink may increase as a result of decreasing pressure.

PLASTIC POWER TRANSISTORS AND THYRISTORS

RCA power transistors and thyristors (SCR's and triacs) in molded-silicone-plastic packages are available in a wide range of power-dissipation ratings and a variety of package configurations. The following paragraphs provide guidelines for handling and mounting of these plastic-package devices, recommend forming of leads to meet specific mounting requirements, and describe various mounting arrangements, thermal considerations, and cleaning methods. This information is intended to augment the data on electrical characteristics, safe operating area, and performance capabilities in the technical bulletin for each type of plastic-package transistor or thyristor.

Lead-Forming Techniques

The leads of the RCA VERSAWATT in-line plastic packages can be formed to a custom shape, provided they are not indiscriminately twisted or bent. Although these leads can be formed, they are not flexible in the general sense, nor are they sufficiently rigid for unrestrained wire wrapping

Before an attempt is made to form the leads of an in-line package to meet the requirements of a specific application, the desired lead configuration should be determined, and a lead-bending fixture should be designed and constructed. The use of a properly designed fixture for this operation eliminates the need for repeated lead bending. When the use of a special bending fixture is not practical, a pair of long-nosed pliers may be used. The pliers should hold the lead firmly between the bending point and the case, but should not touch the case.

When the leads of an in-line plastic package are to be formed, whether by use of long-nosed pliers or a special bending fixture, the following precautions must be observed to avoid internal damage to the device:

1. Restrain the lead between the bending point and the plastic case to prevent relative movement between the lead and the case.
2. When the bend is made in the plane of the lead (spreading), bend only the narrow part of the lead.
3. When the bend is made in the plane perpendicular to that of the leads, make the bend at least 1/8 inch from the plastic case.
4. Do not use a lead-bend radius of less than 1/16 inch.
5. Avoid repeated bending of leads.

The leads of the TO-220AB VERSAWATT in-line package are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement tends to impose axial stress on the leads, some method of strain relief should be devised.

Wire wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. Soldering to the leads is also allowed. The maximum soldering temperature, however, must not exceed 275°C and must be applied for not more than 5 seconds at a distance not less than 1/8 inch from the plastic case. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions.

The leads of RCA molded-plastic high-power packages are not designed to be reshaped. However, simple bending of the leads is permitted to change them from a standard vertical to a standard horizontal configuration, or conversely. Bending of the leads in this manner is restricted to three 90-degree bends; repeated bendings should be avoided.

Mounting

Recommended mounting arrangements and suggested hardware for the VERSAWATT transistors are given in the data bulletins for specific devices and in RCA Application Note AN-4124. When the transistor is fastened to a heat sink, a rectangular washer (RCA Part No. NR231A) is recommended to minimize distortion of the mounting flange. Excessive distortion of the flange could cause damage to the transistor. The washer is particularly important when the size of the mounting hole exceeds 0.140 inch (6-32 clearance). Larger holes are needed to accommodate insulating bushings; however, the holes should not be larger than necessary to provide hardware clearance and, in any case, should not exceed a diameter of 0.250 inch.

Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is specified. Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. An excellent method of avoiding this problem is to use a spacer or combination spacer-isolating bushing which raises the screw head or nut above the top surface of the plastic body. The material used for such a spacer or spacer-isolating bushing should, of course, be carefully selected to avoid "cold flow" and consequent reduction in mounting force. Suggested materials for these bushings are diallphtalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate. Unfilled nylon should be avoided.

Modification of the flange can also result in flange distortion and should not be attempted. The transistor should not be soldered to the heat sink by use of lead-tin solder because the heat required with this type of solder will cause the junction temperature of the transistor to become excessively high.

The TO-220AA plastic transistor can be mounted in commercially available TO-66 sockets, such as UID Electronics Corp. Socket No. PTS-4 or equivalent. For testing purposes, the TO-220AB in-line package can be mounted in a Jetron Socket No. DC74-104 or equivalent. Regardless of the mounting method, the following precautions should be taken:

1. Use appropriate hardware.
2. Always fasten the transistor to the heat sink before the leads are soldered to fixed terminals.
3. Never allow the mounting tool to come in contact with the plastic case.
4. Never exceed a torque of 8 inch-pounds.
5. Avoid oversize mounting holes.
6. Provide strain relief if there is any probability that axial stress will be applied to the leads.
7. Use insulating bushings to prevent hot-creep problems. Such bushings should be made of diallphthalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate.

The maximum allowable power dissipation in a solid state device is limited by the junction temperature. An important factor in assuring that the junction temperature remains below the specified maximum value is the ability of the associated thermal circuit to conduct heat away from the device.

When a solid state device is operated in free air, without a heat sink, the steady-state thermal circuit is defined by the junction-to-free-air thermal resistance given in the published data for the device. Thermal considerations require that a free flow of air around the device is always present and that the power dissipation be maintained below the level which would cause the junction temperature to rise above the maximum rating. However, when the device is mounted on a heat sink, care must be taken to assure that all portions of the thermal circuit are considered.

To assure efficient heat transfer from case to heat sink when mounting RCA molded-plastic solid state power devices, the following special precautions should be observed:

1. Mounting torque should be between 4 and 8 inch-pounds.
2. The mounting holes should be kept as small as possible.
3. Holes should be drilled or punched clean with no burrs or ridges, and chamfered to a maximum radius of 0.010 inch.
4. The mounting surface should be flat within 0.002 inch/inch.
5. Thermal grease (Dow Corning 340 or equivalent) should always be used on both sides of the insulating washer if one is employed.
6. Thin insulating washers should be used. (Thickness of factory-supplied mica washers range from 2 to 4 mils).
7. A lock washer or torque washer, made of material having sufficient creep strength, should be used to prevent degradation of heat sink efficiency during life.

A wide variety of solvents is available for degreasing and flux removal. The usual practice is to submerge components in a solvent bath for a specified time. However, from a reliability stand point it is extremely important that the solvent, together with other chemicals in the solder-cleaning system (such as flux and solder covers), do not adversely affect the life of the component. This consideration applies to all non-hermetic and molded-plastic components.

It is, of course, impractical to evaluate the effect on long-term transistor life of all cleaning solvents, which are marketed with numerous additives under a variety of brand names. These solvents can, however, be classified with respect to their component parts, as either acceptable or unacceptable. Chlorinated solvents tend to dissolve the outer package and, therefore, make operation in a humid atmosphere unreliable. Gasoline and other hydrocarbons cause the inner encapsulant to swell and damage the transistor. Alcohol and unchlorinated freons are acceptable solvents. Examples of such solvents are:

1. Freon TE
2. Freon TE-35
3. Freon TP-35 (Freon PC)
4. Alcohol (isopropanol, methanol, and special denatured alcohols, such as SDA1, SDA30, SDA34, and SDA44)

Care must also be used in the selection of fluxes for lead soldering. Rosin or activated rosin fluxes are recommended, while organic or acid fluxes are not. Examples of acceptable fluxes are:

1. Alpha Reliaros No. 320-33
2. Alpha Reliaros No. 346
3. Alpha Reliaros No. 711
4. Alpha Reliafoam No. 807
5. Alpha Reliafoam No. 809
6. Alpha Reliafoam No. 811-13
7. Alpha Reliafoam No. 815-35
8. Kester No. 44

If the completed assembly is to be encapsulated, the effect on the molded-plastic transistor must be studied from both a chemical and a physical standpoint.

RECTIFIERS AND THYRISTORS

A surge-limiting impedance should always be used in series with silicon rectifiers and thyristors. The impedance value must be sufficient to limit the surge current to the value specified under the maximum ratings. This impedance may be provided by the power transformer winding, or by an external resistor or choke.

A very efficient method for mounting thyristors utilizing packages such as the JEDEC TO-5 and "modified TO-5" is to provide intimate contact between the heat sink and at least one half of the base of the device opposite the leads. These packages can be mounted to the heat sink mechanically with glue or an epoxy adhesive, or by soldering. Soldering to the heat sink is preferable because it is the most efficient method.

The use of a "self-jigging" arrangement and a solder preform is recommended. Such an arrangement is illustrated in RCA Publication MHI-300B, "Mounting Hardware Supplied with RCA Semiconductor Devices". If each unit is soldered individually, the heat source should be held on the heat sink and the solder on the unit. Heat should be applied only long enough to permit solder to flow freely. For more detailed thyristor mounting considerations, refer to Application Note AN3822, "Thermal Considerations in Mounting of RCA Thyristors".

MOS FIELD-EFFECT TRANSISTORS

Insulated-Gate Metal Oxide-Semiconductor Field-Effect Transistors (MOS FETs), like bipolar high-frequency transistors, are susceptible to gate insulation damage by the electrostatic discharge of energy through the devices. Electrostatic discharges can occur in an MOS FET if a type with an unprotected gate is picked up and the static charge, built in the handler's body capacitance, is discharged through the device. With proper handling and applications procedures, however, MOS transistors are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applications, with virtually no problems of damage due to electrostatic discharge.

In some MOS FETs, diodes are electrically connected between each insulated gate and the transistor's source. These diodes offer protection against static discharge and in-circuit transients without the need for external shorting mechanisms. MOS FETs which do not include gate-protection diodes can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs attached to the device by the vendor, or by the insertion into conductive material such as "ECCOSORB* LD26" or equivalent.
   (NOTE: Polystyrene *insulating* "SNOW" is not sufficiently conductive and should not be used.)
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means, for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.

INTEGRATED CIRCUITS

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads,such as those used in RCA 14-lead and 16-lead flat-packages, less than the lead thickness. It is also extremely important that the ends of the bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

COS/MOS (Complementary-Symmetry MOS) Integrated Circuits

1. Handling

All COS/MOS gate inputs have a resistor/diode gate protection network. All transmission gate inputs and all outputs have diode protection provided by inherent p-n junction diodes. These diode networks at input and output interfaces fully protect COS/MOS devices from gate-oxide failure (70 to 100 volt limit) for static discharge or signal voltage up to 1 to 2 kilovolts under most transient or low-current conditions.

Although protection against electrostatic effects is provided by built-in circuitry, the following handling precautions should be taken:

1. Soldering-iron tips and test equipment should be grounded.
2. Devices should not be inserted in non-conductive containers such as conventional plastic snow or trays.

*Trade Mark: Emerson and Cumming, Inc.

2. Operating

Unused Inputs

All unused input leads must be connected to either V_{SS} or V_{DD}, whichever is appropriate for the logic circuit involved. A floating input on a high-current type, such as the CD4009A, CD4010A, not only can result in faulty logic operation, but can cause the maximum power dissipation of 200 milliwatts to be exceeded and may result in damage to the device. Inputs to these types, which are mounted on printed-circuit boards that may temporarily become unterminated, should have a pull-up resistor to V_{SS} or V_{DD}. A useful range of values for such resistors is from 0.2 to 1 megohm.

Input Signals

Signals shall not be applied to the inputs while the device power supply is off unless the input current is limited to a steady state value of less than 10 milliamperes.

Output Short Circuits

Shorting of outputs to V_{SS} or V_{DD} can damage many of the higher-output-current COS/MOS types, such as the CD4007A, CD4009A, and CD4010A. In general, these types can all be safely shorted for supplies up to 5 volts, but will be damaged (depending on type) at higher power-supply voltages. For cases in which a short-circuit load, such as the base of a p-n-p or an n-p-n bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for a safe operation below 200 milliwatts.

For detailed COS/MOS IC Handling Considerations, refer to Application Note ICAN-6000 "Handling Considerations for MOS Integrated Circuits".

SOLID STATE CHIPS

Solid state chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size, and therefore, require special handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
   A. Storage temperature, 40°C max.
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment.
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
4. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

Silicon Transistors for High-Voltage Application

by

D. T. DeFino

This note discusses several new applications for RCA high-voltage silicon transistors (2N3583, 2N3584, 2N3585, 2N3439 and 2N3440). These devices are triple-diffused n-p-n types featuring high frequency response, fast switching speeds, and low cost. Electrical characteristics are listed in Table I.

The advent of these types has made possible many new applications for transistors. Among these applications are circuits in which, until now, the use of transistors was restricted because of high operating voltages (horizontal-deflection circuits, for example). Other applications include those in which the use of a higher supply voltage can enhance circuit design, performance, and economy. High supply voltages reduce the cost of line-operated amplifiers, and improve the efficiency of inverters. Several other important applications are illustrated.

Series Voltage Regulator

A voltage regulator provides a constant output voltage when the input voltage and/or output current is varied over a limited range. As shown in Fig.1, the pass transistor, acting on a signal from the control circuit, prevents the output voltage V_{out} from varying. The control circuit receives a sample of the output voltage, compares it with a reference voltage, and

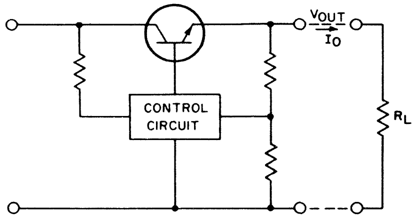


Fig.1 - Basic form of a transistorized series voltage regulator.

amplifies the difference. The resulting error signal corrects the collector current I_C of the pass transistor so that the collector-to-emitter voltage V_{CE} is always

Maximum Ratings, *Absolute-Maximum Values:*

	2N3583	2N3584	2N3585	2N3439	2N3440	
COLLECTOR-TO-BASE VOLTAGE, V_{CBO} . .	250	375	500	450	300	Volts
COLLECTOR-TO-EMITTER VOLTAGE, $V_{CEO}(sus)$	175	250	300	350	250	Volts
EMITTER-TO-BASE VOLTAGE, V_{EBO}	6	6	6	7	7	Volts
CONTINUOUS COLLECTOR CURRENT, I_C .	2	2	2	1	1	Amp
PEAK COLLECTOR CURRENT.	5	5	5	-	-	Amp
BASE CURRENT, I_B	1	1	1	0.5	0.5	Amp
TRANSISTOR DISSIPATION, P_T	35	35	35	5	5	Watts

Table I - Electrical characteristics of RCA high-voltage silicon transistors.

the difference between the input voltage V_{in} and the desired output voltage.

The simplest circuit arrangement for a transistor voltage regulator is shown in Fig.2. The circuit consists of a transistor, a resistor, and a zener diode. Because the zener diode maintains the base of the transistor at a constant voltage, changes in output can result only from variations in the base-to-emitter voltage V_{BE} with current and temperature. A zener diode having a high current rating is required if large currents are drawn from the transistor.

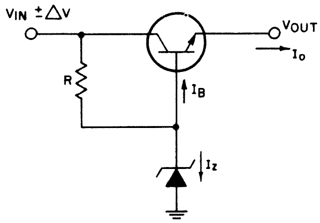


Fig.2 - Simplest circuit arrangement for a transistor voltage regulator.

The maximum value of resistance R which can be used in the circuit is determined as follows:

$$R = \frac{V_{in} - \Delta V - V_{out}}{I_B(max)}$$

Because the maximum base current $I_B(max)$ is equal to $I_o(max)/h_{FE}(min)$, where I_o is the output current and h_{FE} is the dc forward-current transfer ratio, the resistance equation can be rewritten as follows:

$$R = \frac{V_{in} - \Delta V - V_{out}}{I_o(max)} \times h_{FE}(min)$$

The zener diode must be capable of handling a peak current I_Z given by

$$I_Z = \frac{V_{in} + \Delta V - V_{out}}{R} = \frac{[V_{in} + \Delta V - V_{out}]\,[I_o(max)]}{[V_{in} - \Delta V - V_{out}]\,[h_{FE}(min)]}$$

In the series regulator, the pass transistor must remain always in the active region. For this reason, the pass transistor must be chosen carefully to avoid dc forward-bias second breakdown. As shown in Fig.3, under the worst-case condition $I_o(max)$, $V_{in}(min)$, the bias point of the transistor must be within the dc forward-bias second-breakdown rating $P_{s/b}$, or the dc power-dissipation rating P_{dc}, whichever is the limiting factor. From the equations given above, it is obvious that near the operating point h_{FE} should be as high as possible. In general, leakage current and saturation voltage are not important.

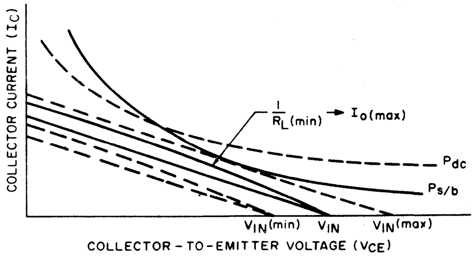


Fig.3 - Transistor load line.

Design Example

The following conditions are specified for a series voltage regulator:

$$V_{out} = 100\ V$$
$$I_o(max) = 400\ mA$$
$$V_{in} = 135 \pm 15\ V$$
$$h_{FE}(min) = 20$$

Circuit values are then determined as follows:

$$R = \frac{(135 - 15 - 100)\ 20}{0.4} = \frac{400}{0.4} = 1\ k\Omega \text{ at } 2.5\ W$$

$$I_B(max) = \frac{0.4}{20} = 20\ mA$$

$$I_Z = \frac{135 + 15 - 100}{1000} = \frac{50}{1000} = 50\ mA$$

Therefore, the zener-diode requirements are $V_Z = 100\ V$, $I_Z = 50\ mA$, $P_Z = 5\ W$. Under worst-case conditions, the transistor must be capable of handling 400 milliamperes at 50 volts, or a dissipation of 20 watts. In addition, the point 50 V and 400 mA must be within the dc second-breakdown rating of the transistor. Fig.4 shows the circuit values for this regulator.

The power-dissipation rating of the resistor and zener diode can be reduced by addition of another transistor (usually much smaller in dissipation) in a configuration such as that shown in Fig.5. This arrangement effectively increases the over-all minimum gain. The two transistors can be regarded as one in which the effective h_{FE} (approximately the product of the gain of the two transistors) can be substituted for h_{FE} in the previous equations. Because the 2N3440 has a minimum gain of 40 at 20 mA, the minimum effective gain is (40)(20) = 800. From this value, the new resistor and zener diode requirements can be calculated as follows:

$$R = \frac{(135 - 15 - 100)\ 800}{0.4} = 40\ k\Omega \text{ at } 0.062\ W$$

$$I_Z = \frac{135 + 15 - 100}{40000} = \frac{50}{40000} = 1.25\ mA$$

$$P_Z = 125\ mW$$

The maximum power dissipated by the 2N3440 transistor in this circuit is (20 mA)(50 V) = 1 W.

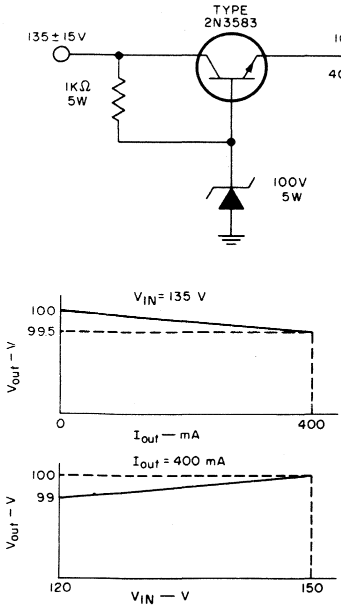


Fig.4 - Schematic diagram of a simple transistor voltage regulator.

The disadvantage of the circuit of Fig.5 as compared with that of Fig.4 is that voltage regulation is less sensitive because there are two junctions to create V_{BE} variations with current and voltage changes.

Fig.6 shows a feedback arrangement designed to improve regulation. In this circuit, the output is sampled and compared with a very stable reference voltage. The resulting error signal is used to adjust the bias on the pass transistor. The requirements for Q3 are determined in the same manner as those for the zener diode in the preceding circuits. The zener-diode current I_Z(max) is equal to the collector current I_C(max) of Q3 divided by the minimum gain of Q3 at I_C(max).

In general, the full load voltage need not be fed back. Instead, a voltage divider can be used to reduce the voltage requirement on the zener diode. Although the voltage divider also degrades the performance, this method must be used if a variable output voltage is required. Fig.7 shows a typical high-voltage regulator that provides an output variable from 175 to 225 volts and delivers up to 150 mA. Performance curves for this circuit are shown in Fig.8.

Switching Regulator

The advantage of a transistorized switching regulator, such as that shown in Fig.9, is its extremely high efficiency. It does not, however, provide the excellent regulation obtainable from a series-type regulator. For this reason, a switching regulator is normally used as a coarse or pre-regulator preceding a series regulator. The switching regulator is highly efficient because the transistor switch is either saturated or cut off. Because both of these conditions are states of low dissipation, very little power is lost in the transistor.

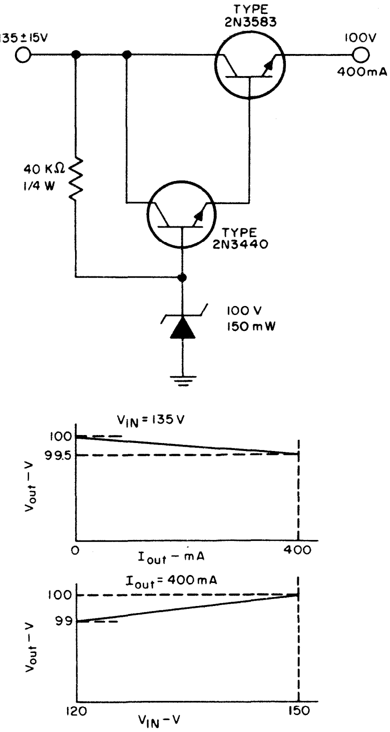


Fig.5 - Schematic diagram of a series voltage regulator using darlington driver.

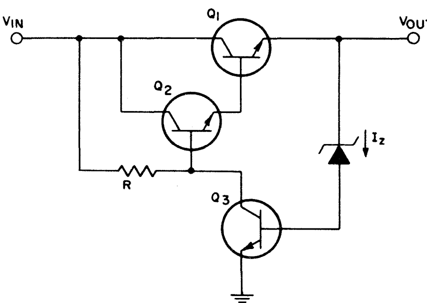


Fig.6 - Schematic diagram of a series voltage regulator employing feedback amplifier.

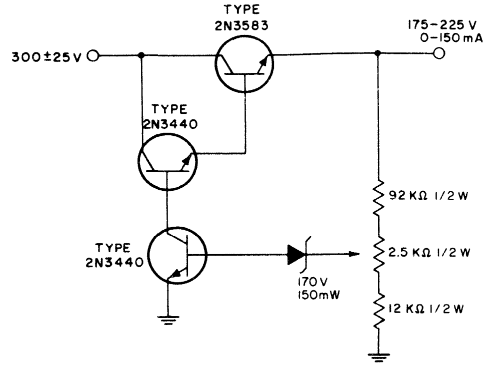


Fig.7 - Schematic diagram of a typical series high-voltage regulator.

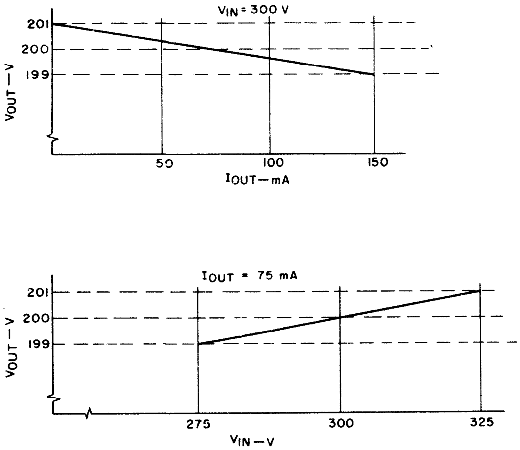


Fig.8 - Regulation characteristics for circuit shown in Fig.7.

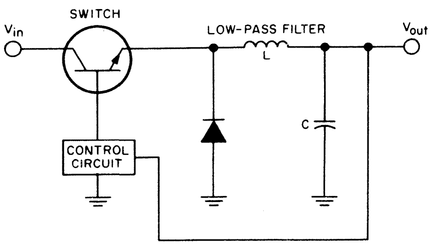


Fig.9 - Simplest form of a transistor switching regulator.

The function of the feedback circuit is to sample the output voltage and compare it with a reference voltage. The difference between these two voltages is used to modulate the pulse width of a pulse generator. This modulated pulse signal is then applied to the base of the switch. Thus, if the output voltage tends to decrease, the pulse width is increased so that the switch remains ON longer to allow the output to increase. Conversely, if the output tends to increase above the desired value, the duty cycle decreases.

When the transistor switch is ON, current flows into the load and into the output capacitor through the inductor. Energy is stored in the inductor and capacitor so that when the switch is OFF, this energy is available to supply the load. During the ON time, the current through the inductor is a linear ramp. The rate of increase of current ($\Delta I/\Delta t$) is determined by the value of the inductance L and the voltage across it ($V_{in} - V_{out}$) as follows:

$$\frac{\Delta I}{\Delta t} = \frac{1}{L}(V_{in} - V_{out})$$

The peak current is therefore given by

$$I_p = \frac{V_{in} - V_{out}}{L}(t_{on})$$

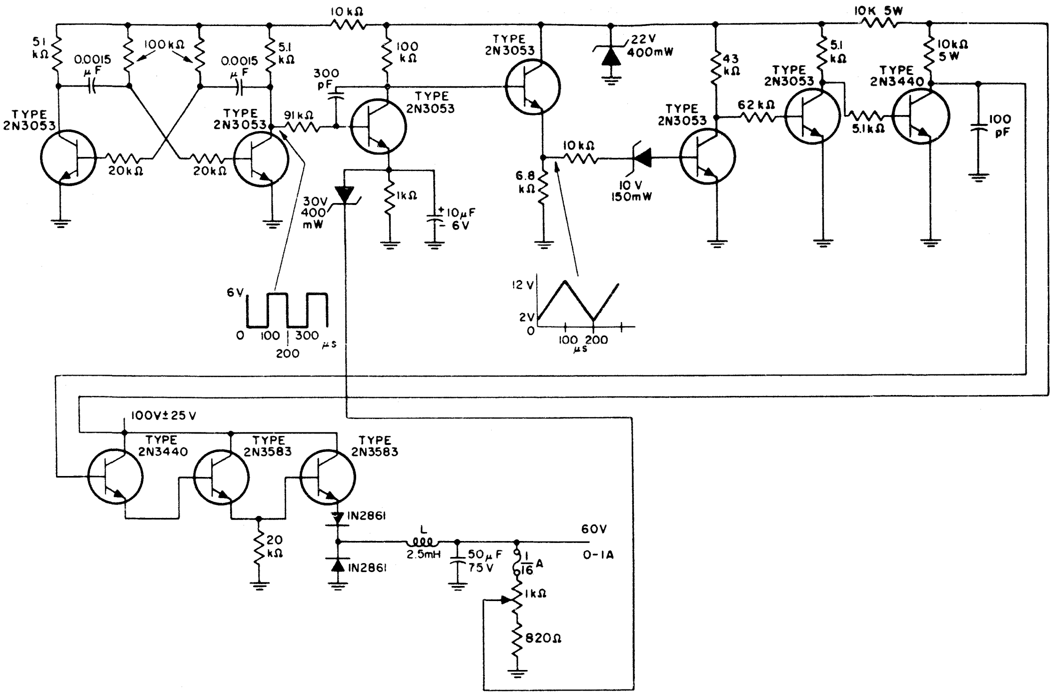
The transistor chosen for this application must provide sufficiently fast switching times, i.e., rise time t_r and fall time t_f. For good regulation over a wide range of input voltage and output current, the duty cycle must be variable from 10 to 90 per cent. Consequently, the minimum pulse width should be one-tenth of the period (1/10f). For low switching losses, the rise and fall times should be about one-fifth of the minimum pulse width, or one-fiftieth of the frequency of the pulse generator (1/50f).

A switching regulator can also be used as a dc step-down transformer. In this application, the regulator provides a very efficient method of obtaining low dc voltage directly from a high-voltage ac line. Fig.10 shows a typical step-down switching regulator which utilizes the dc voltage obtained by rectification of a 117-volt ac line source to provide a regulated 60-volt supply. Performance characteristics for the circuit are shown in Fig.11.

Inverters

An inverter is used to transform dc power to ac power. If the ac output is rectified and filtered to provide dc again, the over-all circuit is referred to as a converter. A converter is normally employed to change the magnitude of an available dc supply.

A transistorized inverter can be made very light in weight and small in size. It is a highly efficient circuit and, unlike its mechanical counterpart, has no



L = 60-turns #18 wire,
core: Carpenter 49 or equiv., 21 E I 0.014-in. laminations not interleaved. Use 0.015-in. air gap.

All resistors 1/2-watt unless specified otherwise.

Fig.10 - Schematic diagram of a typical step-down switching regulator.

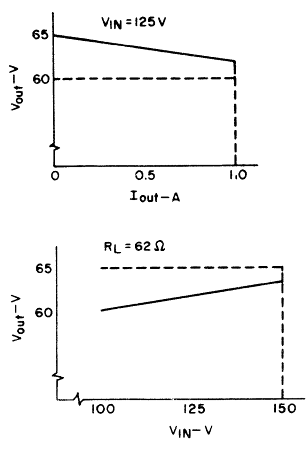


Fig.11 - Performance curves for circuit shown in Fig.10.

moving components. The output from the inverter can be used to drive any equipment which requires an ac supply (motors, ac radios, television receivers, fluorescent lights, and the like). Another very important application of an inverter is in driving the electro-mechanical transducers used in ultrasonic equipment (such as ultrasonic cleaners and sonar detection devices).

The operating frequency of an inverter is usually fixed between 60 Hz and 100 kHz, depending upon the application. For applications in which the operating frequency can be chosen by the designer, the highest possible frequency should be selected.

In general, the size and weight of the inverter can be decreased as the supply voltage and frequency are increased. This relation results mainly from the decreasing size of the transformer needed. The upper frequency and supply voltage are limited by the transistors used. The collector-to-emitter breakdown voltage, for example, must be greater than twice the supply voltage, and the gain-bandwidth product f_T of the device should be greater than ten times the operating frequency. The latter requirement is necessary because switching losses become significant when the rise and fall times of the transistor are greater than about one-fifth of the pulse width.

The important parameters to be considered in the selection of a transistor for an inverter circuit are summarized below:

$V_{CER(sus)} \geq 2V_{CC}$ + leakage reactance spikes

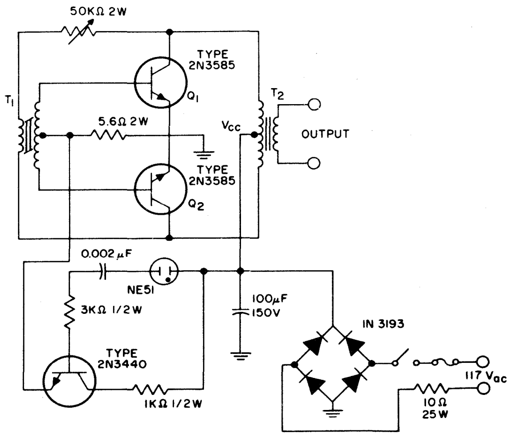
High gain (to reduce feedback power and increase efficiency)

$f_T \geq 10f$ (to reduce switching losses)

$I_{S/b} \geq$ highest starting bias current at V_{CC}

$E_{S/b} \geq$ max. energy stored in the output-transformer leakage inductance.

Fig.12 shows the circuit diagram for a 100-watt inverter which operates directly from a rectified ac-line voltage. The frequency is varied from 25 kHz to 40 kHz by adjustment of the feedback resistor. At 100 watts output, the efficiency is about 90 to 95 per cent, depending upon the frequency. The supply voltage is nominally 140 volts, but can rise to 155 volts during high ac-line-voltage conditions.



T_1 = Allen Bradley RO-3 (E I 102 H 142 A) or equiv.
primary: 160-turn #32 wire;
secondary: each 3-turns #32 wire.

T_2 = Indiana General C2 material (CF216) or equiv.
primary and secondary: 80-turns #28 wire.

Fig.12 - Schematic diagram of a line-operated 100-watt inverter.

Magnetic Deflection Circuit

The electron beam of a magnetically driven display tube is swept across the face of the tube by a linearly changing magnetic field. This deflecting field is produced by a linear ramp of current through the deflection yoke which surrounds the neck of the tube. Fig.13 shows a transistorized magnetic deflection circuit and the corresponding current and voltage waveforms.

The transistor acts as a switch to apply a constant voltage to the inductor. Then, according to the following equation, the current increases linearly to I_p during one-half the sweep time t_S:

$$\frac{\Delta I}{\Delta t} = \frac{V}{L} \quad \Delta I = \frac{V_{CC}}{L}\Delta t, \; I_p = \frac{V_{CC}}{L}\frac{t_S}{2}$$

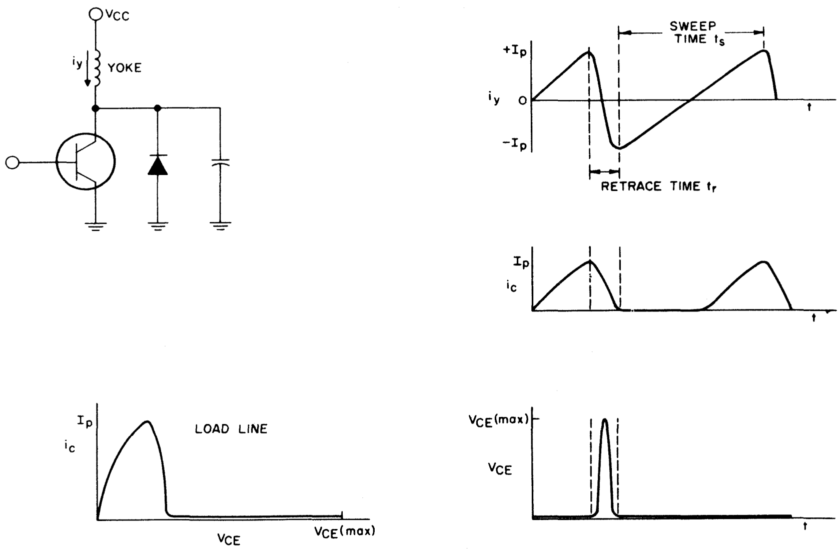


Fig.13 - Basic configuration for a transistor magnetic deflection circuit showing corresponding current and voltage waveforms.

When the transistor is turned off, LC forms a tuned circuit in which the yoke current decreases very rapidly (retrace time t_r) through zero to $-I_p$. At this point capacitor C has a negative voltage across it, the diode is forward-biased, and the yoke current begins to increase toward zero. At this point the cycle begins again.

During the retrace time, when the yoke current is decreasing from I_p to $-I_p$, the voltage across the transistor becomes quite high. The collector-to-emitter voltage is given by

$$V_{CE}(max) = V_{CC} + I_p \omega L$$

The term ω can be expressed as follows:

$$\omega = \frac{1}{\sqrt{LC}} = \frac{\pi}{t_r}$$

Therefore, the equation for $V_{CE}(max)$ may be rewritten as follows:

$$V_{CE}(max) = V_{CC} + \sqrt{\frac{L}{C}}\, I_p.$$

The energy E supplied to the yoke is given by

$$E = \tfrac{1}{2} L I_p^2$$

In the design of a deflection circuit, this required energy is fixed by the picture tube being used. The sweep time and retrace time are both fixed by the application. There are, therefore, only three parameters which can be varied by the designer: I_p, V_{CC}, and L. From the energy equation, it is evident that the value chosen for L determines I_p, and vice versa. However, the value of I_p is given by

$$I_p = \frac{V_{CC}}{L}\frac{t_s}{2}$$

Therefore, for a given value of I_p it is apparent that V_{CC} also becomes fixed. At this point, the peak voltage swing across the transistor can be calculated from the following equation:

$$V_{CE}(max) = V_{CC} + I_p \frac{\pi}{t_r} L$$

When these values have been determined, the designer must choose a transistor to meet the requirements imposed by the circuit.

The breakdown voltage (BV_{CEO}, BV_{CER}, BV_{CES}, BV_{CEX}, depending upon the drive-circuit impedance between the base to emitter of the output transistor), should be greater than 1.3 $V_{EE}(max)$, as determined above. This safety factor allows for stray inductance and transients.

A sustaining voltage rating is not required because the collector current drops to zero before the voltage swings out (as shown by the waveform in Fig.13) if the transistor turn-off time is less than half the retrace time. However, if the turn-off is greater than one-half the retrace time, a sustaining voltage rating should be used. In addition, the transistor not only must be able to handle the peak collector current, but should also have usable current gain at this level ($I_c = I_p$). At the same time, the $V_{CE}(sat)$ of the transistor at I_p should be as low as possible to minimize the power dissipation. In practice, both of these requirements are guaranteed by a specification such as:

$$V_{CE}(sat)\ \ (\text{at } I_C = I_p,\ I_B = \frac{I_p}{15}) = 1.5\ \text{V max.}$$

Another important parameter of the output transistor is switching speed. For good linearity, the turn-on time of the transistor should be less than one-tenth of the total on-time of the device (approximately half the sweep time). The turn-off time, meanwhile, should be at least one-quarter of the retrace time to reduce the high-energy dissipation, which could cause reverse-biased second-breakdown problems.

Design Example

The object of this example is to illustrate the design of a magnetic deflection circuit for a specific yoke. The yoke, Celco HD 428-S560 or equivalent, is used to drive a cathode-ray tube for an alpha-numeric display with a 36-degree full-deflection angle and a 12-kilovolt acceleration potential. The yoke inductance is 250 microhenries and the energy required is 225 microjoules. The sweep time is 50 microseconds and the retrace time 10 microseconds.

From this information, the peak collector current I_p of the deflection-circuit transistor is calculated as follows:

$$I_p = \sqrt{\frac{2\,(225)\,10^{-6}}{250 \cdot 10^{-6}}} = 1.35\ \text{A}$$

The supply voltage V_{CC} required is given by

$$V_{CC} = \frac{2\,L\,I_p}{t_s} = \frac{2\,(250 \cdot 10^{-6})\,(1.35)}{50 \cdot 10^{-6}} = 13.5\ \text{V}$$

The tuning-capacitor value C is given by

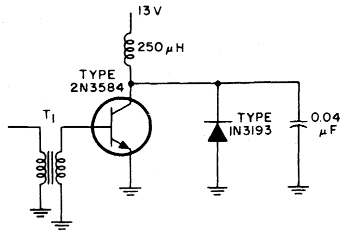
$$C = \left(\frac{t_r}{\pi}\right)^2 \left(\frac{1}{L}\right) = \frac{100 \cdot 10^{-12}}{(\pi)^2\, 250 \cdot 10^{-6}} = .040\ \mu\text{F}$$

Finally, the maximum collector voltage V_{CE} is given by

$$V_{CE} = 13.5 + (1.35)\frac{\pi}{(10) \cdot 10^{-6}} 250 \cdot 10^{-6} = 118\ \text{V}$$

The breakdown voltage, therefore, must be greater than (118) (1.3) = 155 V.

The 2N3584 meets all of the requirements for this application. The transistor switching times are short, its gain is 25 minimum at 1 ampere, and its voltage ratings are well above the required minimum. The circuit diagram and waveforms are shown in Figs.14 and 15, respectively.



T_1 = C.P. ELECTRONICS X-9370 OR EQUIV.

Fig.14 - Schematic diagram of a typical transistor magnetic deflection circuit.

Line-Operated Audio Amplifier

Fig.16 illustrates how high-voltage silicon transistors can be used to produce a compact, low-cost, high-quality audio-power amplifier. This particular circuit shows a class A, 5-watt, line-operated unit. The line voltage is rectified and filtered directly to provide the required dc supply voltage. This method reduces considerably the size, weight, and cost of the circuit by eliminating the need for a power-supply transformer. Negative feedback from the output transformer produces a linear output and good frequency response. Operation is relatively unaffected by normal line variations between 105 and 135 volts, and by temperatures up to 257° F. Amplifier performance curves are shown in Figs.17, 18, and 19. A summary of the amplifier characteristics is listed below:*

Frequency Response: -3 dB from 35 Hz to 35 kHz

Total Harmonic Distortion:
0.6% at 400 Hz and 4 W output
1.5% at 400 Hz and 5 W output

Hum and Noise: 65 dB below 4 W

Input Impedance: 300 ohms

Input Voltage: 0.6 V for power output of 4 W

The 2N3584 transistor used in the output stage satisfies three very important requirements for the successful operation of this amplifier: (1) a high value of voltage breakdown V_{CER}; (2) good gain linearity; (3) a high gain-bandwidth product.

Because the dc supply voltage conceivably can reach 140 volts, the sustaining-voltage rating V_{CER} for the output transistor, at R_{BE} = 500 ohms, must be greater than 280 volts. Circuits designed to permit the use of a transistor having a lower V_{CER} generally compromise performance and should be avoided. For example, one method of reducing this rating involves decreasing the supply voltage by increasing the size of the current-limiting resistors in the power supply. This procedure, however, not only requires the use of expensive power resistors, but also creates high dissipation losses and reduces the power output of the amplifier.

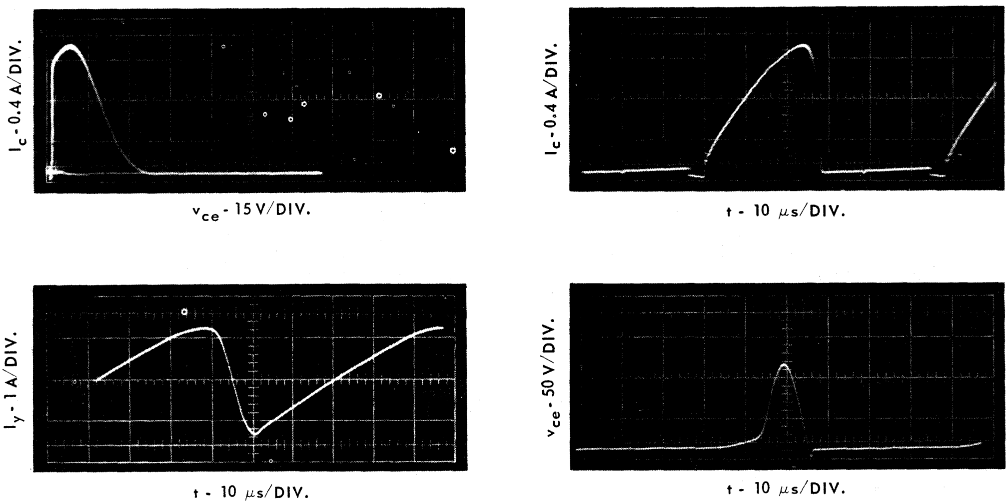


Fig.15 - Current and voltage waveforms produced by circuit shown in Fig.14.

* Additional information concerning this amplifier circuit is given in RCA publication ATC-402.

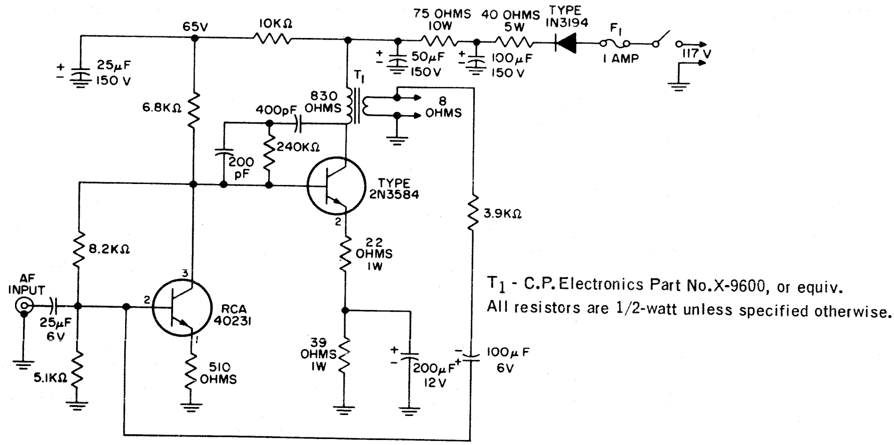


Fig.16 - Schematic diagram of a line-operated, class A, 5-watt audio amplifier.

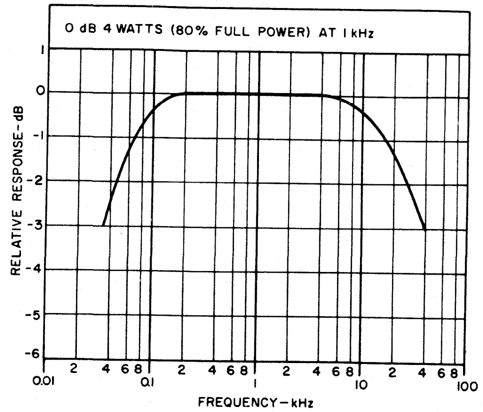


Fig.17 - Response curve for circuit shown in Fig.16.

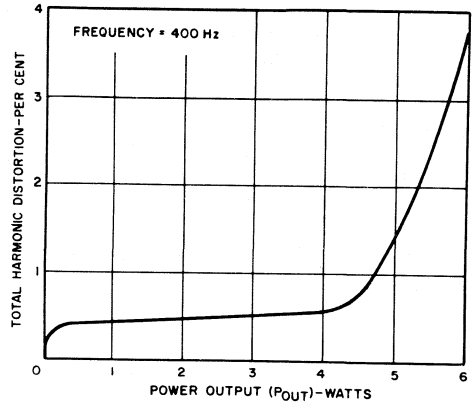


Fig.19 - Harmonic distortion as a function of power output for circuit shown in Fig.16.

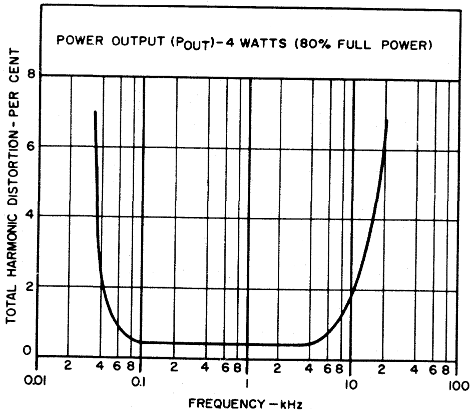


Fig.18 - Total harmonic distortion as a function of frequency for circuit shown in Fig.16.

Changing the design of the circuit may change the conditions on the required breakdown voltage. For example, if the circuit is altered so that the impedance presented to the base-emitter junction is increased to 1000 ohms and the maximum supply voltage is limited to 130 volts, the designer must choose a transistor that has a $V_{CER}(sus)$ rating (R_{BE} = 1000 ohms) of greater than 260 volts.

The excellent gain linearity of the 2N3584 (±10%) from 10 to 300 milliamperes keeps distortion at a very low level. Moreover, the high gain-bandwidth product (1 MHz) provides wide frequency response, and also permits the use of a large negative feedback without affecting circuit stability.

One final consideration is the safe operating area. Under high line voltages and worst-case temperature conditions, the dc bias point for the output transistor must be within the maximum power rating and second-breakdown rating of the device. Fig.20 illustrates this safe-operating region for the 2N3584.

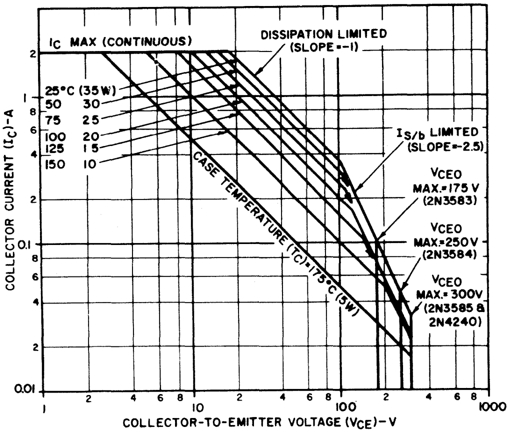


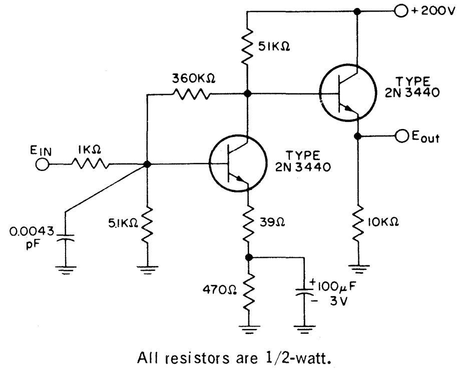
Fig.20 - Safe operating area for the 2N3584 transistor.

Operational Amplifier

Operational amplifiers are used to perform mathematical operations on voltage waveforms. Among other things, an operational amplifier can be used to multiply, add, and integrate electrical signals. It is generally used in one of these capacities in an analog computer. Wave-shaping circuits are another important application; for example, a pulse can be integrated to form a linear voltage ramp.

To function properly, an operational amplifier must have very high open-loop gain. It must also be capable of amplification over a wide passband extending from dc to perhaps 50 kHz. Its phase-shift characteristics must be such that a large negative feedback can be applied without causing oscillations. DC drift must be very low. In addition, the amplifier should have very high input impedance and low output impedance, or vice versa. Generally, the high-input-impedance type is used.

To meet all of these requirements, an operational amplifier normally utilizes a chopper amplifier and other stabilizing circuits. This portion of the amplifier can be designed to operate at low supply voltages. The final stage, however, requires a high supply voltage because it must provide a large voltage swing to drive the high input impedance of the next operational amplifier. A typical final stage that meets this requirement and also provides the necessary low output impedance is shown in Figure 21. Fig.22 shows the performance curves for this circuit.



All resistors are 1/2-watt.

Fig.21 - Schematic diagram of a typical final stage of an operational amplifier.

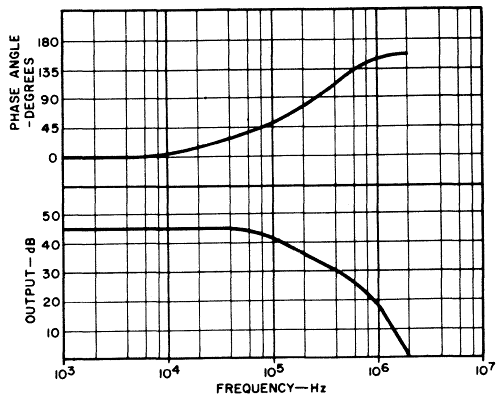


Fig.22 - Performance curves for circuit shown in Fig.21.

In general the transistor requirements for an operational amplifier output are the same as for a class A audio amplifier. These requirements were discussed in detail in the section "Line-Operated Audio Amplifier," and are summarized below:

$V_{CER}(sus) > 2\ V_{CC}$

h_{FE}: must be linear over the operating-current range.

$P_{S/b}/P_D$: the dc bias point must be within the safe operating region.

f_T: the gain-bandwidth product should be as high as possible; a rule-of-thumb minimum is 10 MHz.

Solid State
Division

Power Transistors
Application Note
AN-3565

A 100-Watt, 18-kHz Inverter Using RCA-2N5202 Silicon Power Transistors

by

D.T. DeFino

This Note describes a two-transistor, two-transformer inverter that demonstrates the excellent switching capabilities of the new RCA-2N5202 power transistor. This silicon epitaxial n-p-n device is supplied in the popular TO-66 package. Its fast switching speed makes it especially suitable for use in switching regulators, switching control amplifiers, converters, and inverters. Pertinent characteristics of the 2N5202 are shown in Table I.

Fig.1 shows a schematic diagram of the two-transistor, two-transformer circuit. A saturable base-drive transformer T_2 controls the inverter switching operation. A linearly operating output transformer T_1 transfers the output power to the load. The output transformer T_1 is not allowed to saturate; therefore, the peak collector current through the transistor is determined principally by the value of the load impedance.

Because no two transistors are perfectly matched, one of the transistors in the inverter circuit conducts more rapidly than the other when the power is turned on. This transistor, Q_2 for example, tends toward saturation and causes positive voltages to appear at the dotted ends of the transformers. Thus, there is an effective positive feedback that causes Q_1 to switch off and Q_2 to switch on. The voltage from the collector of Q_1 to the collector of Q_2 is then positive and equal to twice the collector supply voltage V_{CC}. The voltage V_{Rfb} across the feedback resistor R_{fb} is essentially the product of the resistance R_{fb} and the base current referred to the primary of T_2. The voltage across T_2 is equal to $2\ V_{CC} - V_{Rfb}$.

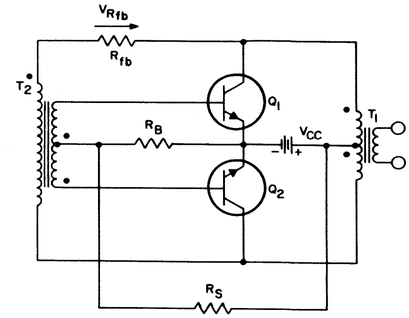


Fig.1 - Schematic diagram of two-transistor/two-transformer inverter.

At the beginning of the next half-cycle, the voltage across R_{fb} increases very slowly with the slowly increasing magnetizing current through T_2. When T_2 reaches its saturation flux density, the magnetizing current increases very rapidly and causes a rapid increase in V_{Rfb}. As a result, the voltage across T_2 decreases rapidly and Q_2 comes out of saturation. The collector voltage of Q_2 then rises, and regenerative action causes Q_1 and Q_2 to reverse states. As these processes are repeated during succeeding half-cycles, oscillations are sustained.

Characteristics of the drive transformer and the output transformer used in the circuit of Fig.1 are de-

TABLE I - TYPICAL CHARACTERISTICS OF RCA-2N5202 SILICON POWER TRANSISTOR

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	MIN	MAX	UNITS
Collector-Cutoff Current	I_{CEV}	V_{CE} = 100 V, V_{BE} = -1.5 V V_{CE} = 100 V, V_{BE} = -1.5 V, T_C = 150°C	- -	10 10	mA mA
Emitter-Cutoff Current	I_{EBO}	V_{EB} = 6 V, I_C = 0	-	10	mA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 1.2 V, I_C = 4 A	10	100	
Collector-to-Emitter Sustaining Voltage	$V_{CER}(sus)$	R_{BE} = 50 Ω, I_C = 0.2 A	75	-	V
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 1.2 V, I_C = 4 A	-	1.9	V
Collector-to-Emitter Saturation Voltage	$V_{CE}(sat)$	I_C = 4 A, I_B = 0.4 A	-	1.2	V
Small-Signal Forward-Current Transfer Ratio	h_{fe}	V_{CE} = 10 V, I_C = 0.5 A, f = 10 MHz	6	-	
Output Capacitance	C_{ob}	V_{CB} = 10 V, I_E = 0, f = 1 MHz	-	175	pF
Second-Breakdown Collector Current	$I_{S/b}$	V_{CE} = 40 V (base forward-biased)	400	-	mA
Second-Breakdown Energy	$E_{S/b}$	V_{BB} = -4 V, R_{BE} = 50 Ω, L = 50 μH	0.4	-	mJ
Saturating Switching Times:					
Delay Time	t_d	V_{CC} = 30 V, I_C = 4 A, I_{B1} = 0.4 A	-	40	ns
Rise Time	t_r	V_{CC} = 30 V, I_C = 4 A, I_{B1} = 0.4 A	-	400	ns
Storage Time	t_s	V_{CC} = 30 V, I_C = 4 A, I_{B1} = 0.4 A, I_{B2} = -0.4 A	-	800	ns
Fall Time	t_f	V_{CC} = 30 V, I_C = 4 A, I_{B1} = 0.4 A, I_{B2} = -0.4 A	-	400	ns
Thermal Resistance, Junction to Case	θ_{J-C}		-	5	°C/W

termined by means of the following equation:

$$N_p = \frac{V}{4fAB} \times 10^8$$

where N_p is the number of turns in the primary winding, V is the peak voltage across the primary winding, f is the operating frequency in hertz, A is the cross-sectional area of the core in square centimeters, and B is the flux density in gauss. In the design of the drive transformer T_2, the value of flux density B is selected to cause the core to saturate. For the output transformer T_1, the value of B is selected to assure that T_1 will not saturate. The base resistor R_B is determined by the voltage at the secondary of T_2 and the base drive required for the transistor. The resistor R_S is selected so that a voltage of 0.7 volt appears across R_B when the power is turned on initially.*

* A complete discussion of inverter design considerations and design information is given in RCA Application Note SMA-37: "High-Speed Inverters Using Silicon Power Transistors" by H.T. Breece.

Fig.2 shows the circuit diagram for a practical 100-watt, 18-kHz inverter using RCA-2N5202 transistors. Performance characteristics for this inverter are shown in Fig.3, and waveforms of output voltage, collector voltage, and collector current as functions of time are shown in Fig.4.

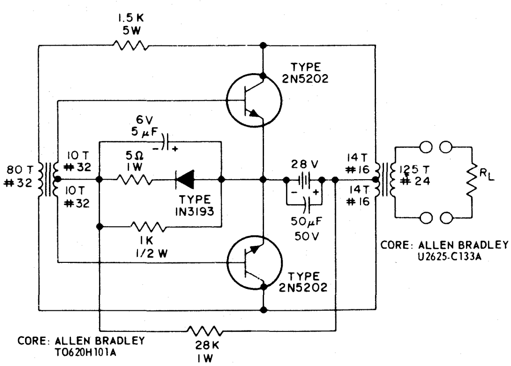


Fig.2 - Circuit diagram for 100-watt, 18-kHz inverter.

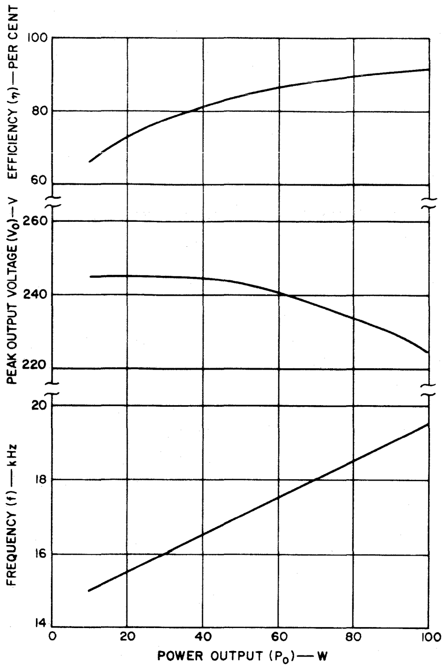


Fig.3 - Performance characteristics of inverter shown in Fig.2.

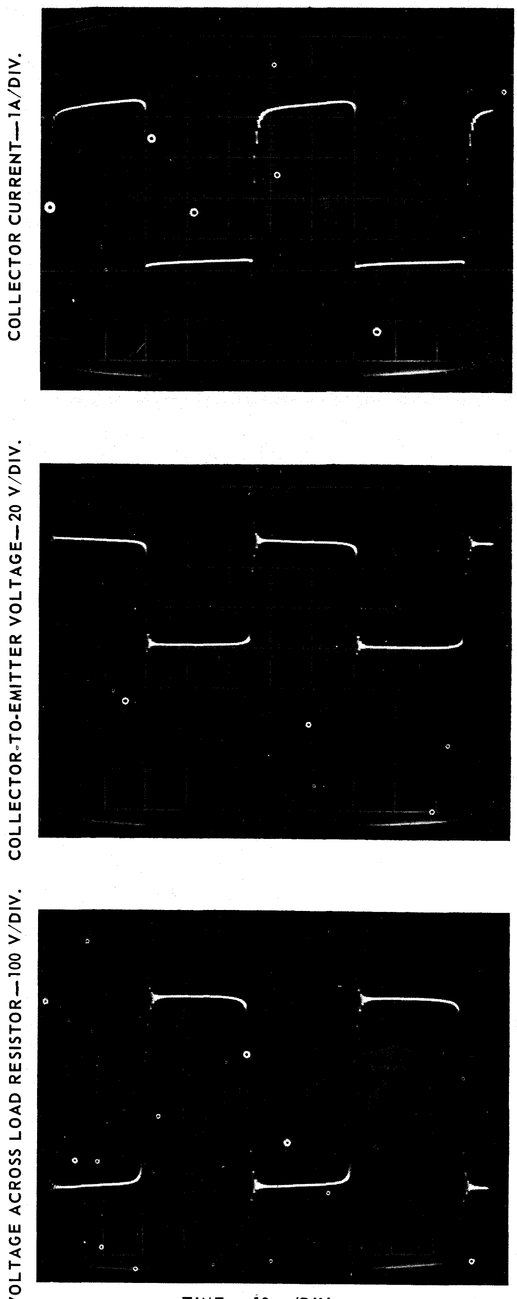


Fig.4 - Waveforms of output voltage, collector voltage, and collector current in inverter of Fig.2.

Solid-State Ballasting of Mercury-Arc Lamps

by

Peter Schiff

Recent advances in the voltage- and current-handling capabilities of power transistors have made possible the design of solid-state switching-regulator ballasts that offer significant advantages over conventional ballasting devices for high-pressure mercury-arc lighting systems. In addition to the usual transistor-circuit benefits of reduced weight and bulk, the new solid-state ballasts provide unmatched power regulation for line-voltage fluctuations and exceptional versatility. The basic solid-state ballast circuit includes a built-in lamp-dimming feature that permits a single design to be used with lamps of various power ratings over a range of 50 to 150 per cent of the power rating specified for the ballast design. Moreover, transistor ballast circuits eliminate the annoying strobe effect associated with conventional ballasting devices and thereby make the long-life, efficient mercury-arc lamps suitable for use in studios and similar critical lighting areas.

RELATIVE MERITS OF VARIOUS LIGHTING SYSTEMS

Table I compares the characteristics and provides a brief cost analysis of incandescent, fluorescent, mercury-arc, Lucalox,* and sodium-lamp lighting systems. The over-all cost of each system is determined by three main factors: (1) power consumed during operation, (2) replacement and maintenance, and (3) initial installation. The cost of initial installation is almost insignificant when compared to the other cost items. In general, power-consumption costs are approximately seven times greater than the costs of initial installation. Replacement-and-maintenance costs, at present, represent two or three times the initial-installation costs, but are rising at a very rapid rate. Because of the higher efficiency and reduced maintenance requirements of gas-discharge (arc) lamps, lighting systems that use these types of lamps have displaced those that use incandescent (tungsten-filament) lamps in most industrial and highway installations.

Fluorescent lighting systems are currently the most widely used of the various gas-discharge types. In view of the rapid rise in maintenance costs, however, the long-life (approximately 20,000 hours) mercury-arc bulbs have become increasingly attractive. The use of mercury-arc lighting systems is increasing at a rate that far exceeds that of fluorescent systems, and mercury-arc lamps are now being used in numerous applications for which fluorescent types were previously employed, as well as in many new applications in the home. In addition, greater expansion of the application of mercury-arc lamps is expected to result from new phosphors which will further develop the light characteristics of these devices.

Another important consideration in selection of a gas-discharge lighting system is whether the lamp is to be operated from an ac or a dc power source. Neither fluorescent nor Lucalox lamps are particularly well suited for dc operation. When fluorescent lamps are operated from dc voltages, the direct currents force the mercury atoms to one end of the arc tube with a resultant dimming of the other end. Moreover, the lamp efficiency for dc operation may be only 70 per cent of that for high-frequency ac operation, and the life of a dc-operated fluorescent is derated 20 per cent. The Lucalox arc tube cannot withstand the temperature differential between the electrodes that is characteristic of dc operation. This temperature differential results because the positive electrode is disproportionately heated by electron bombardment.

* Trade name of the General Electric Company

TABLE I – A COMPARISON OF THE CHARACTERISTICS OF VARIOUS LIGHTING SOURCES

Type	Description	Ingredients	Light Quality	Percent Eff.	Life (hrs)	Warmup Time	Time Before Restart	400W Bulb or Equivalent			Cents/ lumen-hr x 10^{-4}
								Bulb Cost	Indoor Fixture Cost	Ballast Cost	
Incandescent	Filament (point light source)	Tungsten in Nitrogen	Good - much red, no blue (continuous spectrum)	2.6	2,000	None	None	$ 1.25	$10.00		1.80
Fluorescent	Low-pressure vapor with phosphor correction	Mercury	Good	9.5	10,000	Few Seconds	None	$16.00	$25.00	$ 20.00	0.56
Mercury Arc (Color Corrected)	High-pressure vapor with phosphor correction (point source)	Mercury and Argon in Quartz burner	Slightly cold	7.5	20,000	4 min.	5 min.	$20.00	$30.00	$ 45.00	0.70
Lucalox	High-pressure, high-temperature vapor (point source)	Sodium and Mercury in Alumina burner	Sunny, much yellow	15.0	6,000	3.0 min.	1 min.	$45.00	$30.00	$120.00	0.54
Sodium Vapor	High-pressure vapor (point source)	Sodium, Neon	Yellow monochromatic	15.0	6,000	18 min.	None				

NOTE: In the cost analysis, the maintenance factor proportional to life of bulb was not included. The electrical power cost was assumed to cost three cents per kilowatt hour, and the life of the ballast and fixture was estimated to be 60,000 hours.

High-pressure mercury-arc lamps provide the same efficiency for either ac or dc operation. For dc operation, the mercury-arc lamp offers the advantage of no strobe effect. However, because only one arc-tube electrode is bombarded by electrons during dc operation, a slight decrease in tube life results from the overheating of this electrode. A redesign of the electrodes should alleviate this condition.

CHARACTERISTICS OF MERCURY-ARC LAMPS

Fig.1 shows the basic construction of a mercury-arc lamp. The arc tube is made of quartz to withstand the wide extremes and sharp gradients of temperature to which it is subjected. This quarts tube contains some argon in addition to the mercury which evaporated and ionized to provide the arc lighting. The argon is a starting aid and also prolongs the life of the lamp electrodes by retarding electron bombardment and evaporation of the electrodes.

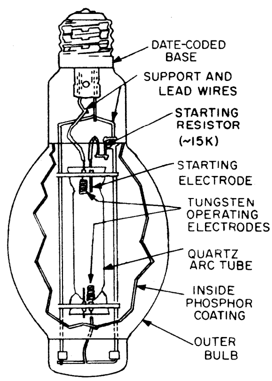


Fig.1 - Cutaway view of a mercury-arc lamp.

A mercury-arc lamp is essentially a varying impedance which is driven from the ac line through an inductive ballast. Fig.2 shows the voltage and current characteristics of the mercury-arc bulb during warmup. The argon in the arc tube ionizes when the voltage across the lamp electrodes rises to 200 volts (point 1 in Fig.2); the voltage then decreases rapidly to 18 volts (point 2 in Fig.2). The lag in current with respect to the bulb voltage, shown in Fig.2(b), results because of the ballasting inductor in series with the lamp electrodes. Warm up of the mercury-arc bulb is completed in approximately 3 minutes. During this period, the mercury vaporizes, and a stable operating point is then attained (point

3 in Fig.2). The inductive ballast is designed so that the slope of the change in voltage between points 2 and 3 results in a reduced warm-up time. If the mercury-arc bulb is turned-off, the mercury cannot be re-ionized until approximately 5 minutes have elapsed, i.e., until the pressure and temperature in the arc tube have decreased sufficiently.

CONVENTIONAL BALLASTING METHODS

For operation of the mercury-arc lamp in 120-volt line applications, a voltage step-up transformer ballast must be used to develop the high starting potential (200 volts) and the required current-voltage slopes [shown in Fig.2(b)]. This transformer ballast, however, must have a large leakage inductance to accommodate the varying

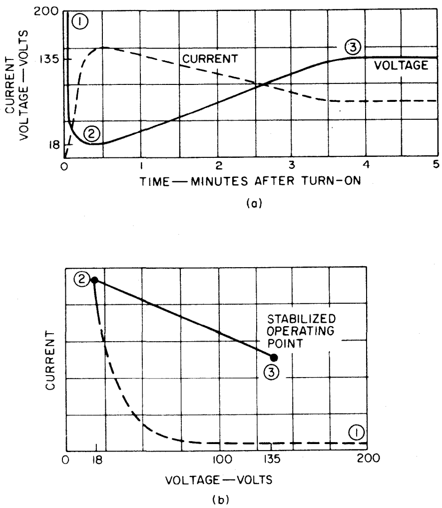


Fig.2 - Warm-up characteristics of a typical (135-volt) mercury-arc lamp: (a) current and voltage as a function time; (b) current as a function of voltage.

bulb characteristics. For operation of the mercury-arc lamp from ac voltages of 220 volts or higher, ballasting may be provided by a simple series reactor. Fig.3 shows the two ballasting arrangements. As shown in the circuit diagrams, a power-factor-correction capacitor (usually an oil type) should be used with each ballast circuit. The efficiency of these circuits ranges from 75 to 95 per cent.

A major disadvantage of conventional ballasting reactors is poor power regulation for line-voltage fluctuations. The power regulation can be improved, as shown in Fig.4(a), by use of a saturating (constant-current) type of ballasting reactor. When this type of ballasting is employed, however, circuit efficiency is reduced, and a longer bulb warm-up period is required. Voltage and current waveshapes of conventional ballasts are shown in Fig.4(b).

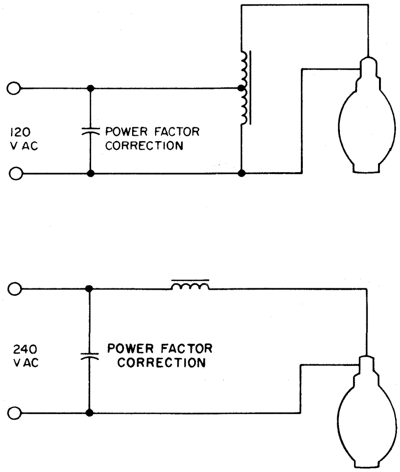


Fig.3 - Conventional ballasts for 120- and 240-volt ac mercury-arc lamps.

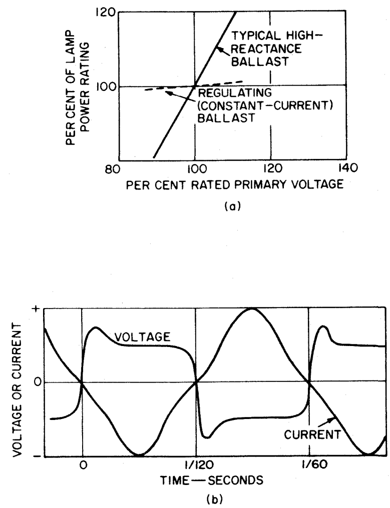


Fig.4 - Characteristics of conventional mercury-arc-lamp ballasts: (a) regulation characteristics; (b) voltage and current as a function of time.

SOLID-STATE BALLASTING CIRCUITS

The block diagram in Fig.5 shows the basic requirements of an electronic type of ballasting circuit for mercury-arc lamps. This type of ballast may be operated from either an ac or dc voltage source; the rectifier bridge, or course, is not required for dc source voltages. AC input voltages are first rectified, and the resultant dc voltage is then converted to the level required for

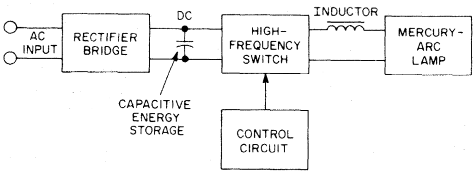


Fig.5 - Block diagram of an electronic ballasting system for mercury-arc lamps.

application to the mercury-arc lamp by some type of inverter or converter (solid-state switch and associated control circuit).

Efficient conversion of a voltage from one level to another level requires the use of an inductive component. If a size advantage is to be realized from the use of an electronic ballasting circuit, the frequency of the solid-state switch must be high enough so that the converter inductor is significantly smaller than a conventional 60-Hz ballasting reactor. A small inductor, however, cannot maintain the arc in a mercury-arc bulb as the ac source voltage swings through zero. If no other storage element were included in the electronic ballasting circuit, the arc would be extinguished; the mercury-arc lamp must then be allowed to cool sufficiently before a new arc can be produced. The electronic ballast, therefore, includes a capacitor for additional energy storage when the circuit is operated from an ac voltage source.

Fig.6 shows three prospective electronic ballasting circuits: a ringing-choke converter, a push-pull inverter, and a switching regulator. Table II summarizes the characteristics of each type. The important considerations in the selection of one circuit in preference to the other circuits are power-regulation capabilities, operating efficiency, small size, and requirements of the solid-state switching element.

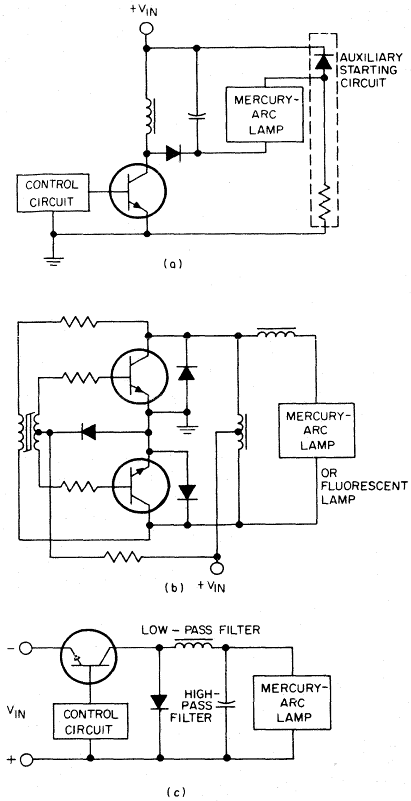


Fig.6 - Three basic circuit configurations that may be used in electronic ballasting systems: (a) ringing-choke converter; (b) push-pull inverter; (c) switching regulator.

TABLE II — CHARACTERISTICS OF VARIOUS ELECTRONIC BALLASTING CIRCUITS

CIRCUIT	V_{IN} - V_{OUT}	DC or AC OUT	REMARKS	REGULATION	APPROX. EFF.	Switching Transistor		
						No. of Devices	V_{CE}	I_C(peak)
Ringing Choke	Independent	DC	Complex Circuit (Open-load protection)	Excellent	70%	1	$V_{IN} + V_{OUT}$	~(4X) I_{OUT}
Push-Pull	Independent	AC	Three magnetic elements	Limited	80%	2	$2V_{IN}$	(4X) I_{OUT}
Switching Regulator*	$V_{IN} > V_{OUT}$	DC	Simple Circuit	Excellent	90%	1	V_{IN}	(2X) I_{OUT}

* The switching regulator offers the greatest efficiency and least stringent switching-transistor requirement.

The ringing-choke inverter offers the advantage of a dc output which is completely independent of the input voltage; its operating efficiency, however, is low in comparison to the other types of ballasting circuits. The push-pull inverter suffers from the fact that it provides an ac output with poor regulation. In addition, this circuit requires three magnetic components, which substantially add to the bulk of the ballast. The switching regulator is the most efficient and provides the best power regulation of the three types of electronic ballasting circuits. This ballasting circuit also imposes the least stringent requirements on the solid-stage power-switching element, the most critical component of any electronic ballast. These factors make the switching regulator the most economical choice for an electronic ballasting circuit. An additional advantage of this circuit is that it requires only a single magnetic component; integrated-circuit construction techniques, therefore can be readily applied to achieve the small sizes desired for ballasting elements. A disadvantage of the switching-regulator ballast is that the output voltage is always less than the input voltage.

120-Volt Switching-Regulator Ballast

For operation in 120-volt line applications, the basic switching-regulator circuit is modified, as shown in Fig.7, so that the solid-state switching element (transistor Q_1) is operated in the positive feedback mode. The rectified 120-volt ac input appears as a dc voltage across the V_{IN} terminals of the circuit. This voltage drives transistor Q_1 into saturation. The collector current of transistor Q_1 rises linearly through the primary (L_1) winding of transformer T_1 until the voltage drop across the current-sensing resistor R_2 increases above a predetermined threshold level. At this point, transistor Q_3 is turned on, and the collector current of this transistor, in turn, drives transistor Q_2 into conduction to create a virtual short between base and emitter of transistor Q_1. In this way, the drive input to transistor Q_1 is effectively removed. The inductive kick from the L_1 primary winding of transformer T_1 that results from the decrease in the collector current of transistor Q_1 is clamped by the commutating diode D_3 so that the current decays linearly through the winding. Positive feedback coupled from the secondary (L_2) winding of transformer T_1 holds switching transistor Q_1 in the "off" state until the current through the transformer primary winding decreases to zero. The cycle is then repeated. Fig.8 shows the significant current and voltage waveshapes for the circuit. It is apparent from these waveshapes that switching losses occur only during turn-off.

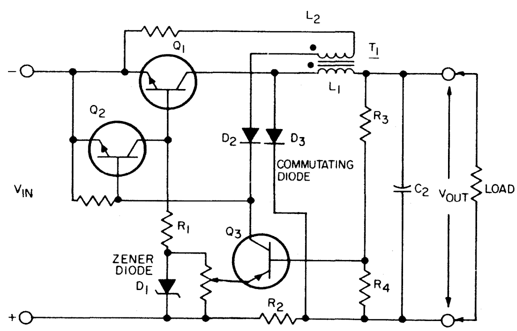


Fig.7 - 120-volt switching regulator.

The equations for the turn-on (t_{on}) and turn-off (t_{off}) times and the switching frequency (f) of the switching-regulator ballasting circuit can be derived from the following basic relationship for the voltage developed across an inductor:

$$E_L = L \frac{di}{dt} \quad (1)$$

During turn on, the voltage across the regulator inductor is essentially the algebraic difference between the input and output voltages (i.e., $E_L = V_{in} - V_{out}$). Because both of these voltages are constant, their difference results in a linearly increasing current through inductor L_1. The rate of change of the current (di/dt) is then the peak value to which the current rises divided by the turn-on period (i.e., $di/dt = I_{peak}/t_{on}$). For those conditions, Eq. (1) may be rewritten in the following form:

$$V_{in} - V_{out} = L_1 \frac{(I_{peak})}{t_{on}} \quad (2)$$

If this equation is solved for t_{on}, the following result is obtained:

$$t_{on} = \frac{L_1 (I_{peak})}{V_{in} - V_{out}} \quad (3)$$

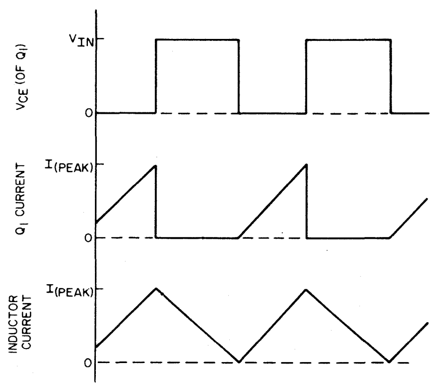


Fig.8 - Typical voltage and current waveforms for the switching regulator shown in Fig.7.

The equation for the turn-off time can be similarly derived. During this period, however, the voltage across inductor L_1 is essentially equal to the output voltage. The current decays linearly through the inductor so that the rate of change of current is constant over the turn-off period. When these conditions are imposed on Eq. (1), the following equation for the turn-off time can be derived:

$$t_{off} = \frac{L_1 (I_{peak})}{V_{out}} \qquad (4)$$

By use of Eqs. (3) and (4), the switching frequency of the switching-regulator ballast can be expressed in terms of the inductor L_1, the peak current, and the input and output voltages:

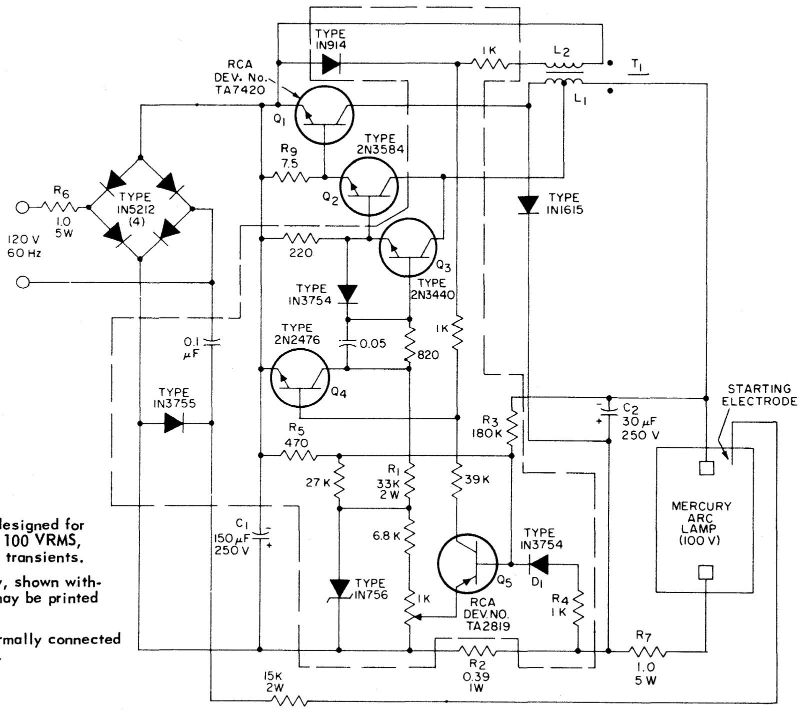
$$f = \frac{1}{t_{on} + t_{off}}$$

$$= \frac{V_{out} + (V_{in} - V_{out})}{L_1 (I_{peak}) (V_{in})} \qquad (5)$$

The peak current and associated output voltage of the switching-regulator circuit can be varied by adjustment of potentiometer R_6. For any given setting of the potentiometer, however, these quantities are constant and are independent of the input voltage. Another factor of interest, which is apparent from Eq. (5), is that a change in power level (i.e., in V_{in} or I_{peak}) results in an inverse change in switching frequency.

Fig.9 shows a practical 100-watt switching-regulator ballasting circuit designed for 120-volt line applications in which the output voltage and current are both sampled to reduce bulb warm-up time. This circuit has a voltage-current characteristic very similar to that shown in Fig.2(b) for a conventional ballasting reactor.

The 120-volt ac input is rectified by a full-wave bridge rectifier. The dc output from the rectifier, is developed across filter capacitor C_1. Because the input drive to the emitter-base circuit of the switching transistor is applied through a resistance network, the relatively high supply voltage can lead to serious I^2R loss-



NOTES: 1. This circuit is designed for operation above 100 VRMS, with 250 V peak transients.

2. Control circuitry, shown within dotted line, may be printed circuit.

3. Diode D_1 is thermally connected to transistor Q_5.

Mercury arc lamp = 90-to-100-volt type with separate starting electrodes

L_1 = 120 turns of No.22 wire tapped 1 turn from collector

L_2 = 18 turns of No.34 wire

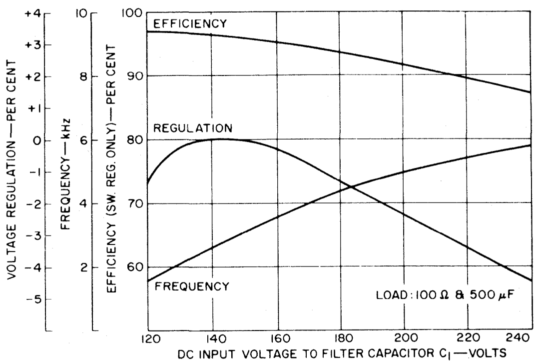
T_1 = Arnold AH 361 (or equiv.) with 0.036" gap (6.7:1 turns ratio)

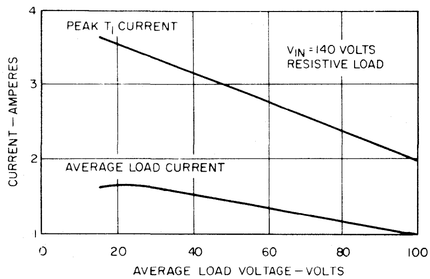
Fig.9 - 100-watt, 120-volt ac switching-regulator ballasting circuit.

es unless the drive current is maintained at a very small value. This condition is made possible by use of two transistors Q_2 and Q_3 in a Darlington configuration to provide the current gain necessary to increase the low value of drive current to the level required to saturate the switching transistor.

Because the switching regulator is a "down converter," has limited filtering, and operates from relatively low line voltages, a special low-voltage (100-volt rather than the more common 135-volt) mercury-arc lamp is used with the 100-watt, 120-volt ballasting circuit. The low-voltage arc tube contains slightly less mercury than the higher-voltage type. High starting potentials are obtained by use of a half-wave voltage doubler, wired to a separate starting electrode (with a current-limiting resistor).

Performance data of the 100-watt switching regulator are shown in Fig. 10. These data are shown as a function of the dc input voltage to filter capacitor C_1. The overall efficiency of the circuit, including the rectifier bridge and filter capacitor, is 87 per cent for a 120-volt ac input. The output is adjustable from 15 to 150 watts for operation of the circuit into a 100-ohm load impedance. The excellent regulation characteristics are achieved in part, by the action of resistor R_5, which offsets a rise in output voltage with a corresponding rise in input voltage. Fig. 11 shows a photograph of the 100-watt, 120-volt switching-regulator ballasting circuit, together with a mercury-arc lamp.





(b)

Fig.10 - Performance characteristics of the 100-watt, 100-volt switching-regulator ballasting circuit: (a) voltage regulation, frequency response, and efficiency; (b) output characteristics.

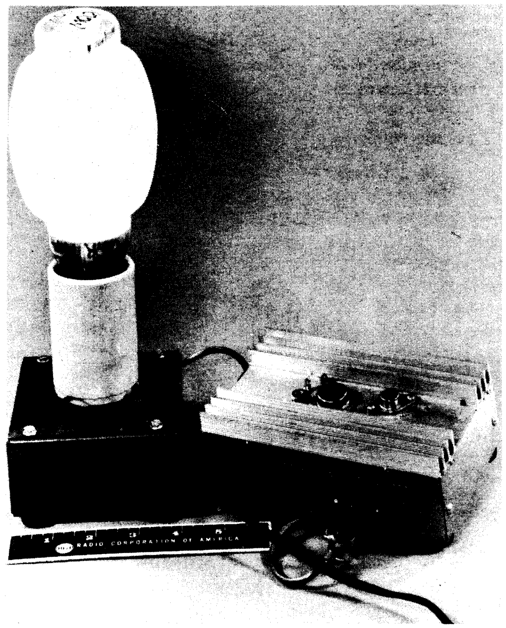


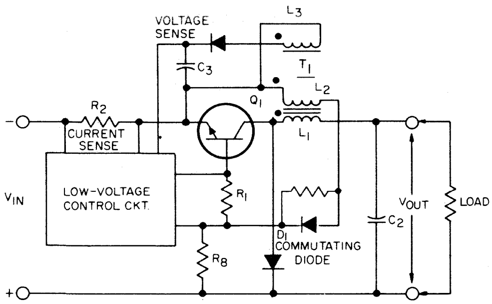
Fig.11 - Photograph of the 100-watt, 120-volt switching-regulator ballasting circuit.

The 120-volt ballast circuit has a relatively small conduction angle, because of a necessarily large filter capacitor (C_1). The associated surge currents make the use of bulbs in excess of 200 watts impractical. The ballast has two 1-ohm surge-current-limiting resistors, R_7 and R_{10}. Resistor R_{10} limits ac line transients; the resistor R_7 limits bulb current during ionization.

200-to-300-Volt Switching-Regulator Ballasts

For industrial and highway lighting installations, 240-volt single-phase, 277-volt single-phase, and 208-volt three-phase ac power sources are readily available. For these voltages, a sufficient differential between the arc-tube voltage and input voltage exists to permit the transistor switching element to be driven from a secondary winding on the inductor of a low-pass filter. Relatively high drive currents can then be obtained without high power losses.

Fig.12 shows the basic configuration for a switching regulator designed to operate from ac source voltages between 200 and 300 volts. Eqs. (1) through (5) and the waveshapes shown in Fig.8, given for the 120-volt switching-regulator ballasts, are also applicable to higher-voltage ballasts of the type shown in Fig.12. A unique feature of the higher-voltage circuits is that only the high-current switching transistor Q_1 is required to have a breakdown-voltage capability sufficient to withstand the full value of the dc input voltage including transients applied across the V_{IN} terminals. All the transistors in the control circuit are low-voltage, low-dissipation types. The design for the higher-voltage ballast also features built-in short-circuit protection.

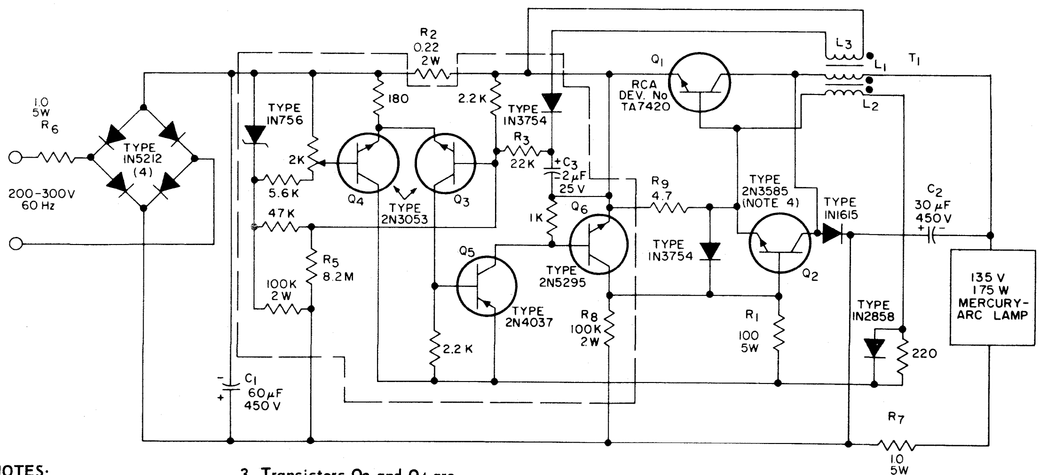


NOTE: This circuit needs only one high-voltage switching element.

Fig.12 - 200-to-300-volt ac switching regulator.

In the switching-regulator circuit shown in Fig.12, the dc voltage applied in the V_{IN} terminals drives a switching transistor (Q_1) that is slightly forward-biased by a small current (approximately 3 milliamperes) through a base-circuit resistor (R_8). Transistor Q_1 is immediately driven into saturation by the positive feedback from its collector circuit supplied by the L_2 secondary winding of transformer T_1. The L_2 secondary winding also supplies the drive power to the control circuit. The collector current of switching transistor Q_1 rises linearly through the L_1 primary winding of transformer T_1 until the voltage across the current-sensing resistor R_2 triggers the control circuit in shunt with the base-emitter junction of transistor Q_1. The transistor is then held cut off by the feedback voltage from the L_2 secondary winding of the transformer until the current through L_1 primary winding decays to zero. The inductive kickback that results from the decrease in current through L_1 is clamped by the commutating diode D_1 and, therefore, is the same as the output voltage on C_2. The L_3 winding of transformer T_1 then charges capacitor C_3 to a voltage proportional to the output voltage. During the next cycle, the control circuit samples a combination of the voltage across capacitor C_3 and the current through resistor R_2. In this way, an output characteristic similar to that of a conventional ballast, shown in Fig.2(b), is obtained.

The schematic diagrams and performance data for two practical ballasting circuits, designed for use with 175-watt and 400-watt memory-arc bulbs, that use the approach illustrated by the basic circuit configuration shown in Fig.12 are shown in Figs.13 and 14 and Figs.15



NOTES:
1. Maximum transient voltage = 450 V.
2. Control circuit shown within dotted line may be printed circuit.
3. Transistors Q_3 and Q_4 are thermally connected.
4. Transistor Q_2 is selected for a $V_{CER(sus)}$ at 200 ohms greater than 500 volts.

T_1 = 2 x Arnold AH-108 (or equiv.) with 0.054" air gap 17:1.7:1 turns ratio

L_1 = 120 turns of No.22 wire

L_2 = 12 turns of No.32 wire

L_3 = 7 turns of No.32 wire

Fig.13 - 175-watt, 200-to-300-volt switching-regulator ballasting circuit.

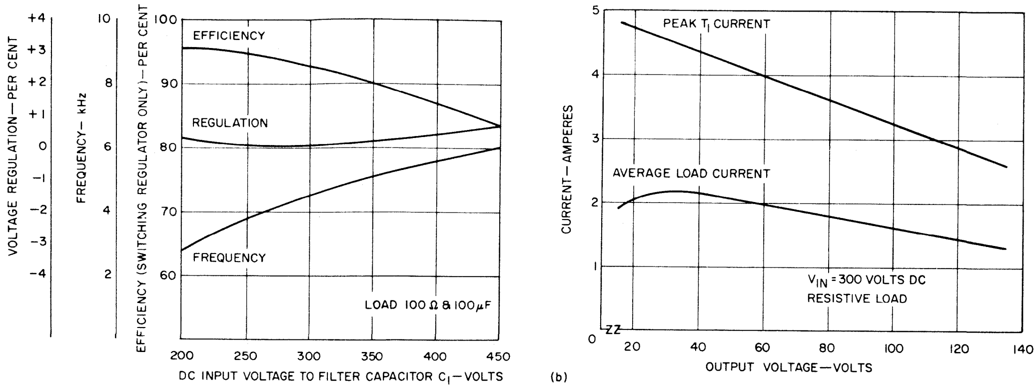
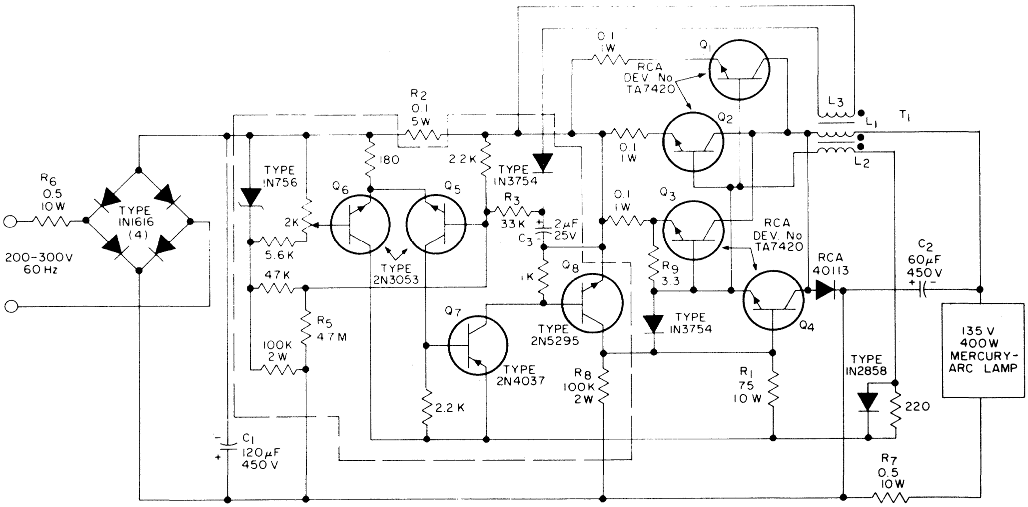


Fig.14 - Performance characteristics of the 175-watt, 200-to-300-volt ballasting circuit: (a) voltage regulation, frequency response, and efficiency; (b) output characteristics.



Notes:
1. Maximum transient voltage = 450 V.
2. Control circuit shown within dotted line may be printed circuit.
3. Transistors Q_1 through Q_4 are selected to have a $V_{CER(sus)}$ at 20 ohms greater than 500 volts.
4. Transistors Q_5 and Q_6 are thermally connected.

T_1 = Arnold AH-223 (or equiv.) with 0.125 inch air gap, 17:1.7:1 turns ratio
L_1 = 98T turns of No.18 wire
L_2 = 10T turns of No.32 wire
L_3 = 6T turns of No.32 wire

Fig.15 - 400 watt, 200-to-300 volt switching-regulator ballasting circuit.

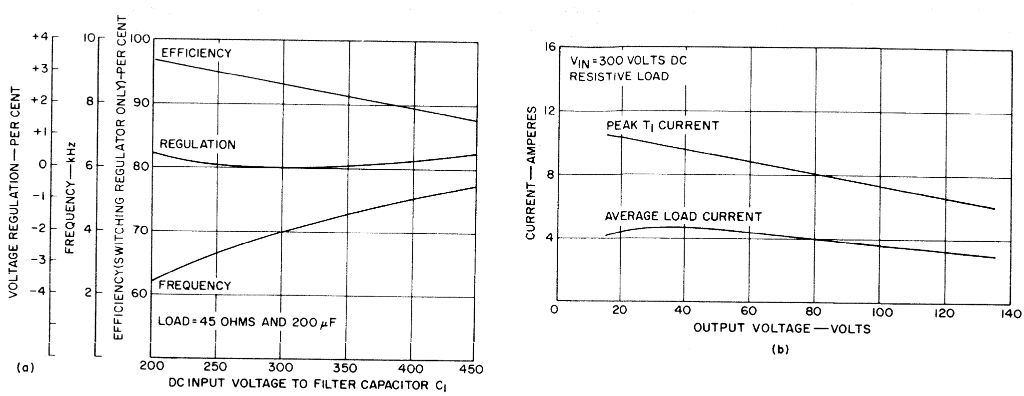


Fig.16 - Performance characteristics of the 400-watt, 200-to-300-volt switching-regulator ballasting circuit: (a) voltage regulation, frequency response, and efficiency; (b) output characteristics.

and 16, respectively. Performance data are shown as a function of the dc input voltage to filter capacitor C_1. Excellent regulation is obtained for dc input voltages from 200 to 450 volts. Fig.17 shows a photograph of the two ballasting circuits.

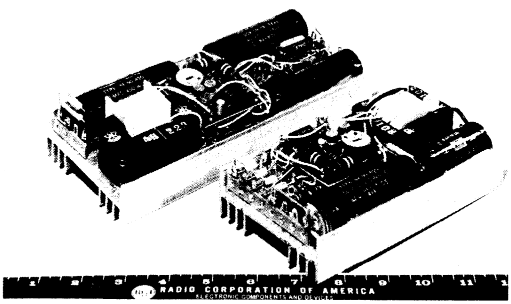


Fig.17 - Photograph of 175-watt and 400-watt 240-volt switching-regulator ballasts for mercury-arc lamps.

DESIGN PROCEDURE

The design of solid-state switching-regulator ballasts for mercury-arc lamps involves three critical operations: (1) selection of the mercury-arc lamp and the peak starting current, (2) selection of the reactor element, and (3) selection of the switching transistor and other circuit components.

Mercury-Arc Lamp and Peak Starting Current

The type of mercury-arc lamp used and the peak starting current that must be supplied to this lamp by the ballast circuit are dictated by the value of the ac source voltage, the amount of lamp power (P_L) required, and the warm-up time of the lamp. For operation from a 120-volt ac line at lamp power levels up to 200 watts, the special low-voltage (90-to-100-volt) type of mercury-arc lamp should be used. The peak starting current is then determined from the following relationship:

$$I_{peak} = 4 \left(\frac{P_L}{100V}\right) \qquad (6)$$

For operation from ac source voltages in the range of 200 to 300 volts, the more conventional 135-volt type of mercury-arc lamp is used. The peak starting current, for a specified bulb power rating P_L, is then determined as follows:

$$I_{peak} = 4 \left(\frac{P_L}{135V}\right) \qquad (7)$$

Switching-Regulator Reactor Element

The series inductor selected for the switching-regulator ballasting circuit should have a maximum core cross-sectional area and minimum air gap, consistent with the required inductance value, so that the minimum physical size is obtained. The circuit shown in Fig.18 permits simple di/dt measurements that eliminate the

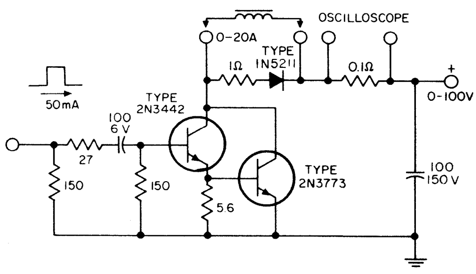


Fig.18 - Inductor tester.

need for repetitive calculations in determination of the required inductances. In this test circuit, the inductor is connected in series with a switching transistor and a dc voltage. The switching transistor is maintained in the "on" state until the inductor saturates. The following equation then becomes the basis for the determination of the inductor parameters:

$$V_{in} = L_1 \left(\frac{Isat}{t_{on}} \right) \quad (8)$$

The desired flux density for the inductor is some fraction of that producted by the saturation current. The air gap, number of turns, and the core are selected as required to obtain the desired value. The turns ratio from the series inductor winding (primary) to the secondary windings is as indicated in the circuit schematics (Fig.9, 13, or 15) of the type of switching-regulator ballast being designed.

If an iron core is used for the inductor, the core laminations should be 4 mils thick (only a negligible increase in efficiency results from the use of thinner laminations). For stabilized operation and to avoid overheating of the inductor, the switching frequency of the ballasting circuit should be less than 5 kHz and the flux density in the inductor should be less than 6 kilogauss. For an inductor that uses a ferrite core, the flux density (determined for worst-case conditions) is usually 3 kilogauss, and the frequency is limited by only the transistor switching losses.

Switching Transistor and Other Circuit Components

A switching transistor used as the switching element in a switching-regulator ballast must have a collector-to-emitter voltage-breakdown capability $V_{CER(sus)}$ high enough so that the device can withstand the total input dc voltage together with the maximum transient input voltage that may be developed in the circuit. In all the ballasting circuits described in this paper, the transistor used as the high-current switching element is the RCA Dev. No. TA7420. The specifications of the TA7420 are given in Table III.

The Darlington transistor circuit in shunt with the emitter-base junction must drive the switching transistor well into the saturation region for the particular I_{peak}.

1. For the 120-volt ballast-circuit design,

   I_B (max) < 10 mA

2. For the 200-to-300-volt ballast-circuit design,

   I_B (max) < 300 mA

Approximately 20 per cent of the base drive to the switching transistor is diverted by resistor R_9 (in Figs.9, 13, and 15) to achieve rapid turn-off of the transistor.

The power dissipated by the transistor selected for use as the switching element should not exceed 10 per cent of the power rating (P_L) of the mercury-arc bulb. The transistor power dissipation (P_D) is calculated for

TABLE III – SPECIFICATIONS FOR THE RCA DEV. NO. TA7420 TRANSISTOR

Parameter	TEST CONDITIONS AT 25°C ± 3°C						Unit	Limit	
	I_C	R_{BE}	V_{BE}	V_{CE}	I_B	L		Min.	Max.
	A	OHMS	V	V	A	μH			
$V_{CER(sus)}$	0.2	50					V	375	
$V_{CEO(sus)}$	0.2						V	300	
I_B	0.5			5.0			A	0.005	
$V_{CE(sat)}$	3.0				0.375		V		1.0
θ_{J-C}							°C/W		1.75
$I_{S/b}$ (1 second)				40			A	2.5	
$E_{S/b}$		20	-4			500	A	4.0	
$t_{f(1)}$	3.0			200	0.375		μS		0.5

NOTES: 1. $I_{B1} = I_{B2} = 0.375$ A; ($h_{FE} = 8$)

2. The RCA Dev. No. TA7420 is an epitaxial-overlay switching transistor in a JEDEC TO-3 case.

a hot, stabilized bulb ($I_{Cmax} = I_{STAB} = 2\, I_{avg}$) as follows:

P_D = saturation loss + turn-off loss

$$= \frac{t_{on}}{t_{on} + t_{off}} \int_0^{I_{STAB}} i\, R_{(sat)}\, di + \frac{f_{(STAB)} V_{IN}\, t_f}{2}$$

$$\left(\frac{I_{STAB}\, f}{2}\right) \left[t_{on} \left(I_{STAB}\right) \left(R_{sat}\right) + V_{IN}\, t_f \right] \qquad (8)$$

In Eq.8, $R_{(sat)}$ is the saturation resistance of the switching transistor, and t_f is its turn-off time for the particular circuit conditions. [It should be noted that the turn-off time is not directly related to the gain-bandwidth product (f_T).]

The total base drive resistance of the switching-regulator ballasting circuits can be estimated on the basis of the current and voltage relationships for peak-current conditions.

1. For the 120-volt design, the voltage drop across the total of the resistors in the base drive circuit is the dc input voltage less the voltage (8.2 volts) across the 1N756 Zener diode. The maximum value for the drive-circuit resistance I_{peak}, therefore, can be calculated by use of following equation:

$$R_{IN} = \frac{V_{IN\,(min)} - 8.2\ V}{I_{B(max)}} = \frac{100}{I_{B(max)}} \qquad (9)$$

   Eq.(9) indicates that the drive-circuit resistance for the 120-volt ballast design must be greater than 9000 ohms for a permissible $I_{B(max)}$ of 10 milliamperes.

2. For the 200-to-300-volt design, the total drive-circuit resistance is estimated as follows:

$$R_{in} = \frac{V_{in(min.)} - V_{out(min.)}\ \frac{L_2}{L_1} - 2\ V}{I_{B(max.)}} \qquad (10)$$

   In this case, the drive-circuit resistance must be greater than 60 ohms for the 300 milliamperes of maximum permissible drive in the circuits presented.

The values of capacitors C_1 and C_2 and of resistors R_2, R_7, and R_{10} are determined on the basis of the type of circuit being designed and the power rating of the mercury-arc lamp with which this circuit is to be used. When the lamp power rating (P_L) differs from that shown in the circuit diagrams of Figs.12 and 14, the values of C_1, C_2, $1/R_2$, $1/R_7$, and $1/R_{10}$ should be increased or decreased in direct proportion to the change in the lamp power rating, i.e.,

$$\frac{C_1}{C_1'} = \frac{C_2}{C_2'} = \frac{R_2'}{R_2} = \frac{R_7'}{R_7} = \frac{R_{10}'}{R_{10}} = \frac{P_L}{P_L} \qquad (11)$$

where the prime (') indicates the new circuit values.

The bridge-rectifier diodes and the commutation diode are selected on the basis of the maximum voltage and current requirements of the ballasting circuit.

The value of resistor R_3 is determined from the desired voltage-current slope of the ballast circuit.

$$VI_{(slope)} = - \frac{I_{bulb\ (hot)}}{V_{bulb\ (hot)}} \qquad (12)$$

An increase in the warm-up time for a given bulb and ballasting circuit arrangement can be achieved by the use of a larger resistor R_3 in both the 120-volt and 200-to-300-volt designs. This larger resistor would result in a smaller voltage-current slope, as shown in Fig.19, and the collector current during starting (I_{PEAK}) would then be reduced.

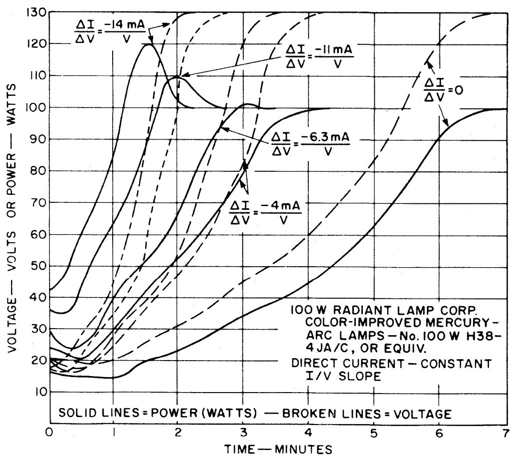


Fig.19 - Typical warm-up characteristics for a 100-watt mercury-arc lamp.

The value of R_5 is selected to provide the best voltage regulation.

ADVANTAGES OF SOLID-STATE MERCURY-ARC-LAMP BALLASTING

The circuit configuration and design procedure for the solid-state ballasts present several noted advantages over conventional ballasts.

1. Because no strobe effect is associated with the solid-state ballasts, it is possible to use long-life, efficient mercury-arc lamps in studios and

in similar critical lighting areas. In such applications, the low lighting cost and the advantage of more light with less heat are decisive factors in favor of mercury-arc lamps.

2. Solid-state ballasts provide unmatched power regulation for line voltage fluctuations.
3. The new ballasts offer the physical advantages of reduced weight and bulk in comparison to conventional ballasts. For example, the weight of a 400-watt conventional ballast is approximately 13 pounds, while the weight of an equivalent solid-state ballast is only 2.4 pounds. It is anticipated that the weight and bulk of solid-state ballasts will be further reduced by the use of hybrid circuit techniques and ultrasonic operating frequencies.
4. A solid-state photocell control is required to switch only milliwatts of power to actuate a solid-state ballast, rather than the kilowatts that would be required for a conventional ballast.
5. The circuits permit adjustment of 70 to 150 per cent of rated bulb wattage. Outside this range, the negative-impedance characteristics of the bulb cause the arc to be extinguished. However, one basic ballast circuit may be used for bulbs of various power ratings.
6. The solid-state ballast supplies dc power to the bulb so that there are no RFI radiation problems.

In a comparison of solid-state and conventional ballasts, the initial cost factor must be considered. In regard to the initial cost, the simple magnetic ballast has a decided advantage. In general, however, initial cost is only 10 per cent of the total costs of the lighting system, and this advantage is clearly outweighed when a less efficient lighting means is displaced.

From the standpoint of reliability, proper design should result in solid-state ballasts that match the performance of conventional ballasts.

In the ballast circuit described in this paper, only transistors were used. Thyristors (SCR's and triacs) are also suited for use in ballasting circuits for arc-discharge lighting systems, particularly at high power levels.

Significant future growth in mercury-arc lighting for both home and office should favor the transistor ballast at voltage and power levels below 120 volts and 100 watts.

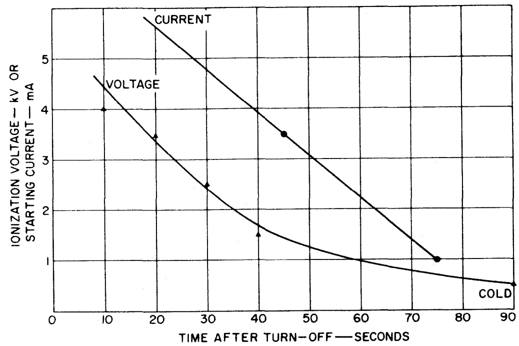


Fig.20 - Hot restart characteristics for a 100-watt mercury-arc lamp.

ADDITIONAL DEVELOPMENTS

A major disadvantage of mercury-arc lamps is the cooling-off period (approximately 5 minutes) required before a lamp previously in use can be restarted. Fig.20 shows the measured hot restart characteristics of a 100-watt mercury-arc lamp. These curves were obtained by use of only the main electrodes of the quartz burner. This technique effectively halved the cooling time. Work is currently underway to solve the problem through the development of new circuits that permit instant hot restarts of mercury-arc lamps.

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Solid State Division

Power Transistors and Thyristors

Application Note
AN-4124

Handling and Mounting of RCA Molded-Plastic Transistors and Thyristors

by W.J. Hepp, J.S. Vara, and J. Gaylord

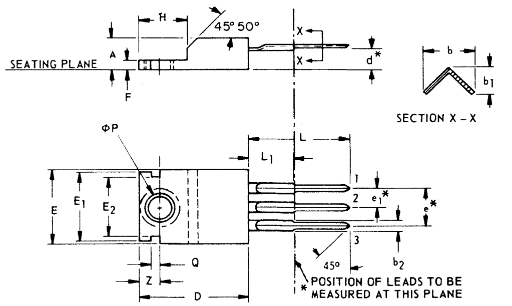
RCA power transistors and thyristors (SCR's and triacs) in molded-silicone-plastic packages are available in a wide range of power-dissipation ratings and a variety of package configurations. This Note provides detailed guidelines for handling and mounting of these plastic-package devices, and shows different types of packages and suggested mounting hardware to accommodate various mounting arrangements. Recommendations are made for handling of the packages during the forming of leads to meet specific mounting requirements. Various mounting arrangements, thermal considerations, and cleaning methods are described. This information is intended to augment the data on electrical characteristics, safe operating area, and performance capabilities in the technical bulletin for each type of plastic-package transistor or thyristor. (Data on mechanical and environmental capabilities of RCA plastic-package transistors are also available in a periodically updated **Reliability Report**, RCA Publication No. HBT-600.)

TYPES OF PACKAGES

Two basic types of molded-plastic packages are used for RCA solid-state power devices. These types include the RCA Versawatt packages for medium-power applications and the RCA high-power plastic packages, both of which are specifically designed for ease of use in many applications. Each basic type offers several different package options, and the user can select the configuration best suited to his particular application.

Figs. 1 through 3 show the options currently available for devices in RCA Versawatt packages. The JEDEC Type TO-220AB in-line-lead version, shown in Fig. 1, represents the basic style. This configuration features leads that can be formed to meet a variety of specific mounting requirements. Fig. 2 shows a package configuration that allows a Versawatt package to be mounted on a printed-circuit board with a 0.100-inch grid and a minimum lead spacing of 0.200 inch. Fig. 3 shows a JEDEC Type TO-220AA version of the Versawatt package. The dimensions of this type of transistor package are such that it can replace the JEDEC TO-66 transistor package in a commercial socket or printed-circuit board without retooling. The pin-connection arrangement of thyristors supplied in TO-220AA packages, however, differs from that of thyristors supplied in conventional TO-66 packages so that some hardware changes are required to effect a replacement. The TO-220AA Versawatt package is also supplied with an integral heat sink. Fig. 4 shows the dimensional outline for this heat sink. The use of the integral heat sink reduces the junction-to-air thermal resistance of the package from 70°C per watt to 35°C per watt.

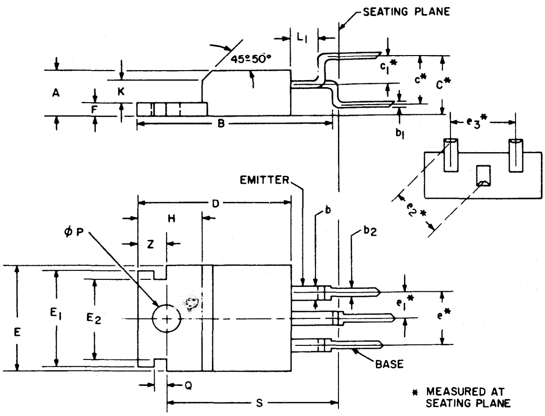
The RCA molded-plastic high-power packages are also supplied in several configurations for flexibility of application. The JEDEC Type TO-219AB, shown in Fig. 5, is the basic high-power plastic package. Fig. 6 shows a JEDEC Type TO-219AA version of the high-power plastic package.



SYMBOL	INCHES	
	MIN.	MAX.
A	.140	.190
b	.020	.038
b_1	.012	.045
b_2	.045	.070
D	.560	.625
d	.080	.115
E	.330	.420
E_1	.365	.385
E_2	.300	.320

SYMBOL	INCHES	
	MIN.	MAX.
e	.190	.210
e_1	.090	.110
F	.045	.055
H	.230	.270
L	.500	.562
L_1		.250
ΦP	.139	.147
Q	.040	.060
Z	.100	.120

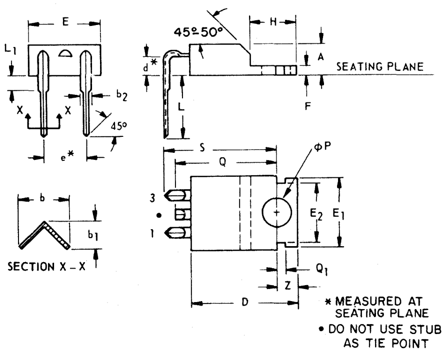
Fig. 1 - Dimensional outline of the JEDEC TO-220AB in-line-lead Versawatt transistor package.



SYMBOL	INCHES	
	MIN.	MAX
A	.140	.190
B		.850
b	.045	.070
b_1	.015	.030
b_2	.020	.038
C	.230	.270
c	.180	.220
c_1	.130	.170
D	.560	.625
E	.330	.410
E_1	.365	.385
E_2	.300	.320

SYMBOL	INCHES	
	MIN.	MAX
e	.190	.210
e_1	.090	.110
e_2	.203	.243
e_3	.190	.200
F	.045	.070
H	.230	.270
K	.080	.085
L_1	.070	.090
ΦP	.139	.147
Q	.040	.060
S	.655	.685
Z	.100	.120

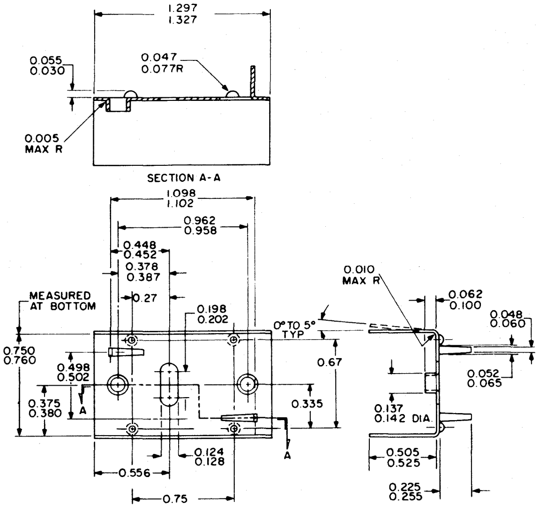
Fig. 2 - Dimensional outline of Versawatt transistor package designed for mounting on printed-circuit boards.



SYMBOL	INCHES	
	MIN.	MAX.
A	.140	.190
b	.020	.038
b_1	.012	.045
b_2	.045	.070
D	.560	.625
d	.080	.115
E	.330	.420
E_1	.365	.385
E_2	.300	.320
e	.190	.210

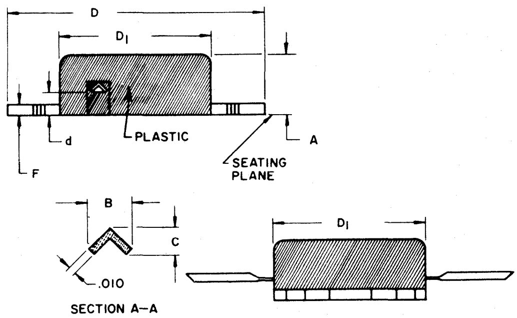
SYMBOL	INCHES	
	MIN.	MAX.
F	.045	.055
H	.230	.270
L	.360	.422
L_1		.050
φP	.139	.147
Q		.610
Q_1	.040	.060
S	.580	.610
Z	.100	.120

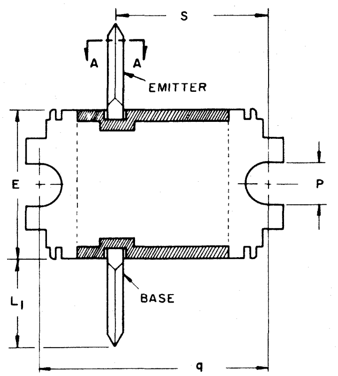
Fig. 3 - JEDEC TO-220AA Versawatt transistor package designed for direct replacement of the JEDEC TO-66 package.



ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SHOWN. TOLERANCES ARE: ±0.02 FOR 2ND PLACE; ±0.005 FOR 3RD PLACE AND ±1/2° FOR ANGULAR DIMENSION.

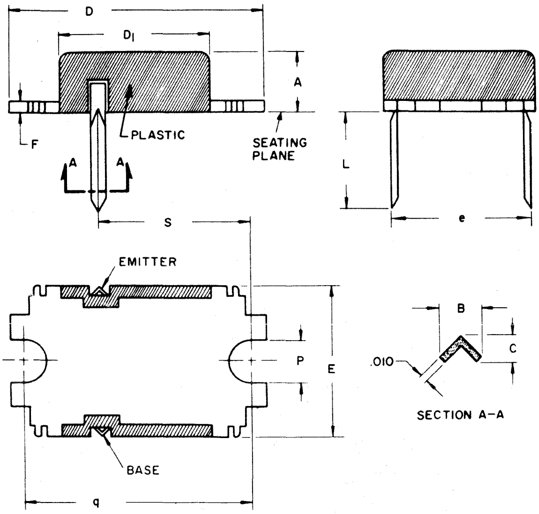
Fig. 4 - Integral heat sink used with the TO-220AA Versawatt package shown in Fig. 3.





SYMBOL	INCHES	
	MIN.	MAX.
A	.160	.200
B	.045	.060
C	.025	.045
D	.890	.910
D_1	.480	.515
d	.100	.120
E	.480	.520
F	.055	.070
L_1	.415	.560
p	.128	.150
q	.740	.760
S	.500	.520

Fig. 5 - JEDEC TO-219AB high-power molded-plastic transistor package.

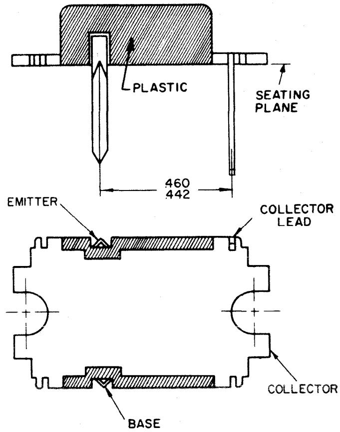


SYMBOL	INCHES	
	MIN.	MAX.
A	.160	.200
B	.045	.060
C	.025	.045
D	.890	.910
D1	.480	.515
E	.480	.520

SYMBOL	INCHES	
	MIN.	MAX
e	.460	.505
F	.055	.070
L	.370	.450
P	.128	.150
q	.740	.760
S	.500	.520

Fig. 6 - JEDEC TO-219AA plastic package designed for use as a direct replacement for the hermetically sealed JEDEC TO-3 transistor package.

The RCA high-power plastic package is also available with an attached header-case lead, as shown in Fig. 7. This three-lead package is designed for mounting on a printed-circuit board.



ALL DIMENSIONS IN INCHES

Fig. 7 - TO-219AA plastic transistor package designed for mounting on printed-circuit boards.

use of a properly designed fixture for this operation eliminates the need for repeated lead bending. When the use of a special bending fixture is not practical, a pair of long-nosed pliers may be used. The pliers should hold the lead firmly between the bending point and the case, but should not touch the case. Fig. 8 illustrates the use of long-nosed pliers for lead bending. Fig. 8(a) shows techniques that should be avoided; Fig. 8(b) shows the correct method.

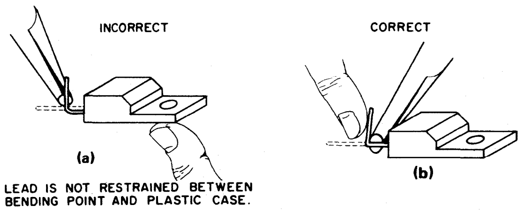


Fig. 8 - Use of long-nosed pliers for lead bending: (a) incorrect method; (b) correct method.

LEAD-FORMING TECHNIQUES

RCA Versawatt plastic packages are both rugged and versatile within the confines of commonly accepted standards for such devices. Although these versatile packages lend themselves to numerous arrangements, provision of a wide variety of lead configurations to conform to the specific requirements of many different mounting arrangements is highly impractical. However, the leads of the Versawatt in-line package can be formed to a custom shape, provided that they are not indiscriminately twisted or bent. Although these leads can be formed, they are not flexible in the general sense, nor are they sufficiently rigid for unrestrained wire wrapping.

Before an attempt is made to form the leads of an in-line package to meet the requirements of a specific application, the desired lead configuration should be determined, and a lead-bending fixture should be designed and constructed. The

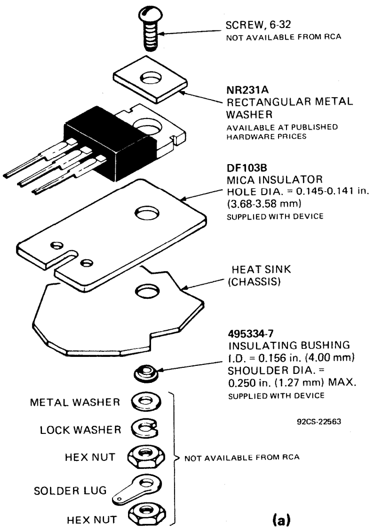
When the leads of an in-line plastic package are to be formed, whether by use of long-nosed pliers or a special bending fixture, the following precautions must be observed to avoid internal damage to the device:

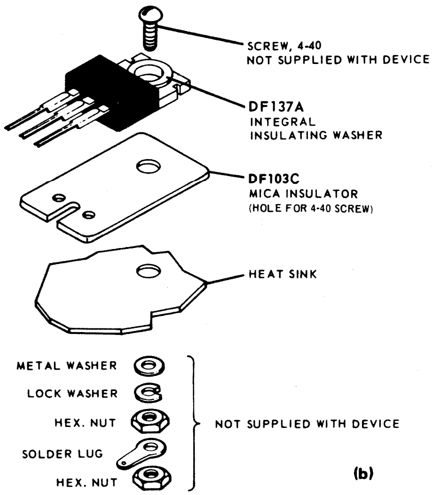
1. Restrain the lead between the bending point and the plastic case to prevent relative movement between the lead and the case.
2. When the bend is made in the plane of the lead (spreading), bend only the narrow part of the lead.
3. When the bend is made in the plane perpendicular to that of the leads, make the bend at least 1/8 inch from the plastic case.
4. Do not use a lead-bend radius of less than 1/16 inch.
5. Avoid repeated bending of leads.

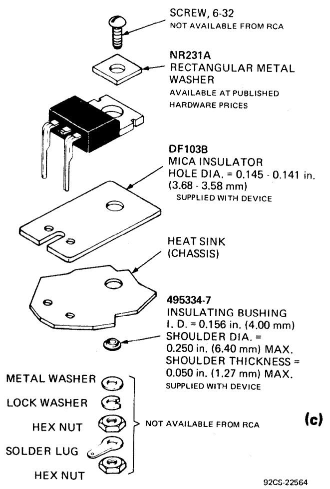
The leads of the TO-220AB Versawatt in-line package are not designed to withstand. excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement tends to impose axial stress on the leads, some method of strain relief should be devised. Fig. 2 illustrates an acceptable lead-forming method that provides this relief.

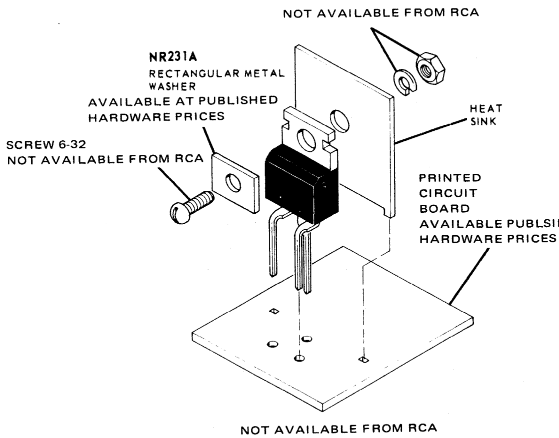
Wire wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. Soldering to the leads is also allowed; the maximum soldering temperature, however, must not exceed 275°C and must be applied for not more than 5 seconds at a distance greater than 1/8 inch from the plastic case. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions.

The leads of the RCA molded-plastic high-power packages are not designed to be reshaped. Simple bending of the leads, however, is permitted to change them from a standard vertical to a standard horizontal configuration, or conversely. Bending of the leads in this manner is restricted to three 90-degree bends; repeated bendings, therefore, should be avoided.









In the United Kingdom, Europe, Middle East, and Africa, mounting-hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 9 - Mounting arrangements for Versawatt transistors: (a) and (b) methods of mounting in-line-lead types; (c) chassis mounting; (d) mounting on printed-circuit boards.

MOUNTING

Fig. 9 shows recommended mounting arrangements and suggested hardware for the Versawatt transistors. The rectangular washer (NR231A) shown in Fig. 9(a) is designed to minimize distortion of the mounting flange when the transistor is fastened to a heat sink. Excessive distortion of the flange could cause damage to the transistor. The washer is particularly important when the size of the mounting hole exceeds 0.140 inch (6-32 clearance). Larger holes are needed to accommodate insulating bushings; however, the holes should not be larger than necessary to provide hardware clearance and, in any case, should not exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is specified. Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. An excellent method of avoiding this problem is to use a spacer or combination spacer-isolating bushing which raises the screw head or nut above the top surface of the plastic body, as shown in Fig. 10. The material used for such a spacer or spacer-isolating bushing should, of course, be carefully selected to avoid "cold flow" and consequent reduction in mounting force. Suggested materials for these bushings are diallphthalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate. Unfilled nylon should be avoided.

Modification of the flange can also result in flange distortion and should not be attempted. The transistor should not be soldered to the heat sink by use of lead-tin solder because the heat required with this type of solder will cause the junction temperature of the transistor to become excessive.

The TO-220AA plastic transistor can be mounted in commercially available TO-66 sockets, such as UID Electronics Corp. Socket No. PTS-4 or equivalent. For testing purposes, the TO-220AB in-line package can be mounted in a Jetron Socket No. CD74-104 or equivalent. Regardless of the mounting method, the following precautions should be taken:

1. Use appropriate hardware.
2. Always fasten the transistor to the heat sink before the leads are soldered to fixed terminals.
3. Never allow the mounting tool to come in contact with the plastic case.
4. Never exceed a torque of 8 inch-pounds.
5. Avoid oversize mounting holes.
6. Provide strain relief if there is any probability that axial stress will be applied to the leads.
7. Use insulating bushings to prevent hot-creep problems. Such bushings should be made of diallphthalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate.

Fig. 11 shows the recommended hardware and mounting arrangements for RCA high-power molded-plastic transistors. These types can be mounted directly in a socket similar to that shown in Fig. 11(b). The precautions listed for the Versawatt packages should also be followed in the mounting of the high-power molded-plastic packages.

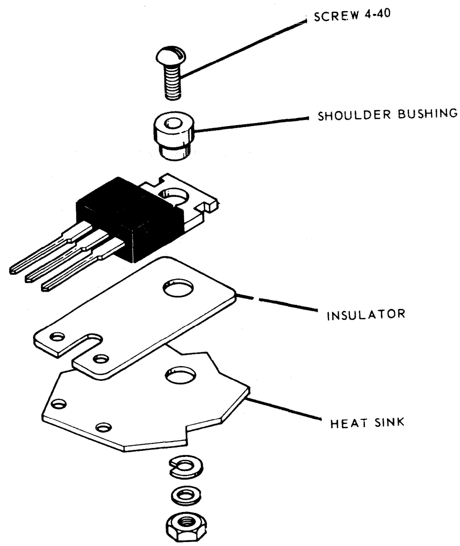


Fig. 10 - Mounting arrangements in which an isolating bushing is used to raise the head of the mounting screw above the plastic body of the Versawatt transistor.

THERMAL-RESISTANCE CONSIDERATIONS

The maximum allowable power dissipation in a solid-state device is limited by its junction temperature. An important factor to assure that the junction temperature remains below the specified maximum value is the ability of the associated thermal circuit to conduct heat away from the device.

When a solid-state device is operated in free air, without a heat sink, the steady-state thermal circuit is defined by the junction-to-free-air thermal resistance given in the published data on the device. Thermal considerations require that there be a free flow of air around the device and that the power dissipation be maintained below that which would cause the junction temperature to rise above the maximum rating. When the device is mounted on a heat sink, however, care must be taken to assure that all portions of the thermal circuit are considered.

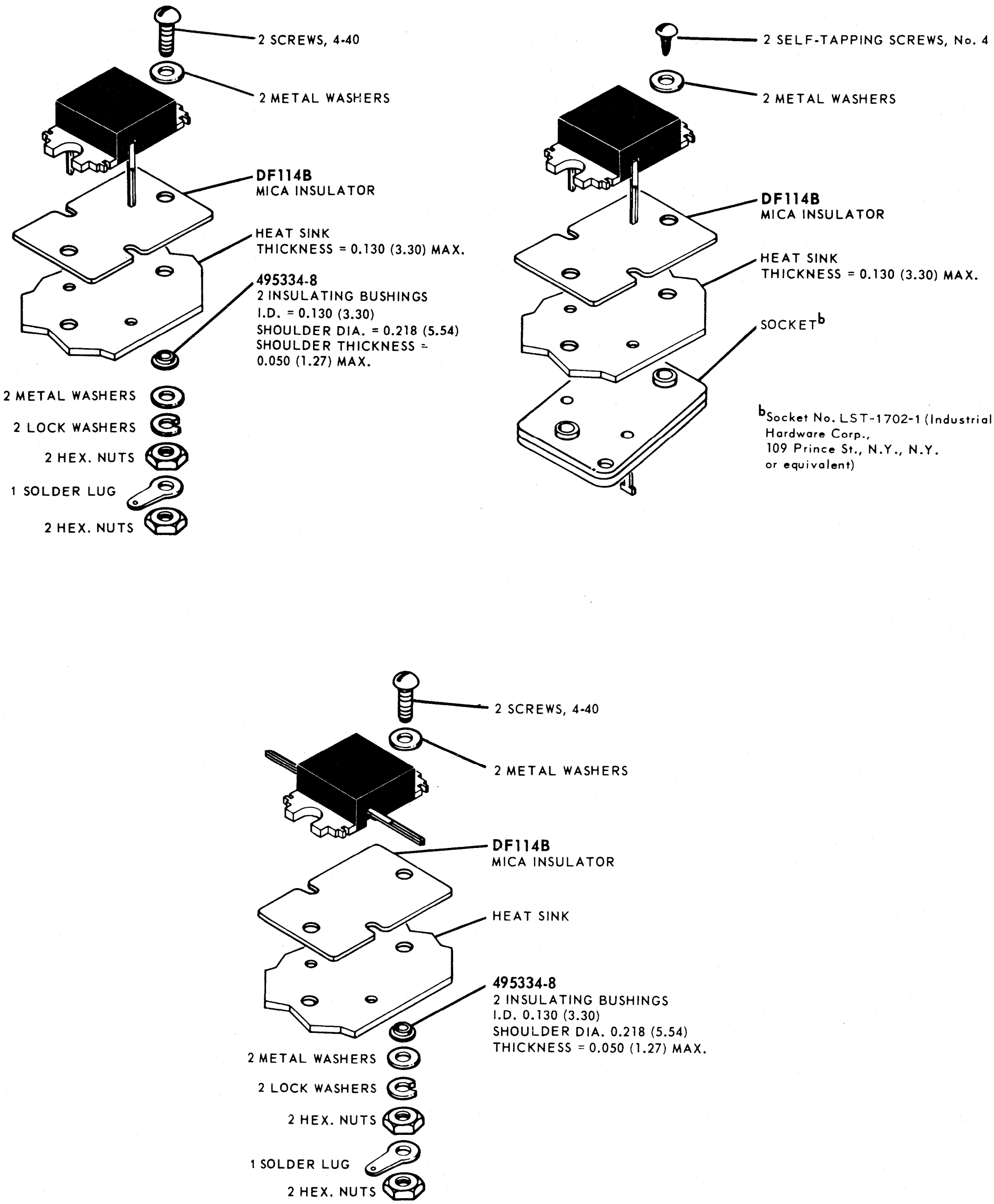


Fig. 11 - Mounting arrangements for high-power plastic-package transistors: (a) chassis mounting; (b) socket mounting; (c) printed-circuit-board mounting.

Fig. 12 shows the thermal circuit for a heat-sink-mounted transistor. This figure shows that the junction-to-ambient thermal circuit includes three series thermal-resistance components, i.e., junction-to-case, $\theta_{J\text{-}C}$; case-to-heat-sink, $\theta_{C\text{-}S}$; and heat-sink-to-ambient, $\theta_{S\text{-}A}$. The junction-to-case thermal resistance of the various transistor types is given in the individual technical bulletins on specific types. The heat-sink-to-ambient thermal resistance can be determined from the technical data provided by the heat-sink manufacturer, or from published heat-sink nomographs. The case-to-heat-sink thermal resistance depends on several factors, which include the condition of the heat-sink surface, the type of material and thickness of the insulator, the type of thermal compound, the mounting torque, and the diameter of the mounting hole in the heat-sink.

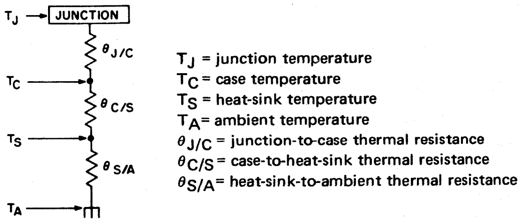


Fig. 12 - Thermal equivalent circuit for a transistor mounted on a heat sink.

Fig. 13 shows a set of curves of typical case-to-heat-sink thermal resistance of the Versawatt transistor as a function of mounting torque for several mounting arrangements. Curves A through D show typical case-to-heat-sink thermal resistance for the mounting arrangements shown in Figs. 9(a) through 9(d). Curves E and F are representative of a Versawatt transistor mounted over a heat-sink mounting hole that has a diameter of 0.140 inch (No. 6 screw clearance). Curve E shows the wide variation in thermal resistance with torque when the transistor is mounted dry. Curve F shows the effect on contact thermal resistance of a thin layer of Dow Corning No. 340 silicone grease applied between transistor and heat sink. For torques within the recommended range of 4 to 8 inch-pounds, contact thermal resistance is reduced to between 18 and 25 per cent of the dry values.

The curves shown in Fig. 14 represent typical case-to-heat-sink thermal resistance of the high-power molded-plastic transistor package as a function of mounting torque. The thermal resistances shown by curves A and C are representative of the mounting arrangements shown in Fig. 11(a) through 11 (c). Curves B and D are typical for mounting without mica over heat-sink mounting holes that have a diameter of 0.113 inch (No. 4 screw clearance). The effect of a thin layer of silicone grease on contact thermal resistance is illustrated by a comparison of curves B and D.

Operation of the transistor with heat-sink temperatures of 100°C or greater results in some shrinkage of the insulating bushing normally used to mount power transistors. The degradation of contact thermal resistance (refer to Figs. 13 and 14) is usually less than 25 per cent if a good thermal compound is used. (A more detailed discussion of thermal resistance, including nomographs, can be found in the **RCA Solid State Power Circuits**, Technical Series SP-52.)

During the mounting of RCA molded-plastic solid-state power devices, the following special precautions should be taken to assure efficient heat transfer from case to heat sink:

1. Mounting torque should be between 4 and 8 inch-pounds.
2. The mounting holes should be kept as small as possible.
3. Holes should be drilled or punched clean with no burrs or ridges, and chamfered to a maximum radius of 0.010 inch.
4. The mounting surface should be flat within 0.002 inch/inch.
5. Thermal grease (Dow Corning 340 or equivalent) should always be used (on both sides of the insulating washer if one is employed).
6. Thin insulating washers should be used (thickness of factory-supplied mica washers ranges from 2 to 4 mils).
7. A lock washer or torque washer should be used, together with materials that have sufficient creep strength to prevent degradation of heat-sink efficiency during life.

A wide variety of solvents is available for degreasing and flux removal. The usual practice is to submerge components in a solvent bath for a specified time. From a reliability standpoint, however, it is extremely important that the solvent, together with other chemicals in the solder-cleaning system (such as flux and solder covers), not adversely affect the life of the component. This consideration applies to all non-hermetic and molded-plastic components.

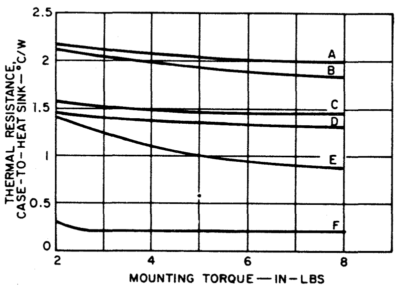
It is, of course, impractical to evaluate the effect on long-term transistor life of all cleaning solvents, which are marketed under a variety of brand names with numerous additives. These solvents can, however, be classified with respect to their component parts, as either acceptable or unacceptable. Chlorinated solvents tend to dissolve the outer package and, therefore, make operation in a humid atmosphere unreliable. Gasoline and other hydrocarbons cause the inner encapsulant to swell and damage the transistor. Alcohol and unchlorinated freons are acceptable solvents. Examples of such solvents are:

1. Freon TE
2. Freon TE-35
3. Freon TP-35 (Freon PC)
4. Alcohol (isopropanol, methanol, and special denatured alcohols, such as SDA1, SDA30, SDA34, and SDA44)

Care must also be used in the selection of fluxes in the soldering of leads. Rosin or activated rosin fluxes are recommended, while organic or acid fluxes are not. Examples of acceptable fluxes are:

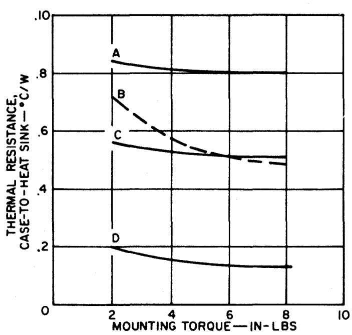
1. Alpha Reliaros No. 320-33
2. Alpha Reliaros No. 346
3. Alpha Reliaros No. 711
4. Alpha Reliafoam No. 807
5. Alpha Reliafoam No. 809
6. Alpha Reliafoam No. 811-13
7. Alpha Reliafoam No. 815-35
8. Kester No. 44

If the completed assembly is to be encapsulated, the effect on the molded-plastic transistor must be studied from both a chemical and a physical standpoint.



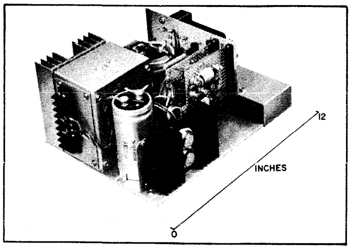
CURVE	MOUNTING ARRANGEMENT FIGURE	HEAT SINK HOLE DIA. (IN.)	MICA THICKNESS (MILS)	THERMAL COMPOUND
A	9(a)	.250	4	Dow Corning No.340
B	9(b)	.113	4	Dow Corning No.340
C	9(a)	.250	2	Dow Corning No.340
D	9(b)	.113	2	Dow Corning No.340
E	—	.140	None	None
F	—	.140	None	Dow Corning No.340

Fig. 13 - Typical case-to-heat-sink thermal resistance as a function of mounting torque for an RCA Versawatt transistor.



CURVE	MOUNTING ARRANGEMENT FIGURE	MICA THICKNESS (MILS)	THERMAL COMPOUND
A	11(a) thru 11(c)	4	Dow Corning No.340
B	—	None	None
C	11(a) thru 11(c)	2	Dow Corning No.340
D	—	None	Dow Corning No.340

Fig. 14 - Typical case-to-heat thermal resistance as a function of mounting torque for an RCA high-power plastic-package transistor.



Compact 5-Volt Power Supplies Using High-Voltage Power Transistors

By R.S.Myers

This Note discusses the use of low-cost, industrial-type, high-voltage power transistors and fast-recovery rectifiers to achieve size and weight reductions and efficiency improvements in 5-volt dc power supplies with output currents of 50 amperes or more. The power supplies described, like those used in high-reliability aerospace applications, use switching rather than dissipating regulators to eliminate the need for a 60-Hz power transformer and heat sinks for the transistors. As a result, these supplies achieve three important advantages over conventional power supplies:

- Size – Volume is reduced by a factor of four. This size reduction does not cause any cooling problems, because these supplies dissipate very little power (approximately 0.33 W/in.^{3}).
- Efficiency – Power dissipation in the regulator is virtually eliminated; only the power rectifiers require cooling. The reduction of heat dissipation in a 250-watt supply can be 200 to 300 watts, which represents a substantial economic saving.
- Weight – Weight is reduced by a factor of five. Portability is improved, mounting is simplified, and chassis cost is decreased.

A complete switching-regulator power supply that uses high-voltage transistors is described in detail. This unit produces 250 watts at 5 volts with an efficiency of 70 per cent. The performance of this supply is compared with that of a conventional supply in Table I. The design can be modified for more or less power, multiple outputs, or higher output voltages.

THE POWER-SUPPLY CONCEPT

In a switching-regulator type of power supply, the output voltage is regulated by a technique referred to as "pulse-width modulation", in which pulses of variable duty cycle are averaged with an inductor-capacitor filter. Regulation is accomplished by the variation of the duty cycle. The pulses constitute a two-state signal (power on and power off) that is supplied to the filter, as shown in Fig. 1. However, to permit use of a smaller isolation transformer, the "power-on" state is operated in a push-pull mode that is then rectified by full-wave power rectifiers. The time ratios of the push, pull, and off conditions are controlled by a modulator circuit.

Table I – Comparison of Power Supplies

	CONVENTIONAL SUPPLY	NEW SUPPLY	
Output Current at 5 volts	25	50	A
Power Losses (Max)	300	100	W
Size	1600	470	in.^{3}
Weight	50	10	lb.
Recovery Time	50	500	μs
Regulation (Half load to full load)	>0.25	0.5	%
Line Regulation	>0.25	0.5	%

The on-state voltage is unregulated and is always greater than the required output voltage from the filter. It is supplied by a low-impedance source that consists of a transformer with closely coupled windings, the main supply, and a saturated transistor. The on-state voltage is decreased to the specified output value by an inductor that forms part of the filter. Thus the filter, which converts the ac signals to a dc output, is a "choke-input" type.

The switching-regulator supply operates at a frequency above the audio range to permit use of a small isolation transformer, and also to prevent sound generation.

POWER-SUPPLY ELEMENTS

The design of a switching-regulator power supply involves the six major elements shown in Figs. 1 and 2: (1)

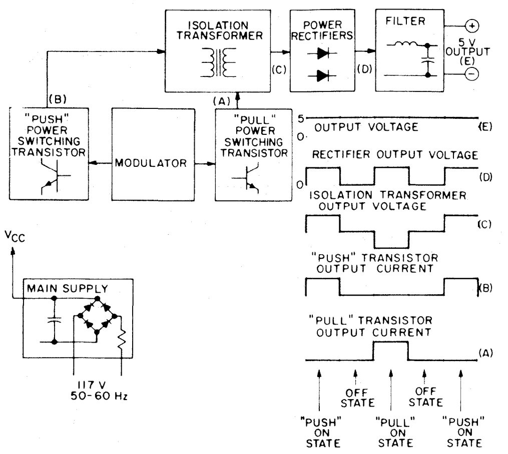


Fig. 1 - Block diagram of switching-regulator power supply, showing voltage waveforms at various points.

the main power supply, (2) the power-switching transistors, (3) the isolation transformer, (4) the modulator circuits, (5) the power rectifiers, and (6) the filter. The important parameters of these elements are discussed below.

Main Power Supply. The main supply provides the power that ultimately becomes the output power. It rectifies and filters the line voltage without use of a 60-Hz transformer. The design of such a supply is well covered in available literature[1-3]. In the case of a switching-regulator type of power supply, the main supply may be designed for high ripple without increased regulator losses (such as would occur in a conventional series regulator). Therefore, smaller capacitors and lower-cost rectifiers can be used. Some resistance must be added in series with the power line to prevent damage to the rectifiers during turn-on.[1, 2] The voltage delivered by the main power supply varies with line-voltage and load variations. The peak output voltage of the main supply at the maximum line conditions (with transients) determines both the collector-voltage rating required for the power-switching transistors and the turns ratio of the isolation transformer. Table II shows the relationship between line voltage and transistor collector voltage rating.

Power-Switching Transistors. The power-switching transistors are the most important components in the switching-regulator power supply. In the past, the high cost of these devices limited their use to aerospace applications; however, recent developments have made them economically competitive with other devices. The performance capabilities of the power supply are determined by the switching transistors, because they are the parts least able to withstand overloads such as those caused by load faults or misuse. Therefore, the switching transistors must have the following characteristics (listed in order of importance):

- High forward-bias second-breakdown capability. The transistors must carry high currents at high voltage, as shown in the switching load line of Fig. 3.[2]
- Ability to withstand the collector voltages specified in Table II in the cut-off condition. A leakage current (I_{CEV}) specification guarantees this capability.
- Short rise and fall times (t_r and t_f), for low power dissipation in the transistors and thus high efficiency of the power supply.
- Reasonably low V_{CE}(sat), for low dissipation and economical transistor heat sinks.
- Stable leakage current (I_{CEV}). The magnitude of the leakage is not important (even 20 milliamperes at 500 volts contributes less than 5 watts to the average dissipation per transistor), but it should be stable.

Table III lists the recommended specifications for the switching transistors.

Isolation Transformer. The isolation transformer is a ferrite-core transformer that operates at 20 kHz. Its design formulas are the same as those for conventional 60-Hz transformers, but the results are significantly different. The number of turns is never greater than 200, and may be as low as one. These turns always fit in the large "windows" in the ferrite core. Leakage inductance is reduced in the primary turns by sectioning the primary winding.[4] Leakage in the secondary is less important because the secondary is loaded by a filter choke. The copper losses can easily be made negligible, and the copper wire costs are small. The size of the transformer core is determined by the need to dissipate the heat generated in the core material; the Indiana General Co. recommends that dissipation be kept below 0.25 W/in.[2,5,6] The 20-kHz ferrite core is much smaller than a 60-Hz core (3 in.^{3} vs. 140 in.^{3}), and is much lighter (1 lb. vs. 33 lbs.).

The design of a 20-kHz power transformer involves three basic problems: core material selection, windings to keep peak flux below saturation, and compensation for unbalanced direct currents.

If a core has too much loss, it will overheat. If it has too many turns, the flux density will be below saturation, but the copper losses will be greater than necessary. The number of turns is kept low to avoid unnecessary copper loses, but must be great enough to keep the peak flux in the core below saturation.

The core will saturate if its cross section is too small, if there are not enough turns in the primary winding, or if the primary direct current is unbalanced. Core saturation causes the power-switching transistors to draw excessive currents

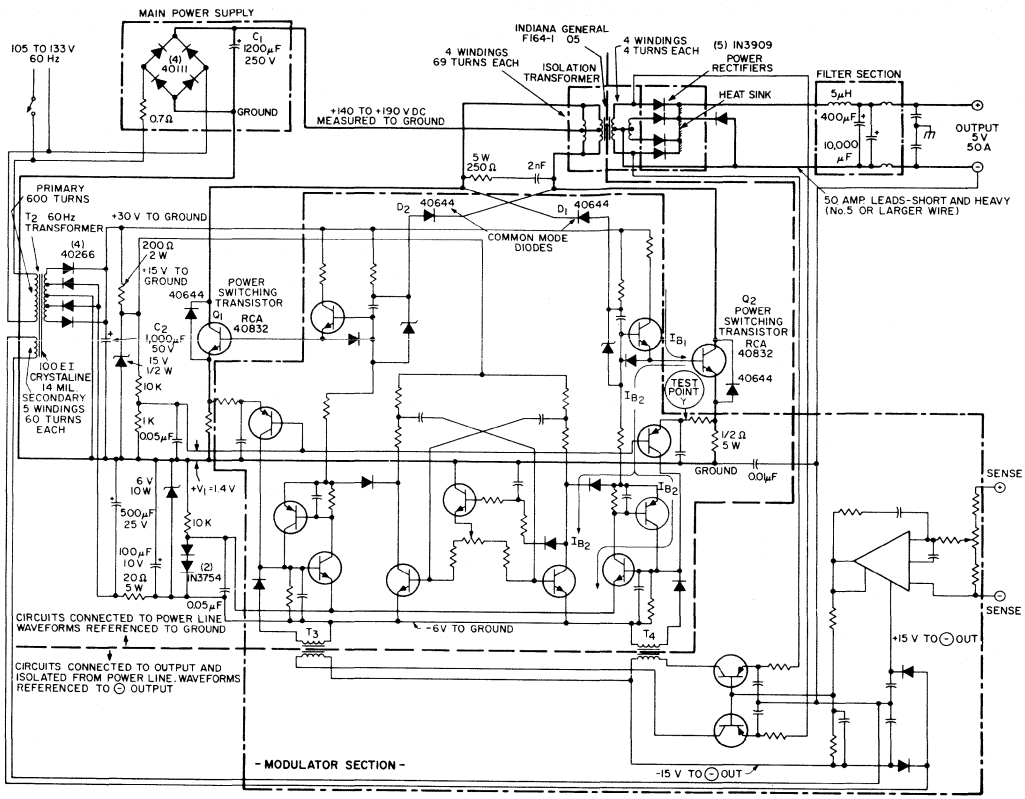


Fig. 2 - Circuit diagram of switching-regulator power supply, with major elements indicated.

that can increase collector dissipation to destructive levels. To prevent these high currents, the power supply includes a monitor circuit that cuts off the base drive to the switching transistors when emitter current reaches the maximum safe value.

Fig. 4 shows the emitter-current waveform of a power-switching transistor, monitored at point Y in Fig. 2, for different numbers of primary turns. If the emitter current is excessive, the circuit reduces the duty cycle to protect the power-switching transistor. Fig. 5 shows the waveforms for unbalanced dc drive. These unbalanced currents result from unequal duty cycles, caused by oscillator unbalance or by unbalance or faults in the modulator. Because such unbalances occur in normal operation, the protective circuits must be included in the power supply design.

Modulator Circuit (Oscillator, drivers, modulators, and latches). These circuits, which are indicated in the circuit diagram of Fig. 6 and are described in Table IV, deliver the base drive to the power-switching transistors. The forward drive must be sufficient to keep the transistors saturated under all conditions, and must have a short rise time to provide fast transistor turn-on and low dissipation. The reverse drive must have short rise time and a magnitude equal to or greater than the forward base drive. The circuits also sense excessive emitter current in the power-switching transistors, and compensate by adjustment of the duty cycle, as noted above.

These circuits eliminate common-mode conduction in the power-switching transistors. This conduction occurs in a driven inverter when the transistor that has been "off" is

Table II – Relationship Between Line Voltage and the Required Collector Voltage Rating for the Switching Transistors.

RMS LINE VOLTAGE (V)	PEAK LINE VOLTAGE (V)	NOMINAL COLLECTOR VOLTAGE (V)	SAFE (15% ADDED) COLLECTOR VOLTAGE RATING (V)	
90	127.3	254.5	292	
95	134.3	268.7	309	
100	141,4	282.8	325	
105	148.5	296.9	341	↑
110	155.5	311.1	357	
115	162.6	325.2	374	Operating
120	169.7	339.4	390	Range
125	176.7	353.5	406	
130	183.8	367.6	422	
135	190.0	381.8	439	↓
140	198.0	395.9	455	
145	205.0	410.1	471	
150	212.1	424.2	487	

turned "on"; the other transistor continues to conduct because of its storage time. For several microseconds both transistors conduct, and the current is not limited by the collector circuit. The transistor that has just been switched on has high current and voltage simultaneously, and therefore high dissipation (perhaps 50 per cent of the rated power-supply output). This power dissipation is wasteful and may even damage the transistor.

The oscillator frequency should be stable to minimize rectifier losses, and should be greater than 20 kHz to eliminate sound. All of the circuits should be insensitive to component-value variations, component drift, and random or stray interference.

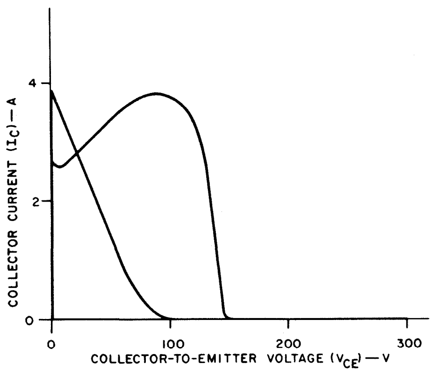


Fig. 3 - Typical load line for a switching transistor in the switching-regulator power supply.

Table III – Recommended Specifications for Switching Transistor

PARAMETER	MEASUREMENT CONDITIONS: GENERAL	MEASUREMENT CONDITIONS: FOR TRANSISTORS USED IN DESIGN EXAMPLE	VALUE
I_{CEV}	V_{CE} from Table II	$V_{CE} = 450$ V	5 mA max.
	$V_{BE} \leqslant V_{EE}$(1)	$V_{BE} = 1.5$ V	
I_{EBO}	$V_{EB} = V_{EE}$(1)	$V_{EB} = 6$ V	5 mA max.
$I_{S/b}$	$I_C = I_C$ (max.)	$I_C = 4$ A	(must pass test)
	$V_{CE} = V_{CC}$ (max.)	$V_{CE} = 200$ V	
	$t \geqslant 50\ \mu s$	$t = 100\ \mu s$	
V_{CE} (sat)	$I_C = I_C$ (max.) I_B as provided by driver circuit	$I_C = 4$ A $I_B = 0.8$ A	< 3 V
V_{BE}(sat)	"	"	< 2 V(2)
t_r	$I_C = I_C$ (max.) I_{B1} and I_{B2} as provided by driver circuits	conditions(3)	$< 1\ \mu s$
t_f	"	"	$< 1\ \mu s$

(1) V_{EE} is negative voltage source applied to the base.

(2) Importance depends upon drive-circuit design. For the design shown, V_{BE}(sat) is not critical.

(3) Because of the great variations in parameters and waveforms, some standard test condition is used for control. The manufacturers standard conditions are usually adequate control.

Power Recifiers. Most of the losses in the power supply occur in the power rectifiers. In a 5-volt, 50-ampere supply, for example, each of the four 1N3909 rectifier diodes carries a nominal peak current of 25 amperes at 50-per-cent duty cycle. The forward power loss in the rectifier can be calculated from the current and voltage values. The voltage

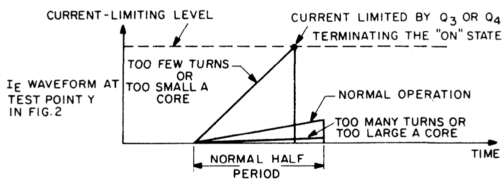


Fig. 4 - Waveform of emitter current in power-switching transistor showing effects of core-size and number of primary turns, with regulation defeated (see note on Fig. 6).

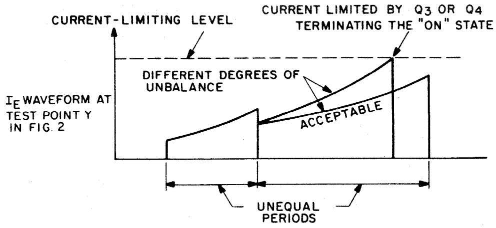


Fig. 5 - Waveform of emitter current in power-switching transistor showing effect of unbalanced direct current, with regulation defeated and load current of 25 amperes.

drop is not specified for 25-ampere operation, but the rectifier has a maximum voltage drop of 1.4 volts at a current of 30 amperes. Because this 30-ampere data is close to 25-ampere operation (and unbalance could cause the current to exceed 25 amperes), the maximum forward-drop rectifier losses can be estimated from the 30-ampere specifications: 1/2 x 1.4 V x 30 A x 4 = 84 watts at maximum rated output.

Reverse recovery losses in the diodes add to the total dissipation; these losses, which are significant at 20 kHz, depend on the rectifiers used, the leakage inductances in the wiring and the isolation transformer, the transistor switching times, and the operating frequency. Because of the many variables (and unknowns) involved, the rectifier losses should

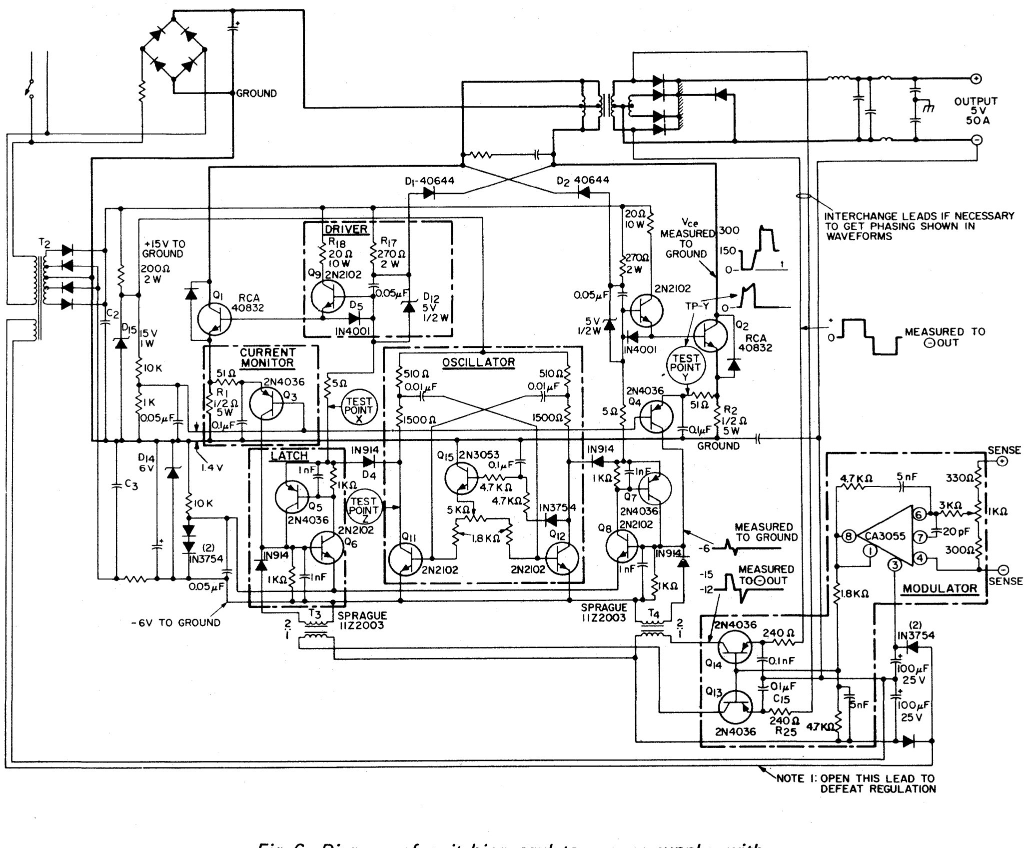


Fig. 6 - Diagram of switching-regulator power supply, with modulator circuits emphasized.

Table IV – Functional Description of Modulator Circuits

MODULATOR CIRCUIT SECTIONS	MAIN PARTS IN SECTION	FUNCTION OF SECTION
Oscillator	Q_{11}	Provides basic operating frequency. Holds off driver Q_9 through D_4 to keep Q_1 off for half the period. Provides reverse base drive for Q_1 at 100% duty cycle through D_4 and D_5. Resets the latch circuits.
	Q_{15}	Insures oscillator starts, by removing base drive if Q_{12} saturates too long.
Latch	Q_5	Terminates power-on cycle by latching and causing reverse base to Q_1.
	Q_6	Is triggered on by either the current monitor Q_3 or the modulator Q_{13} through T_3, and is held on by regenerative action. Is turned off by the oscillator.
Modulator	Q_{13} CA3055 R_{25} C_{15}	Compares the voltage developed by the CA3055 with a triangular waveform developed by R_{25} C_{15}. When the triangular voltage exceeds the other, Q_{13} conducts and triggers on the latch through T_3.
Driver	Q_9 D_{12} D_5 D_1 D_4 R_{18}	Supplies the forward base drive to Q_1, which is set by R_{18}. Prevents common-mode conduction. Diode D_1 senses V_{CE} of Q_2 and prevents base drive to Q_9 and thus to Q_1. Zener D_{12} causes Q_1 to be held off until V_{CE} of Q_2 exceeds the zener voltage (5V).
Current Monitor	Q_3 R_1	Limits the emitter current through Q_1. That current produces a voltage across R_1 which is filtered; if it exceeds 2.0 V, Q_3 conducts and triggers the latch to terminate the power-on cycle.
Low-Voltage Supplies	T_2 C_2 C_3 D_{14} D_{15}	A 30-volt unregulated supply is used to supply the base drive for Q_1 and Q_2. It is regulated to 15 volts by D_{15} to supply the oscillator. A -12-volt unregulated supply is regulated to -6 V by D_{14}. It supplies reverse base drive to Q_1 and Q_2, and operates the oscillator circuit. An isolated supply operating from T_2 supplies bias to the modulator circuit.

be determined by measurement of circuit efficiency or heat-sink temperature. A total rectifier loss of 45 per cent of the rated output power of the regulator is to be expected.

Filter. The use of ac power to generate dc outputs that are free of ac signals requires a good filter. Moreover, in a power supply that delivers high current, the filter components must be of high quality: the inductor must have high Q, and the capacitor must have both low resistance and low inductance.

The inductor carries a current equal to the dc output. It can have small size and low resistance because it has a low inductance (3 to 8 microhenries). The inductance value used is a compromise between the need for a high value to limit peak currents and thus permit good transistor utilization, and the need for a low value to permit fast response to sudden current demands. Fig. 7 shows how the inductor controls the ratio of peak collector current to average collector current in the power-switching transistors under steady-state operation. Smaller inductors cause higher peak currents, which require larger transistors and result in poor utilization of the transistor capabilities. The minimum value of inductance is determined by the peak collector current allowed, as follows:

$$L_{min} = \frac{t_{off}(max)\ E_{out}}{n_T\ \ I_c(peak) - I_{load}}$$

where n_T is the turns ratio of the isolation transformer. However, as shown in Fig. 8, the inductor also establishes the maximum rate of rise of current to the capacitor, and thus determines the ability of the power supply to respond to sudden demands for load current. For quick response, a low value of inductance is desirable.

The filter capacitors for this application must be selected for 20-kHz operation. Ceramic and paper types are best, but tantalum or high-quality aluminum electrolytics can be used for large values of capacitance. The capacitance must be sufficient to prevent the output voltage from decreasing excessively when the load is suddenly increased and the

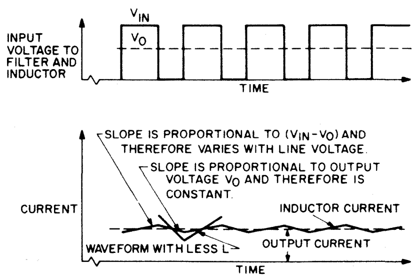


Fig. 7 - Waveforms for filter inductor under steady-state operation at 60-per-cent duty cycle.

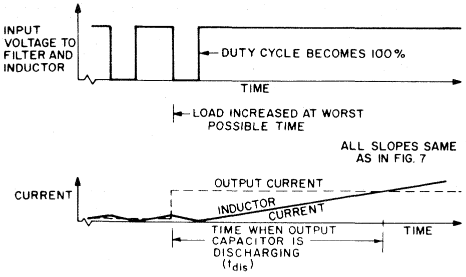


Fig. 8 - Waveforms for filter inductor under sudden increase of load current.

inductor supplies less than the load current. The minimum capacitance is given by

$$C_{min} = \frac{I_{load}(t_{dis} + 2t_{off}(max))}{2(\Delta V) \text{ allowed}}$$

where

$$t_{dis} = \frac{L\ I_{load}}{\frac{V_{CC}(min)}{n_T} - V_o - 1.0}$$

and $t_{off}(max)$ is 12.5 microseconds for this design.

A SPECIFIC DESIGN EXAMPLE

A power supply that uses the circuits shown in Figs. 1, 2, and 6 can deliver a load current of 50 amperes at 5 volts. All of the pulse-width modulation circuits, drivers, and latches are duplicated for each power-switching transistor. This duplication uses more than the minimum number of components, but it provides wide design margins and more reliable operation.

Voltage regulation and overload regulation are accomplished by reducing the duty cycle of the power-switching transistors. The duty cycle is reduced by triggering the latches on (see Fig. 6 and Table IV), either from pulse transformers T3 and T4 to regulate the output voltage, or from transistors Q3 and Q4 to prevent excessive emitter currents in the power-switching transistors. The excessive currents could be caused by overloads at the output or by transformer core saturation resulting from unbalanced duty cycles.

Input-to-output isolation is maintained through the main isolation transformer (T1), the 60-Hz transformer (T2), and the pulse transformers (T3 and T4). This circuit isolation is indicated in Fig. 2.

This power supply is capable of operating into any load impedance, including short circuits, without damage. It can operate at duty cycles from less than 10 per cent to 100 per cent. With a duty cycle of 100 per cent, the supply operates as a straight inverter at the full capacity of the transistors, transformers, and rectifiers.

The base drive for the power-switching transistors is direct-coupled, and is supplied by an unregulated low-voltage power supply that operates from a 60-Hz transformer. Direct coupling of the base drive provides positive control over transistor bias. The reverse base drive is supplied by the two-transistor latch circuits Q5 and Q6 or Q7 and Q8, or by the oscillator transistors (Q11 and Q12) if the duty cycle is 100 per cent. The reverse base voltage is obtained from a 6-volt regulated supply.

The frequency is controlled by the astable transistor oscillator that operates from 15-volt and −6-volt regulated sources. A potentiometer for equalization of the duty cycle is shown, but is not normally required. Transistor Q15 insures that the oscillator does not "hang up."

Common-mode conduction is reduced by cross-coupled diodes D1 and D2. These diodes conduct when V_{CE} of the power-switching transistor is less than 5 volts (breakdown of the zener diode), and prevent conduction of the opposite power-switching transistor; this operation is illustrated in the waveforms of Fig. 9. These diodes are of critical importance because the storage time of the power-switching transistors is several microseconds at light load conditions ($I_{B_1} > 0.5$ amperes and $I_C < 0.5$ amperes).

A major consideration in the design of this power supply is the protection of the switching transistors and the load circuit from damage caused by transients or faults in the modulator. The faults most likely to occur are lock-up in the oscillator, transient turn-on of the latching transistors caused by dv/dt at point X in Fig. 6, and magnetic pickup in the pulse transformers. The circuit is designed so that any of these faults will cause the power-switching transistors to turn off; this design protects the transistors and keeps the output voltage low. The overcurrent protection circuit is made independent of the proper functioning of the output regulator or its associated circuits, and is dc-coupled to minimize the possibility of failure. Finally, if the low-voltage supplies fail, the output voltage merely falls to zero without any harmful surges.

Table IV gives a full description of the modulator circuits. For simplicity, the discussion is limited to the components on the left side of the symmetrical circuit layout shown in Fig. 6.

VARIATIONS ON THE DESIGN

The design discussed above and shown in Figs. 2 and 6 can be modified for different performance.

More Output. Larger transistors, such as the 2N5805, can be used as the power switches to increase the output by as much as 100 per cent. These transistors would require more base drive, which can be supplied by the circuit shown

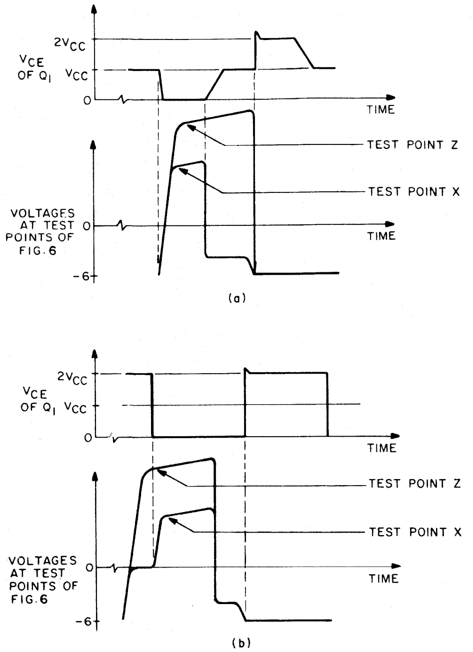


Fig. 9 - Suppression of common-mode conduction: (a) 50-per-cent duty cycle; (b) 100-per-cent duty cycle.

in Fig. 10 if the capacity of the 30-volt supply is increased.

Simpler Construction. Custom integrated circuits can reduce the number of parts in this unit.

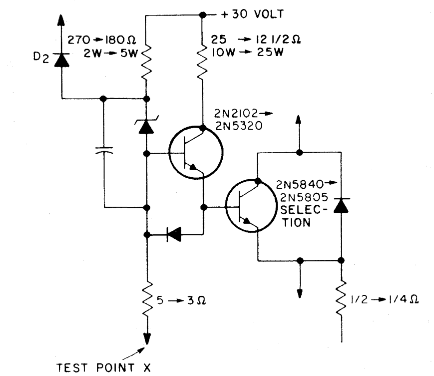


Fig. 10 - Changes in power-switching transistor drive circuit to produce increased output from larger power-switching transistors.

Smaller Package. A 20-kHz "off-the-line" inverter can be used in place of the 60-Hz transformer to reduce the size of the supply further. The smaller transformers, capacitors, and resistors for 20-kHz operation would, however, increase the cost.

Sensing. The output-voltage sensing can be improved, and output-current sensing can be added if required. The short-circuit protection in the circuit can be improved by adding an IC regulator that senses the output current by means of a current-sampling resistor.

Low-Voltage Supplies. Different voltages and different types of regulation can be used in the low-voltage supplies. One alternative, shown in Fig. 11, is the use of an extra winding on the isolation transformer to supply the base-drive transistors. This circuit reduces the cost of smoothing capacitor C2 in Fig. 2, and reduces the size of the 60-Hz transformer.

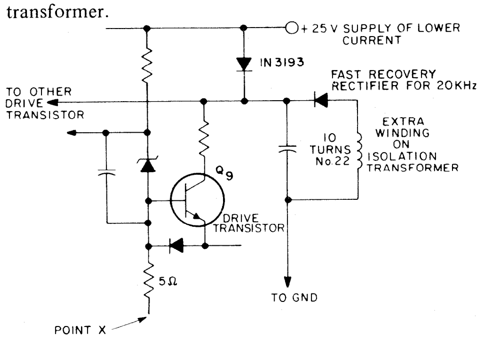


Fig. 11 - Use of a separate isolation-transformer winding to supply the base-drive transistors.

DESIGN NOTES

The switching-regulator type of power supply is more complex than a conventional dc series regulator. Because tests must be made with regard to waveforms, an oscilloscope is a required diagnostic tool. A special problem is that most of the components in these supplies are not isolated from the power line. Although the test equipment can be used "floating", the safest practice is to use an isolation transformer during tests of the power supply.

Finally, the design and construction of the filter are important to reduce spikes on the output. The filter unit should be sealed to prevent radiation.

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A 60-Watt, 20-Volt Regulated Power Supply Using a Single Pass Transistor

by D. Morris and R. H. Smith

This Note discusses a regulated constant-voltage power supply that uses RCA integrated circuits and a rugged RCA hometaxial transistor to attain high output-power capability. A 20-volt, 3-ampere supply that uses a single RCA-2N3055 pass transistor is described in detail; the discussion includes circuit descriptions, operating characteristics, component specifications, and suggestions for layout and construction. Thermal-fatigue effects and safe operating conditions for power transistors are considered. Finally, guidance is provided for those who may want to develop a similar circuit for their own needs.

DESCRIPTION OF CIRCUIT

Specifications for the 60-watt, 20-volt supply are listed in Table I, and a block diagram is shown in Fig. 1. The circuit uses an external pass transistor and driver to extend the current capability of the RCA-CA3055 integrated-circuit voltage regulator; the overload protection provided by a fold-back current-limiting circuit permits operation of the transistor at a dissipation level close to its limit. This foldback circuit achieves high efficiency by use of an RCA-CA3030 integrated-circuit operational amplifier.

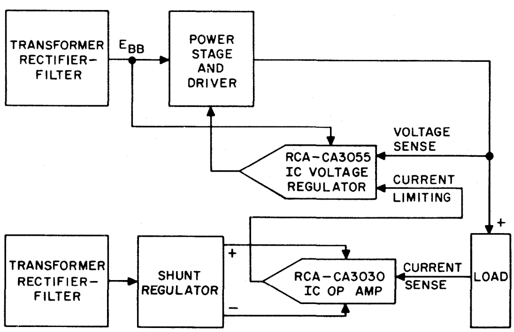
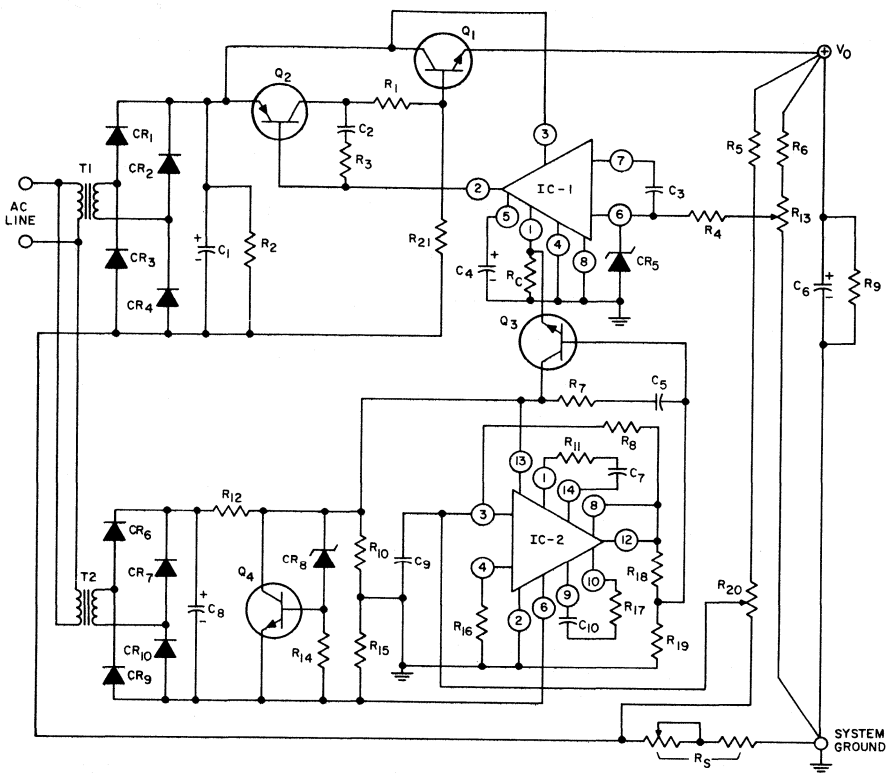


Fig. 1— Block diagram of regulated power supply with foldback current limiting.

Table I - Power-Supply Specifications

V_{input}	105-130 V, Single Phase 55-420 cps
V_{output}	20 V ±0.5 V
$I_{load}(max)$	3 A
Ambient Temperature	0 to +55°C
Voltage spikes	None at turn on or turn off
Regulation	Line: ±0.25%
	Load: ±0.25%
Ripple	33 mV pp; 9.5 mV rms
Transients:	
No load to full load:	100 mV, recovery within 50 μs
Full load to no load:	100 mV, recovery within 50 μs
Drift	20 mV in 8 hours of operation at constant ambient temperature
Short Circuit and overcurrent protection	Foldback technique

The over-all operation of the circuit can be understood with the aid of the schematic diagram shown in Fig. 2. Transformer T1 and its rectifiers supply the raw dc power that is regulated by pass transistor Q1; this pass transistor is driven by driver Q2, which is driven by the control circuit IC1. Transformer T2, with its rectifiers and shunt regulator Q4, provides positive and negative supplies for operational amplifier IC2; this operational amplifier drives the current-limiting control Q3. Output voltage is sensed at resistance string (R6 + R13), and load current is sensed by R_S.



T1	Signal Transformer Co., Part No. 24-4 or equivalent
T2	Signal Transformer Co., Part No. 12.8-0.25 or equivalent
CR1-CR4	RCA-1N1614
CR5	Zener Diode, 1N5225 (3.3 V)
CR6, CR7, CR9, CR10	Power Rectifier, RCA-1N3193
CR8	Zener Diode, 1N5242 (12 V)
C1	5900 μF, 75 V, Sprague Type 36D592F075BC or equivalent
C2	0.005 μF, ceramic disc, Sprague TGD50 or equivalent
C3, C7, C10	50pF, ceramic disc, Sprague 30GA-Q50 or equivalent
C4	2μF, 25 V, electrolytic, Sprague 500D G025BA7 or equivalent
C5	0.01 μF, ceramic disc, Sprague TG510 or equivalent
C6	500 μF, 50 V, Cornell-Dubilier No. BR500-50 or equivalent
C8	250 μF, 25 V, Cornell-Dubilier BR 250-25 or equivalent
C9	0.47 μF, film type, Sprague Type 220P or equivalent
R1	5 ohms, 1 watt, IRC type BWH or equivalent
R2	1000 ohms, 5 watts, Ohmite type 200-5 1/4 or equivalent
R3	1200 ohms, 1/2 watt, carbon, IRC type RC 1/2 or equivalent
R4	100 ohms, 1/2 watt, carbon, IRC Type RC 1/2 or equivalent
R5	430 ohms, 2 watts, wire wound, IRC Type BWH or equivalent
R6	9100 ohms, 2 watts, wire wound, IRC Type BWH or equivalent
R7	470 ohms, 1/2 watt, carbon, IRC type RC 1/2 or equivalent
R8	5100 ohms, 1/2 watt, carbon, IRC type RC 1/2 or equivalent
R9, R14	1000 ohms, 2 watts, wire wound, IRC type BWH or equivalent
R10, R15	250 ohms, 2 watts, 1% wire wound, IRC type AS-2 or equivalent
R11, R17	1000 ohms, 1/2 watt, carbon, IRC type RC 1/2 or equivalent
R12	82 ohms, 2 watts, IRC type BWH or equivalent
R13	1000 ohms, potentiometer, Clarostat Series U39 or equivalent
R16	1200 ohms, 2 watts, wire wound, IRC type BWH or equivalent
R18	510 ohms, 1/2 watt, carbon, IRC type RC 1/2 or equivalent
R19	10,000 ohms, 1/2 watt, carbon, IRC type RC 1/2 or equivalent

Fig. 2— Schematic diagram of 60-watt, 20-volt regulated power supply with foldback current limiting.

R20	300 ohms, potentiometer, Clarostat Series U39 or equivalent
R21	510 ohms, 3 watts, wire wound, Ohmite type 200-3 or equivalent
R_C	240 ohms, 1%, wire wound, IRC type AS-2 or equivalent
R_S	(See text for fixed portion); 1 ohm, 25 watts, Ohmite type H or equivalent
IC1	RCA-CA3055
IC2	RCA-CA3030
Q1	RCA-2N3055
Q2	RCA-2N5781
Q3, Q4	RCA-40347

Miscellaneous

(1 Req'd)	Heat Sink, Delta Division Wakefield Engineering NC-423 or equivalent
(3 Req'd)	Heat Sink, Thermalloy #2207 PR-10 or equivalent
(1 Req'd)	8-pin socket Cinch #8-ICS or equivalent
(1 Req'd)	14-pin DIL socket, T.I., #IC 014ST-7528 or equivalent
(2 Req'd)	TO-5 socket ELCO #05-3304 or equivalent
	Vector Board #838AWE-1 or equivalent
	Vector Receptacle R644 or equivalent
	Chassis – As required
	Cabinet – As required
	Dow Corning DC340 filled grease

Fig. 2– Schematic diagram of 60-watt, 20-volt regulated power supply with foldback current limiting. (cont.)

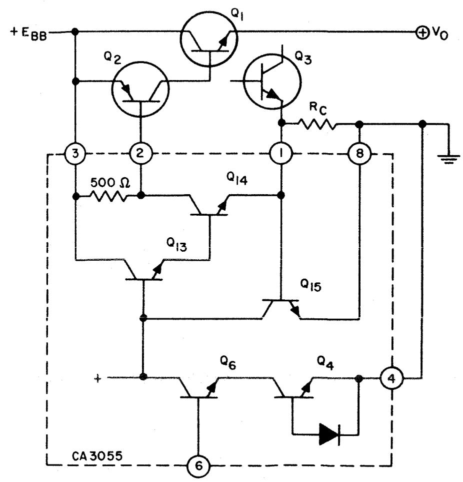


Fig. 3– CA3055 control of the power transistors.

Voltage Regulation

The power-supply output voltage is sampled by the voltage divider (R6 + R13), and a portion is fed to terminal No. 6 (the inverting input) of the CA3055. (This portion is less than the 3.3-volt breakdown voltage of zener diode CR5; the zener is present only to protect the integrated circuit from accidental overvoltages.) If the output voltage decreases, the base-to-emitter voltage of Q2 increases, as explained in the next paragraph. Therefore the pass transistor Q1 is driven harder, and as a result the output voltage increases to its original value (minus the error dictated by the system gain).

The process by which a voltage decrease at terminal No. 6 of the CA3055 produces an increase of Q2 base-to-emitter voltage can be understood with the aid of Fig. 3, which shows some of the internal circuitry of the CA3055.[1] The drop of voltage at terminal No. 6 causes a higher base-to-emitter voltage at the Darlington combination Q13-Q14. Therefore the collector current of Q14 increases, and thus increases the voltage drop across the 500-ohm resistor, which is the base-to-emitter voltage of Q2.

Foldback Current Limiting

The purpose of the current-limiting circuit is to prevent the power supply from passing a load current that could damage the pass transistor if a very low impedance (or a short circuit) is placed across the output terminals. Fig. 4 shows the effect of this circuit. The supply voltage remains constant until the load current reaches the threshold for activation of the limiting circuit; any further decrease of load impedance causes output voltage V_O and load current I_O to decrease, so that the V_O-I_O characteristic folds back to limit the power dissipation in the pass transistor. Activation of foldback disables the voltage-regulation circuit.

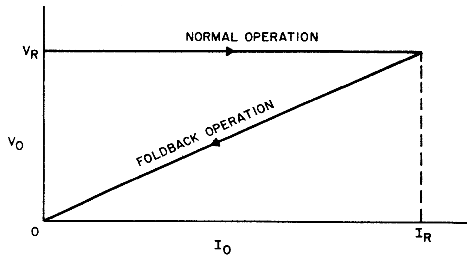


Fig. 4– Foldback current-limiting characteristic.

The circuitry for foldback current limiting, shown in Fig. 5, uses the CA3030 integrated circuit as a differential amplifier.[2-5] A signal from the voltage divider RR1 and RR2*, which is across V_O and the E_{BB} return, is applied to

*RR1 actually consists of R5 and the upper portion of R20 in the schematic diagram of Fig. 2; RR2 is the lower portion of R20.

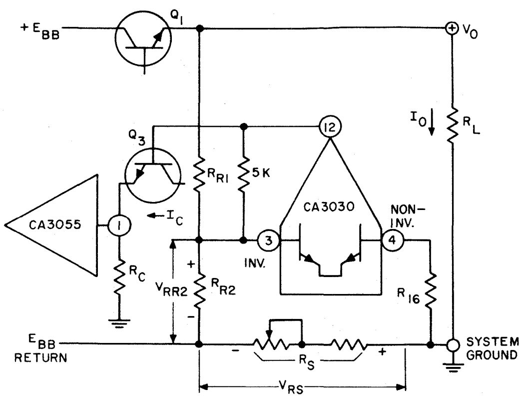


Fig. 5— Circuitry for foldback current limiting.

the inverting input (terminal No. 3) of the differential amplifier. The non-inverting input is tied to system ground through R16. Thus the base-to-base signal that actuates the differential amplifier is the difference between V_{RS} ($=I_O R_S$) and V_{RR2}. The CA3030 output, which is the voltage at terminal No. 12, varies linearly with the actuating voltage, as shown in Fig. 6. When the load current is zero* , V_{RS} is zero; therefore (V_{RS} - V_{RR2}) is negative, terminal 12 is negative with respect to ground, and Q3 is back-biased (i.e., cut off). Therefore Q3 does not interfere with the normal voltage-regulated operation of the supply. As the load current increases, V_{RS} increases and the voltage at terminal 12 increases.

The value of resistor R_S is adjusted so that when the load current reaches the foldback-activation value (about 3 amperes in the power supply shown), the voltage at terminal No. 12 of the CA3030 becomes positive. At about 0.7 volt, transistor Q3 begins to conduct; current flows through the current-limiting resistor R_C, with the result that terminal No. 1 of the CA3055 control circuit is driven positive. Q15 of Fig. 3 turns on, and the base-to-emitter voltage of Q13-Q14 is therefore reduced; the base-to-emitter voltage of Q2 is reduced, and the output voltage of the power supply decreases. This decrease of V_O tends to reduce the load current; however, V_{RR2} also decreases with V_O, so that (V_{RS}-V_{RR2}) remains fixed and Q3 continues to conduct at the same emitter current. If the load impedance is reduced, Q3 will be driven even harder, and therefore the output voltage and the load current will decrease even further. Fig. 4 shows the foldback as R_L decreases.

This process is reversible. If the load impedance R_L is increased, I_O and V_O will increase. When I_O reaches the foldback-activation level, Q3 will cut off again and the power supply will return to regulated operation.

* The currents in the 1-kilohm bleeder resistor and the 10-kilohm sensing string are neglected in this discussion.

The CA3030 must be operated as a linear voltage amplifier in the foldback circuit, so that the gain is as shown in Fig. 6. If the CA3030 is adjusted otherwise, a Schmitt trigger action can occur. Such operation may be desirable in latching-type current protection, e.g., in circuits that switch off at overload. However, those circuits introduce other problems such as lack of automatic turn-on, hysteresis effects on varying loads during the shutdown process, and capacitive and nonlinear loads; therefore, latching protection is not considered in this Note.

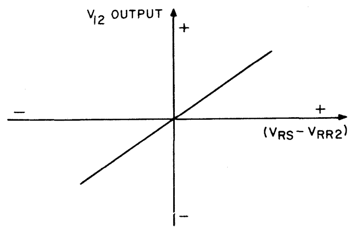


Fig. 6— Output voltage from the CA3030 operational amplifier as a function of actuating voltage.

DESIGN CONSIDERATIONS

For maximum performance from this power-supply circuit, several design features must be analyzed. These features include the equivalent source resistance of the rectifier filter circuit, the foldback-circuit parameters, and the maximum power dissipation in the pass transistor. In addition, safe-operation and thermal-fatigue ratings for the transistors are important.

Equivalent Resistance of the Raw DC Source

A full-wave bridge rectifier[6] provides the raw dc power for this supply; the rectifier and its filter are shown in Fig. 7(a). The output current and power capability would be improved by use of a custom-wound transformer, and even greater capability would be attained by use of a full-wave center-tapped rectifier circuit with a custom transformer. However, a custom transformer would increase the unit cost, particularly if no winding facilities were available; therefore, a commercially available transformer is used in this supply.

The load regulation of the transformer is approximately 10 per cent. This value is used as the approximate R_g/R_L parameter in Schade's curves[7] to select input capacitor C1. The value of C1 that will keep peak-to-peak ripple below 2.4 volts is found to be 5900 microfarads. With this capacitance, the measured value of equivalent source (generator) resistance R_g is 2 ohms. Fig. 7(b) shows the equivalent circuit of the rectifier and filter.

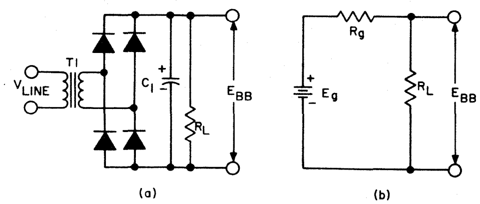


Fig. 7— Full-wave bridge rectifier and filter that provide raw dc for power supply: (a) circuit diagram; (b) equivalent circuit.

At high line voltage (130 volts ac) the cold-temperature, no-load dc voltage of the rectifier filter is 39.4 volts; this value is just below the 40-volt maximum rated voltage of the CA3055. At low line voltage (105 volts ac) the hot full-load dc voltage of the rectifier filter is 25.4 volts; the theoretical minimum necessary voltage for the supply is shown in Appendix A to be 25.4 volts.

Foldback-Circuit Parameters

A simple conventional foldback circuit, in which a single-ended amplifier is used instead of the differential amplifier described above, is shown in Fig. 8(a). The equivalent circuit is shown in Fig. 8(b). Analysis of this circuit (see Appendix B) shows that the ratio of maximum load current just before foldback activation, I_X, to the rated load current I_R, is approximately given by

$$\frac{I_X}{I_R} = \frac{V_D + V_{BE} + V_{RR}}{V_D + V_{RR}} \quad (1)$$

in which V_D is the voltage drop across the diode (= 0.7 volt for a silicon diode). I_R is the zero-bias level for Q_X; when I_O exceeds I_R, Q_X becomes forward-biased and causes loss of regulation.

The ratio of the short-circuit current, I_{SC}, to the rated load current is approximately given by

$$\frac{I_{SC}}{I_R} = \frac{V_D + V_{BE}}{V_D + V_{RR}} \quad (2)$$

When the values of the circuit components are inserted into these equations, these ratios have the following values:

$$\frac{I_X}{I_R} = 1.23 \quad (3)$$

$$\frac{I_{SC}}{I_R} = 0.47 \quad (4)$$

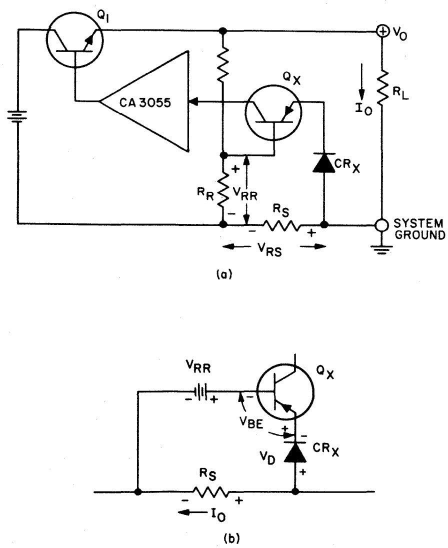


Fig. 8— A simple conventional foldback circuit that uses a single-ended amplifier instead of a differential amplifier: (a) circuit diagram; (b) equivalent circuit.

Eq. (3) shows that the pass transistor must have a current capability 23 per cent greater than the rated current value of the supply, or, equivalently, that the pass transistor is utilized at only 77 per cent of its current and power-dissipation capabilities at rated supply current. This utilization is reduced even further by the source resistance of the generator, as discussed below.

Another disadvantage of the simple foldback circuit is indicated in Appendix A: the minimum voltage across filter capacitor C1 is increased by at least ($V_D + V_{BE} + V_{RR}$).

The foldback circuit used in the supply shown, which uses a differential amplifier and a low actuating signal, is free of the drawbacks encountered in the simple conventional circuit. Actual values measured on the differential-amplifier foldback circuit, set for a 0.2-volt actuating signal and a rated load current of 3 amperes, are as follows:

$$I_{SC} = 0.125\ \text{A}$$

$$I_X = 3.15\ \text{A}$$

$$\frac{I_X}{I_R} = \frac{3.15}{3} = 1.05$$

$$\frac{I_{SC}}{I_R} = \frac{0.125}{3.00} = 0.042$$

The maximum load current to actuate foldback is 5 per cent greater than the rated current, and the short-circuit current is 4 per cent of the rated current.

Maximum Power Dissipation in the Pass Transistor

Power dissipation in the pass transistor reaches maximum during foldback. This worst-case value can be calculated by the analysis given in Appendix C, which uses the equivalent circuit shown in Fig. 9. (The use of a power-sharing resistor in parallel with the pass transistor is neglected in this discussion because transformer T1 operates at its maximum capacity.) Because the maximum-dissipation situation might occur during operation, the power supply must be designed to withstand this worst-case condition.

Maximum power dissipation occurs when the output voltage is given by

$$V_{OX} = \frac{E_g}{2(1 + \sigma R_g)} \quad (5)$$

where E_g is the generator voltage, σ is the load conductance ($\sigma = I_R/V_R = 1/R_L$, I_R is the rated current, V_R is the rated voltage, and R_g is the generator resistance. The value of the maximum power, P_X, is given by

$$P_X = \frac{\sigma E_g{}^2}{4\,(1 + \sigma R_g)} \quad (6)$$

The rated current is determined as a function of rated voltage, maximum power, generator voltage, and generator resistance, as follows:

$$I_R = V_R\ \frac{4P_X}{E_g{}^2 - 4\,P_X\,R_g} \quad (7)$$

The maximum power limit for the pass transistor, P_X, depends on the heat sink. Appendix D shows that for the particular case under discussion the maximum power is 47 watts. Therefore, I_R is given by

$$I_R = 20\,\frac{4 \times 47}{(40)^2 - 4 \times 47 \times 2} = 3.07\ \text{A}$$

The value of V_{OX} is then determined as follows:

$$V_{OX} = \frac{E_g}{2(1 + I_R/V_R\,R_g)} = \frac{40}{2(1 + \frac{3.07}{20} \times 2)} = 15.4\ \text{V} \quad (8)$$

Idealized curves of various power-supply parameters in regulated operation and in foldback are shown in Fig. 10. Maximum dissipation is 46 watts, at V_{OX} = 15.4 volts. This condition can occur if the supply is turned on with a load that causes worst-case foldback operation. As the transformer heats up, the capacitor voltage decreases (i.e., R_g increases), and dissipation is slightly reduced. Even at maximum dissipation in the transistor, however, the power supply can provide continuous trouble-free operation.

Safe Operation of Power Transistors

The current capability of the circuit can be increased almost indefinitely by use of drivers and output transistors with higher current and dissipation capability, by paralleling transistors, or by providing one or more additional stages in a Darlington configuration, along with increased heat sinking, transformer and rectifier capability, and filter capacitance. Information on the proper operation of transistors can be

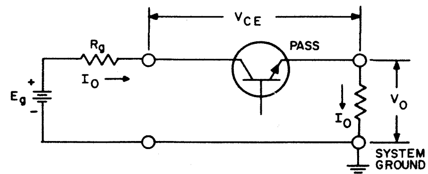


Fig. 9— Equivalent circuit used for calculation of power dissipated in pass transistor.

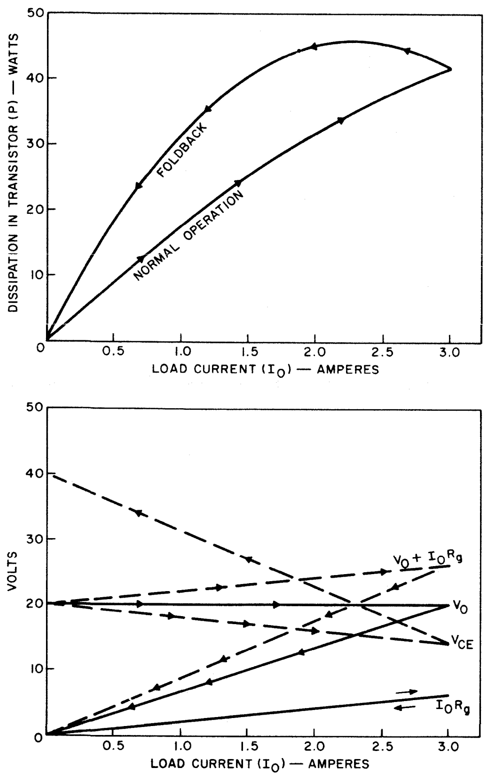


Fig. 10– Idealized operating characteristics of foldback current-limiting circuit.

found in published data sheets.[8,9] Safe-area charts, derating curves, thermal resistance, and maximum junction-temperature specifications are given in the data sheets. Worst-case-operation conditions for the transistors can be determined for a number of possible values of rated voltage and current, and these values can be checked against the specified ratings.

The current capability of linear series regulators is usually limited by the safe dissipation levels of the pass devices, rather than by maximum current ratings or available gain, especially if simple (not foldback) current limiting is used, as for an adjustable voltage supply. Safe operating area encompasses the limitations of power dissipation and second breakdown.[10] RCA hometaxial-base transistors, such as the 2N3055, show little or no second-breakdown limitation in the safe area. Because the published safe area is guaranteed by 100-per-cent factory testing, the user is sure of reliable service even in such severe applications as linear regulators.

Thermal-Fatigue Considerations

A transistor is constructed of materials that have various thermal-expansion coefficients. When the transistor is subjected to a range of internal temperatures in the course of normal operation, the different coefficients of expansion result in stresses on various parts of the internal transistor structure. These stresses are proportional to the change in temperature, the difference in expansion coefficients between two materials in contact, and the pellet size. When the stresses are severe enough and are repeated enough times, they can cause the transistor to fail, usually by rupture of the solder bonds between the pellet and the top contacts or between the pellet and the mounting base. Large power transistors that operate at high power levels, such as the pass devices in linear series regulators (e.g., the RCA-2N3055 family of transistors in the circuit described in this Note), operate in a mode of high thermal-fatigue stress.

RCA has recognized the thermal-fatigue problem and has developed transistors that are extremely resistant to thermal-fatigue failure. This resistance to thermal-fatigue failure is the result of a proprietary Controlled Solder Process (CSP), by which impurities and voids are reduced or eliminated from the solder system. Impurities enhance the propagation of cracks induced by thermal-fatigue stresses, and thus contribute to early failure of the solder bonds. Voids under the pellet act as insulation, and can lead to hot spots that cause high thermal-fatigue stresses. CSP is now employed on all RCA hermetic power transistors.

RCA has developed power-transistor thermal-cycling ratings that indicate expected life, in number of thermal cycles, as a function of power dissipation and case-temperature change. These ratings are calculated from theoretical models based on actual measurements.[11,12] This rating system shows that the RCA-2N3055 pass transistor, used as described in this Note (maximum power dissipation of 46 watts, case-temperature change of 43°C), can survive more than 50,000 thermal cycles without failure. The RCA-2N5781 and the smaller devices in the circuit should last even longer.

The combination of homotaxial construction for ruggedness and CSP for long thermal-fatigue life makes these power transistors the best choice for power-supply applications.

OPERATIONAL PERFORMANCE

Adjustment of Current-Sensing Resistor R_S

The fixed portion of current-sensing resistor R_S is simply a short length of resistance wire; its resistance is about 0.064 ohm. This resistor must be adjusted on each power supply, because both the over-all loop system gain and the current-limiting voltage across terminals 1 and 8 of the CA3055 can vary from unit to unit. The two-step procedure for adjusting the fixed portion of the R_S is as follows:

(a) Set the reference voltage by adjusting the 250-ohm potentiometer (R20) until the voltage from the arm of the potentiometer to ground is 200 millivolts (with the load current zero, and total sensing resistor $R_S = 0$).

(b) Use a variable resistor across the output terminals to set the load current at 3.15 amperes. Then insert the fixed portion of the sensing resistance and increase it until current foldback is just initiated. Initiation of foldback is evidenced by sudden reduction in output voltage.

This fixed resistor should be made of resistance wire such as Driver Harris Manganin #18 (0.176 ohms per foot) or equivalent. Copper wire can be used provided I^2R heating does not change its resistance, and effects of ambient-temperature change are taken into consideration. (The temperature coefficient of copper wire is 3.9×10^{-3} per ^oC. If the copper resistor were adjusted at 20^oC, and the ambient temperature then changed to 55^oC, the current required to activate foldback would be reduced from 3.15 amperes to 2.7 amperes).

The variable portion of current-sensing resistor R_S is a 1-ohm potentiometer. It is used to set the current-limitation threshold at levels below 3 amperes, if such operation is desired.

Adjustment of Current-Limiting Resistor R_C

The CA3055 voltage regulator would function most effectively if current-limiting resistor R_C were zero, but R_C is necessary for foldback operation. Therefore, as a compromise between regulation and protection sensitivity, R_C is adjusted to provide an over-all regulation of $\pm$ 0.25 per cent for all load currents from 0 to 3 amperes. This value of R_C results in a reasonable short-circuit current (0.125 amperes). If R_C is made smaller (to permit better regulation), the ratio R8/R16 must be increased to provide more gain in the current-limiting circuit. This change may require restabilization of the circuit.

Power-Supply Performance

With the circuit adjusted as described above, the power supply performs as shown in Table II.

CONSTRUCTION

Fig. 11 shows the assembled power supply; it is 8 inches long, 8 inches wide, and 5 3/4 inches high (these dimensions can be reduced if necessary). The chassis is made of 0.052-inch aluminum, perforated on top and sides for ventilation; a commercial chassis such as the BUD CA1751 or equivalent could also be used.

The control circuit is built on a pre-punched fiber board. Good wiring techniques are observed, all leads to the integrated circuits are kept as short as possible, and heat sinks are attached where required.

The positive and negative supplies for the operational amplifier are also constructed on pre-punched fiber board. The board is attached with an L-bracket to the diode support, as shown in the diagram.

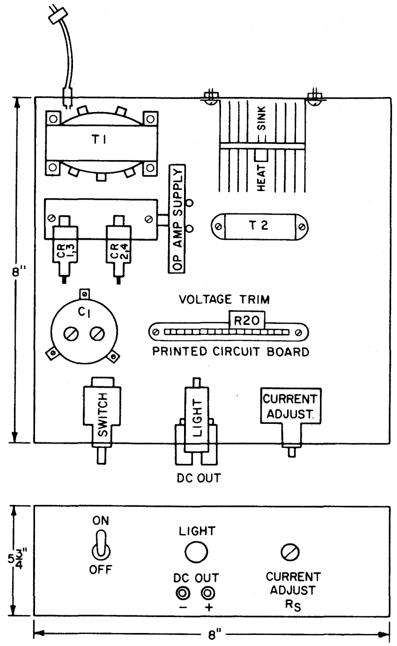


Fig. 11– Layout of power supply.

The pass-transistor heat sink is mounted vertically, with 1/4-inch clearance from the bottom of the chassis to provide adequate convection. The circuit board is mounted as far as possible from the pass-transistor heat sink to achieve maximum thermal isolation.

Construction of this supply is flexible. Wiring is not critical, but heavy wire should be used for the leads that carry high current. The total allowable IR drop in the wiring is 0.1 volt; at a current of 3 amperes, therefore, the total allowable resistance (including contact resistance) is 33 milliohms.

As in all error-detecting systems, the sampling should be accomplished at the terminals of the power supply, i.e., at the +20-volt and ground terminals. Therefore all of the system ground points indicated in Fig. 2 are connected with heavy wire to avoid ground loops. Output capacitor C6 is wired directly to the output terminals.

APPENDIX A. Minimum Voltage Across Filter Capacitor

The minimum voltage across filter capacitor C1 is obtained as follows:

$$V_{Cap\ (min)} = V_O + V_{O\text{-}PK} + V_{BE}\ 2N3055$$

$$+ V_{CE}\ 2N5781 + V_{R1} + V_{TOL} + V_{RS} + V_{LD}$$

Table II - Performance of Regulated Power Supply

Normal Operation: V_O set at 20.000 VDC with I_O = 3 A @ V_{line} = 115 VAC.		
PARAMETER	CONDITIONS	VALUE
Load regulation	$I_O = 0 \rightleftarrows 3A$, V_{Line} = 105 VAC	±0.25%
Load regulation	$I_O = 0 \rightleftarrows 3A$, V_{Line} = 115 VAC	±0.25%
Load regulation	$I_O = 0 \rightleftarrows 3A$, V_{Line} = 130 VAC	±0.25%
Line regulation	$I_O = 0$, $V_{Line} = 105 \rightleftarrows 130$ VAC	±0.25%
Line regulation	$I_O = 3A$, $V_{Line} = 105 \rightleftarrows 130$ VAC	±0.25%
Total regulation spread	$0 \leqslant I_O \leqslant 3A$, $105 \leqslant V_{Line} \leqslant 130$ VAC	0.77%
Ripple (peak-to-peak)	I_O = 3 A	33 mV
Ripple (rms)	I_O = 3 A	9.5 mV
Transients	Full load (3 A) to no load (O A)	$\leqslant$ 100 mV, $t_{recovery} \leqslant 50\ \mu s$
Transients	No load (O A) to full load (3 A)	$\leqslant$ 100 mV, $t_{recovery} \leqslant 50\ \mu s$
Transients	Turn on (105 or 130 VAC)	0
Transients	Turn off (105 or 130 VAC)	0
Drift	I_O = 3 A	$\leqslant$ 15 mV/8 hours
Case Temperature Rise:	After 8 hours @ I_O = 3 A and V_{Line} = 130 VAC	
2N3055		43°C
2N5781		49°C
CA3055		15°C
I_{SC}	V_{Line} = 105 or 130 VAC	0.125 A

Abnormal Operation: Circuit in fold back operation at worst-case condition (V_O = 15.4 VDC)			
PARAMETER	CONDITIONS	VALUE	
Case Temperature Rise:	After 8 hours in foldback @ V_{Line} = 130 VAC	Measured	Calculated
2N3055		50°C	60°C
2N5781		63°C	85°C
CA3055		17°C	–

where

V_O = output voltage = 20 V
$V_{O\text{-}PK}$ = ripple voltage (zero to peak = 1/2 peak to peak) = 1.2 V
V_{BE} 2N3055 = worst case V_{BE} of pass transistor = 1.4 V
V_{CE} 2N5781 = worst case V_{CE} of driver transistor = 1 V
V_{R1} = Voltage across collector resistor R1 = 1 V
V_{TOL} = 0.5-volt tolerance on output = 0.5 V
V_{RS} = voltage of current-sensing resistor = 0.2 V
V_{LD} = voltage drop in wiring = 0.1 V

Therefore

V_{Cap} (min) = 20 + 1.2 + 1.4 + 1 + 1 + 0.5 + 0.2 + 0.1 = 25.4 volts

APPENDIX B. Foldback Parameters

As a first approximation, the following equations describe the three conditions of load current in the circuit of Fig. 8(b):

General equation: $I_O R_S = V_D + V_{BE} + V_{RR}$

At rated current I_R, it is desirable that $V_{BE} = 0$.

$$\therefore I_R R_S = V_D + V_{RR}$$

At maximum load current, just before foldback is initiated,

$$I_X R_S = V_D + V_{BE} + V_{RR}$$

At short-circuit current, $V_O = 0$, and therefore $V_{RR} = 0$.

$$I_{SC} R_S = V_D + V_{BE}$$

By dividing appropriate equations,

$$\frac{I_X}{I_R} = \frac{V_D + V_{BE} + V_R}{V_D + V_R}$$

and

$$\frac{I_R}{I_{SC}} = \frac{V_D + V_R}{V_D + V_{BE}}$$

To make the maximum current close to rated current,

$$V_D + V_{BE} + V_R \approx V_D + V_R$$

$$\therefore (V_D + V_R) \gg V_{BE}$$

However, if V_D is large, the initiating voltage must also be large. Therefore, the minimum voltage across C1 must also be increased.

If V_D is one diode drop (0.7 volt) and if $(V_D + V_R)$ is 3 volts as a compromise, then V_R = 2.3 volts, and

$$\frac{I_X}{I_R} = \frac{0.7 + 2.3 + 0.7}{0.7 + 2.3} = 1.23$$

and

$$\frac{I_R}{I_{SC}} = \frac{0.7 + 2.3}{0.7 + 0.7} = 2.14$$

$$\therefore I_{SC} = \frac{I_R}{2.14} = 0.468\, I_R$$

APPENDIX C. Maximum Power Dissipation in the Pass Transistor

The equivalent circuit used to calculate the power dissipation in the pass transistor is shown in Fig. 9. R_g includes the 64-milliohm resistance used for sensing the 3.15-ampere actuating current. The additional current supplied for I_{CO} of Q1 and the current supplied to the CA3055 regulator are neglected.

The voltage across the transistor is given by

$$V_{CE} = E_g - V_O - I_O R_g = E_g - (V_O + I_O R_g)$$

The power dissipated in the transistor is given by

$$P = [E_g - (V_O + I_O R_g)]\, I_O$$

The ideal foldback characteristic is shown in Figs. 4 and 10. The measured values are within 5 per cent of the ideal values. Therefore a small error is introduced if the ideal characteristic is used for the analysis.

Equations that describe operation during foldback are derived as follows:

$$y = mx + b = mx + 0$$

$$m = \frac{V_R}{I_R}$$

$$V_O = \frac{V_R}{I_R} I_O$$

$$I_O = V_O \frac{I_R}{V_R} = V_O \sigma$$

$$P = E_g I_O - V_O I_O - I_O^2 R_g$$

$$= E_g V_O \sigma - V_O^2 \sigma - V_O^2 \sigma^2 R_g$$

$$P + V_O^2 [\sigma + \sigma^2 R_g] - V_O [\sigma E_g] = 0$$

or

$$P + V_O^2 A - V_O B = 0$$

$$P = BV_O - AV_O^2$$

$$\frac{dP}{dV_O} = B - 2AV_O$$

For maximum power, $\frac{dP}{dV_O} = 0$; therefore,

$$B - 2AV_O = 0$$

$$2AV_O = B$$

$$V_O = \frac{B}{2A} = \frac{1}{2}\left[\frac{\sigma E_g}{\sigma + \sigma^2 R_g}\right] = \frac{1}{2}\left[\frac{E_g}{1 + \sigma R_g}\right]$$

Thus maximum power occurs when

$$V_O = \frac{E_g}{2(1 + \sigma R_g)}$$

Substitution of this solution into the power equation yields

$$P = BV_O - AV_O^2$$

$$= \sigma E_g V_O - (\sigma + \sigma^2 R_g) V_O^2$$

$$= \sigma E_g \left[\frac{\frac{E_g}{2}}{1 + \sigma R_g}\right] - (\sigma + \sigma^2 R_g)\left[\frac{\left(\frac{E_g}{2}\right)^2}{(1 + \sigma R_g)^2}\right]$$

However,

$$\sigma + \sigma^2 R_g = \sigma(1 + \sigma R_g)$$

$$\therefore P = \frac{\sigma \frac{E_g^2}{2}}{1 + \sigma R_g} - \frac{\sigma(1 + \sigma R_g)\left(\frac{E_g}{2}\right)^2}{(1 + \sigma R_g)^2}$$

$$P = \frac{\sigma \frac{E_g^2}{2}}{1 + \sigma R_g} - \frac{\sigma \frac{E_g^2}{4}}{1 + \sigma R_g} = \frac{\sigma \frac{E_g^2}{4}}{1 + \sigma R_g}$$

$$\frac{4P}{E_g^2} = \frac{\sigma}{1 + \sigma R_g}$$

Let

$$\frac{4P}{E_g^2} = G$$

Solving for σ,

$$\sigma = G(1 + \sigma R_g)$$

$$\sigma = G + \sigma G R_g$$

$$\sigma(1 - GR_g) = G$$

$$\sigma = \frac{G}{1 - GR_g}$$

Because $\sigma = \frac{I_R}{V_R}$

then

$$I_R = V_R \left[\frac{G}{1 - GR_g}\right] = \frac{V_R 4P}{E_g^2 - 4PR_g}$$

APPENDIX D. Maximum Power Dissipation Allowable for a Given Thermal Resistance

The heat sink selected is a Wakefield (Delta Division #NC-423) type. This heat sink has a thermal resistance to air in convection cooling of 0.8°C/watt. Any heat sink with similar or lower thermal resistance is suitable.

The case-to-junction thermal resistance of the 2N3055 is rated at 1.5°C/watt, and the heat-sink-to-case thermal resistance is 0.5°C/watt maximum if a mica washer and DC340 filled grease or equivalent are used.

The total junction-to-air thermal resistance is:

Ambient to Heat Sink	0.8°C/watt
Heat Sink to Case	0.5
Case to Junction	1.5
TOTAL	2.8°C/watt

If it is assumed that the ambient temperature is 55°C and the junction temperature is 200°C,

$$200^{o}C - 55^{o}C = 145^{o}C$$
$$145^{o}C/2.8^{o}C/W = 52 \text{ watts}$$

If a 10-per-cent safety factor is allowed, the maximum allowable power dissipation by the pass transistor is 52 - 5 = 47 watts.

ACKNOWLEDGMENT

The authors wish to thank W. Williams and A. Cole for their helpful suggestions and comments.

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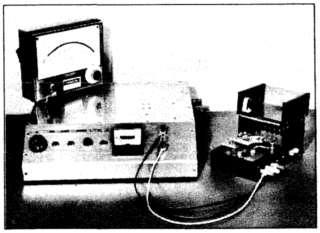


Testing for Forward-Bias Second Breakdown in Power Transistors

by D. A. Moe

The addition of "safe-operating-area" curves to power-switching transistor data for JEDEC registration and to manufacturers' data sheets has made necessary the development of non-destructive forward-bias second-breakdown test facilities. This Note describes the design of a test facility which determines the forward-bias second-breakdown safe operating locus for power transistors and shows detailed schematic diagrams of test circuits which can be used for devices with collector-current ratings up to 2.5 amperes and sustaining collector-to-emitter voltage $V_{CEO}(sus)$ ratings up to 300 volts, or with ratings to 5 amperes and 100 volts.

Causes of Second Breakdown

The safe operating area of a power transistor is bounded by a locus divided into four discrete segments, each representing a particular limiting condition. As shown in Fig. 1, the limiting factors are the maximum continuous-collector-current rating of the transistor, the maximum power-dissipation rating, second breakdown, and the sustaining voltage $V_{CEO}(sus)$ of the device.

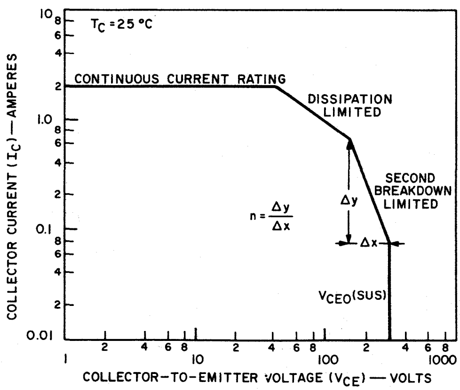


Fig. 1— A typical safe-operating-area curve.

Forward-bias second breakdown ($I_{S/b}$) in a power device is manifested by localized heating of the transistor pellet, as shown in Fig. 2. The average collector-junction temperature, T_J, of a power transistor may be calculated as follows:

$$T_J = T_C + P_{avg}\theta_{J\text{-}C}$$

where T_C is the case temperature in ^oC, P_{avg} is the average power dissipation in watts, and $\theta_{J\text{-}C}$ is the junction-to-case thermal resistance in ^oC per watt. However, the actual junction temperature can vary from point to point on the chip as a result of current-crowding that causes higher isolated dissipation. As a result, a localized thermal runaway may occur. In the forward-biased mode, such local heating is most likely to occur at the emitter edge because, under forward-bias conditions, lateral base current creates an electric field or voltage gradient in the base, as shown in Fig. 2. The direction of this voltage gradient causes greater forward bias at the emitter periphery than at the center. Therefore most injection occurs at the periphery, and the current density is greater. As the concentrated current flows across the depletion region, local power dissipation occurs and causes local heating. If the current density exceeds a

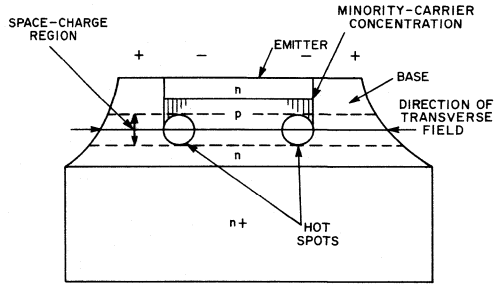


Fig. 2— Cross-section of a power transistor showing development of hot spots under forward bias.

critical level, the heat that is generated causes the local base-to-emitter voltage to decrease to a level that causes further injection, and collector-to-emitter current flow becomes regenerative. If this regenerative process is allowed to continue, device destruction follows. The current crowding may be aggravated by a non-homogeneous collector-base junction or by mounting-system imperfections such as solder voids.

A Second-Breakdown Test Facility

Fig. 3 shows a simplified schematic of a test set designed to determine the forward-bias second-breakdown safe operating locus for power transistors. This test facility is capable of determining this locus non-destructively, and therefore can be used to perform 100-per-cent tests of transistor capability in production without destroying transistors. This type of production test is usually made at one point of the second-breakdown locus shown on the published data. Determination of the second-breakdown limit for registration of a new device of a particular structure and geometry previously required the destructive finding of the $I_{S/b}$ limit of many individual transistors. Although each device would yield one data point, the points would not necessarily be on the same second-breakdown locus because the relative second-breakdown capability would vary from device to device. This procedure would therefore not yield accurate information about the actual shape of the $I_{S/b}$ locus. It has been found that the slope, n, of the forward-bias second-breakdown locus ($I = KV^{-n}$) plotted on log-log coordinates is essentially constant for a particular device structure and geometry.

The second-breakdown test set shown in Fig. 3 operates in either of two modes: "normal" operation or "shut-down" operation. There are two feedback drive amplifiers in the circuit. One drives the transistor under test to the magnitude of collector current programmed by adjustment of a potentiometer. The current-sensing feedback loop is arranged so that only actual collector current flows through the sensing resistor; no base current flows in the mesh common to that resistor. The second amplifier compares the collector-to-emitter voltage of a transistor in series with the one being tested to a reference voltage and maintains the pass-transistor voltage constant at six volts, independent of test-current magnitude.

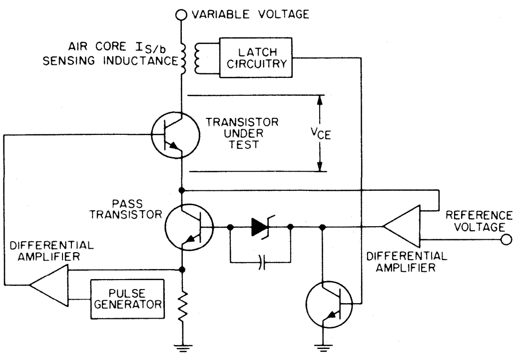


Fig. 3– Simplified schematic of test set for second-breakdown current ($I_{S/b}$).

The test voltage, V_{CE}, is varied by adjustment of the power-supply voltage across the transistor under test, the series pass transistor, and a one-ohm sensing resistor. During a normal test, the pulse generator applies an essentially square pulse of current through the transistor under test; the relatively short rise and fall times can be neglected. The current through the pass transistor tracks the current through the transistor under test. If the device being tested is operating within its safe area, no anomalies in transistor current or voltage occur and no degradation results during the test.

If the transistor is operated beyond its safe operating area, distinct changes occur in current and voltage at the initiation of second breakdown. The collector-to-emitter voltage of the transistor suddenly drops to a low value, while the current rises sharply. The second-breakdown test method shown in Fig. 3 takes advantage of this rapid rise in collector current.

For detection of second breakdown, an air-core inductor is placed in series with collector of the transistor under test. During normal operation of the test set, the voltage developed across this inductor is small because of the relatively long test-current-pulse rise time. During second breakdown, however, the rapidly rising collector current creates a high voltage across the inductor. A secondary winding then ac couples this voltage to a detection circuit which reverse-biases the series pass transistor. The inductive-detection approach is independent of test-current magnitude and reacts instead to the magnitude of its first derivative.

The 2.5-Ampere/300-Volt and 5-Ampere/100-Volt Test Circuits

Two forward-bias second-breakdown facilities are shown in Fig. 4. The first is capable of making second-breakdown tests at collector-current levels to 2.5 amperes and collector-to-emitter voltage levels to 300 volts; the second makes similar tests to 5 amperes and 100 volts.

In both facilities a voltmeter V is placed across the Current-Level-Adjust potentiometer during setting of the test conditions. The drive amplifier is disconnected so that no current flows through the transistor under test. The test transistor must not be preheated before the actual test voltage is applied because the second-breakdown limit decreases with increasing temperature. While the test is being performed, the voltmeter V is switched across the one-ohm sensing resistor and monitors actual test current.

A test is initiated by application of a pulse to the gate of a 2N3228 SCR, Q1, which begins to conduct and closes a mercury relay. A unijunction transistor fires to end the test. The pulse-width potentiometer can be varied to obtain test conditions varying from dc (2 seconds) to a short pulse (100 milliseconds). The setting of the Current-Level-Adjust potentiometer determines the amplitude of the test current during the pulse. The capacitor connected across this potentiometer maintains the rise time of the pulse applied to the differential-drive amplifier at approximately 25 milliseconds, as shown in Fig. 5. If the rise time were too short, the inductive detector would trigger the latch circuitry at the beginning of a pulse and would incorrectly indicate second breakdown.

The pass-transistor regulator maintains a constant voltage across the transistor under test. The series pass transistor is always operated in the active region so that it can turn off the transistor under test within one microsecond if second breakdown occurs.

The two differential amplifiers are stabilized by means of capacitors located at several points. Stabilization of these test facilities is difficult because they are required to perform tests on devices having gain-bandwidth products f_T up to 100 MHz and at all test currents and voltages within the test-set ratings. The problem is compounded by the fact that f_T is a function of collector voltage and current and may vary for individual devices at different test conditions.

Particular care is necessary in the physical layout of a second-breakdown test facility to avoid oscillation. High-frequency oscillations may then incorrectly appear to the inductive detector as second-breakdown failures and cause the protection circuitry to be triggered. Leads should be as short as possible.

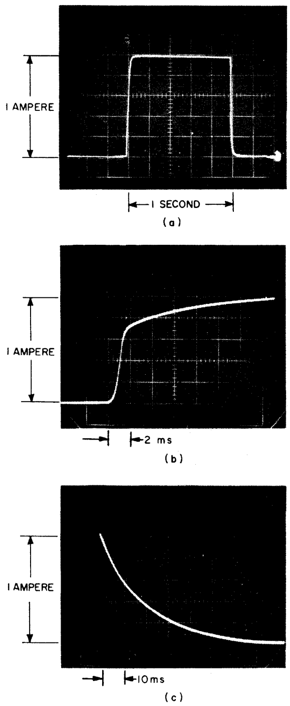


Fig. 5– Waveforms for $I_{S/b}$ test circuits of Fig. 4: (a) applied pulse; (b) turn-on time; (c) turn-off time.

In the event of second breakdown, the large current change di/dt causes a voltage to be coupled to the second-breakdown latch circuitry, Q24 and Q25. This regenerative circuitry drives the pass-transistor regulator, Q16, which then applies instantaneous negative voltage at the base of the pass transistor to interrupt the test current. A light on the front panel of the test set indicates second breakdown. The coupling capacitor in the reset circuitry for the latch is selected so that it cannot override a pulse from the second-breakdown-sensing transformer. If a shorted transistor is placed in the test socket and the reset button is depressed, the resulting instantaneous rise in primary current triggers the latch. Therefore, it is impossible to reset the facility with a shorted transistor in the socket. Although the primary inductance of the sensing transformer is very small, it helps to keep collector current from rising instantly during second breakdown. A diode clamp is employed to damp ringing voltages that might otherwise exceed the avalanche breakdown voltage of the transistor under test.

If the transistor under test has large leakage current, or if a slow thermal runaway occurs, the collector current does not rise fast enough to trigger Q24 and Q25. The latch is then triggered by back-up circuitry. The back-up circuit, which consists of Q21, Q22, and Q23, is a Schmitt trigger set to switch at a collector test current ten per cent higher than the rated value of the test facility. In this case, a relatively long time may be needed to exceed this rating.

Transistor Characterization for Forward-Bias Second Breakdown

Actual second-breakdown measurements for the RCA-2N5240 are shown in Fig. 6. The three curves indicate differences in second-breakdown capability at different case temperatures, but show that the second-breakdown loci have essentially identical slopes. The 2N5240 is a double-diffused triple epitaxial silicon power transistor having eight separate emitter sites. A small ballast is provided in series with each emitter to extend second-breakdown limits.

Characterization of a transistor for second breakdown and power handling is performed in two steps. First, the dc and pulsed power-dissipation capability of the device are calculated on the basis of its steady-state and transient thermal resistance. These curves are then checked empirically to determine at what value of collector-to-emitter voltage second breakdown begins to dominate.

To obtain a single point on the curve, the desired collector-to-emitter voltage V_{CE} is applied to the transistor under test, and a test is performed at a test-current magnitude below the expected capability of the device. If failure does not occur, the test-current magnitude is increased in steps until failure does occur. This procedure is repeated at several values of V_{CE}. During each trial, the transistor case must be at the temperature for which second-breakdown capability is being determined. Usually a

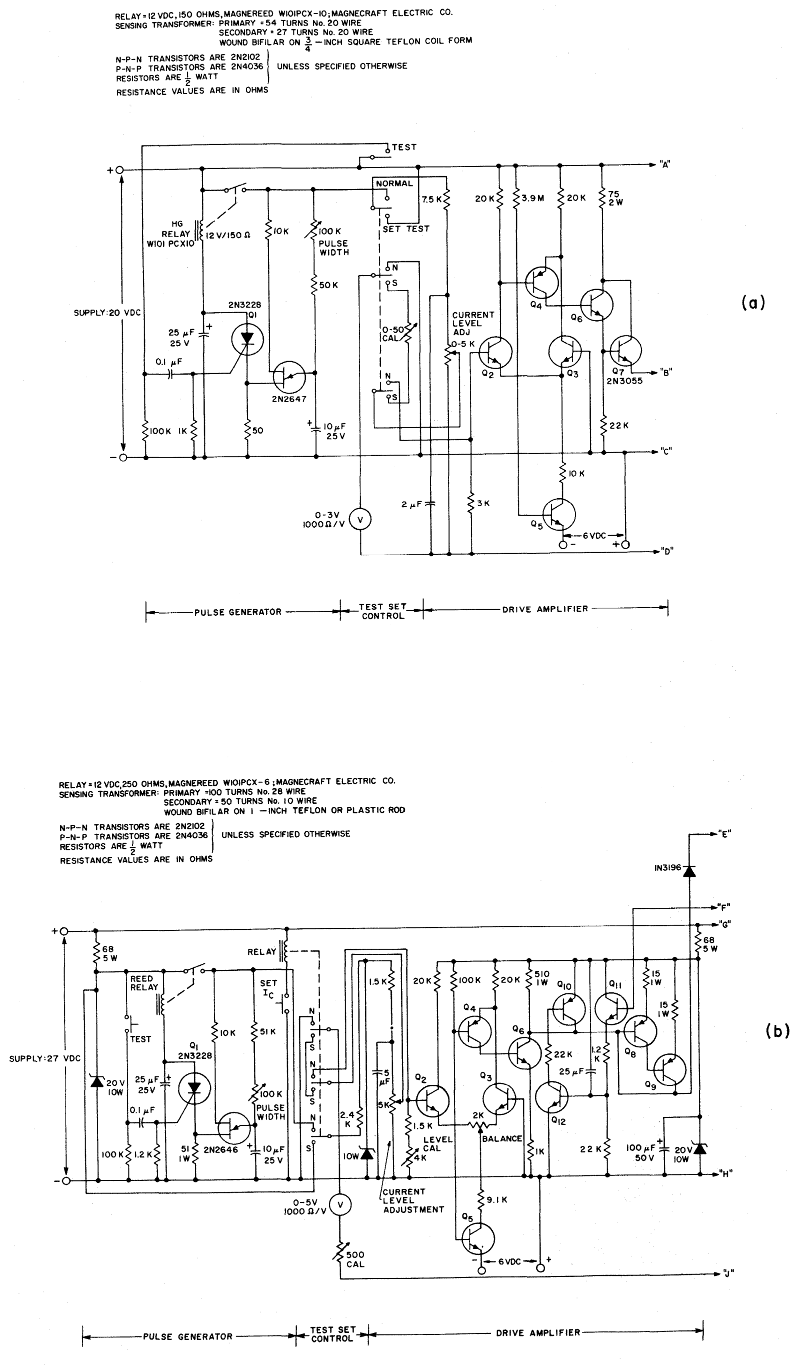
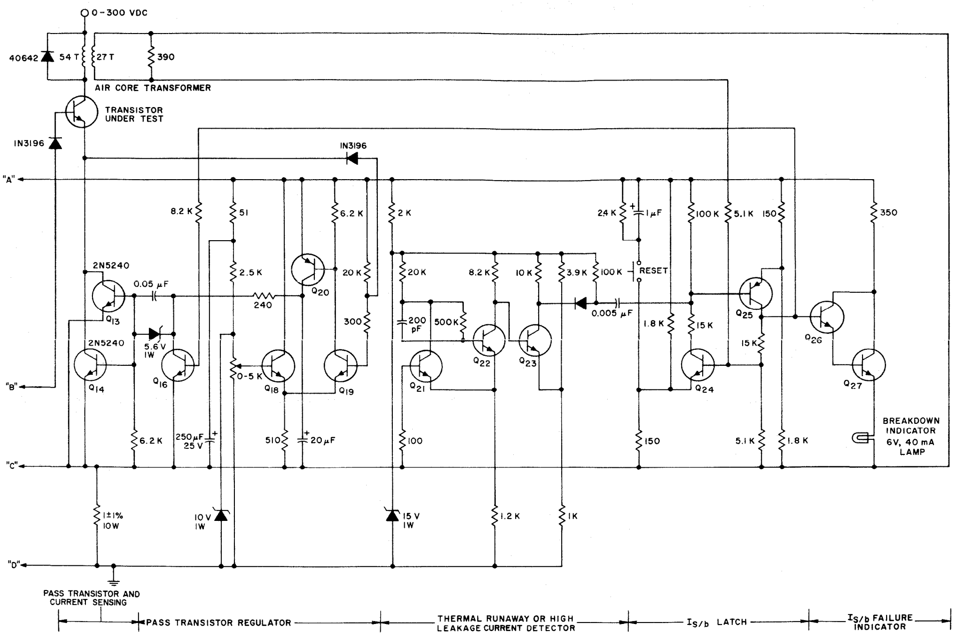


Fig. 4— Schematic diagram of $I_{S/b}$ test facilities for (a) currents to 2.5 amperes and voltages to 300 volts, and (b) currents to 5 amperes and voltages to 100 volts.

(a)



(b)

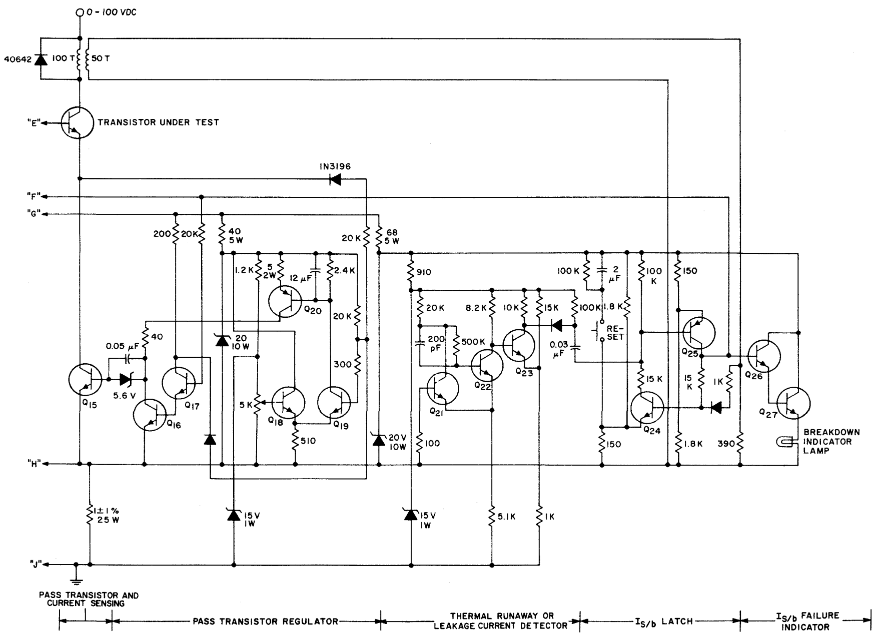


Fig. 4— Schematic diagram of $I_{S/b}$ test facilities for (a) currents to 2.5 amperes and voltages to 300 volts, and (b) currents to 5 amperes and voltages to 100 volts.

heat sink having a large thermal capacity is used. An approximate test for degradation may be made by repeating the second-breakdown test at the current level just preceding device failure; the device should pass this test. Another

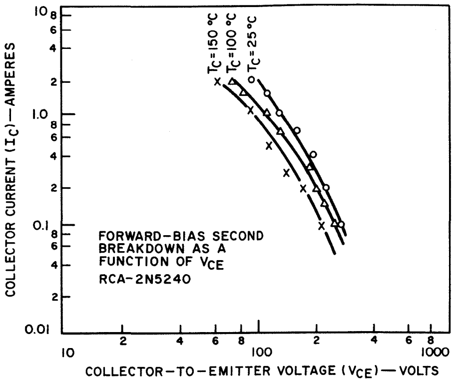


Fig. 6— Forward-bias second breakdown of RCA-2N5240 as a function of collector-to-emitter voltage for different case temperatures.

method is to measure changes in collector cutoff current I_{CBO} after second-breakdown failure.

The final second-breakdown curve plotted to characterize the device for registration, which is shown in the table of device characteristics on the data sheet, has a slope greater than that of the family of devices represented. To guarantee this published curve, a 100-per-cent test is performed in production at the $I_{S/b}$ specification point.

It should be noted that there is not an abrupt change in power-handling capability along the safe-area locus, but rather a gradual change in the slope of the curve. The slope becomes less at lower collector-to-emitter voltages because the electrical base width in the transistor varies as a function of voltage. As V_{CE} decreases, the depletion-region width decreases and the electrical base width increases. These changes have the effect of decreasing current density because the minority carriers in the base have a greater distance over which to diffuse outward laterally, as shown in Fig. 2.

RCA
Solid State Division

Power Transistors
Application Note

AN-4612

Thermal-Cycling Rating System for Silicon Power Transistors

by W. D. Williams

Thermal fatigue is a wear-out type of failure that may occur in silicon power transistors as a result of the thermal cycling produced by changes in power dissipation or in the ambient temperature. When a transistor is alternately heated and allowed to cool, cyclic mechanical stresses are produced within the device because of differences in the thermal expansion of the silicon pellet and the metallic materials to which the pellet is attached. In the past, the effect of such stresses has been almost completely ignored in the design of power-transistor circuits. The circuit designer should realize, however, that, just as a wire that is continuously flexed at one point will eventually break because of metal fatigue, cyclic thermal stresses can similarly lead to fatigue failures in power transistors.

This Note briefly analyzes the basic causes of thermal fatigue in silicon power transistors and describes a rating chart that makes it possible for a circuit designer to avoid such failures during the operating life of his equipment. Examples are provided on the use of this chart to determine the transistor operating conditions required to assure a desired thermal-cycling capability and to determine whether the thermal-cycling capability of a transistor is adequate for the requirements of a given application.

Analysis of Thermal Fatigue in Silicon Power Transistors

Power transistors are subjected to some thermal stresses in all practical circuits in which they may be employed. In many common applications, these stresses are very severe, as indicated by the examples of the thermal-cycling requirements of several typical applications listed in Table I. The cyclic stresses may eventually result in physical damage to the semiconductor pellet or the mounting interface.

In most silicon power transistors, the small silicon pellet is bonded to a copper header. The coefficient of thermal expansion for silicon (3×10^{-6}) is much less than that of copper (17.5×10^{-6}). Temperature variations within the transistor, therefore, result in cyclic stresses at the mounting interface of the silicon pellet and the copper header because of the difference in the thermal expansions of these parts. If a hard solder, such as silicon gold, is used to bond the pellet to the header, these stresses are transmitted to the silicon pellet. Silicon is relatively weak in tensile strength and is highly "notch sensitive." Such stresses therefore, often result in pellet fractures. In general, however, lead solder is used to bond the silicon pellet to the copper header. The cyclic thermal stresses then are absorbed by non-elastic deformation of the soft lead solder, and very little stress is transmitted to the pellet.

The continuous flexing that results from cyclic temperature changes in the transistor may eventually cause fatigue failures in the lead solder. Such failures are a function of the amount of change in temperature at the mounting interface, the difference in the thermal-expansion coefficients of the silicon pellet and the material to which the pellet is attached, and the maximum dimensions of the mounting interface.[1] Fatigue failures occur whenever the cyclic stresses damage the solder to the point at which the transfer of heat between the pellet and the surface to which it is mounted becomes impaired. This condition may exist in only a small portion of the pellet. This portion, however, overheats, and transistor failure results because of conditions that very closely approximate those encountered during second breakdown.[2]

Thermal-fatigue failures in power transistors are accelerated because of dislocation "pile-ups" that result from impurities in the lead solder.[3] RCA has developed a process that substantially reduces the amount of impurities introduced into the solder. Use of this proprietary "controlled solder process" (CSP) makes it possible to avoid the microcracks that propagate to cause fatigue failure in power transistors and, therefore, greatly increases the thermal-cycling capability of these devices.[4]

Thermal-Cycling Rating Chart

The mathematical relationship among the factors that affect fatigue failure in silicon power transistors can be expressed, in terms of the number of thermal cycles to failure N, as follows:[1]

$$N = Ae^{\psi_o / [\Delta T(\alpha_A - \alpha_B) L]}$$

Table I - Thermal-Cycling Requirements for Typical Applications of Power Transistors

Application	Circuit	P_T (W)	ΔT_C (°C)	Minimum Equipment Life Required (years)	Typical Thermal-Cycling Rating Required (cycles)
Auto radio audio output	Class A	8	75	5	5,000
	Class AB	2	45	5	5,000
Power supply	Series regulator	50	65	5	5,000
	Switching regulator	15	65	5	5,000
Hi-Fi audio amplifier	Class AB	35	50	5	5,000
Computer power supply	Series regulator	50	65	10	10,000
Computer peripheral equip.	Solenoid driver	5	5	10	1.3×10^8
Television	Vertical output	10	75	5	5,000
	Audio output	8	75	5	5,000
Sonar modulator	Linear amplifier	100	55	10	144×10^3

where A is a constant determined by the mounting system, ΔT is the change in temperature at the mounting interface, a_A and a_B are the thermal-expansion coefficients of the silicon and the metal under the solder joint, ψ_O is a material constant proportional to the change in temperature ΔT and the difference in the thermal-expansion coefficients a_A and a_B, and L is the maximum length of the solder joint under the pellet.

For a given transistor, the only variable in the thermal-cycling equation that can be controlled by the circuit designer is the change in temperature at the interface of the silicon pellet and the material to which the pellet is mounted. This change in temperature ΔT is, of course, less than the change in transistor junction temperature ΔT_J, but is greater than the change in case temperature ΔT_C.

RCA has devised a rating chart that relates the thermal-cycling capability of a silicon power transistor to total device dissipation and the change in case temperature. This chart is presented in the form of a log-log presentation in which power dissipation is shown on the vertical axis and the number of thermal cycles is shown on the horizontal axis. Rating curves are shown for various magnitudes of case-temperature swings. Fig. 1 shows an example of a typical rating chart of this type.

A circuit designer may use the rating chart to define the limiting value to which the change in case temperature must be restricted to assure that a power transistor is capable of operation at a specified power dissipation over the number of thermal cycles required in a given application. Conversely, if the power dissipation and the change in case temperature are known, the designer may use the rating chart to determine whether the thermal-cycling capability of the transistor is adequate for the application. These uses of the rating chart are illustrated by examples on the chart shown in Fig. 1.

The chart shows the thermal-cycling ratings for an experimental silicon power transistor that has a thermal

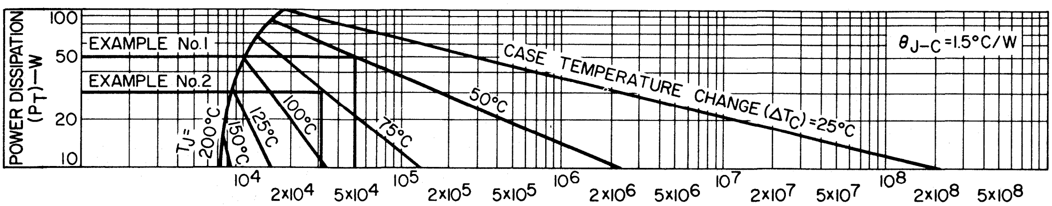


Fig. 1— Thermal cycling rating chart

resistance from junction to case of 1.5°C per watt. If a designer wishes to determine the maximum allowable change in the case temperature of this transistor for the thermal-cycling requirements of a given application, he simply plots the point of intersection of a horizontal projection of the total device dissipation with a vertical projection of the total number of thermal cycles required in the application. If this point lies exactly on one of the power-dissipation curves, the maximum allowable change in case temperature can be read directly from the chart; if not, the allowable temperature change can be approximated by linear interpolation. This use of the rating chart is illustrated by example No. 1 in Fig. 1.

For this example, it is assumed that the transistor is to be operated intermittently at a power dissipation level of 50 watts and that a thermal-cycling capability of 5.0×10^4 cycles is required to assure that the life of the transistor exceeds that of the equipment in which it is to be used. The point of intersection of line projections of the power dissipation and the required number of thermal cycles indicates that the change in case temperature must be restricted to a maximum value of 50°C per thermal cycle. This value determines the requirements of the transistor heat sink. If the thermal cycles are long in comparison to the thermal time constant of the heat sink, the total thermal resistance from case to ambient should not exceed 1°C per watt. If the thermal cycles are short relative to the thermal time constant, a higher thermal resistance is permissible provided that the thermal capacitance of the heat sink is sufficient to assure that the change in case temperature does not exceed 50°C during the thermal cycle.

Example No. 2 in Fig. 1 illustrates the use of the rating chart to determine whether the thermal-cycling capability of a transistor is adequate for a given application. In this example, a transistor dissipation of 30 watts and a case-temperature swing (measured) of 75°C are assumed. A vertical projection of the 30-watt point on the $\Delta T_C = 75°C$ power-dissipation curve indicates that, for these operating conditions, the transistor has a thermal-cycling rating of 3.2×10^4 cycles. If this rating is not adequate for the intended application, either the power dissipation must be reduced or a larger heat sink must be used so that a smaller change in case temperature will result during a thermal cycle.

In many applications, a power transistor may be subjected to thermal cycles that differ in both duration and magnitude. In such instances, the fractional amount of the thermal-cycling life of the transistor used by the total number of thermal cycles of each type during the required life of the equipment must be separately determined and then added together to ascertain whether the thermal-cycling rating of the transistor will be exceeded in the application. The ratio of the total number of cycles of each type to which the transistor will be subjected during the life of the equipment to the total number of cycles of the same type that the transistor is rated to withstand before fatigue failure is obtained for all the dissimilar thermal cycles. If the sum of these ratios is less than unity, the transistor is obviously operated within ratings in the application. If the sum is greater than unity, the thermal-cycling rating of the transistor is exceeded in the application, and device failure may occur during the operating life of the equipment.

The technique used to determine whether the thermal-cycling ratings of a transistor are exceeded in a specific application in which the transistor is subjected to different types of thermal cycles can be illustrated by use of the examples of different operating conditions shown in Fig. 1. If the transistor is assumed to be subjected to the conditions specified for examplele No. 1 for 2.5×10^4 thermal cycles and to the conditions specified for example No. 2 for 1.6×10^4 thermal cycles, the following summation is made to determine whether the transistor will be operated within its thermal-cycling ratings:

$$\frac{2.5 \times 10^4}{5.0 \times 10^4} + \frac{1.6 \times 10^4}{3.2 \times 10^4} = 1$$

This summation indicates that, for the conditions assumed, the transistor is operated exactly to the limit of its thermal-cycling rating.

The RCA thermal-cycling ratings allow a circuit designer to use silicon power transistors with assurance that no fatigue failures of these devices will occur during the operating life of his equipment. These ratings provide valid indications of the thermal-cycling capability of silicon power transistors for all types of operating conditions and, therefore, enable the circuit designer to "design out" the possibility of transistor thermal-fatigue failures.

Obviously, all power transistors cannot be tested to determine their thermal-cycling capability because such tests are expensive, time consuming, and destructive. The validity of the thermal-cycling ratings results from the application of stringent process controls at each step in the manufacture of the transistors and from the testings of a statistically significant number of samples. Thermal-cycling ratings for silicon power transistors provide the same type of assurance that a device will not fail when operated within ratings as that provided by the more familiar voltage, current, and second-breakdown ratings.

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RCA

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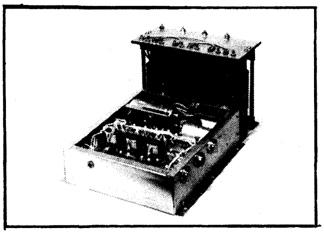
Power Transistors Application Note AN-4673



A 750-Watt Three-Phase Frequency Converter

by W. J. Beiswinger

Military equipment frequently uses three-phase 400-Hz power, and industrial plants and laboratories often require power at a variety of low frequencies. Ac-to-ac converters, driven from standard power lines, can be used to meet these requirements. This Note describes a frequency converter with output frequency from 380 Hz to 1250 Hz that delivers up to 750 watts of three-phase power at 120/208 volts rms. The circuit uses a three-phase bridge inverter supplied from a rectified ac line; the input can be single-phase or three-phase, 120 volts or 208 volts, at any frequency from 47 Hz to 1250 Hz. The RCA-2N5805 power transistor used in this converter is especially suited for power-switching circuits.

CIRCUIT DESCRIPTION

As shown in the block diagram of Fig. 1, the converter has four basic components:

- a power supply, which consists of a rectifier and a filter, to change the ac line power to dc power for the three-phase bridge inverter;
- the three-phase bridge inverter;
- three-phase logic and driver circuits to switch the transistors of the inverter in the proper sequence; and
- an output transformer.

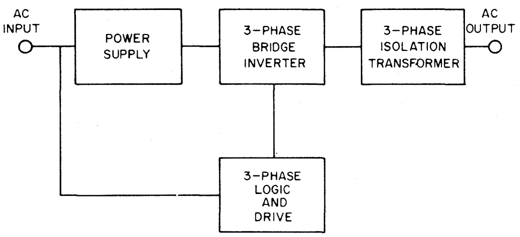


Fig. 1— Block diagram of 750-watt three-phase converter.

Fig. 2 is a schematic diagram that shows the power supply, inverter, and output transformer. The logic and driver circuits are shown in Figs. 3 and 4.

The Power Supply

The bridge rectifier will operate from either a single-phase or three-phase line; the circuit shown in Fig. 2, which uses 1N1204A rectifiers, is designed for either a 120-volt or a 208-volt line. The 11,000-microfarad filter capacitor keeps ripple below 50 millivolts even when a single-phase input line is used.

The Inverter

The three-phase bridge inverter uses pairs of RCA-2N5805 switching transistors that are transformer-driven from the logic circuit. The switching transistors in turn control the flow of current through the delta-connected primary of the output transformer.

The Logic and Driver Circuits

The logic and driver circuits include a low-voltage dc supply, which operates from a single phase of the ac line. A stepdown transformer reduces the line voltage to 12 volts, and provides isolation from the power line. This transformer, T4, has a frequency range from 47 Hz to 1250 Hz; its parameters are shown in Table I. The supply voltage is regulated by a pass transistor and a 12-volt zener diode.

The logic sequence begins with a tunable unijunction oscillator that delivers timing pulses to a six-stage ring counter, as shown in Fig. 3. The timing of these pulses is determined by the oscillator frequency; adjustment of the 75-kilohm potentiometer can set the frequency of the pulse sequence from 380 Hz to 1250 Hz. The output pulses from the ring counter are coupled to a diode matrix, shown in Fig. 4, to activate the inverter drive transistors.

The drive transistors provide drive to the inverter through transformers T1, T2, and T3. The first timing pulse produces a positive voltage across one half of the primary of T1, a negative voltage across one half of the primary of T2, and a

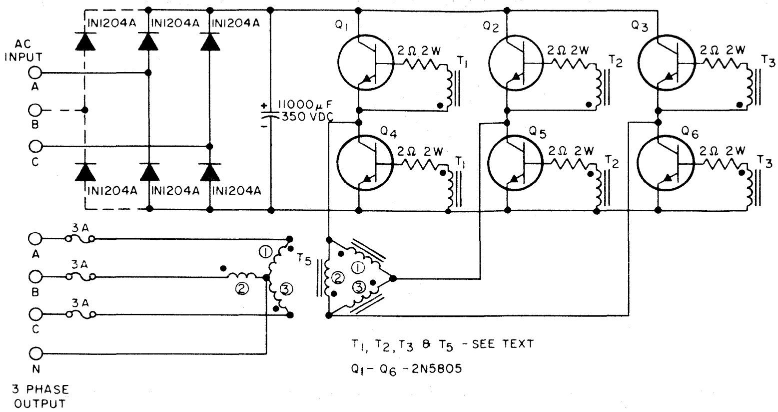


Fig. 2— Schematic diagram of three-phase frequency converter, showing the dc supply, the inverter, and the output transformer.

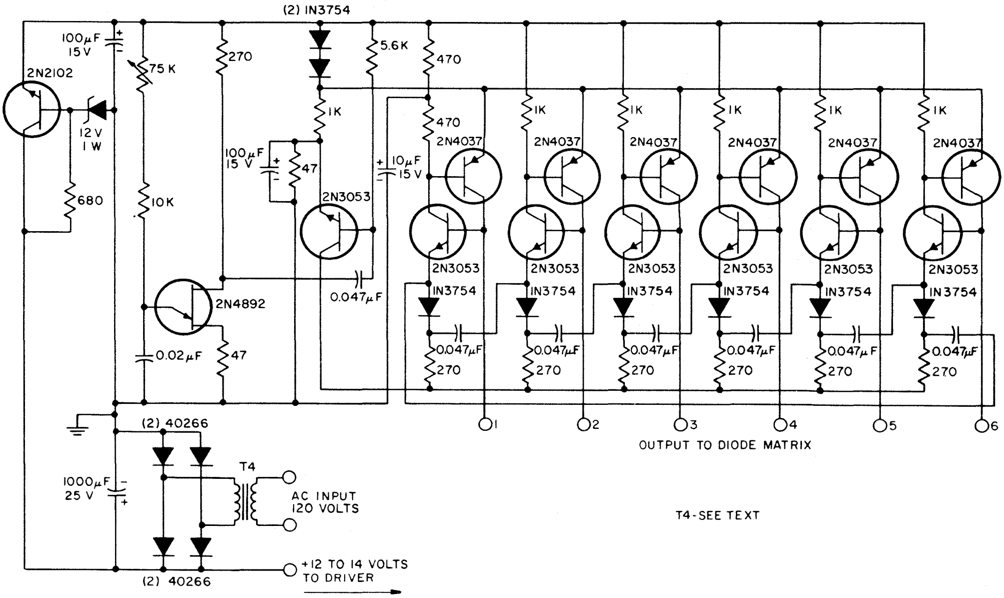


Fig. 3— Oscillator and six-stage ring counter for the logic circuit of the three-phase frequency converter.

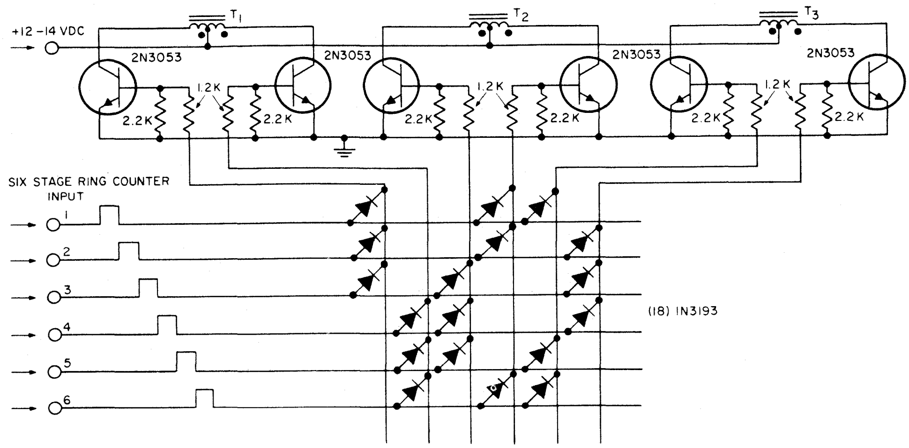


Fig. 4— Diode matrix and driver for output devices of three-phase frequency converter.

Table I — Stepdown Isolation Transformer for Logic Circuit Supply

CORE	– Square Stack 75EI Microsil (0.006) Magnetic Metals Co. 75EI3306
PRIMARY	– 120 Volts 1200 Turns #32 Wire 100 Turns Per Layer 12 Layers
SECONDARY	– 12 Volts 128 Turns #22 Wire 32 Turns Per Layer 4 Layers

Table II — Pulse Polarities at Primary Coils of T1, T2, and T3

Pulse	V_{T1}	V_{T2}	V_{T3}
1	+	–	+
2	+	–	–
3	+	+	–
4	–	+	–
5	–	+	+
6	–	–	+

positive voltage across one half of the primary of T3; the second timing pulse produces a positive voltage across one half of the primary of T1, and a negative voltage across halves of the primaries of T2 and T3; and so forth. The sequence of these voltages is tabulated in Table II and displayed graphically in Fig. 5 to show that the periodic voltages across the three transformers are offset by 120-degree intervals.

Design information on transformers T1, T2, and T3 is shown in Table III.

The Output Transformer

The output transformer, T5, isolates the output circuit from the power line, transforms the voltage up or down to produce a 120/208-volt output, and reduces harmonic distortion. The primary is delta-connected, and the secondary is wye-connected to provide three-phase, four-wire service.

The primary coils carry the full supply voltage. The waveshapes in the primary and secondary coils are the same, and are shown in Fig. 6; the polarities of these pulses are

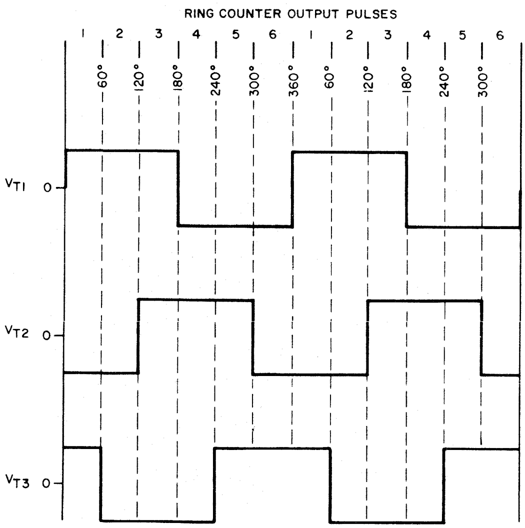
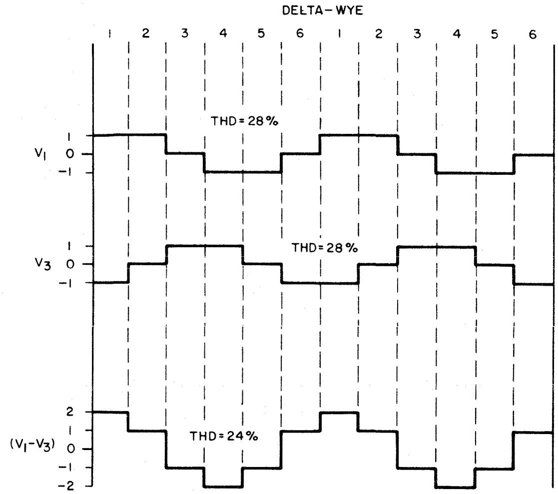


Fig. 5— Sequence of voltages across drive transformers T1, T2, and T3.



1	V1 − V3 = 1 − (−1) = 2
2	V1 − V3 = 1 − 0 = 1
3	V1 − V3 = 0 − (1) = −1
4	V1 − V3 = −1 − (1) = −2
5	V1 − V3 = −1 − 0 = −1
6	V1 − V3 = 0 − (−1) = 1

Fig. 6— Phase-to-neutral and phase-to-phase voltages in the delta-wye output transformer.

shown in Fig. 7. The manner in which the secondary coil voltages add to reduce distortion is also shown in Fig. 6. The voltage across secondary terminals A and C is equal to the difference of the voltages in secondary coils 1 and 3. Subtraction of waveform V3 from waveform V1 results in the output waveform (V1 - V3), which is more sinusoidal than V1 or V3. The measured value of total harmonic distortion (THD) in each coil is 28 per cent; the THD across the output terminals is 24 per cent.

Table III — Driver Transformer Design Information

CORE	— Square Stack 21EI Microsil (0.006) Magnetic Metals Co. 21EI3306
PRIMARY	— 14 Volts 140 Turns Bifilar #29 Wire (in Series) 20 Turns Per Layer 7 Layers
SECONDARY	— 4 Volts 52 Turns Bifilar #29 Wire 13 Turns Per Layer 4 Layers

Design information for the output transformer to operate from a 120-volt line or a 208-volt line is given in Table IV.

Table IV — Output Transformer Design Information

CORE	— Square Stack 1.2EI3ϕ Microsil (0.006) Magnetic Metals Co. 1.2EI3ϕ3306
PRIMARY (DELTA)	— 120 Volts 188 Turns #17 Wire 47 Turns Per Layer 4 Layers
	OR
	— 208 Volts 325 Turns #19 Wire 55 Turns Per Layer 6 Layers
SECONDARY (WYE)	— 120/208 Volts 200 Turns #17 Wire 50 Turns Per Layer 4 Layers

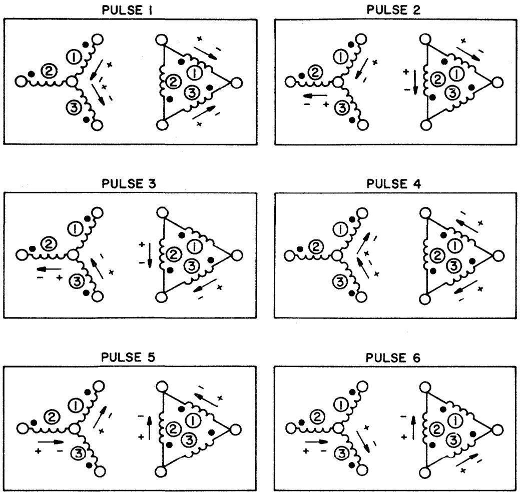


Fig. 7— Pulse polarities in output transformer T5.

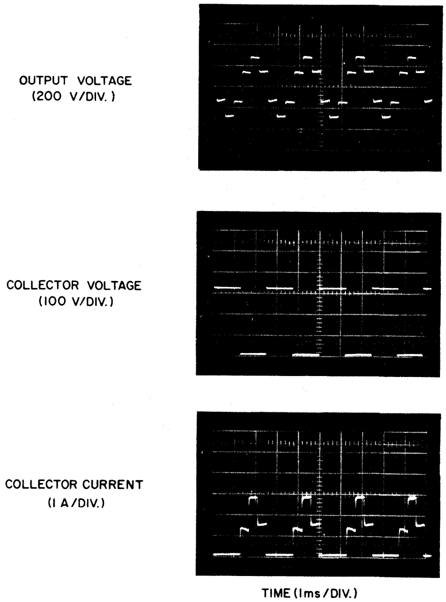


Fig. 8— Waveforms of transformer output voltage, collector voltage, and collector current.

CONVERTER PERFORMANCE

A photograph of the output waveform from the 400-Hz converter is shown in Fig. 8. Waveforms of the collector voltage and current in one of the switching transistors (Q1) are also shown in Fig. 8.

Fig. 9 shows the output performance of the converter. Both the efficiency and the regulation are good. Efficiency rises from 50 per cent at low load current to 75 per cent at the rated load current of 2.1 amperes. The rms output voltage varies by only 10 volts between low- and high-current loading.

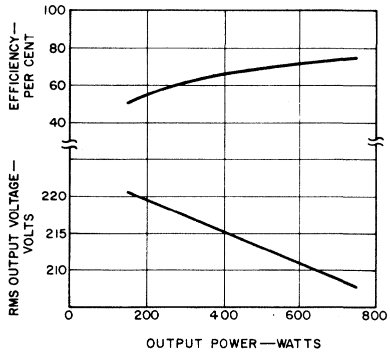


Fig. 9— Performance characteristics of the three-phase converter.

Solid State Division

Power Transistors

Application Note AN-4783

Thermal-Cycling Ratings of Power Transistors

by V. J. Lukach, L. J. Gallace, and W. D. Williams

SUMMARY

This Application Note discusses a testing program used to determine the capability of a particular power transistor design for withstanding thermal cycling over a wide range of operating conditions. A sufficient number of tests were performed to verify a rating chart which can be applied by an equipment designer to any practical operating condition. The discussion covers a brief description of thermal fatigue, a method of "scaling the environment" to determine the proper test conditions, specialized test equipment and techniques to insure that the proper stresses were applied to the transistor, and the test results and the transistor predicted capability chart.

INTRODUCTION

Thermal fatigue is a wearout failure mechanism in silicon power transistors caused by repeated temperature cycling from either changes in power dissipation or ambient temperature differences. In a transistor where the silicon die is mounted with lead-tin or other "soft" solder, a failure normally occurs because of a degradation of the joint between the silicon die and the surface to which it is mounted. This degradation results in localized overheating and eventual localized thermal runaway. The failure mode is very similar to that encountered in forward-biased second breakdown[1]. In many cases where the current is not limited during the resulting short circuit, the transistor chip is destroyed and it is impossible to determine what caused the failure.

In a transistor mounted with a gold-silicon eutectic or other "hard" solder, the failure due to thermal fatigue usually occurs from fracturing of the silicon die, which often also results in a shorted transistor and destruction of the silicon die.

The causative factors in thermal fatigue and device design methods of alleviating it have been covered in the literature[2]. A system of rating a power transistor to clearly delineate thermal-cycling capability was described in an earlier Application Note[3]. This Note describes a testing program to determine whether the rating chart computed by use of the theory suggested in the above references truly represents the capability of a silicon power transistor over a wide range of stress levels.

THERMAL-FATIGUE BACKGROUND

In almost any application, a silicon power transistor is subjected to some cyclical thermal stress. Often this stress is quite severe and frequent. Table I shows some typical applications of power transistors and the expected thermal-cycling-life requirements. The number N of cycles to failure in terms of the device characteristics and operating conditions has been expressed as[2]

$$N = Ae^{\frac{\psi_o}{\Delta T (a_1 - a_2)L}}$$

where A and ψ_o are constants for a given power transistor structure, (a_1-a_2) is the difference in thermal coefficient of expansion between the silicon die and the material on which it is mounted, L is the maximum dimension of the silicon chip, and ΔT is the change in temperature at the interface between the silicon chip and the material to which it is mounted. In practical applications, the temperature swing at this interface is the sum of the case-temperature change and the temperature rise equal to the thermal resistance between the interface and the case multiplied by the power dissipation.

By use of these relationships, and a small amount of empirical data, a thermal-cycling rating chart was drawn for the RCA-2N3055 power transistor, as shown as Fig. 1. Verification and/or correction of this rating chart was one purpose of the testing program described in this Note.

TEST PROGRAM

Objectives

There were multiple objectives in this program. First was the determination of thermal-fatigue capability for the RCA-2N3055. Second was the mathematical representation

Table I – Thermal-Cycling Requirements for Typical Applications of Power Transistors

Application	Circuit	P_T (W)	ΔT_C (^oC)	Minimum Equipment Life Required (years)	Typical Thermal-Cycling Rating Required (cycles)
Auto radio audio output	Class A	8	75	5	5,000
	Class AB	2	45	5	5,000
Power supply	Series regulator	50	65	5	5,000
	Switching regulator	15	65	5	5,000
Hi-Fi audio amplifier	Class AB	35	50	5	5,000
Computer power supply	Series regulator	50	65	10	10,000
Computer peripheral equip.	Solenoid driver	5	5	10	1.3×10^8
Television	Vertical output	10	75	5	5,000
	Audio output	8	75	5	5,000
Sonar Modulator	Linear amplifier	100	55	10	144×10^3

of this capability in various tables and on appropriate charts. Finally, since thermal-fatigue rating charts were theoretically generated, independent appraisal and statistical approaches were used to compare the predicted response with the actual response.

Experimental Design

Because of the interrelationships among variables, this study requires a nonclassical approach. A thermal-fatigue test is basically a cyclical operating-life test. Fig. 2 shows one of the life-test racks used in this program. It accommodates 40 transistors and allows as many as four different thermal-fatigue tests simultaneously. Eight fans cool the units quickly during the "off" cycle. The photograph shows a free-air test; however, the plug-in sockets can be removed and devices on heat sinks or devices of another configuration substituted. Monitoring jacks are available on the front panel. The connections to the power supplies are not shown. Timers and relays are manually set for a variety of on/off conditions. The test circuit, shown in Fig. 3, is a common-emitter circuit that permits a smaller-current base power supply to be used. A common-base circuit could also be used. For room-

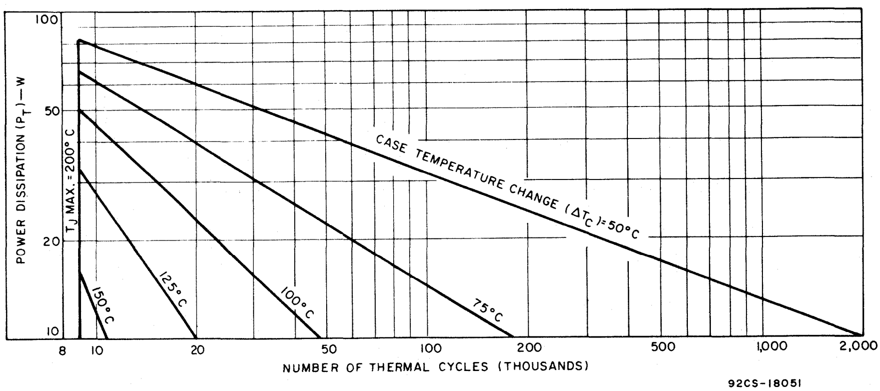


Fig. 1– Thermal-cycling rating chart for the RCA-2N3055 power transistor.

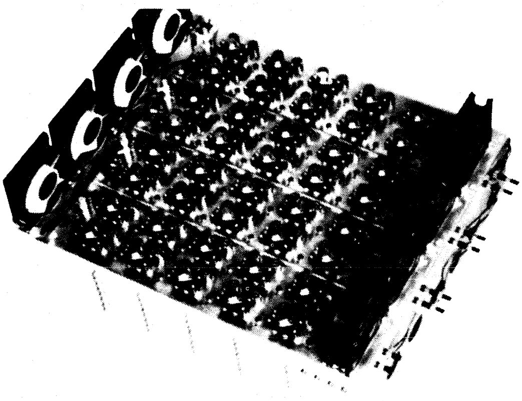


Fig. 2— Thermal-fatigue test rack.

ambient testing, the input variables include the heat-sink size, on/off cycle time, and power dissipation (collector-emitter voltage and collector current, V_{CE} and I_C). The response variables are the change in case temperature ΔT_c, and maximum junction temperature $T_{j(max)}$. The final response, of course, is the effect on the device, whether it be an open, short, or a change in an electrical parameter. Some of these variables are independent and some dependent. For example, with a given heat sink and cycle time, a change in power dissipation P_T will change both ΔT_c and $T_{j(max)}$. It is impossible to preset levels of these variables and achieve these conditions. This key point prevents utilization of a factorial design in a classical statistical approach.

The interdependency of some of the variables requires a complex preliminary set of experiments *before* the performance of a thermal-fatigue test on product capability. This preliminary work is called "scaling the environment". In the case of the 2N3055 transistor, it was necessary to determine 150 practical test (sampling) points that naturally exist when the bounds of the above-mentioned variables are considered. Table II shows parameter values for some of the 150 empirically derived test cells. From this data, test cells

Table II – Scaling the Environment

V_{CE} (V)	I_C (A)	P_D (W)	On/Off Time (Sec.)	Heat Sink	$T_{j(max.)}$ (°C)	ΔT_{case} (°C)
17	1	17	100/200	H_0	188	150
17	1	17	180/180	H_0	230	190
30	1	30	50/130	H_0	190	145
27	1	27	50/130	H_0	178	125
30	1	30	50/130	H_0	235	170
30	1.4	41	100/200	H_1	200	145
30	1	30	100/200	H_1	165	120
27	1	27	150/300	H_2	150	100
28	2	56	15/25	H_1	150	50
33.3	3	100	50/100	H_3	170	80
33.3	3	100	100/150	H_3	185	100
5	1	5	50/100	H_0	70	32
10	1	10	100/200	H_1	80	58
35	2	70	180/180	H_3	155	86
7.5	1	7.5	180/180	H_1	154	113
10	1	10	300/300	H_2	92	63
45	2	90	50/100	H_3	150	93
30	1	30	600/600	H_3	103	61
10	1	10	300/300	H_0	223	130
5	1	5	150/300	H_2	54	43

H_0 = Free air
H_1 = 11°C/W thermal resistance
H_2 = 6.3°C/W thermal resistance
H_3 = 1.3°C/W thermal resistance
Thermal resistances of heat sinks are steady-state values
$T_{j(max)} = T_{c(max)} + \theta_{j\text{-}c}P_D$
$(\theta_{j\text{-}c} \approx .5°C/W)$

were selected to give sizable spread to the primary variables, P_T ($V_{CE} \cdot I_C$) and ΔT_c. The points chosen are shown on the theoretical rating chart of Fig. 4. Many of the points are outside of the projected safe area. This fact illustrates another consideration in the total study, time. To minimize testing time and still generate meaningful data, a form of accelerated testing was built into the program. The usual precautions were employed in utilizing accelerated testing; i.e., failure analysis and data analysis were used to verify the existence of a true acceleration and to assure that failures had not been created that had no correlation with a bearing on the more typical lower stress levels.

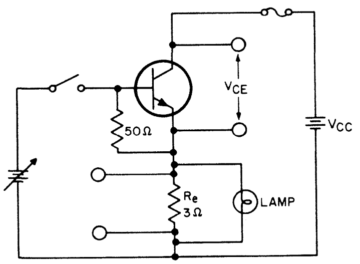


Fig. 3— Test circuit.

Data

Table III is a tabulation of the data obtained from the 2N3055 thermal-fatigue rating program. Fig. 5 is a graphical representation of the cycles-to-failure for each test group. A visual examination of the data indicates that devices tend to fail sooner on tests with large ΔT_c and high junction temperatures, as expected.

Table III – 2N3055 Thermal-Fatigue Ratings

No. of Devices	Power (W)	Heat Sink	T_c (°C)	ΔT_c (°C)	$T_{j(max.)}$ (°C)	Cycle Time (sec.) On	Cycle Time (sec.) Off	Cycles @ Down Period	Cumulative Cycles	Catastrophic Failures
20	17	H_0	30 to 180	150	188.5	100	200	35,952	43,032	1 @ 2000 hrs. 2 @ 40,207 hrs.
20	17	H_0	30 to 220	190	228.5	180	180	30,525	36,442	1 @ 20,719 hrs. 1 @ 22,185 hrs. 1 @ 28,266 hrs. 1 @ 34,672 hrs.
20	30	H_0	35 to 180	145	195	50	130	52,851	72,061	1 @ 50,989 hrs. 1 @ 60,138 hrs. 1 @ 68,701 hrs. 1 @ 69,185 hrs.
20	27	H_0	40 to 165	125	178.5	50	130	53,402	72,479	1 @ 11,520 hrs. 1 @ 40,003 hrs.
20	30	H_0	50 to 220	170	235	50	130	18,698	70,564	1 @ 6036 hrs. 2 @ 11,808 hrs. 1 @ 18,703 hrs. 1 @ 36,846 hrs. 1 @ 62,616 hrs.
20	30	H_1	35 to 150	120	165	100	200	14,702	70,901	1 @ 65,200 hrs.
20	41	H_1	35 to 180	145	200.5	100	200	14,702	41,668	1 @ 449 hrs. 1 @ 1400 hrs. 1 @ 19,917 hrs. 1 @ 25,157 hrs. 1 @ 32,334 hrs. 1 @ 32, 642 hrs.
20	27	H_2	30 to 135	105	148.5	150	300	12,274	62,395	1 @ 50,100 hrs.
20	56	H_2	70 to 120	50	148	15	25	231,202	264,675	1 @ 8500 hrs. 1 @ 10,480 hrs. 1 @ 144,632 hrs. 1 @ 241,379 hrs.

H_0 = Free air (30°C/W)
H_1 = 11°C/W
H_2 = 6.3°C/W

Failure Analysis

The basic failure analysis procedure for all failing devices was as follows:

1. Electrical test
2. Leak test (Helium and freon bubble)
3. Gas Analysis (Mass spectrometer)
4. Decap unit
5. Electrical test
6. Visual inspection
7. Remove silicone conformal coating
8. Retest electrically
9. Remove solder
10. Cross section
11. Check pellet-to-header bond
12. Photograph results

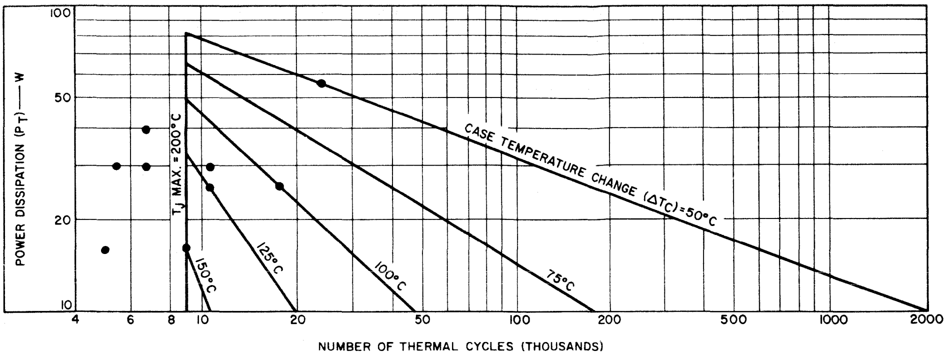


Fig. 4— Theoretical rating chart.

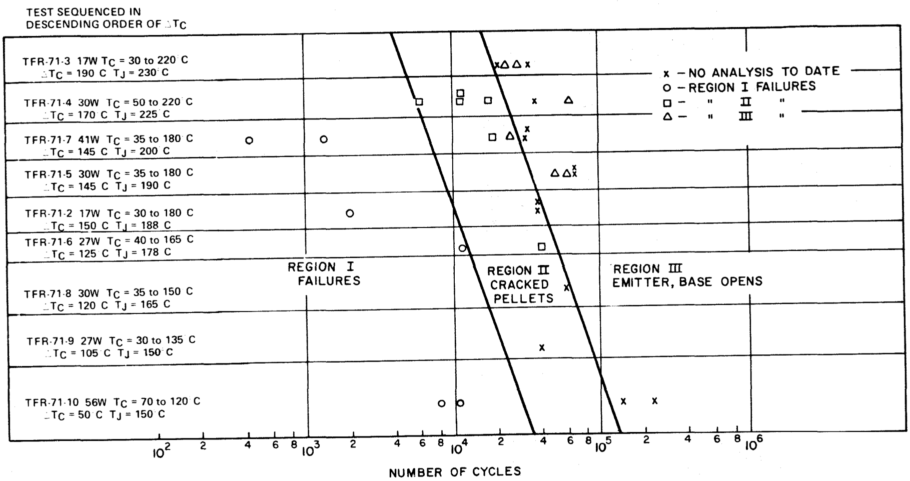


Fig. 5— Graphical representation of the cycles-to-failure number for various test groups.

Three basic types of failures were found in the analysis of failing devices using this procedure. These types were categorized as follows:

1. Non-controlled-solder-process* failures, Region I
2. Cracked pellets in Region II
3. Open emitter and base contacts (solder fracture) and nickel delamination on both collector and emitter-base side of pellet, Region III

*The controlled solder process is a proprietary process developed by RCA.

Corrective action has eliminated failures in Region I; such failures will not be discussed further. Figs. 6 and 7 illustrate the types of failures encountered in Regions II and III.

The cracked-pellet failures presented the problem of determining whether the silicon chip was cracked during assembly or as the result of thermal stresses. Analysis indicated that the cracks occur at points where high pressure is applied during assembly or where pellets are located over a solder void. Such failures are not expected to occur in devices using the controlled-solder-process solder system where the total strain of the system is taken up by the solder.

The third category of failures, open emitter and base contacts and pellet lifting, occurs very late in the cycle life of the device and is probably the only real wearout mechanism encountered in the test program. The interfaces between the emitter, base, and collector contacts consisting of nickel-lead/tin materials expand and contract at different rates during thermal cycling, and, consequently, strain occurs. Because of the difference in the coefficients of expansion of these materials, an appreciable amount of shearing takes place and causes fatigue failure at the contact point.

Curve Fitting – Predictive Model

In determining the number N(y) of cycles to first failure, it is assumed that a function exists and that the form of the function depends upon the measurable variables, as follows:

$$N(y) = f(\Delta T_C, \text{Power}, T_{j(max.)}, \text{Cycle Time } \theta_{h\text{-}s})$$

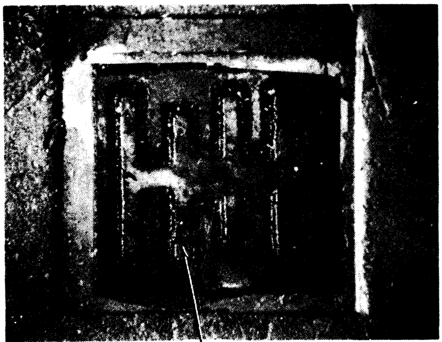


Fig. 6– Pellet showing failure as the result of a crack.

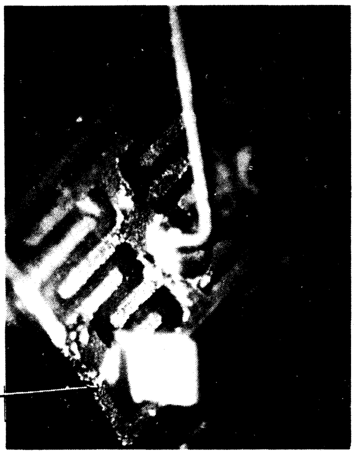


Fig. 7– Pellet showing failure as the result of an open base.

Regression analysis techniques are used to minimize the estimation error; the method of least squares is employed for multiple regression, i.e.

$$S = \sum_{i=1}^{n} (N_i - \hat{N}_i)^2$$

is minimized; N_i is the actual value of failing cycles and $\hat{N}_i$ is th calculated value of cycles.

Because a functional exponential model exists from th previous theory and because the experimental data imply that an exponential model should be fitted by the regressio equation, the following relation is postulated:

$$N(y) = \exp.^{(C_1 \Delta T_c + C_2 \Delta T_{j(max.)} + C_3 P_D + C_4 \theta_{h\text{-}s} t_r + \text{error}}$$

vhere ΔT_C is the case-temperature swing, $T_{j(max.)}$ is th maximum junction temperature, t_r is the ratio of "on" tim t_{on} to "off" time t_{off}, P_D is the applied power, $\theta_{h\text{-}s}$ is th thermal resistance of the heat sink, and error is approximatel normal $(0, \sigma^2)$

The coefficients of this equation should be highl correlated so that prediction will be restricted to the spac from which the data were derived. The correlation matrix Table IV, shows that the "independent" variables are highl correlated. This correlation illustrates the problem c designing the experiment in the classical manner, a mentioned in an earlier section.

Table IV – Correlation Matrix

	N	ΔT_J	$T_{j(max.)}$	P	$\theta_{h\text{-}s} \times t_r$
N	1	-0.89	-0.74	0.688	-0.52
ΔT_J		1	-0.928	-0.66	0.724
$T_{j(max.)}$			1	-0:42	0.702
P				1	-0.72
$\theta_{h\text{-}s} \times t_r$					1

Table V shows the data used in the regression analysi No Region I failures are used in the regression analysis sinc they have been eliminated on future product throug corrective action.

Following modified step-wise regression procedures, th equation that best fits the data is $Y = 724e^{-.02\Delta T_j}$, wher $\Delta T_j = \Delta T_c + P_D (\theta_{j\text{-}c})$. Because the present data are limite especially between the ΔT_c range of 50 and 125°C, furth data and more analyses may result in slight modifications c this equation. Fig. 8 is a plot of the data and equation.

Table V – Data Used in the Regression Analysis

Power (W)	ΔT_j (°C)	ΔT_c (°C)	$T_{jmax.}$ (°C)	t_r	$\theta_{h\text{-}s} \times t_r$ (°C/W)	Y (First Failure Kc)
17	158.5	150	188	$\frac{100}{200} = 0.5$	15	40,207
17	198.5	190	230	$\frac{180}{180} = 1$	15	20,719
30	160	145	195	$\frac{50}{130} = 0.375$	11.2	50,989
27	138.5	125	178	$\frac{50}{130} = 0.375$	11.2	40,003
30	185	170	235	$\frac{50}{130} = 0.375$	11.2	6,036
30	135	120	165	$\frac{100}{200} = 0.5$	5.5	65,200
41	165.5	145	200	$\frac{100}{200} = 0.5$	5.5	19,917
27	118.5	105	150	$\frac{150}{300} = 0.5$	3.15	50,100
56	78.0	50	150	$\frac{15}{25} = 0.6$	3.8	144,632

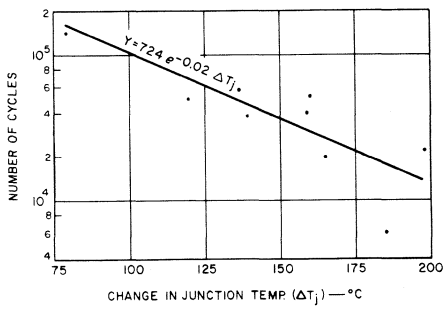


Fig. 8– Plot of change in junction temperature as a function of number of cycles.

CONCLUSIONS

There are a variety of causes for thermal-fatigue failures. Region I failures were completely corrected by the controlled solder process. Region II cracked-pellet failures are a function of mounting techniques and process control. Region III failures represent a wearout mechanism which occurs well beyond the normal use of the device.

Empirical determination of thermal-cycling capability is a long and difficult process requiring specialized equipment and techniques. At present, the prime factor affecting thermal-cycling capability is change in junction temperature, $\Delta T_j = \Delta T_c + (P_D \times \theta_{j\text{-}c})$. The RCA-2N3055 power transistor has demonstrated a thermal-fatigue capability far in excess of theoretically postulated values published in the thermal-fatigue rating chart.

ACKNOWLEDGMENT

The authors acknowledge the contributions made in "scaling the environment" by F. Wehrfritz.

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RCA Solid State Division

Power Transistors

Application Note AN-6145

A Test Set for Nondestructive Safe-Area Measurements Under High-Voltage, High-Current Conditions

R. B. Jarl

Techniques for determining the safe operating area of power transistors at moderate voltages, currents, and dc conditions have been available for some time. Circuitry for accomplishing this task nondestructively has also been available. A more difficult task has been to test devices nondestructively at high voltage/ampere products under pulsed and repetitive-pulsed conditions which more closely simulate the electrical environment in an actual equipment. The usual method has been to use a statistically significant sample and to test the devices to destruction to produce a rating curve. Then, by comparing the point of failure of the sampled units to the results of the dc tests, the pulse rating of the units is correlated to the dc tests. Because this procedure is obviously rather imprecise, users needing devices with high levels of reliability frequently require that devices be 100-per-cent tested to specific voltage, current, time, and duty-cycle conditions. This testing may be performed in a "sudden death" circuit where inadequate units are destroyed. However, this situation is unsatisfactory, both analytically and economically.

This Note describes a test equipment designed to perform the tests described above, for the most part, nondestructively. A photograph of the interior of the equipment and the control panel is shown in Fig. 1; an enlargement of this photograph is shown in Fig. 9, page 7. The equipment has a current range of 200 milliamperes to 20 amperes, a voltage range of 10 volts to 350 volts, a pulse width of 10 microseconds to two seconds, and a pulse repetition rate limited only by external equipment restrictions.

System Philosophy

As shown in the block diagram of Fig. 2, the transistor under test, TUT, is connected in a common-base configuration modified by a series base diode. V_{CC} is applied, and the TUT emitter is then driven by a constant-current source which is

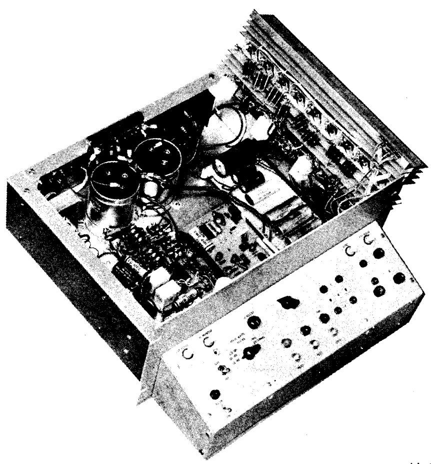

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Fig. 1– Interior and control panel of test equipment. (See Fig. 9, page 7, for enlarged photograph.)

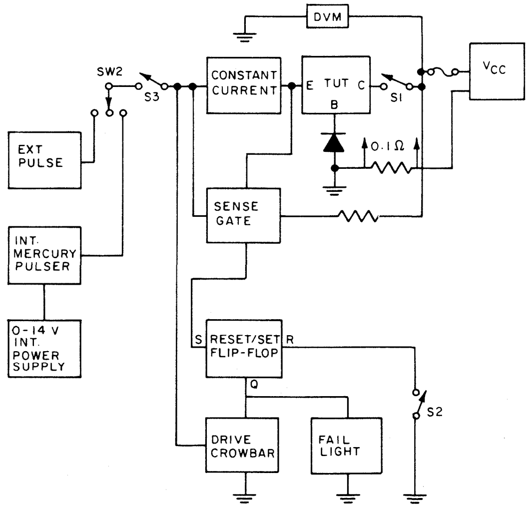

Fig. 2– Block diagram of test equipment.

driven, in turn, by a large-signal pulse generator, such as an HP 214A, or a mercury-wetted relay pulser. Voltage at the TUT emitter is monitored by a sensing network and a high-speed, bistable flip-flop. The collector of the TUT is tied to a V_{CC} supply appropriately filtered for high-current/fast-rise-time loads.

A device failure is observed as a sudden increase in voltage at the emitter of the TUT, which normally holds at a voltage, below ground, equivalent to twice the drop across the series base diode. A +3-volt, 50-nanosecond change is sufficient to switch the state of the flip-flop. The flip-flop then turns on a crowbar circuit which shorts out the voltage drive to the emitter current source. When the emitter current becomes less than the collector current, the series base diode becomes back-biased and opens the base-collector loop. The total shutdown procedure takes less than 0.5 microseconds.

System Design

The system is made up of seven "building blocks":

1. The V_{CC} power supply and filters
2. The V_{EE} power supply and filters
3. The pulse-timing block
4. The emitter-current-source block
5. The sense-gate, failure-detection, crowbar, and fail-light block
6. The TUT socketing and metering block
7. The relay-sequencing block

These circuits are shown interconnected in the system schematic diagram of Fig. 3. Fig. 4 shows the schematic diagram for the zero-to-20-volt drive power supply, V_{BB}.

The V_{CC} supply must have adequate current capability to cover the intended spectrum of pulse widths and duty cycles. Its voltage regulation must be such that any spiking caused by stepped changes in load can be absorbed by reasonable filtering on the TUT test chassis. The filtering arrangement shown in Fig. 3 is adequate for the design current of 20 amperes. Whenever fast rise and fall times are a factor, Mylar[1] or the best quality paper capacitors must be used to supplement the electrolytic capacitors. The filter capacitors must be chosen to act in the same manner as a storage battery for a length of time sufficient for the V_{CC} supply to recover from the load change.

The same comments apply to the -14-volt V_{EE} supply, which must not only provide the power for the

[1] Trademark of E. I. duPont de Nemours & Co., Inc.

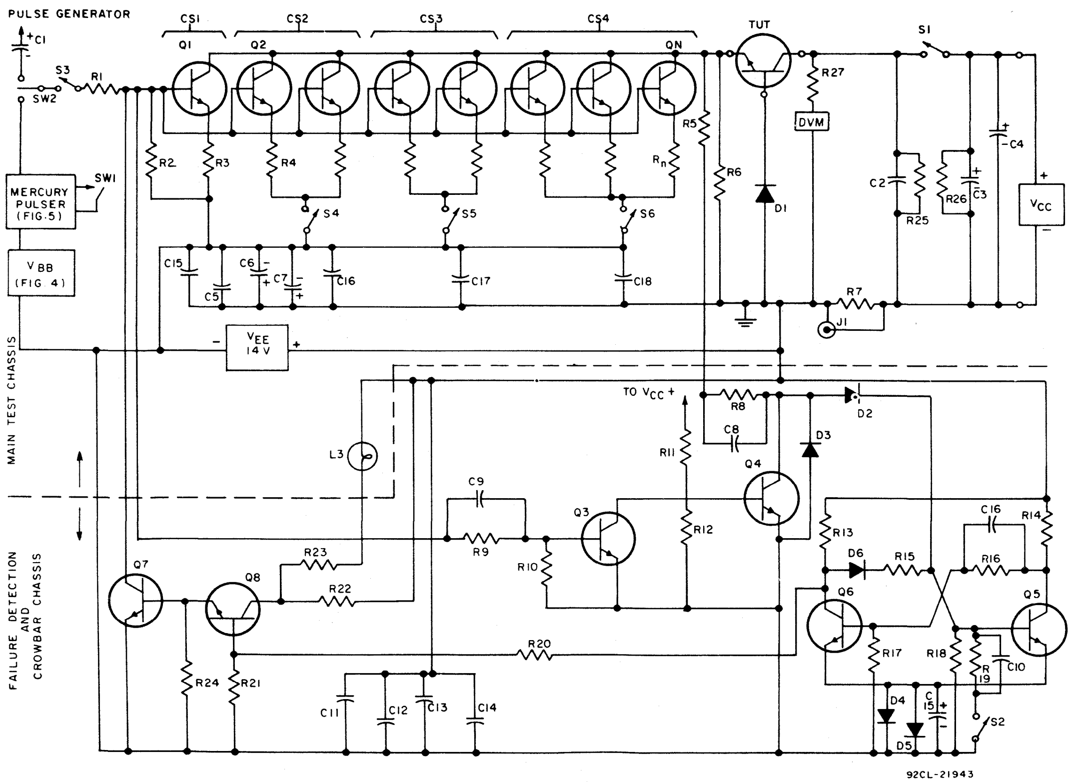

Fig. 3– Schematic diagram of main test chassis (parts list on pages 6 and 8).

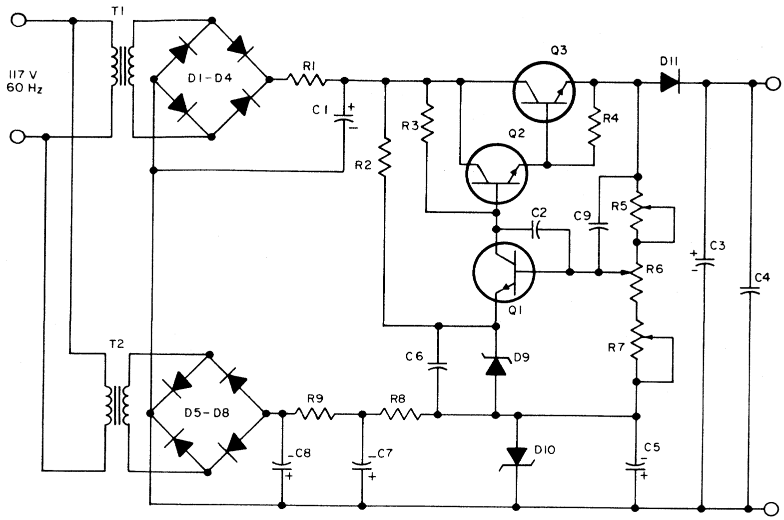

Fig. 4– Schematic diagram of zero-to-20-volt, drive power-supply, V_{BB} (parts list on page 8).

constant-current supply, but must also operate the relay system, the panel lights, and the failure-detection circuitry.

The pulse-timing block, shown in detail in Fig. 5, consists of an HP 214A pulse generator, a mercury-wetted-relay pulse timer, a small zero-to-20-volt power supply, and a selector switch. The HP generator is used for single or multiple pulse testing where the pulse widths are 10 milliseconds or less.

To accomodate the design current of 20 amperes, the current source consists of eight 2N5240 transistors, Q_1 through Q_N, with bases and collectors in parallel and with the emitters connected through 4-ohm ballasting resistors R_2 through R_N. The 2N5240 was chosen for its high voltage breakdown, fast fall time, and good current-handling characteristics.

To achieve the wide current range desired, a current-source selector switch is used which, by means of relays, either adds or subtracts current-source drivers to fit the requirements of the desired test. Fig. 6 shows this arrangement. Each driver can provide 2.5 amperes to the load. Hence, referring to the top of the circuit diagram of Fig. 3 and to Fig. 6:

For 0.2 A to 2.5 A use CS1 only
For 2.0 A to 7.5 A use CS1 and CS2
For 6.0 A to 12.5 A use CS1, CS2, and CS3
For 8 A to 20 A use CS1, CS2, CS3, and CS4

The sensing circuit monitors the voltage at the emitter of the TUT. The existence of a positive-going pulse of 3 volts for a minimum of 50 nanoseconds is sufficient to trip the flip-flop (Q_5 and Q_6). The sense line must be gated so that the emitter of the TUT is sensed only during the power pulse. The gate is made up of Q_3 and Q_4, and is actuated through an RC combination (R_9, C_9) from the base of the current source. The gate is necessary to prevent turn-off transients from falsely firing the flip-flop. The turn-off transient comes from the sweep-out current of the disconnect diode, D_1, and the stored charge in the TUT. The sense-line coupling capacitor, C_8, is paralleled by a 20,000-ohm bleeder resistor, R_8, which assures that the 0.05-microfarad capacitor, C_8, is discharged between test periods; R_8 also provides direct coupling to the flip-flop if the failure of the TUT is of a gradual nature, in which case the 0.05-capacitor, C_8, would be insufficient. The flip-flop drives the crowbar transistor, Q_7, which, when triggered, shorts out the current-source drive to the −14-volt supply, thus shutting off the power to the TUT emitter. The series-base diode, D_1, disconnects the base of the TUT within 100 nanoseconds after the emitter current of the TUT falls below its collector current.

The previous paragraph states that power is shut off to the EMITTER of the TUT. The series base diode effects the disconnection of the collector power to the TUT. The selection of the proper diode for this function is critical. It must have a reverse recovery time that is comparable to the shutdown time of the flip-flop "crowbar" current-source combination. However, it must have a breakdown voltage greater than the highest-rated test voltage of the equipment. R_7 is a 0.1-ohm, non-inductive, precision resistor used in the observation and setting of the current in the collector loop.

The TUT socketing block is arranged to accommodate, on banana plugs spaced three-quarters of an inch apart, both the six-pin, Kelvin, heavy-duty sockets used for production work and the Tektronix[1] sockets. This arrangement offers some interesting possibilities, such as testing of the $I_{s/b}$ capability of paired devices. The banana plugs also provide external access for the application of base-emitter terminations, such as R_{BE}

[1] Trademark of Tektronix, Inc.

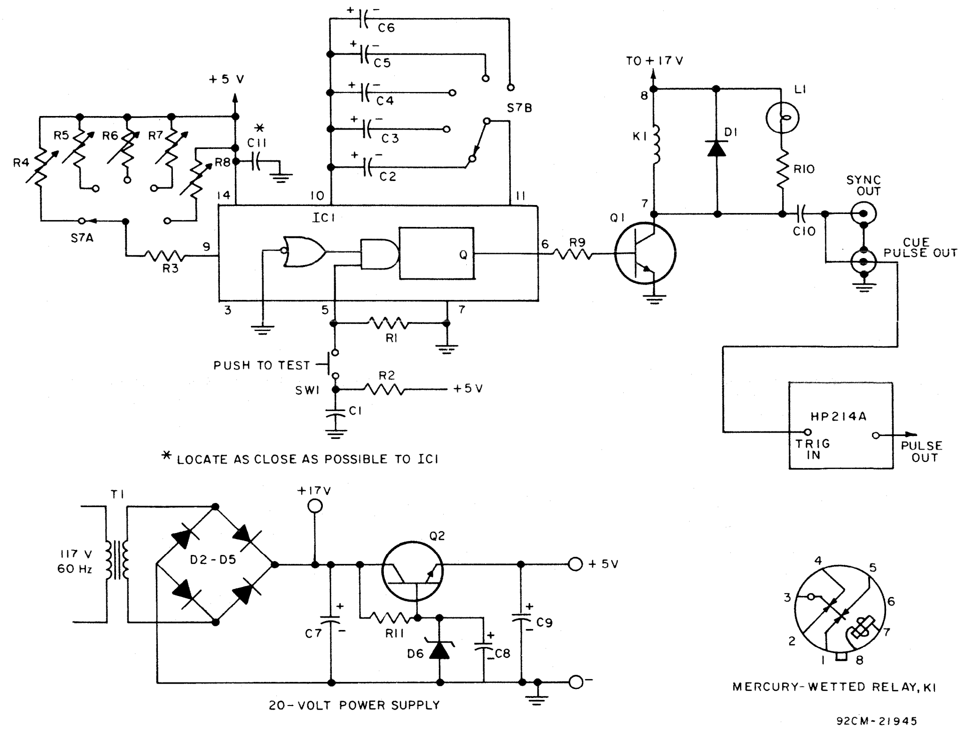

Fig. 5—Schematic diagram of pulse-timing-block components (parts list on page 8).

and V_{EB}. R_5 and R_6 are connected directly to the emitter terminals, and D_1 is connected directly to the base terminal.

The sequencing relay circuit, Fig. 7, is arranged so that the sequence of switching events shown below occurs when the Start button is depressed at the initiation of a test:

1. S_1 closes, applies V_{CC} to the TUT, and lights the Start light.
2. S_2 closes momentarily and resets the flip-flop.
3. S_3 closes and connects the pulse source to the current drivers.

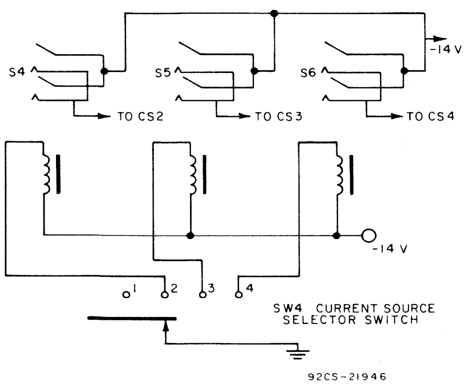

Fig. 6– Relay circuit for current-source selection.

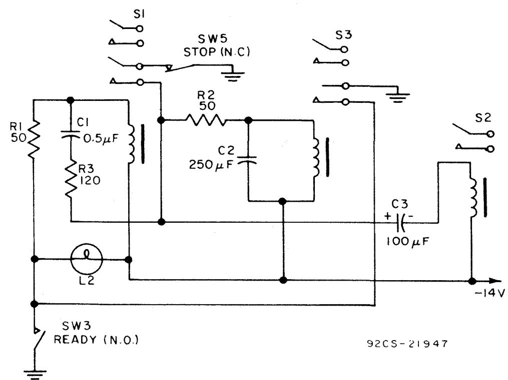

Fig. 7– Sequencing-relay circuit (parts list on page 8).

The sequence at the end of the test when the Stop button is depressed is as follows:

1. S_3 opens and disconnects the pulse drive.
2. S_1 opens and removes V_{CC}, and the Start light goes out.

Construction

Lead dress is not critical; however, there are some wiring restrictions that must be strictly observed:

1. Low-level signals and high-level signals must not be carried in the same wires.
   a. The -14 volts for the flip-flop and gates must be carried on a separate bus which joins the -14-volt supply at the RI - RN bussing point.
   b. The common line for the flip-flop and gates must be a separate line and must meet the system common only at the indicated ground point.
   c. The sense line must connect directly to the emitter jack of the TUT socket.
   d. The pulse-gate drive line must connect through a separate wire to the bases of the current source.
   e. The collector of the crowbar transistor, Q_7, must connect through its own wire to the bases of the current source.
   f. The disconnect diode, D_1, must be connected directly to the base jack of the TUT socket, and its anode return must be carried on a separate wire to the ground bus.
   g. The I_E and I_C lines are lengths of RG14 coaxial cable with shields tied to the ground bus at the TUT end.
2. Current-source and protection-circuit filtering functions for the -14-volt supply must be separated and located on appropriate sub-assemblies.
3. Multiple capacitors are used for two reasons:
   a. To minimize copper losses (IR drops) through leads and foil;
   b. To achieve complete bypassing and regulation regardless of pulse rise time or duration.
4. Mylar[1] capacitors are used wherever possible because of their higher Q and smaller size.

EXPLANATION OF CONTROLS AND ACCESS CONNECTIONS

Explanation of controls shown in Figs. 1 and 9:

AC On-Off	– Operates main contactor to provide power for entire system.
Cue Pulse	– Provides trigger pulse to external pulse generator when TEST button is pressed.
Ext.-Int.	– Selects either internal mercury-relay timer or external pulse generator.
IC Monitor	– Connects to vertical input of monitoring oscilloscope from 0.1-ohm, collector-current sensing resistor.
Pulse Width	– Sets the width of the desired test pulse on the internal timer.
IC Adjust	– This control is used only with the internal mercury relay timer. It adjusts the voltage drive to the emitter current source.
Sync.	– Provides sync pulse to monitoring oscilloscope.
Ready	– Activates the sequencing relays and applies collector voltage to the TUT, resets the failure-detection circuit, and connects the pulse drive circuits to the current source.
Test	– Activates the internal timer or provides a cue pulse to the external pulse generator.
Stop	- De-energizes the sequencing relays and disconnects the pulse source and the collector voltage.
Ext. Pulse	– Receives drive pulse from external pulse generator.
Current Source Selector (Top middle of control panel)	– Switches in additional current sources CS2 through CS4.

[1] Trademark of E. I. duPont de Nemours & Co., Inc.

OPERATION

Operation at DC to 25 Milliseconds

The interconnection of the test equipment with the external units, the pulse generator and oscilloscope, is shown in Fig. 8.

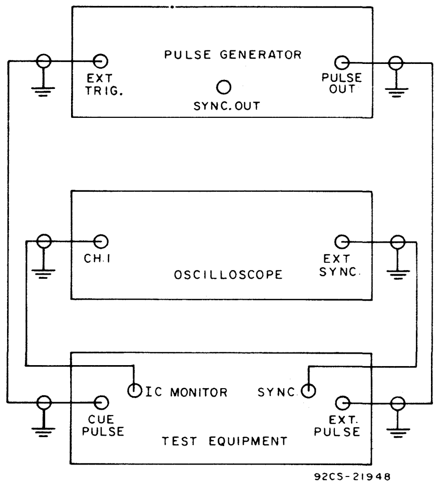

Fig. 8– Test-set interconnections.

The recommended sequence of operation is as follows:

1. Turn all supplies on.
2. Set Ext. - Int. switch to INT.
3. Set Pulse Width switch to 50 milliseconds.

4. Set V_{CC} at 10 volts.
5. Set sweep rate on oscilloscope to 10 ms/div/ext/ + sync.
6. Set oscilloscope sensitivity to dc 0.1 V/div.
7. Turn IC Adjust full counter-clockwise.
8. Set Current-Source Selector switch to desired range.
9. Insert a device into the test socket.
10. Push Ready button; green start light will flash.
11. Push Test button; yellow test light will flash.
12. Adjust sync controls on oscilloscope to obtain a single trace each time Test button is pushed.
13. Turn IC-Adjust control clockwise to obtain negative vertical deflection indicative of desired test current (in this case, 1 division per ampere); for higher currents, change vertical sensitivity to 0.2 or 0.5 V/div. as needed.
14. Switch Pulse Width to that which is required. Change sweep rate on oscilloscope as well.
15. Set V_{CC} at desired test voltage.
16. Push Stop button. Remove set-up device.
17. Insert device to be tested.
18. Push Ready.
19. Push Test; observe current trace on oscilloscope.
20. Push Stop and remove units.
21. If a unit fails the test, the red fail light will turn on.
22. The fail circuit and light will reset the next time the Ready button is pushed.
23. The failure-detection circuits may be checked at any time by switching the current-source switch to the next lower range. This action will produce a false failure signal which will trip the protection circuit. Be sure to return the switch to its original position after the test.

Operation at 25 Milliseconds and Less

1. Turn all supplies on.
2. Set Ext.-Int. to Ext. This connects the external pulse generator to the test equipment.
3. Set V_{CC} at 10 volts.
4. Set sweep rate on oscilloscope to range of interest.
5. Set oscilloscope sensitivity to dc 0.1 V/div.
6. Set trigger selector on external generator to ext. Turn pulse amplitude controls to minimum.
7. Set Current-Source Selector switch to desired range.
8. Insert a device into the test socket.
9. Push Ready button; green start light will flash.
10. Push Test button. Adjust synchronizing controls on oscilloscope to give a single trace each time Test button is pushed.
11. Adjust pulse-amplitude control on generator to secure a usable vertical deflection while repeatedly pushing Test button. Then adjust Pulse-Width control to obtain desired current.
12. Re-adjust pulse-amplitude control to obtain desired current.
13. Set desired V_{CC}.
14. Push Stop. Remove set-up device.
15. Insert device to be tested.
16. Push Ready.
17. Push Test.
18. Push Stop.

The remainder of the procedure is identical to that followed for operation at dc to 25 milliseconds.

MAIN-TEST-CHASSIS PARTS LIST (Fig. 3)

C_1 = 1000 microfarads, 60 volts, pulse-coupling capacitor
C_2 = 3 microfarads, 600 volts, paper or Mylar
C_3, C_4 = 860 microfarads, 450 volts, electrolytic
C_5 = 10 microfarads, 200 volts, Mylar
C_6, C_7 = 2000 microfarads, 50 volts, electrolytic
C_{15} - C_{17} = 0.05 microfarad, 200 volts, Mylar
R_1 = 10 ohms, 2 watts, carbon
R_2 = 100 ohms, 2 watts, carbon
R_3, R_4 - R_N = 4 ohms, 6 watts, clusters of three 12-ohm, 2-watt carbon resistors
R_5 = 0.1 kilohm, 1 watt
R_6 = 8 kilohms, 1 watt
R_7 = 0.1 ohm, non-inductive, 20 watts, with Kelvin connections
R_{25} = 250 kilohms, 2 watts
R_{26} = 8 kilohms, 50 watts, wire-wound
R_{27} = 1 kilohm, 1 watt
Q_1, Q_2, Q_N = transistor, type 2N5240
J_1 = current-monitoring jack, BNC female
L_3 = failure-indicator lamp, 14 volts, 80 milliamperes
D_1 = base-disconnect diode, GEA28D or TRWPD2708
S_1 = collector-current relay, 2 Potter and Brumfield KA14DY, paralleled
S_2 = flip-flop reset relay, Potter and Brumfield KHP 17D11, 12-volt coil
S_3 = pulse-source relay, Potter and Brumfield KHP 17D11, 12-volt coil
S_4 - S_6 = current-source range relays, Potter and Brumfield KHP 17D11, 12-volt coil
SW_1 = test switch
SW_2 = pulse-source selector switch
SW_3 = Ready switch
SW_4 = current-source selector switch
V_{CC} = 0-125 volt, 25-ampere power supply or 0-400 volt, 2-ampere power supply
V_{EE} = 14-volt, 15-ampere power supply
V_{BB} = 9-20-volt, 2-ampere, variable power supply

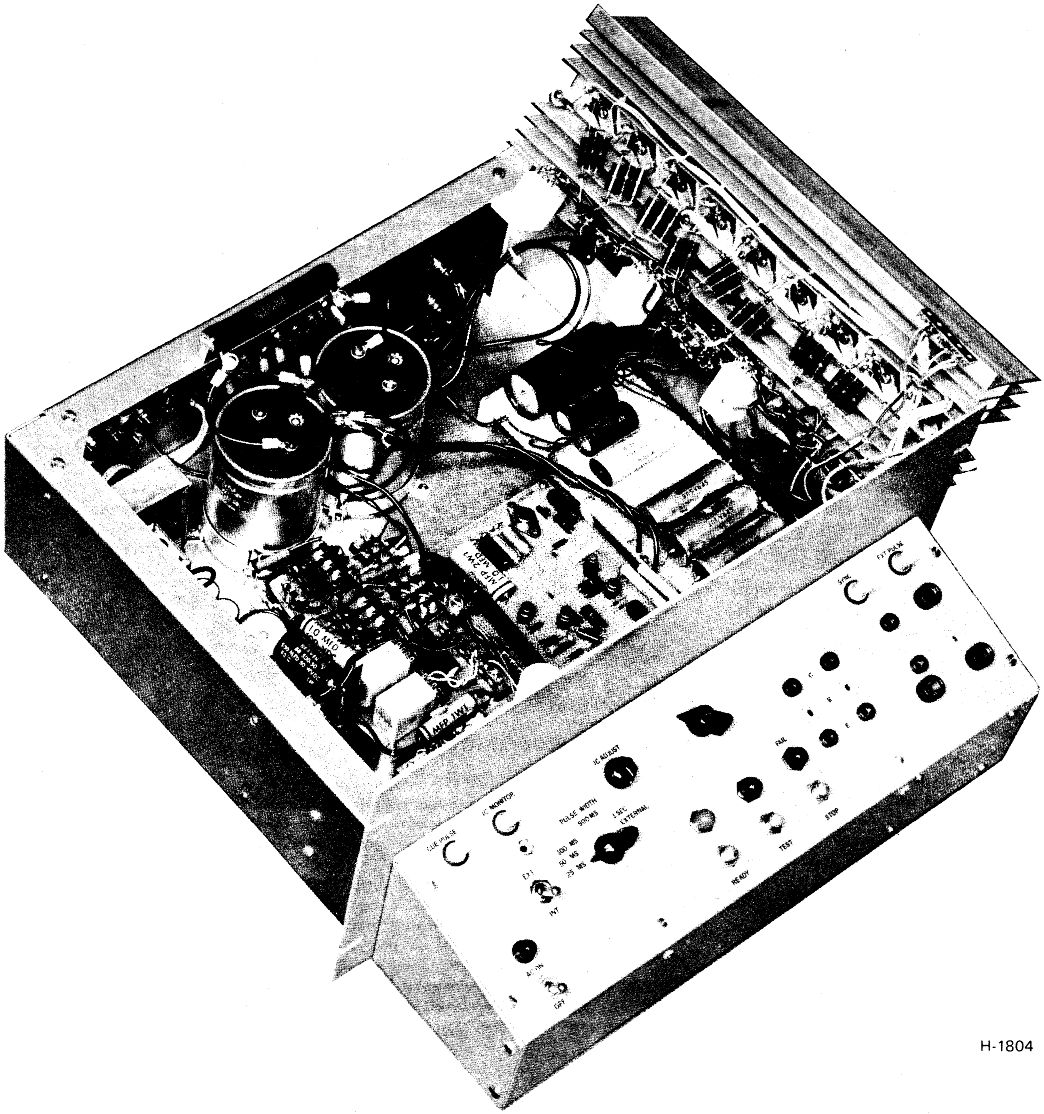

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Fig. 1— Interior and control panel of test equipment.

FAILURE-DETECTION AND CROWBAR-ASSEMBLY PARTS LIST (Fig. 3)

C_8 = 0.05 microfarad, 400 volts, Mylar
C_9, C_{10} = 0.005 microfarad, 200 volts, Mylar
C_{11}, C_{12} = 50 microfarads, 50 volts, electrolytic
C_{13} = 1 microfarad, 200 volts, Mylar or paper
C_{14} = 0.1 microfarad, 200 volts, Mylar or paper
C_{15} = 25 microfarads, 25 volts, electrolytic
C_{16} = 500 picofarads, 200 volts, ceramic
R_8 = 20 kilohms, 1 watt
R_9 = 1.5 kilohms, ½ watt
R_{10} = 1.5 kilohm, ½ watt
R_{11} = 5 kilohms, 20 watts, (two 10-kilohm, 10-watt, wire-wound, in parallel)
R_{12}, R_{14} - R_{16} = 0.5 kilohm, 1 watt
R_{13} = 0.1 kilohm, 2 watts
R_{17} = 10 kilohms, ½ watt
R_{18} = 2.5 kilohms, ½ watt
R_{19} = 250 kilohms, ½ watt
R_{20}, R_{21} = 0.1 kilohm, 1 watt
R_{22} = 73 ohms,(three 220-ohm, 2-watt, in parallel)
R_{23} = 22 ohms, 2 watts
R_{24} = 1 kilohm, 1 watt
D_2 - D_6 = diode, type 1N914A
Q_3 = transistor, type 2N3261
Q_4 - Q_6, Q_8 = transistor, type 2N5262
Q_7 = transistor type 2N3878

ZERO-to-20 VOLT DRIVE POWER-SUPPLY PARTS LIST (Fig. 4)

R_1 = two 1.2-ohm, 2-watt, wire-wound resistors in parallel
R_2 = 6.8 kilohms, ½ watt
R_3 = 10 kilohms, ½ watt
R_4 = 220 ohms, ½ watt
R_5 = trimpot, 5 kilohms, ¼ watt
R_6 = potentiometer, 5 kilohms, 2 watts
R_7 = trimpot, 5 kilohms, ¼ watt
R_8 = 470 ohms, ½ watt
R_9 = 220 ohms, ½ watt
C_1 = 2000 microfarads, 50 volts, electrolytic
C_2 = 0.01 microfarad, 100 volts, ceramic
C_3 = 500 microfarads, 50 volts, electrolytic
C_4 = 1 microfarad, 100 volts, Mylar[1]
C_5 = 50 microfarads, 25 volts, electrolytic
C_6 = 100 microfarads, 25 volts, electrolytic
C_7 = 500 microfarads, 25 volts, electrolytic
C_8 = 500 microfarads, 25 volts, electrolytic
C_9 = 5 microfarads, 50 volts, electrolytic
D_1 - D_4 = 6-ampere bridge assembly, Varo VH247 or equivalent
D_5 - D_8 = 2-ampere bridge assembly, Varo VS247 or equivalent
D_9 = zener, 6.8 volts, 1 watt
D_{10} = zener, 12 volts, 1 watt
D_{11} = diode, type 1N1206
Q_1 = transistor, type 2N2102
Q_2 = transistor, type 2N2102
Q_3 = transistor, type 2N3772
T_1 = transformer: 117-volts primary - 25.2-volt, 2.8-ampere secondary
T_2 = transformer: 117-volt primary - 16.6 volt, 0.3-ampere secondary

PULSE-TIMING-BLOCK PARTS LIST (Fig. 5)

R_1 = 820 ohms, ½ watt
R_2 = 2.2 megohms, ½ watt
R_3 = 2 kilohms
R_4 - R_8 = trimpots, 50 kilohms, ¼ watt; Bourns 200P-1-503 or equivalent
R_9 = 100 ohms
R_{10} = 47 ohms, 1 watt
R_{11} = 270 ohms, ½ watt
C_1 = 0.01 microfarad, 80 volts, PACER
C_2 = 5 microfarads, 50 volts, tantalum; Mallory CL65BJ050KPE
C_3 = 22 microfarads, 25 volts, tantalum; Mallory CL65BG220KPE
C_4 = 68 microfarads, 30 volts, tantalum; Mallory CL65BH681KPE
C_5, C_6 = 100 microfarads, 25 volts, tantalum; Mallory CL65BG101KPE
C_7 = 100 microfarads, 25 volts, electrolytic
C_8 = 10 microfarads, 25 volts, electrolytic
C_9 = 25 microfarads, 25 volts, electrolytic
C_{10} = 1 microfarad, 100 volts, Mylar
C_{11} = 0.1 microfarad, 100 volts, ceramic
D_1 - D_5 = diode, type 1N5395
D_6 = zener, type 1N4734A, 5.6 volts, 1 watt
Q_1, Q_2 = transistor, type 2N5320
IC_1 = integrated circuit, type SN74121N (Signetics)
K_1 = mercury relay, Potter and Brumfield JM11211 or equivalent
L_1 = lamp, No. 382; 14 volts, 0.08 amperes
S_{7A}, S_{7B} = wafer switches, 2-pole, 5-position (matching contacts tied together to make each wafer a single-pole 5-position switch)

SEQUENCING-RELAY-CIRCUIT PARTS LIST (Fig. 7)

S_1 = collector power relay
S_2 = flip-flop reset relay — See Main Test Chassis parts list, page 6
S_3 = current-source drive relay
SW_3 = Ready switch, normally open, push button
SW_5 = Stop switch, normally closed, push button
R_1, R_2 = 50 ohms, 2 watts
R_3 = 120 ohms, 1 watt
C_1 = 0.5 microfarad, 200 volts
C_2 = 250 microfarads, 50 volts
C_3 = 100 microfarads, 50 volts
L_2 = ready lamp, 80 milliamperes, 14 volts

Quantitative Measurement of Thermal-Cycling Capability of Silicon Power Transistors

by L. J. Gallace

This Application Note discusses the methods used to test the thermal-cycling capability of power transistors. A brief description of thermal fatigue, application requirements, and rating charts is given. A detailed discussion of the practical design of thermal-cycling racks is also included along with actual test conditions for various power-transistor types. Acceleration factors, failure indicators, failure mechanisms, and real-time control of thermal-cycling capability of factory product are discussed. Some information is also given on hermetic versus plastic-package thermal-cycling reliability.

In silicon power-transistor applications, thermal cycling of transistors may activate a failure mechanism called thermal fatigue. This phenomenon is caused by the mechanical stresses set up by the differentials in thermal expansion of the various materials used in the transistor assembly and heat sink. Thermal fatigue often causes the silicon pellet to crack or to fail at the silicon/mounting interface.

The number of cycles to failure in terms of device characteristics and operating conditions has been expressed as:

$$N = Ae^{\frac{\psi_0}{(a_1 - a_2)\,\Delta T\,L}}$$

where A and ψ_0 are constants for a given power structure, $(a_1 - a_2)$ is the difference in thermal expansion between the silicon die and the material on which it is mounted, ΔT is the change in temperature at the interface between the silicon chip and the material to which it is mounted, and L is the maximum dimension of the silicon chip.

APPLICATION REQUIREMENTS

Table I shows typical applications of power transistors and the number of cycles or cycle life required of transistors used in equipment in each application to allow the equipment to fulfill its life expectancy. The importance of cycle life can be shown by examining the following simple expression of the failure-rate equation, which characterizes device failure rates:

$$\lambda = \lambda_T \, \pi_Q \, \pi_E \, \pi_L \, \pi_P + \lambda_{\Delta T_c}$$

where λ = failure rate
λ_T = base failure rate due to temperature (Arrenhius)
π_Q = quality factor
π_E = environmental factor
π_L = learning curve
π_P = package factor
$\lambda_{\Delta T_c}$ = change in case temperature

Table I reflects the increasing demand for more thermal-cycle-life capability from equipment manufacturers because of their lengthening warranty periods. This lengthening of warranty period has greatly increased the demand on power-transistor manufacturers to test and ensure product capability over a longer period of time. RCA has developed a rating chart, Fig. 1, that relates the thermal-cycling capability of silicon power transistors to total device dissipation and the change in case temperature. A circuit designer may use the rating chart to define a limiting value below which power dissipation and change in case temperature are not factors in the failure rate equation; i.e., *within this rating chart, the failure rate for power transistors is independent of cycle life.* This statement does not imply that failures will not occur; it does imply, however, that the last term in the failure-rate equation is small enough to be insignificant. Since the change in case temperature is a major consideration in many applications, product with superior capability in this parameter will produce lower field-failure rates.

FAILURE ANALYSIS

Soft-Solder Devices

In soft-solder devices, the metal interfaces between the emitter, base, and collector contacts consist of nickel-lead-tin metals which expand and contract at different rates during thermal cycling, and, consequently, strain occurs. Because of the difference in coefficients of expansion of these materials, an appreciable amount of shearing takes place that causes

TABLE I – THERMAL-CYCLING REQUIREMENTS FOR TYPICAL APPLICATIONS OF POWER TRANSISTORS

APPLICATION	CIRCUIT	P_T (W)	ΔT_C (°C)	MINIMUM EQUIPMENT LIFE REQUIRED (YEARS)	TYPICAL THERMAL-CYCLING-RATING REQUIRED (CYCLES)
Auto radio	Class A	8	75	5	5,000
Audio output	Class AB	2	45	5	5,000
Power supply	Series regulator	50	65	5	10,000
	Switching regulator	15	65	5	10,000
Hi-Fi audio amplifier	Class AB	35	50	5	5,000
Computer power supply	Series regulator	50	65	10	10,000
Computer peripheral equip.	Solenoid driver	5	5	10	1.3×10^8
Television	Vertical output	10	75	5	7,500
	Audio output	8	75	5	7,500
Sonar modulator	Linear amplifier	100	55	10	144×10^3

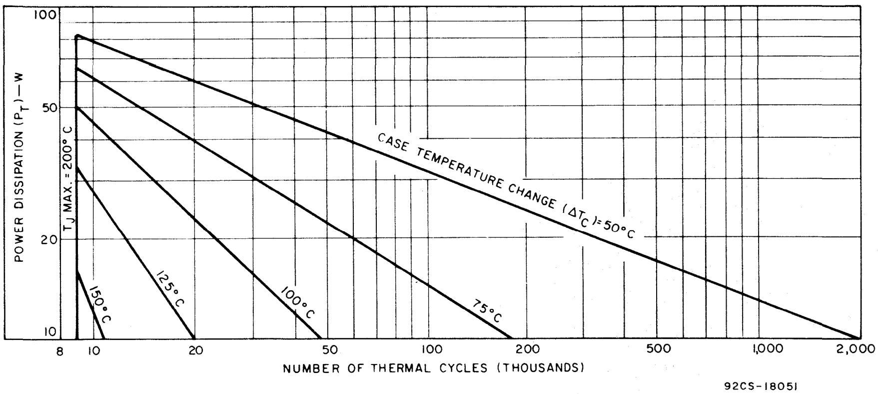


Fig. 1 – Thermal-cycling rating chart for an RCA hermetic power transistor.

fatigue failure at the contact point. The longer the stress continues, the more the solder moves to relieve the stress. If the movement continues long enough, the joints will rupture, and actual physical displacement of the silicon pellet will occur; this displacement is called pellet "walk." Linear movements of as much as 20 mils have occurred.

Hard Solder

The predominant failure mechanism in hard-solder devices is failure in the silicon crystal. Since no plastic flow occurs in hard solder, invariably the silicon must take up some of the strain in the system. Cracks in the silicon, generally under the bonding-wire area, are the most common failure mechanism.

PRACTICAL TESTING

Although analytical techniques have been most helpful in developing an understanding of thermal cycling as a failure producer, testing, the experimental approach, must still be used to determine the ultimate thermal-cycling capability of a power transistor.

Fig. 2 is a schematic diagram of the basic test circuit. Depending on the frequency response of the transistor to be tested, this circuit is modified to avoid parasitic oscillation. Modification generally takes the form of capacitors, usually connected collector-to-emitter, or ferrite beads on the emitter and base leads.

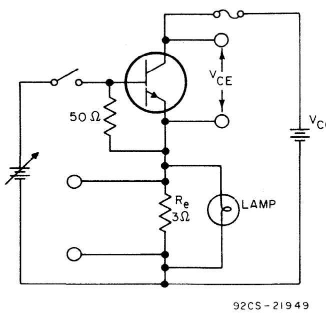


Fig. 2– Test circuit.

Fig. 3 is a photograph of a typical test rack without the associated power supplies. The Appendix contains a complete parts list and mechanical layout for this thermal-cycling rack. In addition, the Appendix shows a layout and parts lists for sockets that accommodate both TO-220 VERSAWATT (plastic) and TO-3 hermetic transistors.

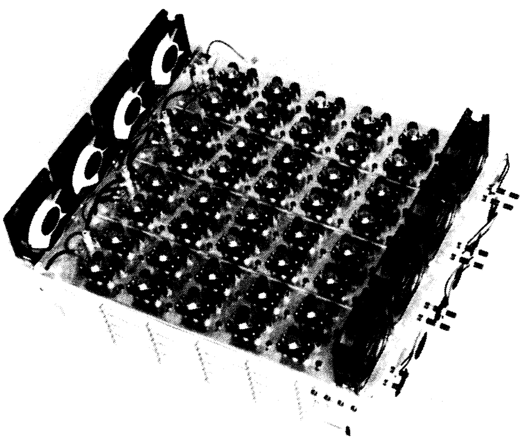


Fig. 3– Test rack used in thermal-fatigue testing.

The design of the test rack stresses simplicity and universal use. By interchanging sockets, 40 devices including almost all power-transistor types can be tested. Eight fans are used to cool the devices on the off cycle. Most tests can be conducted under free-air conditions; however, if heat sinks are used, power levels up to 56 watts per socket can be handled.

Under these higher-power conditions, a temperature gradient will exist across the rack with the highest temperature at the center. A simple method to compensate for this gradient is to increase the size of the heat sink on the sockets as the distance from the fans increases.

Mechanical timers are used to control the on-off cycle time. For very fast cycle time (40 seconds or less), high-torque motors are recommended for longer timer life. Solid-state timers have also been used.

A thermocouple is used to monitor the cycle temperature continuously. For more important tests, when equipment failure cannot be tolerated, over-temperature controls set 5 to 10°C above the maximum temperatures of the test are used. When activated, the control will open the base drive circuit and keep it open until manually reset. This method may also be used to cycle the tests on and off, but the cost is higher than when mechanical timers are used.

Jacks are provided on the front panel of the rack for monitoring emitter current. The light bulb connected across the emitter resistor is a visual aid to help detect intermittent emitter-base contacts. The number of test cycles is automatically recorded on a counter.

Since thermal cycling of power transistors requires high-current power supplies (50 to 100 amperes), consideration must be given to thermal-fatigue-induced power-supply failures. If 50-per-cent duty cycles are used, then switching can be arranged so that there is a constant load on the power supply. For duty cycles other than 50 per cent, resistive loads can be switched in during the transistor off cycle. Multiple timers driven from the same motor can be used to service up to three racks from one collector power supply when more than one rack uses the same cycle time.

TEST CONDITIONS

A thermal-fatigue test is basically a cyclical, operating-life test. For room-ambient testing, the important test parameters are:

P_d, collector dissipation;

ΔT_c, change in case temperature;

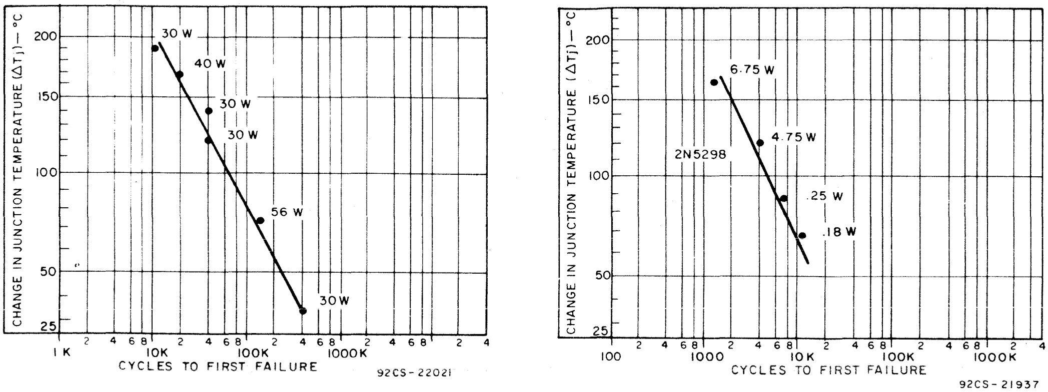
ΔT_j, change in junction temperature;

T_{jmax}, maximum junction temperature;

θ_{jc}, junction-to-case thermal resistance; and cycle time.

In empirically determining the power-cycling capability of a power transistor, it was found that the single most important parameter was ΔT_j. Although T_{jmax} and cycle time were also significant factors, it was shown that most of the predictive methods and acceleration factors could be based on ΔT_j; 70 per cent of the experimental data could be explained by this one parameter as long as the power range for ΔT_j did not exceed a maximum of 3 to 1.

Fig. 4 shows plots of ΔT_j as a function of cycles-to-first-failure on Arrenhius-type paper for a 2N3055 transistor in a hermetic TO-3 package and a 2N5298 transistor in a TO-220 VERSAWATT package. The data show a "good" fit relatively independent of power. These curves can be used to predict power-cycling capability at lower ΔT_j values with good accuracy.



(a) 2N3055

(b) 2N5298

Fig.4 — Change in junction temperature as a function of cycles-to-first-failure for a 2N3055 transistor in a hermitic TO-3 package and a 2N5298 transistor in a TO-220 VERSAWATT package.

Some recommended test conditions for evaluating product to the published rating curves are shown in Table II. All of the test conditions given can be achieved on the test rack shown in Fig. 3 and described in the Appendix.

Although most failures are detected while a device is under operation on the thermal-cycling test racks, sufficient down-period readings should be recorded to indicate shifts in parameters that are indicators of changes in the device metallurgical system. The most critical parameters to record as variables data are thermal resistance (junction to case), beta, V_{BE}, $V_{CE(sat)}$, and I_{CEO}.

Package Differences (Hermetic vs. Plastic)

The thermal-cycling capability of a plastic-packaged device is generally less than that of its hermetically packaged counterpart even though the maximum ratings of the devices are substantially different (150°C plastic, 200°C hermetic). This difference in capability is attributed to the condition which, in the plastic package, allows the emitter and base leads, embedded in the plastic mold, to be continually moved across the silicon chip during thermal cycling, thus causing eventual failure as a result of open contacts. Fig. 5 shows rating curves for the same pellet (2N3055) in both the plastic VERSAWATT and TO-3 hermetic packages.

TABLE II – RECOMMENDED TEST CONDITIONS

PACKAGE TYPE	POWER (WATTS)	T_c(°C)	ΔT_c(°C)	t_{on}	t_{off}	HEAT SINK
TO-220 VERSAWATT	18	55 to 110	55	3 min.	3 min.	3°C/W
	4.75	35 to 155	120	50s	100s	Free Air
TO-3 Hermetic	16	40 to 130	90	50s	100s	Free Air
	56	70 to 120	50	15s	25s	6.3°C/W
TO-66 Hermetic	8.5	35 to 155	120	50s	100s	Free Air
RCA "TO-5" Plastic	1.5	35 to 135	100	60s	90s	Free Air
TO-5 Hermetic	1.5	30 to 115	85	60s	90s	Free Air

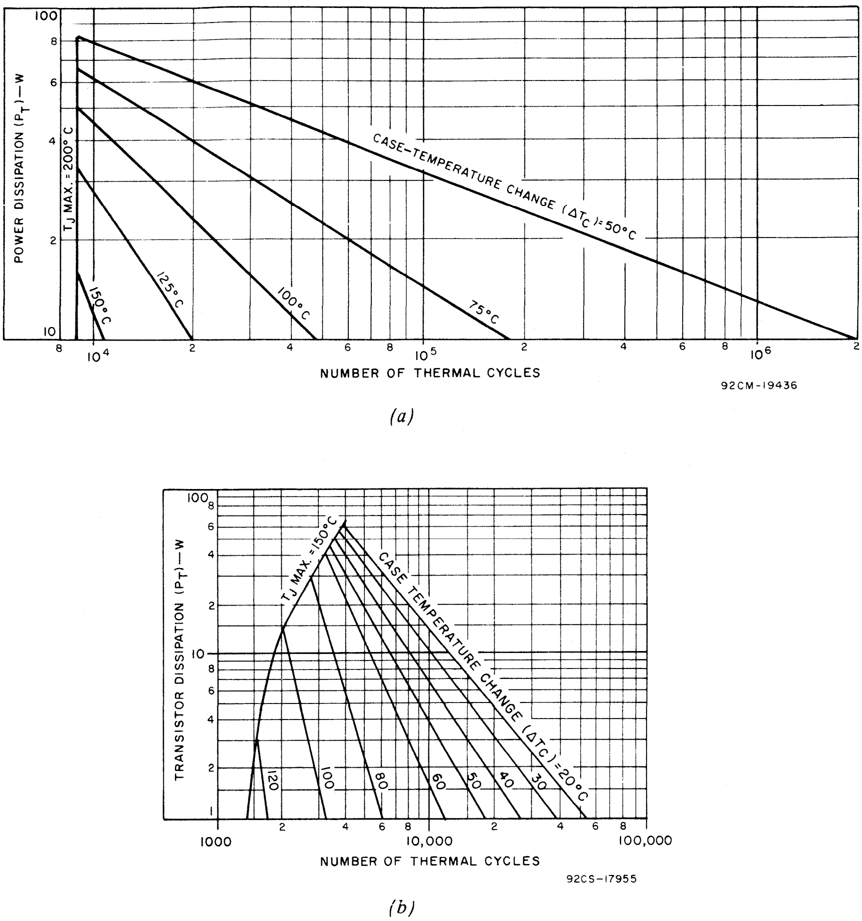


Fig.5 – Thermal-cycling rating curves for a 2N3055 pellet in (a) a TO-3 hermetic package, (b) a plastic VERSAWATT package (2N6103).

There are also cases where performance of a plastic package may be superior to some types of hermetic-package designs. For example, some aluminum TO-3 packages with solder-in emitter-base feedthroughs have shown substantially less capability on thermal cycling than their plastic VERSAWATT counterparts. In addition, the aluminum packages that have been measured become nonhermetic after a relatively low number of thermal cycles (less than 5000). Obviously then, care must be exercised in the selection of power transistors to avoid basing the choice upon package categories as general as "plastic" and "hermetic."

Real-Time Controls (RTC)

A major innovation in using the methods described to test for thermal-cycling capability is to monitor the thermal-cycling capability of factory product on a lot-by-lot basis. Essentially, real-time control, or RTC, makes a continuous acceptance test and interpolation of thermal-cycling data against some established criteria. Information generated internally by RTC on thermal cycling has unquestioned validity because conditions of tests are well controlled and all ambiguities have been removed. Current as well as historical and projected operating information is generated for analysis.

The types of tests which are used in RTC are designed to produce information in three days for providing process control data. Typical examples of real-time control conditions are shown in Table III.

TABLE III – TYPICAL EXAMPLES OF REAL-TIME CONTROL CONDITIONS

TYPE	POWER (WATTS)	T_C(°C)	ΔT_C(°C)	CYCLES/DAY	N	TEST DURATION	AC NO.
TO-220	4.75	35 to 155	120	576	40	1700	0
VERSAWATT						3000	1
TO-3	56	70 to 120	50	2200	40	4400	0
Hermetic						6600	1

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5. RADC (Rome Air Development Center) TR-67-108, Reliability Notebook Vol. II, September, 1967.
6. C. M. Ryerson, "Mathematical Modeling for Predicting Failure Rates of Component Parts," Sixth Annual Reliability Physics Symposium, Los Angeles, California, Nov., 1967.

APPENDIX

Thermal-Cycling Test Rack Parts List
(Figs. A1, A2, A3, A4)

2	Counters	ITT General Controls CE600BS 602 120 V 60 Hz
2	Relays	Potter & Bromfield PR11AY - DPDT - 120 V AC
40	L–10/20 Rated for 10 V Lamps	Mura Corp. Great Neck, N. Y. With Red Lens Cap
8	Fans	IMC Magnetics Corp. Boxer Fan Model No. BS2107F
4	Barrier Blocks	Three Contacts, Thru-Panel Solder Lugs Cinch-Jones - Series 3–142–Y
81	Fuse Holders	Little Fuse Type 342012
1	AC Line Cord	Belden No. 17419 9 Ft. No. 16–3 Type SJ Rubber
4	Switches	SP/ST Cutler-Hammer No. 7580K7
8	Neon Lamps	American Pamcor Paoli, Pa. No. 380627–2
40	3 Ohms - 25 W Resistors	Ohmite No. 0200L Style 270–25
40	Banana Jacks	Red - E.F.Johnson - No. 108–902
80	Banana Jacks	Green - E.F.Johnson - No. 108–904
40	Banana Jacks	Blue - E.F.Johnson - No. 108–910
4	Binding Posts	Blue - E.F.Johnson - No. 111–110
2	Binding Posts	White - E.F.Johnson - No. 111–101
2	Binding Posts	Black - E.F.Johnson - No. 111–103
40	Fuses	4 A Littelfuse 312 004
40	Fuses	½ A Littelfuse 312 500
2	Fuses	2 A Littelfuse 312 002

Sockets

80	TO-3	6/32 Screws 3/4 in. long
80	TO-3	6/32 Nuts 1/4W x 3/32H
80	TO-3	6/32 Nuts 1/4W x 1/2H
80	TO-3	6 Lock Washers
40	TO-220	Socket Base Pomona Electronics Company Pomona, California Model 2095

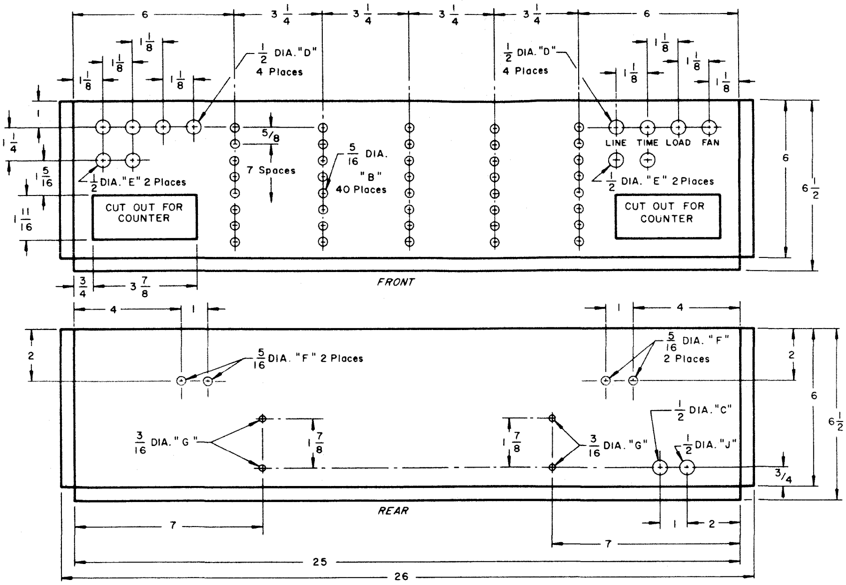
APPENDIX (Cont'd)

Sockets (Cont'd)

40	TO-220	Sockets Jettron Products, Inc. Hanover, N. J. CD 74-104
	TO-220	See Assembly Drawing (Fig. A5)
40	TO-66	Tektronix, Inc. No. 013-0070-01
40	TO-3	Cover Plate for Pomona Socket See Detailed Drawing (Fig. A6)
40	TO-3	Socket Base Pomona Electronics Company Pomona, California Model 2095
40	TO-3	Socket – E B Y No. 9866-15-1
	TO-3	Heat Sink: Wakefield Engineering Delta Division
16	TO-3	NC-631-3 (Wakefield Engineering, Delta Division)
16	TO-3	NC-632-3 (Wakefield Engineering, Delta Division)
8	TO-3	Fabricate – See Detailed Drawing (Figs. A6, A7)

Cycling Control Box

1	Timer	Industrial Timer Corporation Parsippany, New Jersey MC1 with Two Switches (Cycle Time: 4 to 36 secs.) High-Torque Motor With A-36 Gear Rack (115 V - 60 Cycle)
1	Neon Lamp	American Pamcor Paoli, Pa., No. 380627–2
2	Banana Jacks	Red - E.F. Johnson - No. 108–902
2	Banana Jacks	Green - E.F. Johnson - No. 108–904
2	Banana Jacks	Blue - E.F. Johnson - No. 108–910
1	Switch	SP/ST Cutler-Hammer No. 7580K7
1	AC Line Cord	Belden No. 17419 9 Ft. No. 16–3 Type SJ
1	Chassis	Bud - Aluminum 4 x 5 x 6 in. No. AU–1029

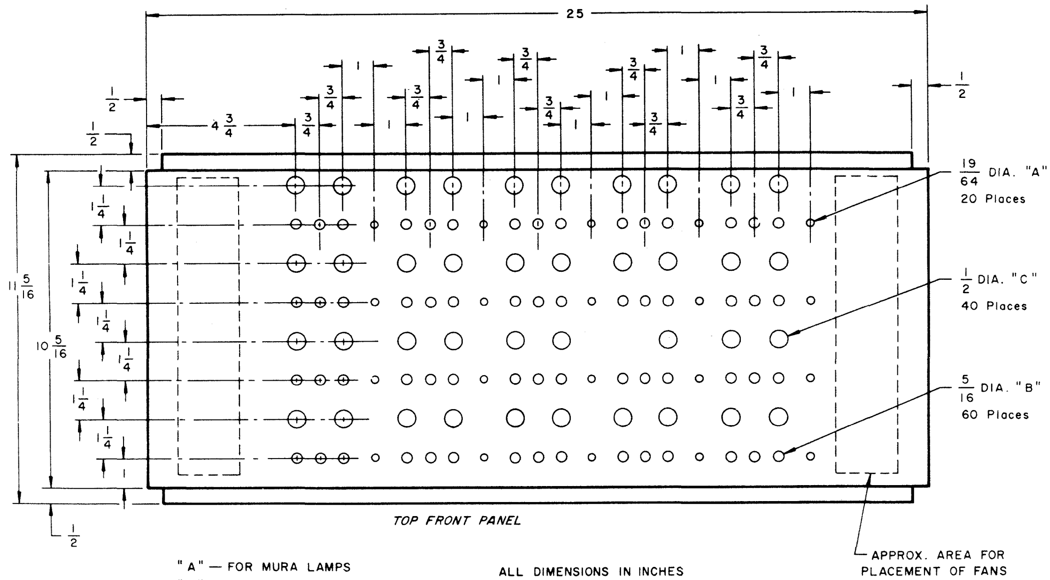


"C" — FOR FUSE HOLDER
"D" — FOR PAMCOR LAMPS
"E" — FOR SWITCHES
"F" — FOR BINDING POSTS
"G" — FOR P.B. RELAYS
"B" — FOR BANANA JACKS
"J" — FOR LINE CORD

ALL DIMENSIONS IN INCHES

92CM-21985

Fig. A1



"A" — FOR MURA LAMPS
"B" — FOR BANANA JACKS
"C" — FOR FUSE HOLDERS

ALL DIMENSIONS IN INCHES

92CM-21984

Fig. A2

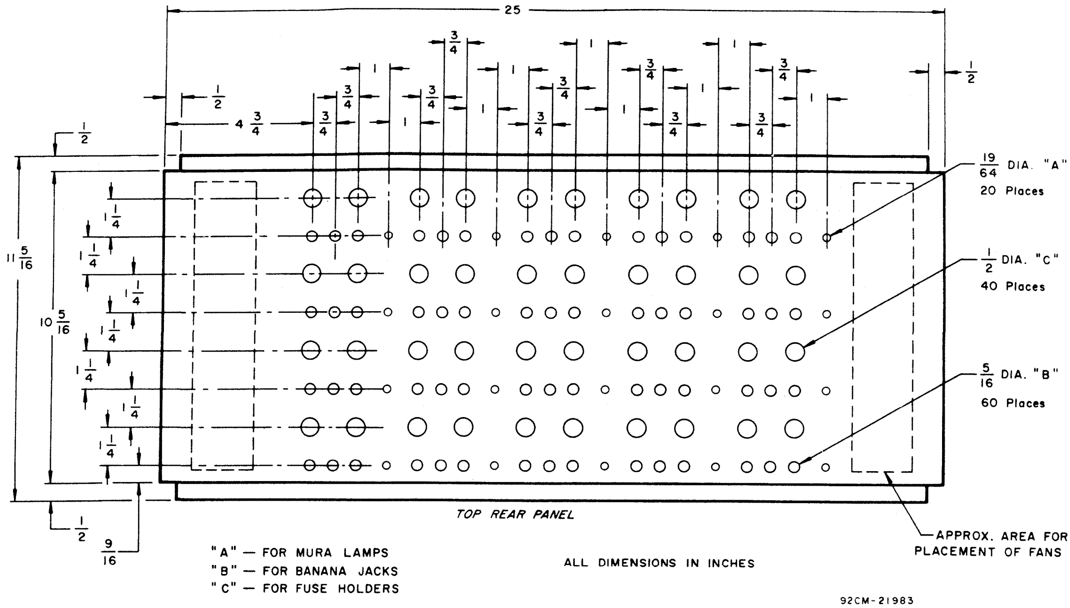

25
19/64 DIA. "A"
20 Places
1/2 DIA. "C"
40 Places
5/16 DIA. "B"
60 Places
TOP REAR PANEL
APPROX. AREA FOR
PLACEMENT OF FANS
"A" — FOR MURA LAMPS
"B" — FOR BANANA JACKS
"C" — FOR FUSE HOLDERS
ALL DIMENSIONS IN INCHES
92CM-21983

Fig. A3

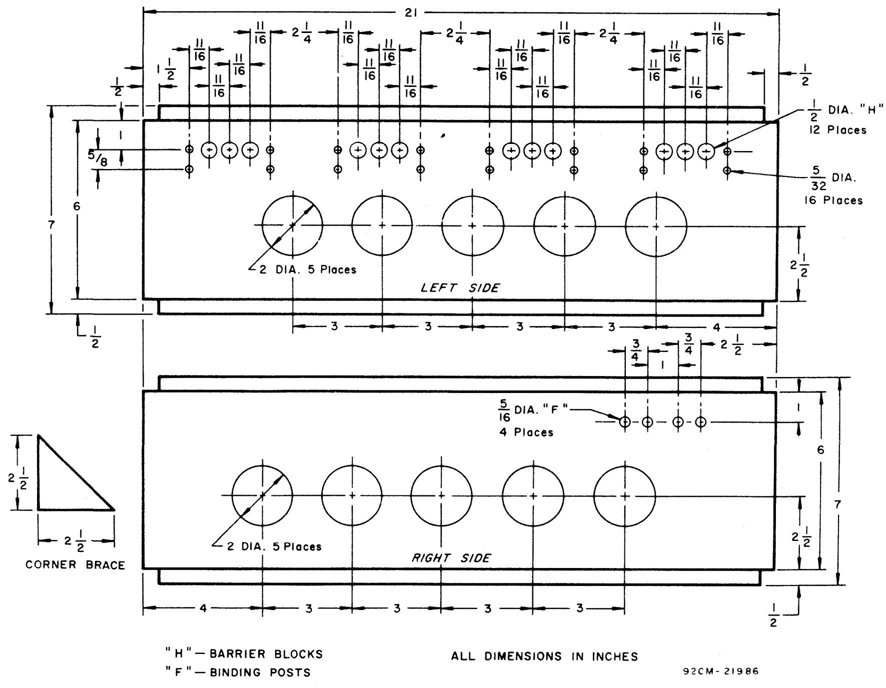

21
1/2 DIA. "H"
12 Places
5/32 DIA.
16 Places
2 DIA. 5 Places
LEFT SIDE
5/16 DIA. "F"
4 Places
2 DIA. 5 Places
RIGHT SIDE
CORNER BRACE
"H" — BARRIER BLOCKS
"F" — BINDING POSTS
ALL DIMENSIONS IN INCHES
92CM-21986

Fig. A4

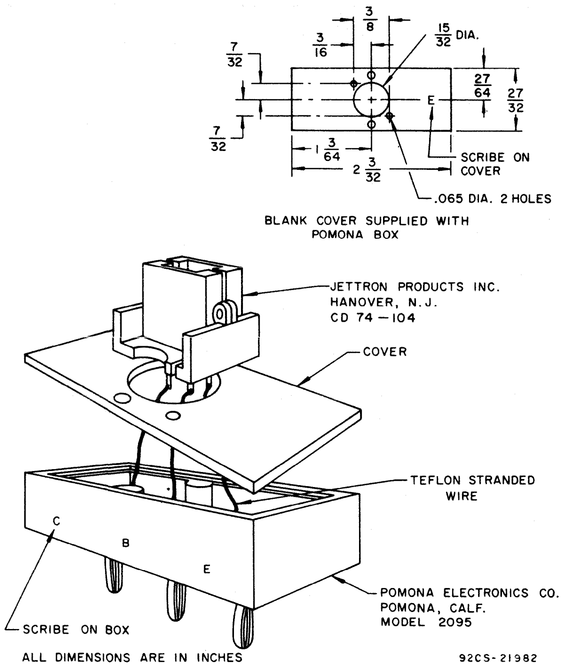


Fig. A5

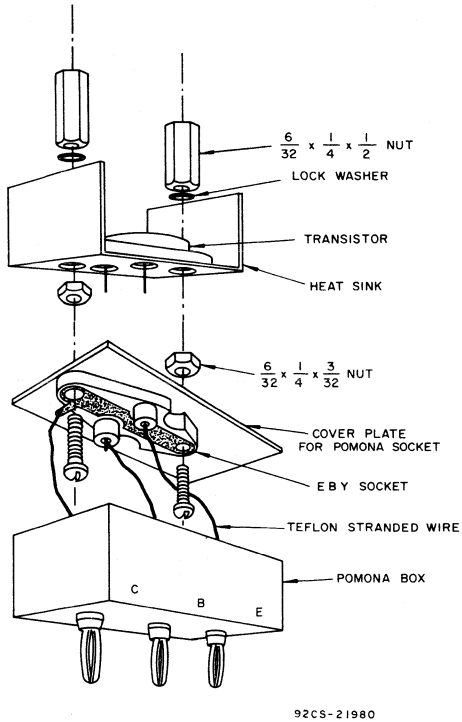


Fig. A7

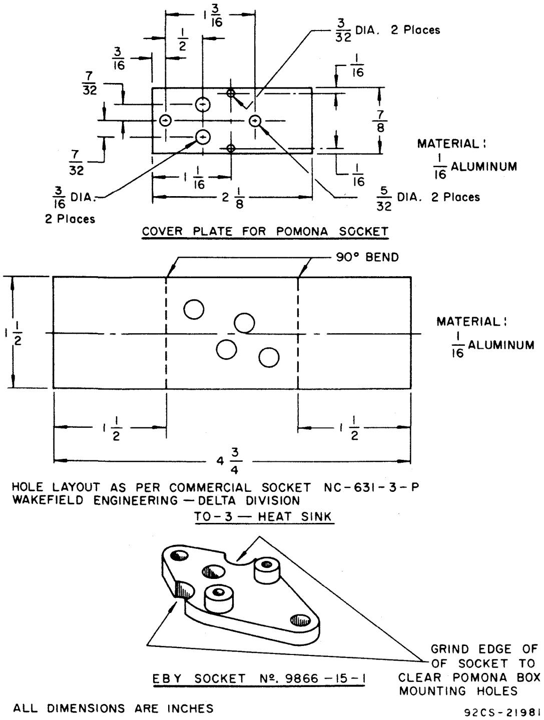


Fig. A6

RCA
Solid State
Division

Power Transistors

Application Note
AN-6215

Interpretation of Voltage Ratings for Transistors

by C. R. Turner

Introduction

Transistor voltage breakdown is a function of both individual device characteristics and associated circuits. This Note describes basic transistor voltage-breakdown mechanisms and their relationship to external circuits. These mechanisms are then used to explain the various types of voltage ratings used by transistor manufacturers.

Voltage ratings can be readily established for transistors designed for use in specific applications for which both the associated circuit parameters and the required device characteristics are known. For example, specific voltage ratings can be assigned to transistors used in applications such as auto radios, portable radios, and computer circuits, and the large number of transistors produced for these uses can be specially tested to meet these particular ratings.

However, multi-purpose transistors must also have clearly defined voltage ratings which can be easily understood so that these devices can be readily designed into a wide variety of applications. The calculation of these voltage ratings requires a fundamental understanding of transistor voltage-breakdown mechanisms and their circuit dependance.

Common-Base Avalanche Breakdown

Collector-base breakdown of transistors operating in a common-base connection is caused by avalanche multiplication. When a voltage is applied between collector and base, a depletion layer or space-charge layer is formed at the collector junction and spreads out into both the collector and base regions. Avalanche multiplication takes place in this depletion layer when a high electric field is present. This multiplication effect, which is similar to the "Townsend effect" in gas tubes, is the result of collisions between rapidly accelerating minority carriers that enter the depletion layer and atoms in the crystal lattice. Energy transferred to the atoms as a result of these collisions causes ionization, which releases valence electrons; these electrons are then also accelerated. Avalanche breakdown differs from Zener breakdown in that no multiplication takes place because no free carriers are present in the Zener condition. All the carriers of the Zener breakdown are formed by stripping of valence electrons in a high-strength field.

The multiplication M that takes place for a given collector-to-base voltage (V_{CB}) is given by the following empirical formula for junction transistors:

$$M = \frac{1}{1 - \left(\frac{V_{CB}}{V_A}\right)^n} \qquad (1)$$

where V_A is the true avalanche or "bulk" breakdown and n is the rate of multiplication; both terms are constant for a device of a given type. These constants are determined for a particular transistor as follows:

For a common-base circuit using constant-current input, the collector current I_C is given by

$$I_C = \alpha M I_E + M I_{CBO} \qquad (2)$$

where α (alpha) is the short-circuit common-base current transfer ratio, I_E is the emitter current, and I_{CBO} is the collector-to-base leakage current. Both I_E and I_{CBO} are multiplied by the multiplication factor M because they cross the depletion layer (the ohmic leakage components of I_{CBO} which do not cross the depletion layer and are not affected by multiplication are not considered here).

If the operating point of a transistor in a common-base circuit is selected so that I_E is much greater than I_{CBO}, then equation (2) can be simplified as follows:

$$I_C \approx \alpha M I_E \qquad (3)$$

9-73

The multiplication factor M is then given by

$$M = \frac{1}{\alpha} \frac{I_C}{I_E} \qquad (4)$$

Because the collector current I_C is related to the multiplication factor M, which is in turn related to the collector-base voltage V_{CB}, particular values of M for values of V_{CB} can be obtained from the following rearrangement of equation (1):

$$\log \frac{M-1}{M} = n \log \frac{V_{CB}}{V_A} \qquad (5)$$

This equation indicates that a log-log plot of (M-1)/M as a function of V_{CB} is a straight line having a slope n and value of V_{CB} equal to the true avalanche breakdown V_A when (M-1)/M is unity, or when M approaches infinity.

Total Alpha

Equation (3) shows that the "total alpha", or total gain factor, for a transistor in a common-base circuit is reflected by the product αM. In addition to the multiplication factor M, therefore, the "total alpha" depends on the short-circuit current transfer ratio α, which is given by

$$\alpha = \beta_o \gamma \qquad (6)$$

where β_o is a transport factor and γ is the emitting efficiency of the transistor.

The transport factor β_o is a measure of the extent of recombination that takes place in the base region of the transistor; it is given by

$$\beta_o = 1 - \tfrac{1}{2}\left(\frac{W}{L}\right)^2; \; L = \sqrt{Dt} \qquad (7)$$

where W is the active base width, L is the minority-carrier diffusion length, D is the minority-carrier diffusion constant for the semiconductor material, and t is the minority-carrier life-time (i.e., the time required for 63 per cent of the minority carriers to recombine in the base region).

The emitting efficiency γ is the ratio of the carriers injected into the base from the emitter to the sum of these carriers plus the carriers injected into the emitter from the base; it is given by

$$\gamma = 1 - \frac{D_b W N_b}{D_e L_b N_e} \qquad (8)$$

where D_b and D_e are the minority-carrier diffusion constants of the base region and the emitter region, respectively, and N_b and N_e are the carrier concentrations of the base and emitter, respectively.

In a practical transistor, the diffusion length L is much greater than the active base width W, and the emitter is much more heavily "doped" than the base (i.e., the emitter conductivity σ_e is much greater than the base conductivity σ_b). As a result of the heavier "doping", the emitter carrier concentration N_e is much greater than the base carrier concentration N_b. Equations (7) and (8) indicate that for these conditions ($L \gg W$ and $N_e \gg N_b$) both the transport factor β_o and the emitter efficiency γ are approximately equal to unity.

Collector characteristics for a transistor operated in a common-base circuit with a constant emitter current are shown in Figure 1. The "total alpha" of the transistor, $\beta_o\gamma$ M, varies from a value of $\beta_o\gamma$ at low voltages, where $\beta_o\gamma$ is close to unity and M equals unity, to a value approaching infinity when V_{CB} equals V_A (because M approaches infinity at this voltage). Because stable operation can be achieved as long as the "total alpha" remains finite, operation of transistors in common base circuits is permissible at all voltages up to the collector-base avalanche voltage V_A.

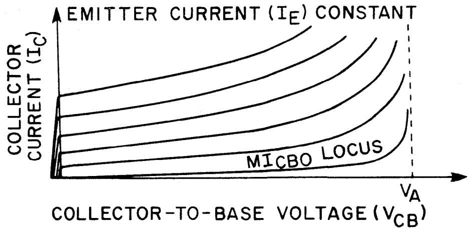


Fig. 1

Common-Emitter Avalanche Breakdown

In common-emitter circuits, avalanche breakdown occurs at the collector-to-base voltage at which the common-emitter current transfer ratio beta (β) becomes infinite. β can be expressed in terms of the common-base current transfer ratio α, as follows:

$$\beta = \frac{\alpha M}{1 - \alpha M} \qquad (9)$$

β becomes infinite when αM equals unity (i.e., when $M = 1/\alpha = 1/(\beta_o\gamma)$).

Avalanche multiplication increases the number of carriers supplied to the collector side of the junction from the depletion layer. The base is then required to supply a similar number of new carriers to the depletion layer to maintain charge neutrality in the layer. At the collector voltage at which the number of carriers supplied to the depletion layer by the base because of multiplication just equals the number of carriers gained by the base through recombination (transport factor βo) plus an effective number of opposite-type carriers injected by the base (emitting efficiency γ)*, the current transfer ratio becomes infinite because no base current is required to support collector-current flow.

* The injection of opposite-type carriers by the base is equivalent to a corresponding gain of similar carriers in the base.

As stated above, β becomes infinite when αM equals unity, or when $M = 1/\alpha$. Substitution of this value in equation (1) produces the following equation for α:

$$\alpha = 1 - \left(\frac{V_{CB}}{V_A}\right)^n \qquad (10)$$

This equation can then be solved for the value of V_{CB} at which αM equals unity (this voltage is represented by $V_{\alpha M} = 1$), as follows:

$$V\alpha M = 1 = V_A \sqrt[n]{1-\alpha} \qquad (11)$$

For collector voltages smaller than $V_{\alpha M} = 1$, base current I_B flows in the normal direction and β is positive. For voltage greater than $V_{\alpha M} = 1$, however, the base-current is reversed and β is negative. β and "total alpha" are shown as functions of V_{CB} in Figure 2.

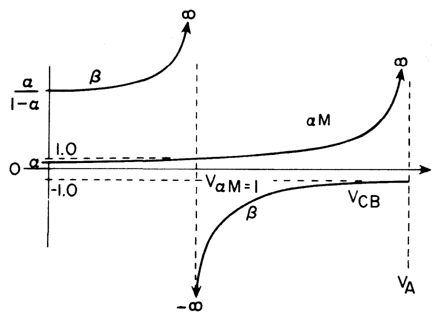


Fig. 2

The collector current I_C of a transistor operating in a common-emitter circuit with a constant-current input is given by

$$I_C = \beta\, I_B + (\beta + 1)\, M\, I_{CBO} \qquad (12)$$

The collector characteristics for such operation are shown in Figure 3.

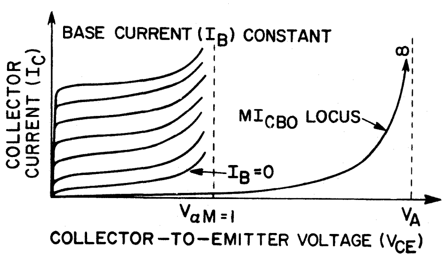


Fig. 3

Although the abscissa for these curves is collector-to-emitter voltage rather than the collector-to-base voltage previously used, no appreciable difference exists between the two except at low collector voltages, where multiplication is negligible in any case.

If negative feedback in the form of emitter resistance is applied to a transistor operating in a common-emitter circuit without constant-current input, as shown in Figure 4, the net effect is an increase in the avalanche breakdown. In the circuit of Figure 4, R_B is the series Thevenin equivalent of all external resistances presented to the transistor base terminal, R_E is the sum of both external and internal emitter resistances, and V_g is the voltage source or Thevenin voltage at the base terminal.

The base-to-emitter voltage V_{BE} can be assumed to be approximately zero, provided the internal base resistance is small compared to R_B. The base current I_B is then given by

$$I_B = \frac{V_g}{R_B} \qquad (13)$$

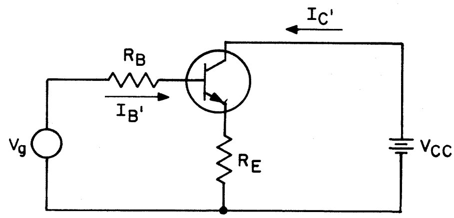


Fig. 4

The collector current I_C' for the circuit with external emitter resistance can be determined in terms of initial base current I_B, as follows:

$$I_C' = \beta\, I_B' = \frac{\beta R_B}{R_B + (\beta + 1)\, R_E} \times \beta \qquad (14)$$

Because the input is a finite source voltage, the effect of the external emitter resistance is to reduce the output or collector current. An artificial current ratio β' can be introduced to account for the change in I_C, as follows:

$$\beta' = \frac{\alpha'}{1-\alpha'} = \frac{R_B}{R_B + (\beta + 1)\, R_E} \times \beta \qquad (15)$$

Equation (15) can then be solved to determine an artificial common-base current transfer ratio α', as follows:

$$\alpha' = \alpha \times \frac{R_B}{R_B + R_E} \qquad (16)$$

This value of α' is not the true common-base current transfer ratio of the transistor, but it defines the feedback effect which results from the use of external emitter resistance when any type of source other than a pure current source is applied to the transistor in the common-emitter circuit. The term α' can be used to determine the common-emitter avalanche voltage for non-constant-base-current conditions when external emitter resistance is used. Combination of equations (11) and (16) provides the avalanche voltage, as follows:

$$V_{\alpha' M=1} = V_A \sqrt[n]{1 - \frac{R_B}{R_B + R_E}\,\alpha} \qquad (17)$$

The collector characteristics for these conditions are similar to the characteristics shown in Figure 3, except that the voltage $V_{\alpha M=1}$ is replaced by the higher voltage $V_{\alpha' M=1}$ as defined in equation (17). If R_B becomes infinite or R_E becomes zero, the condition for constant-base-current operation is reached and $V_{\alpha' M=1}$ reduces to $V_{\alpha M=1}$. If R_E becomes infinite or R_B becomes zero, $V_{\alpha' M=1}$ reduces to V_A, the common-base avalanche breakdown voltage. Therefore when a source voltage and external emitter resistance are used, the common-emitter avalanche breakdown voltage can vary from a low of $V_{\alpha M=1}$ to a high of V_A, depending upon the ratio of R_B to R_E.

Common-Emitter Voltage Breakdown as a Function of Circuit Conditions

The preceding discussion of common-emitter voltage breakdown considers only forward-bias conditions. Other types of breakdown may occur for circuit input conditions when no forward bias is applied. Several of these conditions are discussed below.

Resistive Source R

When a transistor is operated in a common-emitter circuit from a resistive source R, as shown in Figure 5, the collector current I_C is given by

$$I_C = \frac{MI_{CBO}}{1 - \alpha_N\,\alpha_i}\left[1 + \frac{\alpha_N\,(1-\alpha_i)}{(1-\alpha_N) + \frac{K_T}{q}\,\frac{(1-\alpha_N\,\alpha_i)}{I_{EBO}\,R}}\right] \qquad (18)$$

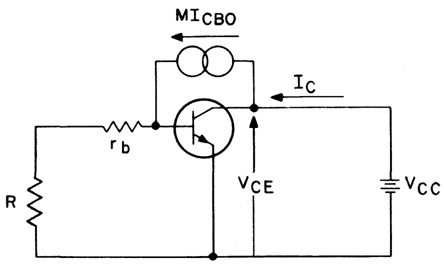


Fig. 5

where α_N is the normal common-base current transfer ratio for the transistor ($\alpha_N = \beta_0\gamma$), α_i is the current transfer ratio for inverted operation, I_{EBO} is the emitter-to-base leakage current, and the term K_T/q is equal to 0.026 volt at 25 degrees centigrade.

The total collector leakage current MI_{CBO} divides at the internal base terminal; a portion flows through the internal base resistance r_b and the source resistance R, and the balance flows through the base of the transistor to produce the collector current given by equation (18). The voltage produced by the portion flowing through r_b + R provides a forward bias between the emitter and the base.

It is assumed that the intrinsic emitter-base diode has a step-function V-I characteristic with a threshold voltage V_d, rather than an exponential characteristic, and also that all leakage current flows through the external base current as long as the forward bias is less than V_d. For this approximate transistor model, emitter injection takes place when the emitter forward bias equals V_d, and collector-to-emitter voltage breakdown occurs. The breakdown condition is given by

$$MI_{CBO}\,(R + r_b) = V_d \qquad (19)$$

Because M is related to V_{CB} and V_{CE}, equation (19) can be solved for V_{CE} for any given value of V_{CB}. The calculated value of V_{CE} would then be designated as the collector-to-emitter breakdown voltage with source resistance R, and would have the symbol BV_{CER}. The value of BV_{CER} is given by

$$BV_{CER} = V_A \sqrt[n]{1 - \frac{I_{CBO}\,(R + r_b)}{V_d}} \qquad (20)$$

Equation (20) indicates that V_{CE} is inversely proportional to the logarithm of R. Therefore, the highest breakdown voltage occurs when R is equal to zero. This voltage is designated as the shorted-base breakdown voltage, and has the symbol BV_{CES}.

If the base is opened (R approaching infinity), the threshold voltage V_d is reached for any finite value of MI_{CBO}, and transistor operation is governed by the common-emitter current transfer ratio β. For this condition, the entire leakage current MI_{CBO} must flow through the transistor base to produce a collector current equal to $(\beta + 1)\,MI_{CBO}$*. This lowest value of breakdown voltage occurs at the collector-to-emitter voltage at which β becomes infinite, which was previously defined as $V_{\alpha M=1}$.

The breakdown voltage for all other source-resistance conditions is greater than $V_{\alpha M=1}$; i.e., when emitter injection starts, total alpha (αM) is greater than unity, and β is negative. Figure 2 shows that when V_{CE} is greater than $V_{\alpha M=1}$, β increases negatively as voltage decreases. At breakdown, emitter injection occurs, and the collector current increases rapidly. This increasing current causes a decrease in collector voltage as a result of the presence of collector, emitter, and supply resistances. The decreasing collector voltage in turn causes an increase in β and collector current, so that the effect

* The intrinsic collector current I_C'' is β times the intrinsic base current I_B'', for this case MI_{CBO}. The actual measured collector current is the intrinsic collector current plus the leakage current, i.e., $I_C = I_C'' + MI_{CBO}$ and $I_C'' = \beta I_B'' = \beta MI_{CBO}$. Therefore, $I_C = \beta I_B'' + MI_{CBO}$, which reduces to $I_C = (\beta + 1)\,MI_{CBO}$.

becomes cumulative. This effect produces a negative-resistance breakdown-voltage characteristic that becomes asymptotic to $V_{\alpha}M = 1$ when β is infinite.

The source-resistance breakdown characteristics are shown in Figure 6.

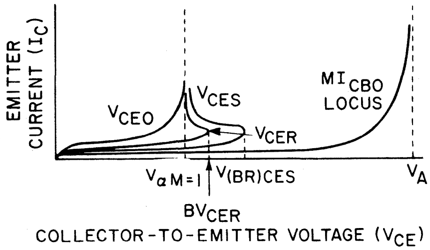


Fig. 6

Reverse Bias Voltage Source

When a reverse bias is applied between emitter and base, as shown in Figure 7, the collector breakdown voltage can be increased above the value BV_{CES}. As in the case of source resistance, no emitter injection takes place as long as the forward emitter bias is less than the threshold voltage V_d. Injection occurs when the drop across r_b resulting from MI_{CBO} is sufficient to overcome both the base supply voltage V_{BB} and V_d. This breakdown condition is given by

$$MI_{CBO}\, r_b = V_d + V_{BB} \tag{21}$$

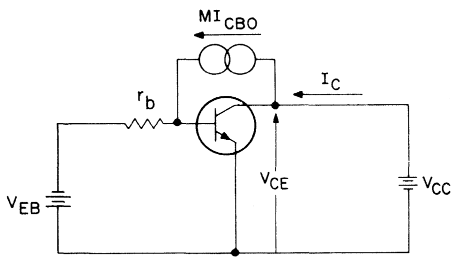


Fig. 7

An increase in V_{BB} increases the value of both M and V_{CE}. Figure 8 shows a series of breakdown curves for difference values of V_{BB}. Negative resistance occurs when the transistor operates in the region of negative β, as discussed previously. The peak value of each characteristic is designated by BV_{CEX}. The value of BV_{CEX} is given by

$$BV_{CEX} = V_A \sqrt[n]{1 - \frac{I_{CBO}\,(R + r_b)}{V_d + V_{BB}}} \tag{22}$$

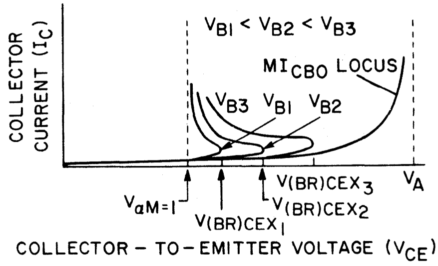


Fig. 8

Transistor Operating Regions

The various breakdown voltages discussed up to this point determine the operating regions for general-purpose transistors. In general, transistor characteristics can be divided into two regions of operation, as shown in Figure 9.

The limits of region A, the forward-bias region, are determined by the common-emitter avalanche breakdown voltage $V_{\alpha}M = 1$ and the maximum collector-current rating for the transistor. Operation anywhere in this region is permissible provided the peak dissipation ratings for the transistor are not exceeded. There are no restrictions on input-circuit conditions unless the region boundary is set by $V_{\alpha'}M = 1$ rather than $V_{\alpha}M = 1$; in this case, the conditions discussed previously apply.

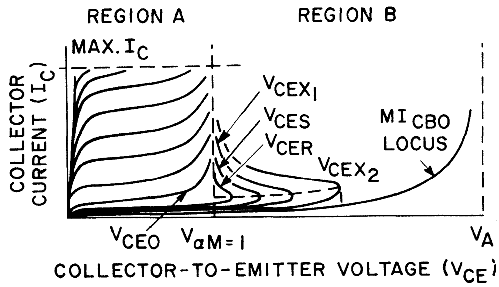


Fig. 9

The lower limit of region B, the negative-resistance is determined by the avalanche breakdown voltage $V_{\alpha}M = 1$, and the upper limit by the respective breakdown voltages for particular input conditions, i.e., BV_{CES}, BV_{CER}, BV_{CEX}, etc.

Additional Considerations

In the previous discussion of common-emitter avalanche breakdown voltage, the term $V_{\alpha}M = 1$ was assumed to be independent of collector current. However, $V_{\alpha}M = 1$ is a function of the common-base current transfer ratio α (as shown in equation 10), which varies with I_C. It follows, therefore, that $V_{\alpha}M = 1$ must change with I_C. β and α vary with I_C differently for abrupt- and graded-junction transistors.

Figure 10 shows the variation of β for typical transistors.

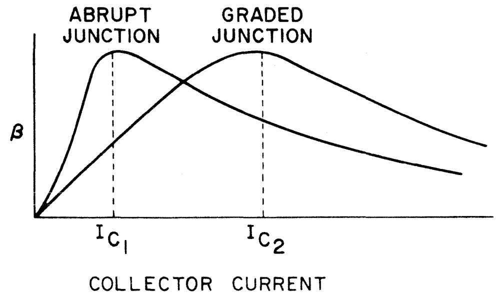


Fig. 10

Because the minimum value of $V_{\alpha M} = 1$ occurs at the peak of the curves shown in Figure 10, it is possible to construct a locus of points on the V_C - I_C curves of a transistor where the total alpha αM is equal to unity, as shown in Figure 11. This locus curve has only a positive-resistance slope for abrupt-junction types, but has both positive and negative-resistance slopes for graded-junction types.

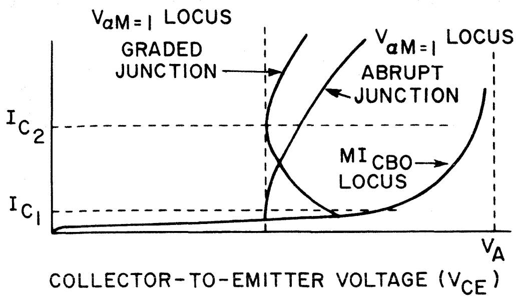


Fig. 11

Because both the forward-bias and reverse-bias curves become asymptotic to $V_{\alpha M} = 1$ for common-emitter operation, this variation of $V_{\alpha M} = 1$ with I_C modifies all the breakdown curves. It also explains why some forward bias curves, such as V_{CEO} can have a negative resistance component for some types of transistors. This effect is observed for most diffused types that have graded junctions; because alloy transistors have abrupt junctions, these types do not normally have negative-resistance forward-biased voltage characteristics.

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TA148	1N540	SSD-206	255	3	RECT
TA149	1N1095	SSD-206	255	3	RECT
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TA1003	1N440B	SSD-206	252	5	RECT
TA1004	1N441B	SSD-206	252	5	RECT
TA1005	1N442B	SSD-206	252	5	RECT
TA1006	1N443B	SSD-206	252	5	RECT
TA1007	1N444B	SSD-206	252	5	RECT
TA1008	1N445B	SSD-206	252	5	RECT
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TA1014	1N2862A	SSD-206	265	91	RECT
TA1015	1N2863A	SSD-206	265	91	RECT
TA1016	1N2864A	SSD-206	265	91	RECT
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TA1054	1N1197A	SSD-206	287	6	RECT
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TA1078	1N1202A	SSD-206	283	20	RECT
TA1079	1N1203A	SSD-206	283	20	RECT
TA1080	1N1204A	SSD-206	283	20	RECT
TA1081	1N1205A	SSD-206	283	20	RECT
TA1082	1N1206A	SSD-206	283	20	RECT
TA1085	1N1183A	SSD-206	291	38	RECT
TA1086	1N1184A	SSD-206	291	38	RECT
TA1087	1N1186A	SSD-206	291	38	RECT
TA1095	1N1197A	SSD-206	287	6	RECT
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TA1121	1N3254	SSD-206	294	41	RECT
TA1122	1N3255	SSD-206	294	41	RECT
TA1123	1N3256	SSD-206	294	41	RECT
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TA1179	2N689	SSD-206	225	96	SCR
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TA1216	1N1189A	SSD-206	291	38	RECT
TA1217	1N1190A	SSD-206	291	38	RECT
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TA1910A	2N697	SSD-204	493	16	PWR
TA1951	2N1493	SSD-205	24	10	RF
TA1986	2N699	SSD-204	495	22	PWR
TA2053	2N1613	SSD-204	498	106	PWR
TA2053A	2N1711	SSD-204	503	26	PWR
TA2053B	2N2102	SSD-204	498	106	PWR
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TA2235A	2N2405	SSD-204	507	34	PWR
TA2267	2N2631	SSD-205	28	32	RF
TA2275	2N2895	SSD-204	517	143	PWR
TA2276	2N2896	SSD-204	517	143	PWR
TA2277	2N2897	SSD-204	517	143	PWR
TA2307	2N3375	SSD-205	52	386	RF
TA2311	2N2876	SSD-205	28	32	RF
TA2333	2N2857	SSD-205	33	61	RF
TA2358	2N918	SSD-205	20	83	RF
TA2358A	2N3600	SSD-205	20	83	RF
TA2363	2N3839	SSD-205	69	229	RF
TA2388	2N3229	SSD-205	45	50	RF
TA2402A	2N3054	SSD-204	45	527	PWR
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TA2442	2N3870	SSD-206	218	578	SCR
TA2444	2N3871	SSD-206	218	578	SCR
TA2447	2N3872	SSD-206	218	578	SCR
TA2458	2N3439	SSD-204	286	64	PWR
TA2462	2N3118	SSD-205	37	42	RF
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TA2616	2N3632	SSD-205	52	386	RF
TA2617	2N3529	SSD-206	144	114	SCR
TA2618	2N3670	SSD-206	203	116	SCR
TA2619	40280	SSD-205	275	301	RF
TA2620	40281	SSD-205	279	68	RF
TA2621	2N3668	SSD-206	203	116	SCR
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TA2655	S3700M	SSD-206	172	306	SCR
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TA2685	T2700D	SSD-206	62	351	TRI
TA2692	2N3733	SSD-205	64	72	RF
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TA2761	40608	SSD-205	291	356	RF
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TA2774	2N4102	SSD-206	144	114	SCR
TA2775	2N4103	SSD-206	203	116	SCR
TA2791	2N5102	SSD-205	113	279	RF
TA2792	2N4933	SSD-205	92	249	RF
TA2793	2N5070	SSD-205	100	268	RF
TA2800	2N5109	SSD-205	118	281	RF
TA2808	2N4348	SSD-204	149	526	PWR
TA2809	2N4347	SSD-204	133	528	PWR
TA2819	2N5415	SSD-204	292	336	PWR
TA2819A	2N5416	SSD-204	292	336	PWR
TA2827	2N5071	SSD-205	105	269	RF
TA2828	2N4932	SSD-205	92	249	RF
TA2836	2N5441	SSD-206	55	593	TRI
TA2837	2N5442	SSD-206	55	593	TRI
TA2838	2N5444	SSD-206	55	593	TRI
TA2839	2N5445	SSD-206	55	593	TRI
TA2840	3N128	SSD-201	634	309	MOS/FET
TA2845	1N5214	SSD-206	270	245	RECT
TA2845A	1N5213	SSD-206	270	245	RECT
TA2845B	1N5212	SSD-206	270	245	RECT
TA2845C	1N5211	SSD-206	270	245	RECT
TA2871	2N4240	SSD-204	304	138	PWR
TA2875	2N4440	SSD-205	87	217	RF
TA2892	T2300A	SSD-206	33	470	TRI
TA2829A	T2302A	SSD-206	33	470	TRI
TA2893	T2300B	SSD-206	33	470	TRI
TA2893A	T2302B	SSD-206	33	470	TRI
TA2894	T2300D	SSD-206	33	470	TRI
TA2894A	T2302D	SSD-206	33	470	TRI
TA2911	2N5294	SSD-204	61	322	PWR
TA5032	CA3000	SSD-201	288	121	LIC
TA5033	CA3001	SSD-201	294	122	LIC
TA5035	CA3002	SSD-201	256	123	LIC
TA5037	CA3004	SSD-201	300	124	LIC
TA5112	CA3005	SSD-201	306	125	LIC
TA5112A	CA3006	SSD-201	306	125	LIC
TA5115B	CA3007	SSD-201	313	126	LIC
TA5124	CA3008	SSD-201	80	316	LIC
TA5158	CA3015	SSD-201	80	316	LIC
TA5164	CD2150	SSD-201	409	308	LIC
TA5165	CD2151	SSD-201	409	308	LIC
TA5166	CD2152	SSD-201	409	308	LIC
TA5180	CA3010	SSD-201	80	316	LIC
TA5183	CA3033	SSD-201	61	360	LIC
TA5183A	CA3033A	SSD-201	61	360	LIC
TA5213	CA3011	SSD-201	262	128	LIC
TA5214	CA3012	SSD-201	262	128	LIC
TA5218	CA3023	SSD-201	276	243	LIC
TA5219	CA3021	SSD-201	276	243	LIC
TA5220	CA3020	SSD-201	268	339	LIC
TA5222	CA3018	SSD-201	160	338	LIC
TA5222A	CA3018A	SSD-201	160	338	LIC
TA5225	CA3019	SSD-201	118	236	LIC
TA5234	CA3013	SSD-201	471	129	LIC
TA5235	CA3014	SSD-201	471	129	LIC
TA5236	CA3022	SSD-201	276	243	LIC
TA5253	CA3016	SSD-201	80	316	LIC
TA5254	CA3030	SSD-201	80	316	LIC
TA5261	CD2153	SSD-201	409	308	LIC
TA5277	CA3001	SSD-201	294	122	LIC
TA5278	CA3029	SSD-201	80	316	LIC
TA5282	CA3004	SSD-201	300	124	LIC
TA5315	CA3043	SSD-201	466	331	LIC
TA5316	CA3041	SSD-201	498	318	LIC
TA5317A	CA3042	SSD-201	506	319	LIC
TA5327C	CA3040	SSD-201	282	363	LIC
TA5333	CA3036	SSD-201	158	275	LIC
TA5334	CA3035	SSD-201	243	274	LIC
TA5334	CA3035V1	SSD-201	243	274	LIC
TA5345	CA3028A	SSD-201	318	382	LIC
TA5345A	CA3028B	SSD-201	318	382	LIC
TA5346	CA3015A	SSD-201	89	310	LIC
TA5347	CA3010A	SSD-201	89	310	LIC
TA5348	CA3030A	SSD-201	89	310	LIC
TA5349	CA3029A	SSD-201	89	310	LIC
TA5350	CA3016A	SSD-201	89	310	LIC
TA5351	CA3008A	SSD-201	89	310	LIC
TA5360	CA3044	SSD-201	484	340	LIC
TA5361B	CD4000A	SSD-203	30	479	COS/MOS
TA5369	CA3040	SSD-201	282	363	LIC
TA5371B	CA3062	SSD-201	367	421	LIC
TA5385CV	CD4024AK	SSD-203	120	503	COS/MOS
TA5401	CA3038	SSD-201	80	316	LIC
TA5401	CA3038A	SSD-201	89	310	LIC
TA5402	CA3037	SSD-201	80	316	LIC
TA5402	CA3037A	SSD-201	89	310	LIC
TA5455B	CD4001A	SSD-203	30	479	COS/MOS
TA5456B	CD4002A	SSD-203	30	479	COS/MOS
TA5457	CA3045	SSD-201	177	341	LIC
TA5458	CA3046	SSD-201	177	341	LIC
TA5460AV	CD4016AK	SSD-203	84	479	COS/MOS
TA5507	CA3050	SSD-201	329	361	LIC
TA5513	CA3026	SSD-201	226	388	LIC
TA5516	CA3039	SSD-201	122	343	LIC
TA5517C	CA3064	SSD-201	490	396	LIC
TA5519V	CD4008AK	SSD-203	49	479	COS/MOS
TA5523A	CA3048	SSD-201	247	377	LIC
TA5537	CA3049T	SSD-201	234	611	LIC
TA5551	CD4000AK	SSD-203	30	479	COS/MOS
TA5553	CD4007AK	SSD-203	43	479	COS/MOS
TA5554	CD4001AK	SSD-203	30	479	COS/MOS
TA5555	CD4002AK	SSD-203	30	479	COS/MOS
TA5556B	CD4006AK	SSD-203	37	479	COS/MOS
TA5561	CA3047A	SSD-201	61	360	LIC
TA5562	CA3047	SSD-201	61	360	LIC
TA5578V	CD4014AK	SSD-203	74	479	COS/MOS
TA5579V	CD4015AK	SSD-203	79	479	COS/MOS
TA5580V	CD4018AK	SSD-203	95	479	COS/MOS
TA5615A	CA3059	SSD-201	338	490	LIC
TA5625A	CA3066	SSD-201	533	466	LIC
TA5628C	CA3089E	SSD-201	455	561	LIC
TA5634	CD2154	SSD-201	421	402	LIC
TA5645	CA3060E	SSD-201	38	537	LIC
TA5649A	CA3070	SSD-201	549	468	LIC
TA5652V	CD4019AK	SSD-203	100	479	COS/MOS
TA5655	CA3051	SSD-201	329	361	LIC
TA5660V	CD4009AK	SSD-203	54	479	COS/MOS
TA5668V	CD4010AK	SSD-203	54	479	COS/MOS
TA5672	CA3052	SSD-201	432	387	LIC
TA5675V	CD4013AK	SSD-203	68	479	COS/MOS
TA5677V	CD4044AK	SSD-203	214	590	COS/MOS
TA5681V	CD4011AK	SSD-203	61	479	COS/MOS
TA5682V	CD4012AK	SSD-203	61	479	COS/MOS
TA5683V	CD4021AK	SSD-203	110	479	COS/MOS
TA5684V	CD4017AK	SSD-203	90	479	COS/MOS
TA5690X	CD2501E	SSD-201	403	392	LIC
TA5702B	CA3071	SSD-201	549	468	LIC
TA5716V	CD4057AK	SSD-203	272	635	COS/MOS
TA5716W	CD4057AD	SSD-203	272	635	COS/MOS
TA5718	CA3054	SSD-201	226	388	LIC
TA5721X	CD2500E	SSD-201	403	392	LIC
TA5733	CA3053	SSD-201	318	382	LIC
TA5752	CA3067	SSD-201	533	466	LIC
TA5757	CA3076	SSD-201	479	430	LIC
TA5758B	CA3085	SSD-201	375	491	LIC
TA5776V	CD4020AK	SSD-203	105	479	COS/MOS
TA5785X	CD2503E	SSD-201	403	392	LIC
TA5786X	CD2502E	SSD-201	403	392	LIC
TA5790	CA3060D	SSD-201	38	537	LIC
TA5795	CA3058	SSD-201	338	490	LIC
TA5797	CA741T	SSD-201	74	531	LIC
TA5799A	CA3084	SSD-201	134	482	LIC
TA5807	CA3078T	SSD-201	52	535	LIC
TA5814	CA3065	SSD-201	514	412	LIC
TA5816	CA3080	SSD-201	30	475	LIC
TA5820	CA3541D	SSD-201	395	536	LIC

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TA5855A	CA3091D	SSD-201	383	534	LIC
TA5858	CA3081	SSD-201	126	480	LIC
TA5866	CA3075	SSD-201	462	429	LIC
TA5867V	CD4023AK	SSD-203	61	479	COS/MOS
TA5867W	CD4023AD	SSD-203	61	479	COS/MOS
TA5867X	CD4023AE	SSD-203	61	479	COS/MOS
TA5872V	CD4027AK	SSD-203	135	503	COS/MOS
TA5873V	CD4028AK	SSD-203	141	503	COS/MOS
TA5876W	CD4035AD	SSD-203	177	568	COS/MOS
TA5878W	CD4034AD	SSD-203	169	575	COS/MOS
TA5884AV	CD4022AK	SSD-203	115	479	COS/MOS
TA5884W	CD4022AD	SSD-203	115	479	COS/MOS
TA5884AX	CD4022AE	SSD-203	115	479	COS/MOS
TA5897X	CD2501E	SSD-201	698	392	LIC
TA5898X	CD2503E	SSD-201	698	392	LIC
TA5899X	CD2500E	SSD-201	698	392	LIC
TA5900X	CD2502E	SSD-201	698	392	LIC
TA5912B	CA3072	SSD-201	549	468	LIC
TA5914C	CA3068	SSD-201	525	467	LIC
TA5920V	CD4025AK	SSD-203	30	479	COS/MOS
TA5920W	CD4025AD	SSD-203	30	479	COS/MOS
TA5920X	CD4025AE	SSD-203	30	479	COS/MOS
TA5925V	CD4029AK	SSD-203	146	503	COS/MOS
TA5925W	CD4029AD	SSD-203	146	503	COS/MOS
TA5925X	CD4029AE	SSD-203	146	503	COS/MOS
TA5926V	CD4036AK	SSD-203	184	613	COS/MOS
TA5926W	CD4036AD	SSD-203	184	613	COS/MOS
TA5932	CA3090Q	SSD-201	440	502	LIC
TA5940V	CD4030AK	SSD-203	153	503	COS/MOS
TA5940W	CD4030AD	SSD-203	153	503	COS/MOS
TA5940X	CD4030AE	SSD-203	153	503	COS/MOS
TA5951V	CD4038AK	SSD-203	164	503	COS/MOS
TA5951W	CD4038AD	SSD-203	164	503	COS/MOS
TA5951X	CD4038AE	SSD-203	164	503	COS/MOS
TA5957	CA3018L	SSD-201	605	515	LIC
TA5958	CA3039L	SSD-201	605	515	LIC
TA5959	CA3045L	SSD-201	605	515	LIC
TA5960	CA3054L	SSD-201	605	515	LIC
TA5963V	CD4032AK	SSD-203	164	503	COS/MOS
TA5963W	CD4032AD	SSD-203	164	503	COS/MOS
TA5963X	CD4032AE	SSD-203	164	503	COS/MOS
TA5964	CA3015L	SSD-201	605	515	LIC
TA5975	CA3028AL	SSD-201	605	515	LIC
TA5978	CA3084L	SSD-201	605	515	LIC
TA5979	CA741L	SSD-201	605	515	LIC
TA5989	CD4031AD	SSD-203	158	569	COS/MOS
TA5998	CA3083	SSD-201	130	481	LIC
TA5999W	CD4037AD	SSD-203	191	576	COS/MOS
TA6007W	CD4051AD	SSD-203	258	Prel.	COS/MOS
TA6010V	CD4047AK	SSD-203	233	623	COS/MOS
TA6010W	CD4047AD	SSD-203	233	623	COS/MOS
TA6010X	CD4047AE	SSD-203	233	623	COS/MOS
TA6011	CD4042AD	SSD-203	210	589	COS/MOS
TA6014	CA3068	SSD-201	525	467	LIC
TA6018V	CD4026AK	SSD-203	126	503	COS/MOS
TA6018W	CD4026AD	SSD-203	126	503	COS/MOS
TA6018X	CD4026AE	SSD-203	126	503	COS/MOS
TA6029	CA741CT	SSD-201	74	531	LIC
TA6031V	CD4041AK	SSD-203	203	572	COS/MOS
TA6031W	CD4041AD	SSD-203	203	572	COS/MOS
TA6031X	CD4041AE	SSD-203	203	572	COS/MOS
TA6033	CA3082	SSD-201	126	480	LIC
TA6037	CA748CT	SSD-201	74	531	LIC
TA5037A	CA748T	SSD-201	74	531	LIC
TA6044	CA3086	SSD-201	183	483	LIC
TA6051	CA3079	SSD-201	338	490	LIC
TA6062W	CD4045AD	SSD-203	220	614	COS/MOS
TA6062X	CD4045AE	SSD-203	220	614	COS/MOS
TA6065V	CD4040AK	SSD-203	197	624	COS/MOS
TA6065W	CD4040AD	SSD-203	197	624	COS/MOS
TA6065X	CD4040AE	SSD-203	197	624	COS/MOS
TA6080V	CD4043AK	SSD-203	214	590	COS/MOS
TA6080W	CD4043AD	SSD-203	214	590	COS/MOS
TA6080X	CD4043AE	SSD-203	214	590	COS/MOS
TA6081V	CD4044AK	SSD-203	214	590	COS/MOS
TA6081W	CD4044AD	SSD-203	214	590	COS/MOS
TA6081X	CD4044AE	SSD-203	214	590	COS/MOS
TA6084	CA3146AE	SSD-201	166	532	LIC
TA6091	CA3118AT	SSD-201	166	532	LIC
TA6094	CA3183AE	SSD-201	166	532	LIC
TA6111	CA1458T	SSD-201	74	531	LIC
TA6111A	CA1558T	SSD-201	74	531	LIC
TA6116V	CD4046AK	SSD-203	226	637	COS/MOS
TA6116W	CD4046AD	SSD-203	226	637	COS/MOS
TA6116X	CD4046AE	SSD-203	226	637	COS/MOS
TA6119	CA3093E	SSD-201	152	533	LIC
TA6122C	CA3100T	SSD-201	98	625	LIC
TA6144B	CA3121E	SSD-201	567	688	LIC
TA6145V	CD4039AK	SSD-203	184	613	COS/MOS
TA6145W	CD4039AD	SSD-203	184	613	COS/MOS
TA6145X	CD4039AE	SSD-203	184	613	COS/MOS
TA6153W	CD4052AD	SSD-203	258	Prel.	COS/MOS
TA6154W	CD4053AD	SSD-203	258	Prel.	COS/MOS
TA6155D	CA3123E	SSD-201	450	631	LIC
TA6157	CA747CE	SSD-201	74	531	LIC
TA6157A	CA747E	SSD-201	74	531	LIC
TA6164	CA3094T	SSD-201	346	598	LIC
TA6165A	CA3094AT	SSD-201	346	598	LIC
TA6181	CA3146E	SSD-201	166	532	LIC
TA6182	CA3118T	SSD-201	166	532	LIC
TA6183	CA3183E	SSD-201	166	532	LIC
TA6189	CA3099E	SSD-201	359	620	LIC
TA6220	CA2111AE	SSD-201	520	612	LIC
TA6228	CA3102E	SSD-201	234	611	LIC
TA6237V	CD4054AK	SSD-203	266	634	COS/MOS
TA6237W	CD4054AD	SSD-203	266	634	COS/MOS
TA6237X	CD4054AE	SSD-203	266	634	COS/MOS
TA6238V	CD4055AK	SSD-203	266	634	COS/MOS
TA6238W	CD4055AD	SSD-203	266	634	COS/MOS
TA6238X	CD4055AE	SSD-203	266	634	COS/MOS
TA6243X	CA3120E	SSD-201	581	691	LIC
TA6246V	CD4049AK	SSD-203	251	599	COS/MOS
TA6246W	CD4049AD	SSD-203	251	599	COS/MOS
TA6246X	CD4049AE	SSD-203	251	599	COS/MOS
TA6250V	CD4048AK	SSD-203	244	636	COS/MOS
TA6250W	CD4048AD	SSD-203	244	636	COS/MOS
TA6250X	CD4048AE	SSD-203	244	636	COS/MOS
TA6251V	CD4056AK	SSD-203	266	634	COS/MOS
TA6251W	CD4056AD	SSD-203	266	634	COS/MOS
TA6251X	CD4056AE	SSD-203	266	634	COS/MOS
TA6265V	CD4050AK	SSD-203	251	599	COS/MOS
TA6265W	CD4050AD	SSD-203	251	599	COS/MOS
TA6265X	CD4050AE	SSD-203	251	599	COS/MOS
TA6269X	CA3095E	SSD-201	189	591	LIC
TA6270X	CA3096E	SSD-201	141	595	LIC
TA6270AX	CA3096AE	SSD-201	141	595	LIC
TA6281X	CA3097E	SSD-201	199	633	LIC
TA6281X	CA3097E	SSD-201	199	633	LIC
TA6289X	CA747CE	SSD-201	74	531	LIC
TA6289AX	CA747E	SSD-201	74	531	LIC
TA6306	CA3401E	SSD-201	113	630	LIC
TA6309	CA3049L	SSD-201	605	515	LIC
TA6314T	CA1458T	SSD-201	74	531	LIC
TA6314T	CA1558T	SSD-201	74	531	LIC
TA6319	CA3126Q	SSD-201	565	Prel.	LIC
TA6330T	CA3094AT	SSD-201	346	598	LIC
TA6368X	CA3600E	SSD-201	213	619	LIC
TA6379X	CA3072	SSD-201	549	468	LIC
TA6389T	CA3080	SSD-201	30	475	LIC
TA6391W	CD4066AD	SSD-203	303	Prel.	COS/MOS
TA7003	2N5470	SSD-205	140	350	RF
TA7005	2N6249	SSD-204	385	523	PWR
TA7006	2N6250	SSD-204	385	523	PWR
TA7007	2N6251	SSD-204	385	523	PWR
TA7016	2N5575	SSD-204	162	359	PWR
TA7017	2N5578	SSD-204	162	359	PWR
TA7032	3N138	SSD-201	639	283	MOS/FET
TA7047	2N4427	SSD-205	81	228	RF
TA7048	1N5218	SSD-206	270	245	RECT
TA7048A	1N5217	SSD-206	270	245	RECT
TA7048B	1N5216	SSD-206	270	245	RECT
TA7048C	1N5215	SSD-206	270	245	RECT
TA7078	40606	SSD-207	168	600	RF
TA7079	40577	SSD-207	148	297	RF
TA7080	40578	SSD-207	155	298	RF
TA7090	JAN2N3866	SSD-207	81	–	RF
TA7121	2N5320	SSD-204	429	325	PWR
TA7122	2N5321	SSD-204	429	325	PWR
TA7124	2N5322	SSD-204	429	325	PWR

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TA7125	2N5323	SSD-204	429	325	PWR
TA7130	2N5804	SSD-204	379	407	PWR
TA7130A	2N5805	SSD-204	379	407	PWR
TA7134	2N6177	SSD-204	278	508	PWR
TA7137	2N5296	SSD-204	61	322	PWR
TA7146	2N5090	SSD-205	109	270	RF
TA7149	40600	SSD-201	712	333	MOS/FET
TA7150	40603	SSD-201	720	334	MOS/FET
TA7151	40604	SSD-201	720	334	MOS/FET
TA7155	2N5293	SSD-204	61	322	PWR
TA7156	2N5295	SSD-204	61	322	PWR
TA7189	40602	SSD-201	712	333	MOS/FET
TA7205	2N5921	SSD-205	181	427	RF
TA7238	2N5262	SSD-204	423	313	PWR
TA7244	3N139	SSD-201	643	284	MOS/FET
TA7262	40601	SSD-201	712	333	MOS/FET
TA7264	2N5954	SSD-204	170	675	PWR
TA7265	2N5955	SSD-204	170	675	PWR
TA7266	2N5956	SSD-204	170	675	PWR
TA7270	2N5781	SSD-204	34	413	PWR
TA7271	2N5782	SSD-204	34	413	PWR
TA7272	2N5783	SSD-204	34	413	PWR
TA7274	3N141	SSD-201	667	285	MOS/FET
TA7275	3N143	SSD-201	634	309	MOS/FET
TA7279	2N6248	SSD-204	217	677	PWR
TA7280	2N6247	SSD-204	217	677	PWR
TA7281	2N6246	SSD-204	217	677	PWR
TA7285	2N5202	SSD-204	443	299	PWR
TA7289	2N5784	SSD-204	34	413	PWR
TA7290	2N5785	SSD-204	34	413	PWR
TA7291	2N5786	SSD-204	34	413	PWR
TA7303	2N5180	SSD-205	130	289	RF
TA7306	3N142	SSD-201	648	286	MOS/FET
TA7311	2N5496	SSD-204	90	353	PWR
TA7312	2N5497	SSD-204	90	353	PWR
TA7313	2N5494	SSD-204	90	353	PWR
TA7314	2N5495	SSD-204	90	353	PWR
TA7315	2N5492	SSD-204	90	353	PWR
TA7316	2N5493	SSD-204	90	353	PWR
TA7317	2N5490	SSD-204	90	353	PWR
TA7318	2N5491	SSD-204	90	353	PWR
TA7319	2N5179	SSD-204	124	288	RF
TA7322	2N5189	SSD-204	418	296	PWR
TA7323	2N5671	SSD-204	481	383	PWR
TA7323A	2N5672	SSD-204	481	383	PWR
TA7327	JANTX2N3866	SSD-207	81	–	RF
TA7328	JANTX2N3553	SSD-207	80	–	RF
TA7329	JANTX2N3375	SSD-207	80	–	RF
TA7337	2N6032	SSD-204	487	462	PWR
TA7337A	2N6033	SSD-204	487	462	PWR
TA7352	3N153	SSD-201	659	320	MOS/FET
TA7353	3N152	SSD-201	654	314	MOS/FET
TA7354	JAN2N4440	SSD-207	80	–	RF
TA7355	JANTX2N4440	SSD-207	80	–	RF
TA7358	JANTX2N5071	SSD-207	81	–	RF
TA7360	JAN2N5071	SSD-207	81	–	RF
TA7361	40605	SSD-205	318	389	RF
TA7362	2N5297	SSD-204	61	322	PWR
TA7363	2N5298	SSD-204	61	322	PWR
TA7364	T2800B	SSD-206	69	364	TRI
TA7365	T2800D	SSD-206	69	364	TRI
TA7367	2N5918	SSD-205	164	448	RF
TA7374	3N159	SSD-201	675	326	MOS/FET
TA7375	3N154	SSD-201	662	335	MOS/FET
TA7381	2N6098	SSD-204	121	485	PWR
TA7382	2N6099	SSD-204	121	485	PWR
TA7383	2N6100	SSD-204	121	485	PWR
TA7384	2N6101	SSD-204	121	485	PWR
TA8385	2N6102	SSD-204	121	485	PWR
TA7386	2N6103	SSD-204	121	485	PWR
TA7399	40673	SSD-201	745	381	MOS/FET
TA7401	D3202U	SSD-206	350	577	DIAC
TA7403	40836	SSD-205	298	497	RF
TA7404	S2800B	SSD-206	166	501	SCR
TA7405	S2800D	SSD-206	166	501	SCR
TA7408	2N5914	SSD-205	152	424	RF
TA7409	2N5915	SSD-205	152	424	RF
TA7410	2N6212	SSD-204	312	507	PWR
TA7411	2N5916	SSD-205	158	425	RF
TA7420	2N5840	SSD-204	356	410	PWR
TA7426	2N5443	SSD-206	55	593	TRI
TA7427	2N5446	SSD-206	55	593	TRI
TA7428	2N5567	SSD-206	92	457	TRI
TA7429	2N5568	SSD-206	92	457	TRI
TA7430	2N5571	SSD-206	85	458	TRI
TA7431	2N5572	SSD-206	85	458	TRI
TA7434	S2600B	SSD-206	156	496	SCR
TA7435	S2600D	SSD-206	156	496	SCR
TA7441	T6401B	SSD-206	107	459	TRI
TA7442	T6401D	SSD-206	107	459	TRI
TA7452	S3705M	SSD-206	187	354	SCR
TA7453	S3706M	SSD-206	187	354	SCR
TA7454	D2601EF	SSD-206	303	354	RECT
TA7455	D2601DF	SSD-206	303	354	RECT
TA7456	D2600EF	SSD-206	303	354	RECT
TA7461	T6411B	SSD-206	107	459	TRI
TA7462	T6411D	SSD-206	107	459	TRI
TA7463	S2620B	SSD-206	156	496	SCR
TA7464	S2620D	SSD-206	156	496	SCR
TA7465	S2610B	SSD-206	156	496	SCR
TA7466	S2610D	SSD-206	156	496	SCR
TA7467	T4101M	SSD-206	92	457	TRI
TA7468	T4100M	SSD-206	85	458	TRI
TA7477	2N5913	SSD-205	146	423	RF
TA7479	2N5569	SSD-206	92	457	TRI
TA7480	2N5570	SSD-206	92	457	TRI
TA7481	T4111M	SSD-206	92	457	TRI
TA7482	2N5573	SSD-206	85	458	TRI
TA7483	2N5574	SSD-206	85	458	TRI
TA7484	T4110M	SSD-206	85	458	TRI
TA7487	2N5920	SSD-205	175	440	RF
TA7500	2N5754	SSD-206	28	414	TRI
TA7501	2N5755	SSD-206	28	414	TRI
TA7502	2N5756	SSD-206	28	414	TRI
TA7503	2N5757	SSD-206	28	414	TRI
TA7504	T6420B	SSD-206	55	593	TRI
TA7505	T6420D	SSD-206	55	593	TRI
TA7506	T6420M	SSD-206	55	593	TRI
TA7507	S6420B	SSD-206	218	578	SCR
TA7508	S6420D	SSD-206	218	578	SCR
TA7509	S6420M	SSD-206	218	578	SCR
TA7513	2N5838	SSD-204	356	410	PWR
TA7514	40964	SSD-205	351	581	RF
TA7518	T2800M	SSD-206	69	364	TRI
TA7530	2N5839	SSD-204	356	410	PWR
TA7532	2N5919A	SSD-205	169	505	RF
TA7534	2N6354	SSD-204	469	582	PWR
TA7542	S3800MF	SSD-206	199	639	ITR
TA7543	S3800M	SSD-206	199	639	ITR
TA7543	S2060Q	SSD-206	138	654	SCR
TA7545	S2060Y	SSD-206	138	654	SCR
TA7546	S2060F	SSD-206	138	654	SCR
TA7547	T4121B	SSD-206	92	457	TRI
TA7548	T4121D	SSD-206	92	457	TRI
TA7549	T4121M	SSD-206	92	457	TRI
TA7550	T4120B	SSD-206	85	458	TRI
TA7551	T4120D	SSD-206	85	458	TRI
TA7552	T4120M	SSD-206	85	458	TRI
TA7553	S7430M	SSD-206	238	408	SCR
TA7554	2N6178	SSD-204	435	562	PWR
TA7555	2N6179	SSD-204	435	562	PWR
TA7556	2N6180	SSD-204	435	562	PWR
TA7557	2N6181	SSD-204	435	562	PWR
TA7563	S6200B	SSD-206	210	418	SCR
TA7564	S6200D	SSD-206	210	418	SCR
TA7565	S6200M	SSD-206	210	418	SCR
TA7570	S6210B	SSD-206	210	418	SCR
TA7571	S6210D	SSD-206	210	418	SCR
TA7579	T2313A	SSD-206	28	414	TRI
TA7580	T2313B	SSD-206	28	414	TRI
TA7581	T2313D	SSD-206	28	414	TRI
TA7582	2N5757	SSD-206	28	414	TRI
TA7582	T2313M	SSD-206	28	414	TRI
TA7583	T6401M	SSD-206	107	459	TRI
TA7584	T6411M	SSD-206	107	459	TRI
TA7588	40965	SSD-205	351	581	RF
TA7589	2N5994	SSD-205	199	453	RF
TA7590	2N3650	SSD-206	238	408	SCR
TA7591	2N3651	SSD-206	238	408	SCR
TA7592	2N3652	SSD-206	238	408	SCR

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TA7599	S6220B	SSD-206	210	418	SCR
TA7600	S6220D	SSD-206	210	418	SCR
TA7601	S6220M	SSD-206	210	418	SCR
TA7602	T6421B	SSD-206	107	459	TRI
TA7603	T6421D	SSD-206	107	459	TRI
TA7604	T6421M	SSD-206	107	459	TRI
TA7614	T4104B	SSD-206	99	443	TRI
TA7615	T4104D	SSD-206	99	443	TRI
TA7616	T4114B	SSD-206	99	443	TRI
TA7617	T4114D	SSD-206	99	443	TRI
TA7618	T4103B	SSD-206	99	443	TRI
TA7619	T4103D	SSD-206	99	443	TRI
TA7620	T4113B	SSD-206	99	443	TRI
TA7621	T4113D	SSD-206	99	443	TRI
TA7626A	HC2000H	SSD-204	555	566	HYB
TA7642	T4105B	SSD-206	99	443	TRI
TA7643	T4105D	SSD-206	99	443	TRI
TA7644	T4115B	SSD-206	99	443	TRI
TA7645	T4115D	SSD-206	99	443	TRI
TA7646	T6405B	SSD-206	114	487	TRI
TA7647	T6405D	SSD-206	114	487	TRI
TA7648	T6415B	SSD-206	114	487	TRI
TA7649	T6415D	SSD-206	114	487	TRI
TA7650	T6405B	SSD-206	114	487	TRI
TA7651	T6405D	SSD-206	114	487	TRI
TA7652	T6414B	SSD-206	114	487	TRI
TA7653	T6414D	SSD-206	114	487	TRI
TA7654	T2304B	SSD-206	41	441	TRI
TA7655	T2304D	SSD-206	41	441	TRI
TA7656	T2305B	SSD-206	41	441	TRI
TA7657	T2305D	SSD-206	41	441	TRI
TA7669	3N187	SSD-201	690	436	MOS/FET
TA7670	S6420A	SSD-206	218	578	SCR
TA7673	2N6078	SSD-204	318	492	PWR
TA7679	40837	SSD-205	298	497	RF
TA7680	40941	SSD-205	342	554	RF
TA7684	3N200	SSD-201	698	437	MOS/FET
TA7686	40893	SSD-205	304	514	RF
TA7706	2N6105	SSD-205	221	504	RF
TA7707	2N6104	SSD-205	221	504	RF
TA7719	2N6211	SSD-204	312	507	PWR
TA7739	2N6175	SSD-204	278	508	PWR
TA7740	2N6176	SSD-204	278	508	PWR
TA7741	2N6107	SSD-204	177	676	PWR
TA7742	2N6109	SSD-204	177	676	PWR
TA7743	SSD-204	SSD-204	177	676	PWR
TA7752	T8430B	SSD-206	130	549	TRI
TA7753	T8430D	SSD-206	130	549	TRI
TA7754	T8430M	SSD-206	130	549	TRI
TA7755	T8440B	SSD-206	130	459	TRI
TA7756	T8440D	SSD-206	130	549	TRI
TA7757	T8440M	SSD-206	130	549	TRI
TA7782	2N6292	SSD-204	177	676	PWR
TA7783	2N6290	SSD-204	177	676	PWR
TA7784	2N6288	SSD-204	177	676	PWR
TA7802	D1201B	SSD-206	278	495	RECT
TA7803	D1201D	SSD-206	278	495	RECT
TA7804	D1201M	SSD-206	278	495	RECT
TA7805	D1201N	SSD-206	278	495	RECT
TA7806	D1201P	SSD-206	278	495	RECT
TA7821	S6400N	SSD-206	218	578	SCR
TA7823	S6410N	SSD-206	218	578	SCR
TA7825	S6420N	SSD-206	218	578	SCR
TA7852	2N5917	SSD-205	158	425	RF
TA7920	2N5992	SSD-205	189	451	RF
TA7921	2N5993	SSD-205	194	452	RF
TA7922	2N5995	SSD-205	205	454	RF
TA7923	2N5996	SSD-205	210	455	RF
TA7936	40819	SSD-201	704	463	MOS/FET
TA7937	T8450B	SSD-206	130	549	TRI
TA7938	T8450D	SSD-206	130	549	TRI
TA7939	T8450M	SSD-206	130	549	TRI
TA7941	40934	SSD-205	329	550	RF
TA7943	40909	SSD-205	321	547	RF
TA7982	40940	SSD-205	337	553	RF
TA7984	D2540A	SSD-206	345	580	RECT
TA7985	D2540B	SSD-206	345	580	RECT
TA7986	D2540D	SSD-206	345	580	RECT
TA7987	D2540M	SSD-206	345	580	RECT
TA7988	S2060A	SSD-206	138	654	SCR
TA7989	S2060B	SSD-206	138	654	SCR
TA7990	S2060C	SSD-206	138	654	SCR
TA7991	S2060D	SSD-206	138	654	SCR
TA7993	2N6265	SSD-205	228	543	RF
TA7994	2N6266	SSD-205	234	544	RF
TA7995	2N6267	SSD-205	240	545	RF
TA7995A	2N6269	SSD-205	246	546	RF
TA7996	D1201F	SSD-206	278	495	RECT
TA7999	40820	SSD-201	724	464	MOS/FET
TA8000	40821	SSD-201	724	464	MOS/FET
TA8001	40822	SSD-201	732	465	MOS/FET
TA8002	40823	SSD-201	732	465	MOS/FET
TA8004	2N6077	SSD-204	318	492	PWR
TA8005	2N6079	SSD-204	318	492	PWR
TA8007	2N6479	SSD-204	454	702	PWR
TA8007B	2N6480	SSD-204	454	702	PWR
TA8100	2N6481	SSD-204	454	702	PWR
TA8100B	2N6482	SSD-204	454	702	PWR
TA8104	40915	SSD-205	325	574	RF
TA8158	S3703SF	SSD206	194	522	SCR
TA8159	S3702SF	SSD-206	194	522	SCR
TA8160	D2103SF	SSD-206	298	522	RECT
TA8161	D2103S	SSD-206	298	522	RECT
TA8162	D2101S	SSD-206	298	522	RECT
TA8172	40970	SSD-205	359	656	RF
TA8197	T6400N	SSD-206	55	593	TRI
TA8198	T6410N	SSD-206	55	593	TRI
TA8199	T6420N	SSD-206	55	593	TRI
TA8201	2N6388	SSD-204	538	610	PWR
TA8202	2N6386	SSD-204	538	610	PWR
TA8210	2N6106	SSD-204	177	676	PWR
TA8211	2N6108	SSD-204	177	676	PWR
TA8212	2N6110	SSD-204	177	676	PWR
TA8231	2N6293	SSD-204	177	676	PWR
TA8232	2N6291	SSD-204	177	676	PWR
TA8236	40936	SSD-205	333	551	RF
TA8242	40841	SSD-201	739	489	MOS/FET
TA8247	40887	SSD-204	278	508	PWR
TA8248	40885	SSD-204	278	508	PWR
TA8249	40886	SSD-204	278	508	PWR
TA8323	2N6488	SSD-204	226	678	PWR
TA8324	2N6487	SSD-204	226	678	PWR
TA8325	2N6486	SSD-204	226	678	PWR
TA8326	2N6491	SSD-204	226	678	PWR
TA8327	2N6490	SSD-204	226	678	PWR
TA8328	2N6489	SSD-204	226	678	PWR
TA8330	2N6213	SSD-204	312	507	PWR
TA8331	2N6214	SSD-204	312	507	PWR
TA8340	41038	SSD-205	397	679	RF
TA8343	2N6478	SSD-204	83	680	PWR
TA8344	40894	SSD-205	309	548	RF
TA8345	40895	SSD-205	309	548	RF
TA8346	40896	SSD-205	309	548	RF
TA8347	40897	SSD-205	309	548	RF
TA8348	2N6385	SSD-204	532	609	PWR
TA8349	2N6383	SSD-204	532	609	PWR
TA8352	2N6372	SSD-204	170	675	PWR
TA8353	2N6373	SSD-204	170	675	PWR
TA8354	2N6374	SSD-204	170	675	PWR
TA8357	T2850B	SSD-206	79	540	TRI
TA8358	T2850D	SSD-206	79	540	TRI
TA8405	2N6477	SSD-204	83	680	PWR
TA8407	2N6268	SSD-205	246	546	RF
TA8411	D2406A	SSD-206	318	663	RECT
TA8412	D2406B	SSD-206	318	663	RECT
TA8413	D2406D	SSD-206	318	663	RECT
TA8414	D2406M	SSD-206	318	663	RECT
TA8415	D2412A	SSD-206	326	664	RECT
TA8416	D2412B	SSD-206	326	664	RECT
TA8417	D2412D	SSD-206	326	664	RECT
TA8418	D2412M	SSD-206	326	664	RECT
TA8419	D2520A	SSD-206	334	665	RECT
TA8420	D2520B	SSD-206	334	665	RECT
TA8421	D2520D	SSD-206	334	665	RECT
TA8422	D2520M	SSD-206	334	665	RECT
TA8425	R47M15	SSD-205	407	605	RF
TA8428	2N6254	SSD-204	102	524	PWR
TA8429	2N6253	SSD-204	102	524	PWR
TA8430	2N6258	SSD-204	141	525	PWR

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TA8432	2N6259	SSD-204	149	526	PWR
TA8433	2N6261	SSD-204	45	527	PWR
TA8434	2N6260	SSD-204	45	527	PWR
TA8435	2N6262	SSD-204	133	528	PWR
TA8436	2N6264	SSD-204	69	529	PWR
TA8437	2N6263	SSD-204	69	529	PWR
TA8439	40898	SSD-205	313	538	RF
TA8440	40899	SSD-205	313	538	RF
TA8442	2N6472	SSD-204	217	677	PWR
TA8443	2N6471	SSD-204	217	677	PWR
TA8444	2N6473	SSD-204	177	676	PWR
TA8445	2N6475	SSD-204	177	676	PWR
TA8485	2N6387	SSD-204	538	610	PWR
TA8486	2N6384	SSD-204	532	609	PWR
TA8493	40971	SSD-205	359	656	RF
TA8504	T2500B	SSD-206	49	615	TRI
TA8505	T2500D	SSD-206	49	615	TRI
TA8559	40954	SSD-205	346	579	RF
TA8561	40955	SSD-205	346	579	RF
TA8562	40967	SSD-205	355	596	RF
TA8563	40968	SSD-205	355	596	RF
TA8647	41025	SSD-205	383	641	RF
TA8648	41026	SSD-205	383	641	RF
TA8649	41027	SSD-205	390	640	RF
TA8650	41028	SSD-205	390	640	RF
TA8651A	HC2500	SSD-204	749	681	HYB
TA8656	2N3656	SSD-206	245	724	SCR
TA8657	2N3658	SSD-206	245	724	SCR
TA8709	2N6468	SSD-204	170	675	PWR
TA8710	2N6467	SSD-204	170	675	PWR
TA8712	R47M10	SSD-205	407	605	RF
TA8713	R47M13	SSD-205	407	605	RF
TA8719	41008	SSD-205	373	616	RF
TA8720	41009	SSD-205	373	616	RF
TA8721	41010	SSD-205	373	616	RF
TA8722	2N6476	SSD-204	177	676	PWR
TA8723	2N6474	SSD-204	177	676	PWR
TA8724	2N6469	SSD-204	217	677	PWR
TA8726	2N6470	SSD-204	217	677	PWR
TA8746	2N6393	SSD-205	270	628	RF
TA8747	2N6390	SSD-205	261	626	RF
TA8748	RCA2003	SSD-205	261	626	RF
TA8749	2N6391	SSD-205	265	627	RF
TA8750	RCA2005	SSD-205	265	627	RF
TA8751	2N6392	SSD-205	270	628	RF
TA8752	RCA2010	SSD-205	270	628	RF
TA8761	40637A	SSD-205	295	655	RF
TA8845S	S3800S	SSD-206	199	639	ITR
TA8846N	S3800SF	SSD-206	199	639	ITR

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JAN2N918	78	RF	301
JAN2N1482	26	PWR	207
JAN2N1486	26	PWR	180
JANTX2N1486	26	PWR	180
JAN2N1490	27	PWR	208
JAN2N1493	78	RF	247
JAN2N2016	27	PWR	248
JAN2N2857	79	RF	343
JANTX2N2857	79	RF	343
JAN2N3055	28	PWR	407
JANTX2N3055	28	PWR	407
JAN2N3375	80	RF	341
JANTX2N3375	80	RF	341
JANTXV2N3375	80	RF	341
JAN2N3439	28	PWR	368
JANTX2N3439	28	PWR	368
JAN2N3441	29	PWR	369
JAN2N3442	29	PWR	370
JAN2N3553	80	RF	341
JANTX2N3553	80	RF	341
JANTXV2N3553	80	RF	341
JAN2N3585	30	PWR	384
JANTX2N3585	30	PWR	384
JAN2N3772	30	PWR	413
JANTX2N3772	30	PWR	413
JAN2N3866	81	RF	398
JANTX2N3866	81	RF	398
JAN2N4440	80	RF	341
JANTX2N4440	80	RF	341
JANTXV2N4440	80	RF	341
JAN2N5038	31	PWR	439
JANTX2N5038	31	PWR	439
JAN2N5071	81	RF	442
JANTX2N5071	81	RF	442
JAN2N5109	82	RF	453
JANTX2N5109	82	RF	453
JAN2N5416	31	PWR	485
JANTX2N5416	31	PWR	485
JAN2N5672	32	PWR	488
JANTX2N5672	32	PWR	488
JAN2N5840	32	PWR	487
JANTX2N5840	32	PWR	487
JAN2N5918	82	RF	473
JAN2N6213	33	PWR	461
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RCA42A	SSD-204	257	PTD-187	588	PWR
RCA42B	SSD-204	257	PTD-187	588	PWR
RCA42C	SSD-204	257	PTD-187	588	PWR
RCA101	SSD-204	262	PTD-187	557	PWR
RCA102	SSD-204	262	PTD-187	557	PWR
RCA103	SSD-204	262	PTD-187	557	PWR
RCA104	SSD-204	262	PTD-187	557	PWR
RCA105	SSD-204	266	PTD-187	556	PWR
RCA201	SSD-204	262	PTD-187	557	PWR
RCA202	SSD-204	262	PTD-187	557	PWR
RCA203	SSD-204	262	PTD-187	557	PWR
RCA204	SSD-204	262	PTD-187	557	PWR
RCA205	SSD-204	266	PTD-187	556	PWR
RCA370	SSD-204	270	PTD-187	558	PWR
RCA371	SSD-204	270	PTD-187	558	PWR
RCA410	SSD-204	326	PTD-187	509	PWR
RCA411	SSD-204	332	PTD-187	510	PWR
RCA413	SSD-204	338	PTD-187	511	PWR
RCA423	SSD-204	344	PTD-187	512	PWR
RCA431	SSD-204	350	PTD-187	513	PWR
RCA520	SSD-204	270	PTD-187	558	PWR
RCA521	SSD-204	270	PTD-187	558	PWR
RCA1000	SSD-204	524	PTD-187	594	PWR
RCA1001	SSD-204	524	PTD-187	594	PWR
RCA2003	SSD-205	261	RFT-700	626	RF
RCA2005	SSD-205	265	RFT-700	627	RF
RCA2010	SSD-205	270	RFT-700	628	RF
RCA3001	SSD-205	401	RFT-700	657	RF
RCA3003	SSD-205	401	RFT-700	657	RF
RCA3005	SSD-205	401	RFT-700	657	RF
RCA3054	SSD-204	53	PTD-187	618	PWR
RCA3055	SSD-204	53	PTD-187	618	PWR
RCA3441	SSD-204	77	PTD-187	666	PWR
RCA6263	SSD-204	77	PTD-187	666	PWR
S2060A	SSD-206	138	THC-500	654	SCR
S2060B	SSD-206	138	THC-500	654	SCR
S2060C	SSD-206	138	THC-500	654	SCR
S2060D	SSD-206	138	THC-500	654	SCR
S2060E	SSD-206	138	THC-500	654	SCR
S2060F	SSD-206	138	THC-500	654	SCR
S2060M	SSD-206	138	THC-500	654	SCR
S2060Q	SSD-206	138	THC-500	654	SCR
S2060Y	SSD-206	138	THC-500	654	SCR
S2061A	SSD-206	138	THC-500	654	SCR
S2061B	SSD-206	138	THC-500	654	SCR
S2061C	SSD-206	138	THC-500	654	SCR
S2061D	SSD-206	138	THC-500	654	SCR
S2061E	SSD-206	138	THC-500	654	SCR
S2061F	SSD-206	138	THC-500	654	SCR
S2061M	SSD-206	138	THC-500	654	SCR
S2061Q	SSD-206	138	THC-500	654	SCR
S2061Y	SSD-206	138	THC-500	654	SCR
S2062A	SSD-206	138	THC-500	654	SCR
S2062B	SSD-206	138	THC-500	654	SCR
S2062C	SSD-206	138	THC-500	654	SCR
S2062D	SSD-206	138	THC-500	654	SCR
S2062E	SSD-206	138	THC-500	654	SCR
S2062F	SSD-206	138	THC-500	654	SCR
S2062M	SSD-206	138	THC-500	654	SCR
S2062Q	SSD-206	138	THC-500	654	SCR
S2062Y	SSD-206	138	THC-500	654	SCR
S2400A	SSD-206	151	THC-500	567	SCR
S2400B	SSD-206	151	THC-500	567	SCR
S2400D	SSD-206	151	THC-500	567	SCR
S2400M	SSD-206	151	THC-500	567	SCR
S2600B	SSD-206	156	THC-500	496	SCR
S2600D	SSD-206	156	THC-500	496	SCR
S2600M	SSD-206	156	THC-500	496	SCR
S2610B	SSD-206	156	THC-500	496	SCR
S2610D	SSD-206	156	THC-500	496	SCR
S2610M	SSD-206	156	THC-500	496	SCR
S2620B	SSD-206	156	THC-500	496	SCR
S2620D	SSD-206	156	THC-500	496	SCR
S2620M	SSD-206	156	THC-500	496	SCR
S2710B	SSD-206	164	THC-500	266	SCR
S2710D	SSD-206	164	THC-500	266	SCR
S2710M	SSD-206	164	THC-500	266	SCR
S2800A	SSD-206	166	THC-500	501	SCR

Type No.	DATA BOOK Vol. No.	Page	Catalog	File No.	Product Line
S2800B	SSD-206	166	THC-500	501	SCR
S2800D	SSD-206	166	THC-500	501	SCR
S3700B	SSD-206	172	THC-500	306	SCR
S3700D	SSD-206	172	THC-500	306	SCR
S3700M	SSD-206	172	THC-500	306	SCR
S3701M	SSD-206	192	THC-500	476	SCR
S3702SF	SSD-206	194	THC-500	522	SCR
S3703SF	SSD-206	194	THC-500	522	SCR
S3704A	SSD-206	180	THC-500	690	SCR
S3704B	SSD-206	180	THC-500	690	SCR
S3704D	SSD-206	180	THC-500	690	SCR
S3704M	SSD-206	180	THC-500	690	SCR
S3704S	SSD-206	180	THC-500	690	SCR
S3705M	SSD-206	187	THC-500	354	SCR
S3706M	SSD-206	187	THC-500	354	SCR
S3714A	SSD-206	180	THC-500	690	SCR
S3714B	SSD-206	180	THC-500	690	SCR
S3714D	SSD-206	180	THC-500	690	SCR
S3714M	SSD-206	180	THC-500	690	SCR
S3714S	SSD-206	180	THC-500	690	SCR
S3800D	SSD-206	199	THC-500	639	ITR
S3800E	SSD-206	199	THC-500	639	ITR
S3800EF	SSD-206	199	THC-500	639	ITR
S3800M	SSD-206	199	THC-500	639	ITR
S3800MF	SSD-206	199	THC-500	639	ITR
S3800S	SSD-206	199	THC-500	639	ITR
S3800SF	SSD-206	199	THC-500	639	ITR
S6200A	SSD-206	210	THC-500	418	SCR
S6200B	SSD-206	210	THC-500	418	SCR
S6200D	SSD-206	210	THC-500	418	SCR
S6200M	SSD-206	210	THC-500	418	SCR
S6210A	SSD-206	210	THC-500	418	SCR
S6210B	SSD-206	210	THC-500	418	SCR
S6210D	SSD-206	210	THC-500	418	SCR
S6210M	SSD-206	210	THC-500	418	SCR
S6220A	SSD-206	210	THC-500	418	SCR
S6220B	SSD-206	210	THC-500	418	SCR
S6220D	SSD-206	210	THC-500	418	SCR
S6220M	SSD-206	210	THC-500	418	SCR
S6400N	SSD-206	218	THC-500	578	SCR
S6410N	SSD-206	218	THC-500	578	SCR
S6420A	SSD-206	218	THC-500	578	SCR
S6420B	SSD-206	218	THC-500	578	SCR
S6420D	SSD-206	218	THC-500	578	SCR
S6420M	SSD-206	218	THC-500	578	SCR
S6420N	SSD-206	218	THC-500	578	SCR
S6431M	SSD-206	228	THC-500	247	SCR
S7430M	SSD-206	238	THC-500	408	SCR
S7432M	SSD-206	245	THC-500	724	SCR
T2300A	SSD-206	33	THC-500	470	TRI
T2300B	SSD-206	33	THC-500	470	TRI
T2300D	SSD-206	33	THC-500	470	TRI
T2301A	SSD-206	40	THC-500	431	TRI
T2301B	SSD-206	40	THC-500	431	TRI
T2301D	SSD-206	40	THC-500	431	TRI
T2302A	SSD-206	33	THC-500	470	TRI
T2302B	SSD-206	33	THC-500	470	TRI
T2302D	SSD-206	33	THC-500	470	TRI
T2304B	SSD-206	41	THC-500	441	TRI
T2304D	SSD-206	41	THC-500	441	TRI
T2305B	SSD-206	41	THC-500	441	TRI
T2305D	SSD-206	41	THC-500	441	TRI
T2306A	SSD-206	47	THC-500	406	TRI
T2306B	SSD-206	47	THC-500	406	TRI
T2306D	SSD-206	47	THC-500	406	TRI
T2310A	SSD-206	33	THC-500	470	TRI
T2310B	SSD-206	33	THC-500	470	TRI
T2310D	SSD-206	33	THC-500	470	TRI
T2311A	SSD-206	40	THC-500	431	TRI
T2311B	SSD-206	40	THC-500	431	TRI
T2311D	SSD-206	40	THC-500	431	TRI
T2312A	SSD-206	33	THC-500	470	TRI
T2312B	SSD-206	33	THC-500	470	TRI
T2312D	SSD-206	33	THC-500	470	TRI
T2313A	SSD-206	28	THC-500	414	TRI
T2313B	SSD-206	28	THC-500	414	TRI
T2313D	SSD-206	28	THC-500	414	TRI
T2313M	SSD-206	28	THC-500	414	TRI
T2316A	SSD-206	47	THC-500	406	TRI
T2316B	SSD-206	47	THC-500	406	TRI

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